TPS62840 1.8V～6.5V、750mA、I_Q 60nA の降圧型コンバータ

1 特長

- 静止電流：60nA
- I_Q 120nA の 100% デューティ・サイクル・モード
- 入力電圧範囲 V_{IN}：1.8V～6.5V
- 出力電流：最大 750mA
- RF 対応 DCS-Control™
- 1μA の I_{OUT} で 80% の効率 (3.6V_{IN} から 1.8V_{OUT} へ)
- VSET ピンで選択可能な 16 の出力電圧
- PFM/PWM 自動遷移モードまたは強制 PWM モード
- 選択可能な強制 PWM モードと STOP モード
- 出力放電機能
- 25nA のシャットダウン電流
- SON-8、WCSP-6、熱特性強化型 HVSSOP-8 パッケージ

2 アプリケーション

- スマート・メーター、スマート・サーモスタット
- アセット・トラッキング・デバイス
- ウェアラブル電子機器
- 医療用センサ・パッチおよび患者モニタ
- 産業用 IoT (スマート・センサ) / NB-IoT
- 試験/測定機器
- ATEX / 本質安全防爆

3 概要

TPS62840 は、静止電流が標準 60nA と極めて小さい、高効率の降圧型コンバータです。本デバイスは、バッテリ持続時間をさらに延長するため、100% モードで I_Q をわずか 120nA に低減するための専用回路を備えています。

本デバイスは、無線に効率よく電力を供給するため DCS-Control を使用しており、1.8MHz (標準値) のスイッチング周波数で動作します。パワーセーブ・モードでは、1μA 以下の負荷電流範囲まで軽負荷時効率を維持できます。

VSET ピンに抵抗を接続することで定義済みの 16 種類の出力電圧を選択できるため、最小限の外付け部品数で各種用途に柔軟に対応できます。

試験および測定システムでノイズ・フリー測定を行うために、本デバイスの STOP ピンはすべてのスイッチング・ノイズを直ちに除去します。

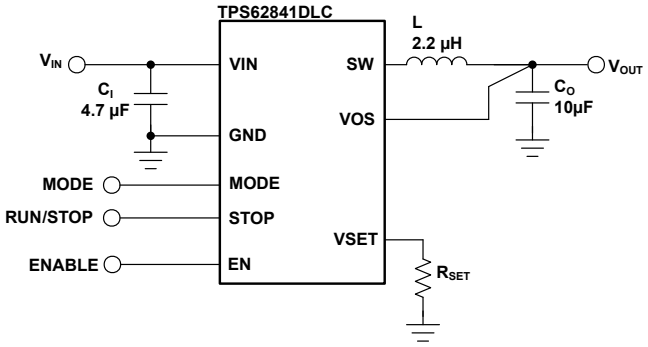
TPS62840 は最大 750mA の出力電流を供給します。1.8V～6.5V の入力電圧に対応する本デバイスは、2S～4S アルカリ、1S～2S Li-MnO_2 または 1S リチウムイオン / Li-$SoCl_2$ など複数の電源をサポートしています。

製品情報(1)

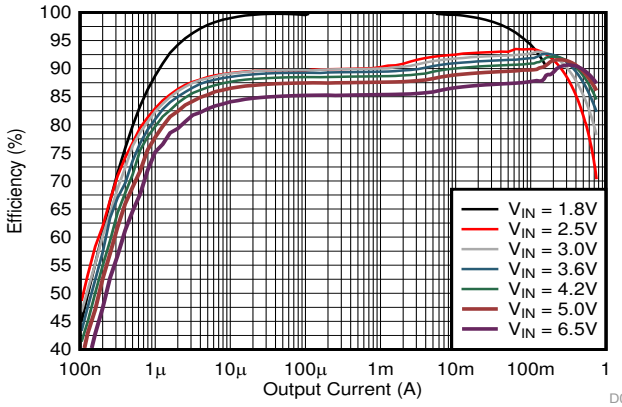
型番	パッケージ	本体サイズ(公称)
TPS6284x	8 ピン DLC (SON)	1.5 mm x 2 mm
	6 ピン YBG (WCSP)	0.97 mm x 1.47 mm
	8 ピン DGR (HVSSOP)	3 mm x 5 mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



効率と負荷電流の関係 (V_{OUT} = 1.8V)



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (November 2019) から Revision D に変更 **Page**

- Updated the *Device Comparison Table* ... 3
- Added efficiency graphs to the *Application Curves* ... 20

Revision B (August 2019) から Revision C に変更 **Page**

- 「*特長*」に SON-8、WCSP-6、熱特性強化型 HVSSOP-8 を追加 ... 1
- 「*アプリケーション*」に ATEX / 本質安全防爆を追加 ... 1
- TPS62842DGR を示すように「代表的なアプリケーション」のイメージを更新 ... 1
- Added orderable part number TPS62841DGR to *Device Comparison Table* ... 3
- Added orderable part number TPS62842DGR to *Device Comparison Table* ... 3
- Updated *Thermal Information* values to support TPS62842DGR ... 6
- Added low-side MOSFET switch current limit to *Electrical Characteristics* ... 8
- Added TPS62841DGR to *Output Voltage Selection* ... 13
- Updated Efficiency Power Save graphs in *Application Curves* ... 20
- Updated Load Transient waveform in *Application Curves* ... 24
- Added PCB layout for DGR package ... 29

Revision A (July 2019) から Revision B に変更 **Page**

- 「事前情報」マーケティング・ステータスを量産データに変更 ... 1

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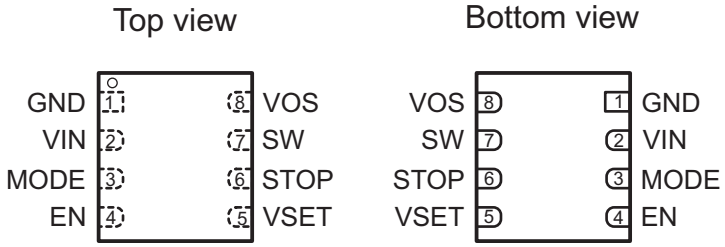
5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT DISCHARGE	MODE PIN	STOP PIN	PACKAGE	PACKAGE MARKING
TPS62840DLC	1.8 V to 3.3 V in 100-mV steps	750 mA	yes	yes	yes	SON-8 (DLC)	E5
TPS62840YBG				no	no	WCSP-6 (YBG)	62840
TPS62841DLC	0.8 V to 1.55 V in 50-mV steps	750 mA	yes	yes	yes	SON-8 (DLC)	E9
TPS62841YBG				no	no	WCSP-6 (YBG)	62841
TPS62841DGR				yes	no	HVSSOP-8 (DGR)	62841
TPS62842DGR	1.8 V, 2.0 V, 2.2 V, 2.4 V to 3.6 V in 100-mV steps	750 mA	yes	yes	no	HVSSOP-8 (DGR)	62842
TPS62849DLC	3.4-V fixed output voltage				yes	SON-8 (DLC)	FF

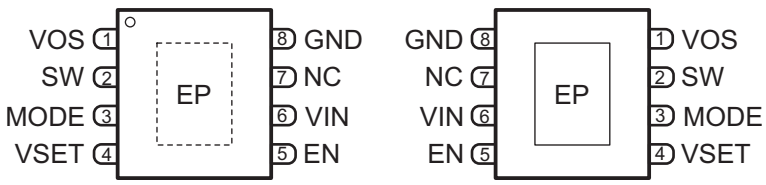
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6 Pin Configuration and Functions

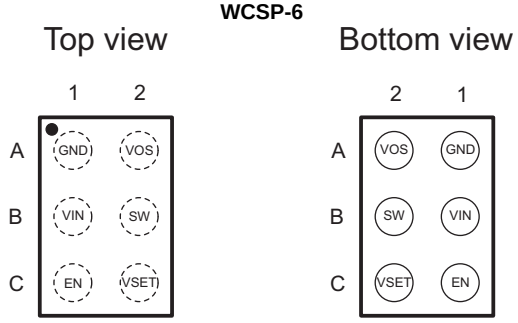
DLC
SON-8



DGR
HVSSOP-8



YBG
WCSP-6



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Pin Functions

PIN				I/O	DESCRIPTION
NAME	DLC (SON-8)	DGR (HVSSOP-8)	YBG (WCSP-6)		
VIN	2	6	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A 4.7-µF ceramic capacitor is required.
SW	7	2	B2	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	1	8	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitors.
VSET	5	4	C2	IN	Connecting a resistor to GND sets the output voltage when the converter is enabled. For the TPS62849, connect this pin to GND.
VOS	8	1	A2	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. When the converter is disabled, this pin discharges V_{OUT} by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace.
EN	4	5	C1	IN	Enable pin. A high level enables the device and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up and the output voltage is regulated. The pulldown resistor is activated again, once a low level has been detected.
STOP	6	n/a	n/a	IN	STOP Switching pin. When this pin is logic high, the converter stops switching in order to provide a quiet supply rail. The output is powered from the charge available in the output capacitor. When this pin is logic low, the device immediately resumes operation. The pin features an internal pulldown resistor, which is disabled once a high level is detected at the input. The pulldown resistor is activated again, once a low level has been detected.
MODE	3	3	n/a	IN	MODE pin. A low level enables Power-Save Mode operation with an automatic transition between PFM and PWM modes. A high level forces the converter to operated in PWM mode. This pin can be toggled during operation. It must be terminated.
NC	n/a	7	n/a		This pin is not connected internally. Do not connect this pin.
EP	n/a	9	n/a	PWR	Exposed thermal pad(1). The PowerPAD must be connected to GND.

(1) For more information about the PowerPAD, see the *PowerPAD™ Thermally Enhanced Package* application report.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	7	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC), less than 10ns(3)	–2.0	8.5	V
	EN, MODE, STOP	–0.3	6.5	V
	VSET	–0.3	V_{IN} + 0.3 < 3.6	V
	VOS	–0.3	3.7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) While switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		6.5	V
L	Effective inductance	1.51	2.2	2.9	µH
C_{OUT}	Effective output capacitance	3	10	40	µF
C_{IN}	Effective input capacitance	1	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			100	pF
R_{SET}	Nominal resistance range for external voltage selection resistor (E96 resistor series)	0.909		267	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		8 Pins DLC Package	6 Pins YBG Package	8 Pins DGR Package	DGR EVM	UNIT
		JEDEC PCB 51-7		JEDEC PCB 51-5	TPS62841-2EVM123	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	133.4	54.4	46.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.7	0.4	58.1	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.9	39.4	25.9	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	0.1	1.2	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	39.4	25.9	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	11.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q_NO_LOAD}$	No load operating input current	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.8V device switching		60		nA
$I_{Q_NO_LOAD}$	No load operating input current	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.2V device switching		80		nA
$I_{Q_NO_LOAD}$	No load operating input current (PWM Mode)	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.8V, MODE = V_{IN} device switching		3		mA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = 25°C (DLC package option)		36	100	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = 25°C (DLC package option)		56	120	nA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = -40°C to 85°C		36	360	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = -40°C to 85°C		56	170	nA
I_{Q_VOS}	Operating quiescent current into VOS pin	EN = V_{IN}, V_{OUT} = 3.3V device not switching		70		nA
		EN = V_{IN}, V_{OUT} < 1.5 V device not switching		5		nA
		EN, STOP = V_{IN}, 3V < V_{OUT} < 3.3V T_J = -40°C to 85°C		5	100	nA
$I_{Q_100\%_MODE}$	Operating quiescent current 100% Mode	V_{IN} = V_{OUT} = 3.3V, T_J = -40°C to 85°C		120		nA
$I_{Q_VIN_STOP}$	Operating quiescent current into pin VIN	STOP = High, V_{OUT} = 1.8V, T_J = -40°C to 85°C		70	175	µA
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN} VSET = GND, T_J = -40°C to 85°C		25	300	nA
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}		1.72	1.8	V
$V_{TH_UVLO–}$		Falling V_{IN}		1.45	1.75	V
EN, MODE, STOP INPUTS						
V_{IH_TH}	High level input voltage		1.1			V
V_{IL_TH}	Low level input voltage				0.4	V
I_{IN}	Input bias current	MODE input, T_J = -40°C to 85°C		1	25	nA
R_{PD}	Internal pull-down resistance	EN, STOP inputs	200	450		kΩ

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Electrical Characteristics (continued)

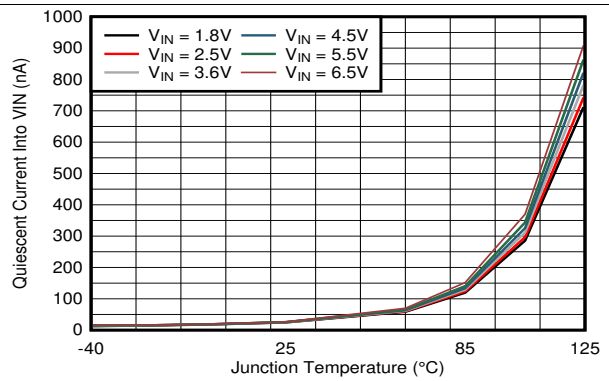
V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCHES						
$R_{DS(ON)}$	High-side MOSFET on-resistance (DLC, YBG package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		430	600	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		340	465	
	Low-side MOSFET on-resistance (DLC, YBG package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		170	240	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		135	180	
	High-side MOSFET on-resistance (DGR package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		460	630	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		370	495	
	Low-side MOSFET on-resistance (DGR package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		200	270	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		165	210	
I_{LIMF_SS}	Soft-start switch current limit(1)		0.15	0.225	0.3	A
I_{LIMF}	High-side MOSFET switch current limit(1)		1.0	1.2	1.4	A
	Low-side MOSFET switch current limit			1.0		A
I_{LIMN}	Negative current limit			533		mA
$t_{I_LIM_DELAY}$	Current limit propagation delay			50		ns
I_{LKG_SW}	Leakage current into SW pin	V_{SW} = 1.8V, T_J = -40°C to 85°C		10		nA
OUTPUT VOLTAGE DISCHARGE						
$I_{DISCHARGE_VOS}$	Output discharge current	EN = GND, sink current into VOS pin, over VIN range V_{OUT} = 1.8V, T_J = -40°C to 85°C	16	35	44	mA
THERMAL PROTECTION						
T_{SD}	Thermal shutdown temperature	Rising junction temperature, PWM Mode		160		°C
	Thermal shutdown hysteresis			5		°C
OUTPUT						
V_{OUT}	Output voltage accuracy	PWM Mode, I_{OUT} = 0 mA, V_{OUT} >= 1.8 V	-1.5	0	1.5	%
		PWM Mode, I_{OUT} = 0 mA, V_{OUT} <= 1.55 V	-2	0	2	%
V_{OUT}	DC output voltage load regulation	PWM Mode		0		%/mA
	DC output voltage line regulation	PWM Mode V_{OUT} = 1.8V, I_{OUT} = 200 mA, over VIN range		0		%/V
f_{SW}	Switching frequency	V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = V_{IN} I_{OUT} = 0mA		1.8		MHz
$t_{STARTUP_DELAY}$	Regulator start up delay time	V_{IN} = 3.6V, from EN = low to high until device starts switching			200	µs
$t_{STARTUP_DELAY}$	Regulator start up delay time	EN ramps with VIN, VIN 0 to 3.6V (< 100us), until device starts switching		10		ms
t_{SS}	Soft-start time	I_{OUT} = 0mA		120		µs
t_{SS_ILIMF}	Reduced current limit soft-start timeout			700	1200	µs

(1) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Switch Current Limit / Short Circuit Protection section).

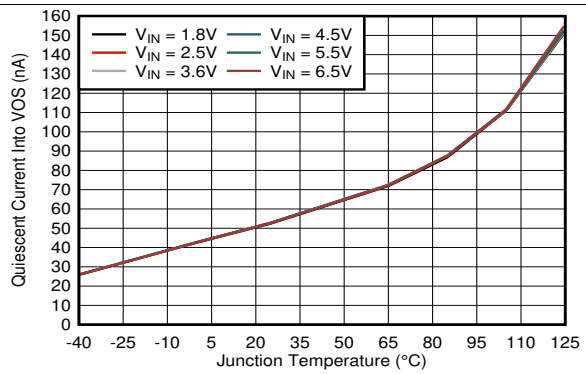
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7.6 Typical Characteristics



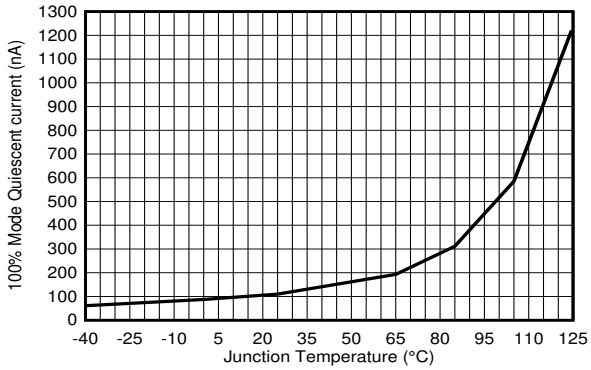
EN = VIN VOUT = 1.55 V Device Not Switching

図 1. Quiescent Current into VIN (I_{Q_VIN})



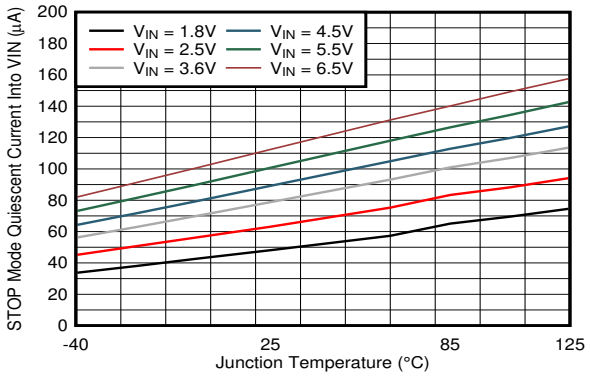
EN = VIN VOUT = 1.55 V Device Not Switching

図 2. Quiescent Current into VOS (I_{Q_VOS})



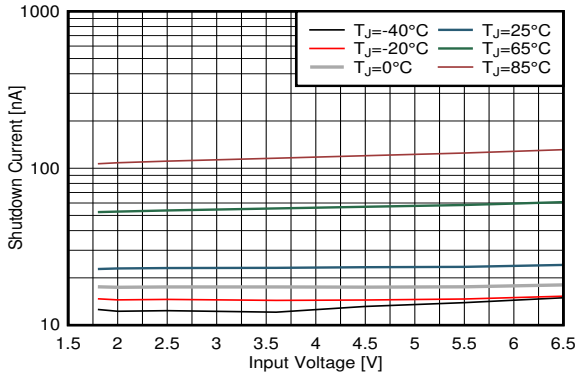
EN = VIN VIN = VOUT = 3.3 V Device Not Switching

図 3. 100% Mode Quiescent Current ($I_{Q_100\%_MODE}$)



EN = VIN VOUT = 1.8 V Device Not Switching

図 4. STOP Mode Quiescent Current into VIN ($I_{Q_VIN_STOP}$)



EN = GND

図 5. Shutdown Current (I_{SD})

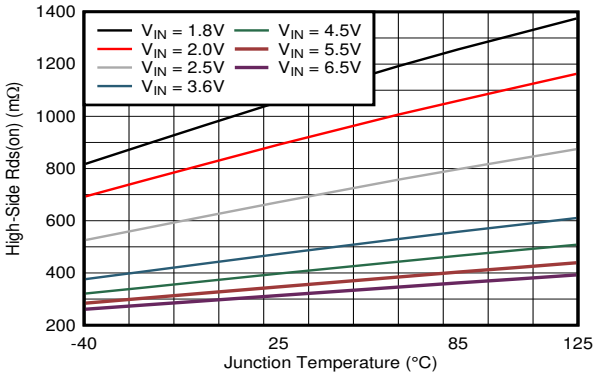


図 6. High-Side R_{DSON} versus Temperature (DLC, YBG packages)

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Typical Characteristics (continued)

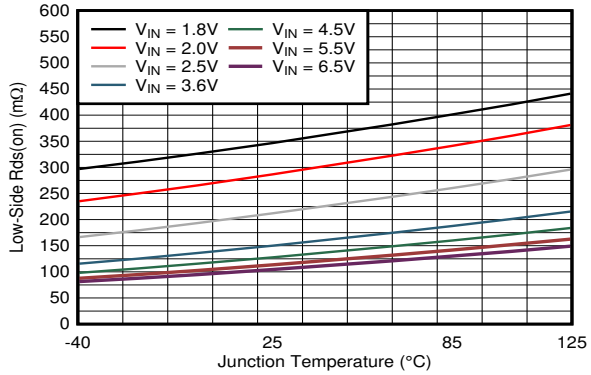


図 7. Low-Side R_{DSON} versus Temperature (DLC, YBG packages)

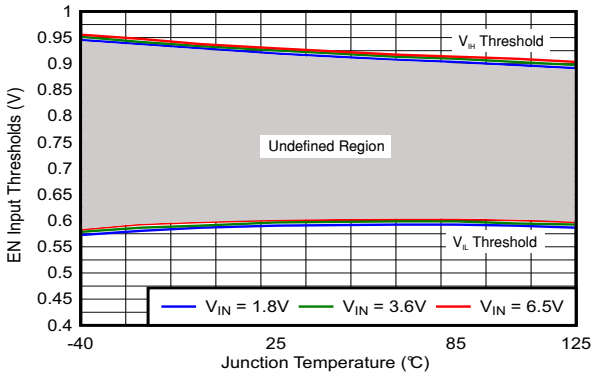


図 8. EN Input Thresholds versus Temperature

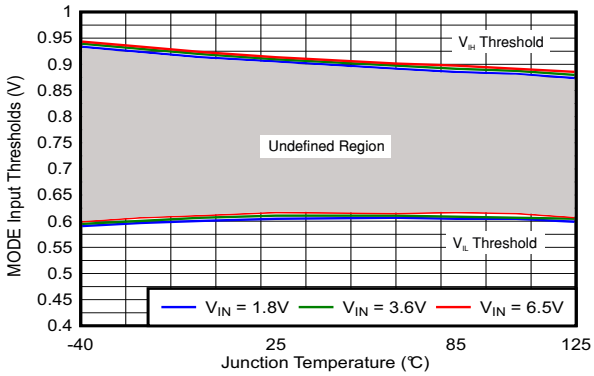


図 9. MODE Input Thresholds versus Temperature

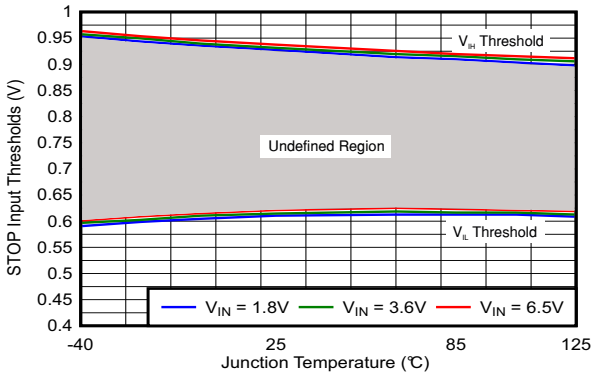
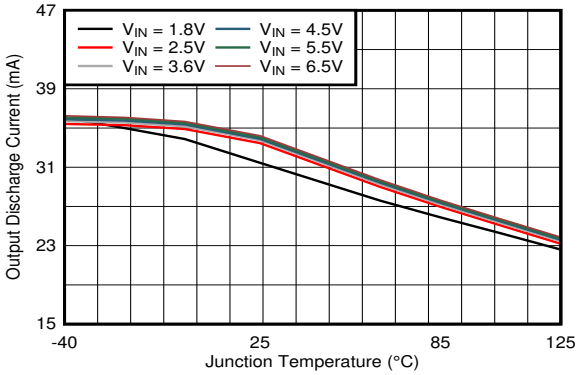


図 10. STOP Input Thresholds versus Temperature



EN = GND VOUT = 1.8 V

図 11. Output Discharge Current versus Temperature

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8 Detailed Description

8.1 Overview

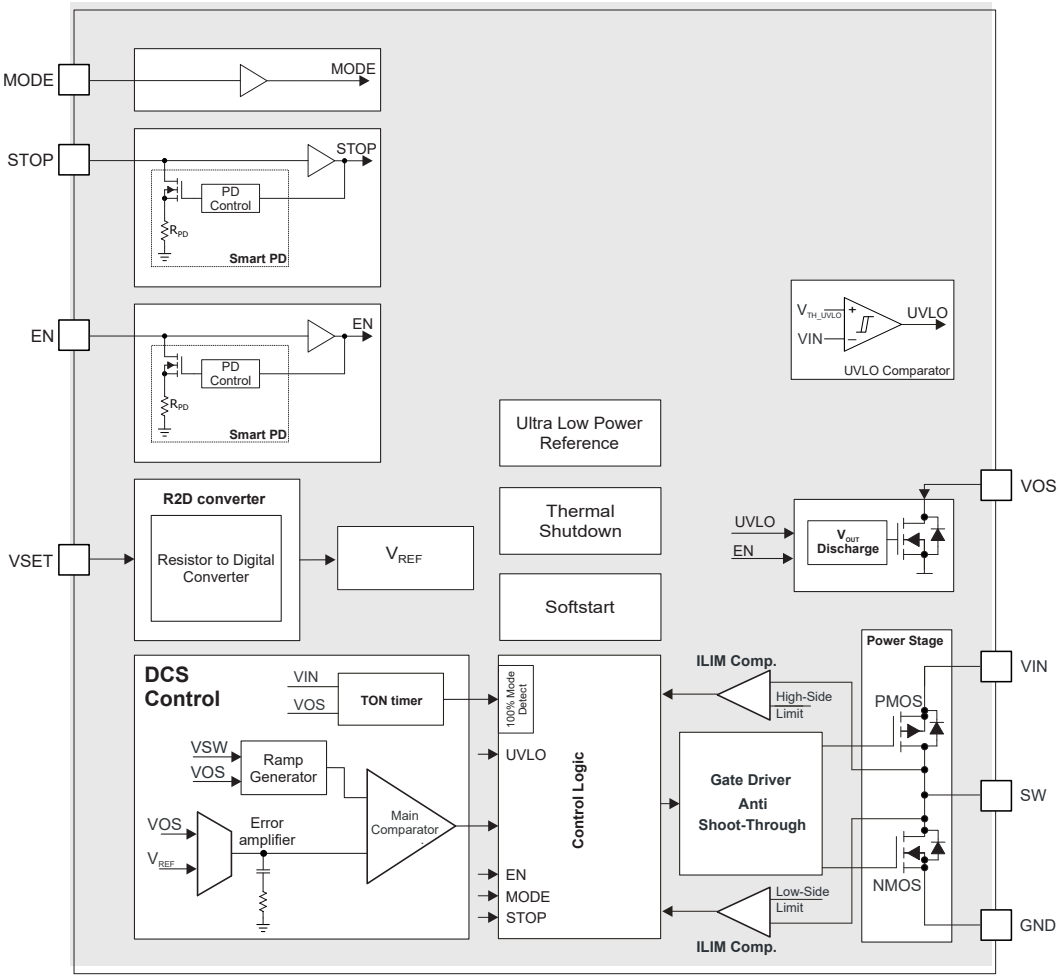
The TPS6284x is a synchronous step-down converter with ultra-low quiescent current consumption. Using TI's DCS-Control topology, the device extends the high efficiency operation area down to micro amperes of load current during Power-Save Mode Operation. Depending on the output voltage, the device consumes quiescent current from both the input and output to reduce the overall input current consumption to 60 nA typical.

DCS-Control™ (Direct Control with Seamless Transition into Power-Save Mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode controls. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM modes. It includes a AC loop which senses the output voltage (VOS pin) and directly feeds this information into a fast comparator stage.

The device operates with a nominal switching frequency of 1.8 MHz. An additional voltage feedback loop is used to achieve accurate DC load regulation. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

In Power-Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control supports both operating modes, the transition from PWM to PFM is seamless with minimum output voltage ripple. The TPS6284x offers both, excellent DC voltage and superior load transient regulation, combined with low output voltage ripple thereby minimizing interferences with Radio Frequency circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Smart Enable and Shutdown

To avoid a floating input, an internal 450-kΩ resistor pulls the EN pin to GND. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven low safely. The device is in shutdown mode when the EN input is logic low.

The device turns on with a logic high EN signal. An internal control circuit disconnects the EN pin pulldown resistor once the device has finished soft start and the output voltage is in regulation. With the EN pin set low, the device enters shutdown mode and the pulldown resistor is activated again.

8.3.2 Soft Start

To protect the battery and system from excessive inrush current, the device features a soft start of the output voltage.

Once the device has been enabled, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time ($t_{STARTUP_DELAY}$). Once this delay expires, the device enters soft start, starts switching, and ramps up the output voltage.

The device operates with a reduced switch current limit (I_{LIMF_SS}) throughout the entire soft-start phase (t_{SS}). The switch current limit is increased to its nominal value (I_{LIMF}) once the output voltage has reached its nominal value or the reduced current limit soft-start time (t_{SS_ILIMF}) has expired, whichever occurs first. The soft-start phase (t_{SS}) can last up to approximately 700 µs. 図 12 shows the start-up procedure.

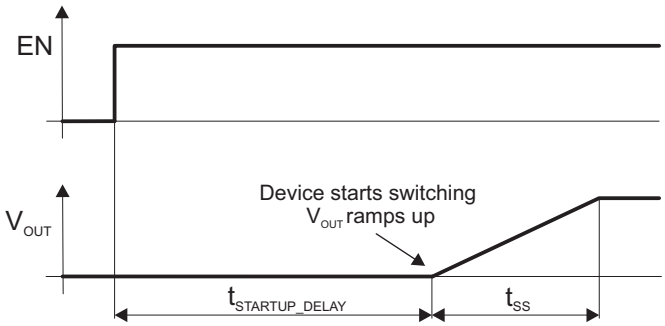


図 12. Device Start-up

8.3.3 Mode Selection: Power-Save Mode (PFM/PWM) or Forced PWM Operation (FPWM)

Connecting the MODE input to GND enables the automatic PWM and power-save mode operation. The converter operates in PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in PWM mode even at light load currents, allowing lower ripple compared to PFM mode switching. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements. The MODE pin must be terminated.

This pin is not available in the YBG package, where the device automatically transitions between power-save and PWM modes.

8.3.4 Output Voltage Selection (VSET)

The output voltage is set with a single external resistor connected between the VSET pin and GND. Once the device has been enabled and the control logic as well as the reference system are powered up, an R2D (resistor to digital) conversion is started to detect the value of the external R_{SET} resistor. A pre-defined fixed output voltage is set based on the R_{SET} value. The output voltage is set once during the start-up delay phase of the device.

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Feature Description (continued)

Once the output voltage is set, the R2D converter is turned off to avoid current flowing through R_{SET}. Care must be taken that no parasitic current, capacitance, or both greater than 100 pF is present between the VSET and GND pins. This can cause false R_{SET} readings and a faulty output voltage to be set. The R2D converter is designed to operate with resistor values out of E96 series. 表 1 shows the allowed R_{SET} values.

表 1. Output Voltage Setting, R_{SET} Resistor

OUTPUT VOLTAGE SETTING V_{OUT} [V]			VSET RESISTANCE TO GND - E96 VALUES [Ω]		
TPS62841YBG TPS62841DLC TPS62841DGR	TPS62840YBG TPS62840DLC	TPS62842DGR	MIN	NOM	MAX
0.8	1.8	1.8	0	GND	0.01 k
0.85	1.9	2.0	0.87 k	0.909 k	0.95 k
0.9	2.0	2.2	1.67 k	1.74 k	1.81 k
0.95	2.1	2.4	2.76 k	2.87 k	2.98 k
1.0	2.2	2.5	4.15 k	4.32 k	4.49 k
1.05	2.3	2.6	5.80 k	6.04 k	6.28 k
1.1	2.4	2.7	8.11 k	8.45 k	8.79 k
1.15	2.5	2.8	11.04 k	11.5 k	11.96 k
1.2	2.6	2.9	15.17 k	15.8 k	16.43 k
1.25	2.7	3.0	20.64 k	21.5 k	22.36 k
1.3	2.8	3.1	27.55 k	28.7 k	29.85 k
1.35	2.9	3.2	36.77 k	38.3 k	39.83 k
1.4	3.0	3.3	50.21 k	52.3 k	54.39 k
1.45	3.1	3.4	68.64 k	71.5 k	74.36 k
1.5	3.2	3.49	97.92 k	102 k	106.08 k
1.55	3.3	3.6	256.32 k	267 k	277.68 k

The output voltage of the TPS62849 is internally set to 3.4 V. Connect VSET directly to GND for this device.

8.3.5 Undervoltage Lockout UVLO

To avoid mis-operation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input below the threshold $V_{TH_UVLO–}$ with falling V_{IN}. The device starts at an input voltage higher than the threshold V_{TH_UVLO+} with rising V_{IN}.

When the device resumes operation from an undervoltage lockout condition, it behaves like being enabled. This means the internal control logic is powered up, the external R_{SET} resistor is read out and a soft-start sequence is initiated.

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8.3.6 Switch Current Limit / Short Circuit Protection

The TPS6284x integrates a current limit on the high-side as well as on the low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle-by-cycle. If the high-side MOSFET current limit (I_{LIMF}) trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp the inductor current down. Once the inductor current decreases below the low-side current limit (I_{LIMF}), the low-side MOSFET turns off and the high-side MOSFET turns on again.

During soft start, the current limit is reduced to I_{LIMF_SS}. After soft start has finished, the current limit value increases to the normal value I_{LIMF}.

Due to internal propagation delay, the actual inductor current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{I_LIM_DELAY} \quad (1)$$

where

- I_{LIMF} is the static current limit, specified in *Electrical Characteristics*
- L is the inductance
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- $t_{I_LIM_DELAY}$ is the internal propagation delay

In forced PWM mode, a negative current limit (I_{LIMN}) is enabled to prevent excessive current flowing backwards to the input. When the inductor current reaches I_{LIMN}, the low-side MOSFET turns off and the high-side MOSFET turns on and kept on until TON time expires.

8.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined ramp-down of the output voltage when the device is disabled.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled or if UVLO is entered. It is not active during Thermal Shutdown. The discharge circuit remains active as long as the input voltage is above 0.7 V.

8.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. The device enters thermal shutdown when the junction temperature exceeds the thermal shutdown threshold (T_{SD}) of 160°C (typ.). Both the high-side and low-side MOSFETs are turned off. The device resumes its operation when the junction temperature falls below typically 155°C again and begins with a soft-start cycle without reading R_{SET} again. In Power-Save Mode, the thermal shutdown feature is disabled.

8.3.9 STOP Mode

The TPS6284x includes the STOP input pin, allowing the user to temporarily stop the switching of the regulator. The STOP pin function does not depend on the setting of the MODE pin. The STOP pin is only present on the DLC package.

When a logic high level is applied to the STOP pin, the regulator is forced to stop switching after the current switching cycle. The application is powered by the charge available in the output capacitor. No switching noise is generated, which can be beneficial in noise-sensitive sampled applications.

An MCU controlling this pin needs to take care to turn the device back on before the output voltage reaches a system critical level. Should this not happen, the output voltage is clamped to about 0.5 V below the set output voltage. In STOP mode, the device consumes typically 70 µA operating quiescent current from the input supply.

When a logic low level is applied to the STOP pin, the regulator immediately resumes switching operation without a start-up delay or soft start. To avoid a floating input, an internal 450-kΩ resistor pulls the STOP pin to GND. A control circuit disconnects the pulldown resistor at the STOP pin once a high level has been detected (similar to the EN pin).

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8.4 Device Functional Modes

8.4.1 Power-Save Mode Operation

The DCS-Control topology supports Power-Save Mode operation. At light loads, the device operates in PFM (Pulse Frequency Modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 60 nA. This low quiescent current consumption is achieved by an ultra-low power reference, an integrated high-impedance feedback divider network, and an optimized Power-Save Mode operation. To achieve a stable switching frequency in steady state operation, the on-time is calculated as in 式 2.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 556\text{ns} \tag{2}$$

In PFM Mode, the switching frequency varies linearly with the load current and is calculated in 式 3. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction mode with a nominal switching frequency (f_{SW}). The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

$$f_{PFM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \tag{3}$$

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to ultra-light loads. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM modes is seamless with minimum output voltage ripple.

8.4.2 Forced PWM Mode Operation

With a high level on the MODE input, the device enters forced PWM Mode and operates with a high switching frequency over the entire load range, even at very light loads. This reduces or eliminates interference with RF and noise-sensitive circuits, but reduces efficiency at light loads. The MODE pin can be changed during operation and must be terminated.

8.4.3 100% Mode Operation

In PWM mode, the duty-cycle of a buck converter is given as $D = V_{OUT}/V_{IN}$. The duty-cycle increases as the input voltage comes closer to the output voltage. Once the input voltage decreases to near 100% duty cycle, the output voltage set point is increased by +30 mV. As the input voltage decreases further, the device enters 100% duty-cycle mode and keeps the high-side MOSFET on continuously. The output (V_{OUT}) is connected to the input (V_{IN}) through the inductor and the internal high-side MOSFET. The minimum input voltage to maintain a given output voltage depends on the load current and is calculated as:

$V_{IN}min = V_{OUT} + I_{OUT} \times (R_{DS(on)}max + R_L)$

where

- I_{OUT} = output current
- $R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor

The TPS6284x contains special circuitry to keep an ultra-low I_Q of 120 nA during 100% mode operation.

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

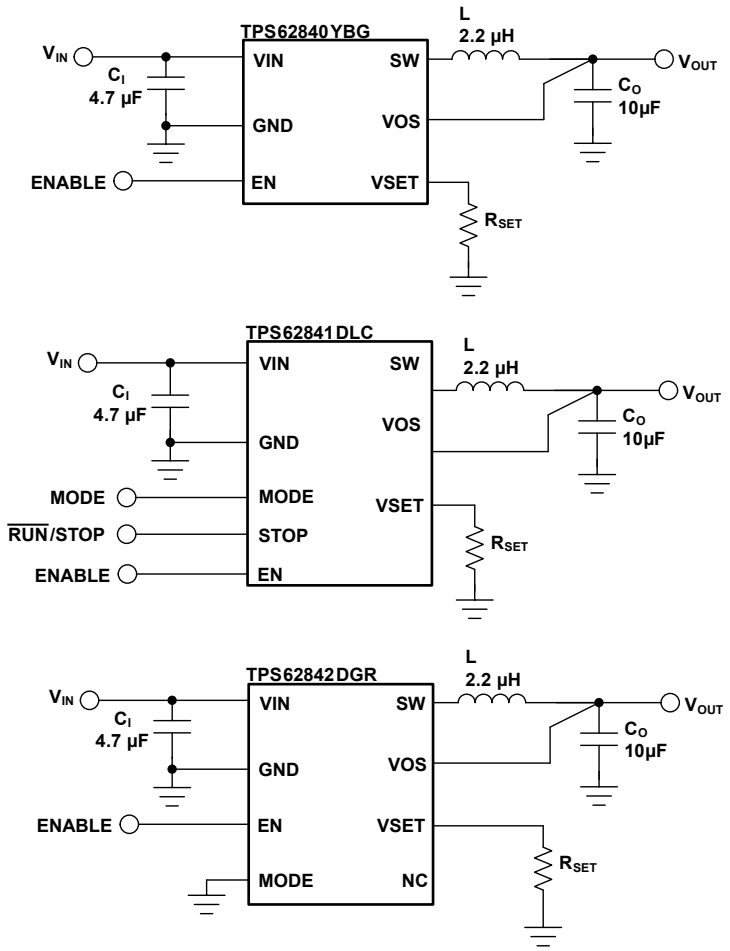


図 13. TPS6284x Application Circuit

Additional circuits are shown in the *System Examples*.

9.2.1 Design Requirements

表 2 shows the list of components for the application circuit and the characteristic application curves.

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Typical Application (continued)

表 2. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	VALUE	SIZE [L x W x T]	MANUFACTURER(1)
IC	TPS6284x step-down converter			TI
C_I	GRM155R61A475MEAAD ceramic capacitor	4.7 µF / 10 V / X5R	(0402) [1 mm x 0.5 mm x 0.65 mm max.]	muRata
C_O	GRM155R60G106ME44D ceramic capacitor	10 µF / 4 V / X5R	(0402) [1 mm x 0.5 mm x 0.65 mm max.]	muRata
L	DFE201612E-2R2M=P2 inductor	2.2 µH / 116 mΩ DCR	(2016) [2.0 mm x 1.6 mm x 1.2 mm max.]	muRata
R_{SET}	Resistor E96 series 1%, TC ±200ppm	See 表 1		

(1) See the *Third-party Products Disclaimer*.

9.2.2 Detailed Design Procedure

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 3 outlines possible inductor and capacitor value combinations.

表 3. Recommended LC Output Filter Combinations

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)	
	10 µF	22 µF
2.2	√(3)	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -20%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, PWM-to-PFM transition point, output voltage ripple, and efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to 式 4.

式 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with 式 5. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (4)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (5)$$

where

- f is the switching frequency
- L is the inductance
- ΔI_L is the peak-to-peak inductor ripple current
- I_{Lmax} is the maximum inductor current

表 4 shows a list of possible inductors.

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表 4. List of Possible Inductors(1)

INDUCTANCE [µH]	INDUCTOR TYPE	SIZE [L x W x T]	SUPPLIER
2.2	DFE201612E	[2.0 mm x 1.6 mm x 1.2 mm max.]	muRata
2.2	DFE201210S	[2.0 mm x 1.2 mm x 1.0 mm max.]	muRata

(1) See the *Third-party Products Disclaimer*.

9.2.2.2 Output Capacitor Selection

The DCS-Control scheme of the TPS62840 allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents, the converter operates in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. Larger output capacitors reduce the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

表 5. List of Possible Capacitors(1)

CAPACITOR VALUE [µF]	CAPACITOR TYPE	SIZE IMPERIAL (METRIC)	SIZE [L x W x T]	SUPPLIER
10	GRM155R60G106ME44D	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata

(1) See the *Third-party Products Disclaimer*.

9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-µF input capacitor is sufficient.

When operating from a high impedance source, a larger input buffer capacitor is recommended to avoid voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. 表 6 shows a selection of input and output capacitors.

表 6. List of Possible Capacitors(1)

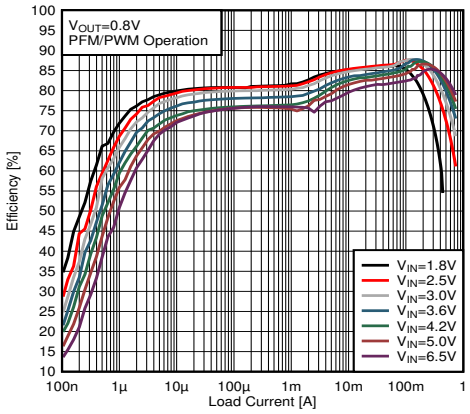
CAPACITOR VALUE [µF]	CAPACITOR TYPE	SIZE IMPERIAL (METRIC)	SIZE [L x W x T]	SUPPLIER
4.7	GRM155R61A475MEAAD	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata
4.7	GRM31CR71H475MA12L	1206 (3216)	[3.2mm x 1.6mm x 1.8mm max.]	muRata
4.7	C1608X7S1A475M080AC	0603 (1608)	[1.6mm x 0.8mm x 1.0mm max.]	TDK
10	GRM155R60J106ME15D	0402 (1005)	[1mm x 0.5mm x 0.65mm max.]	muRata

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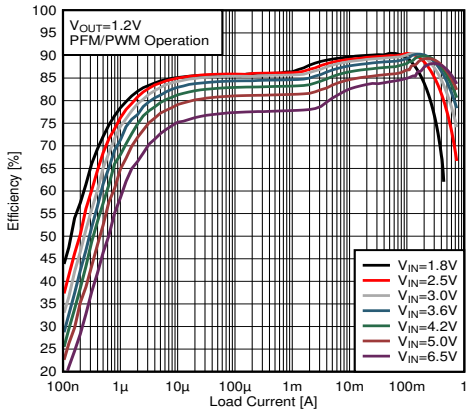
9.2.3 Application Curves

The conditions for the following application curves are V_{IN} = 3.6 V, V_{OUT} = 1.8 V, MODE = GND, STOP = GND, and the used components listed in 表 2, unless otherwise noted.



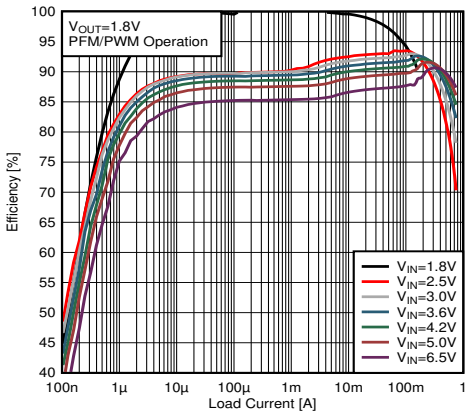
R_{SET} = GND

図 14. Efficiency Power Save Mode
V_{OUT} = 0.8 V



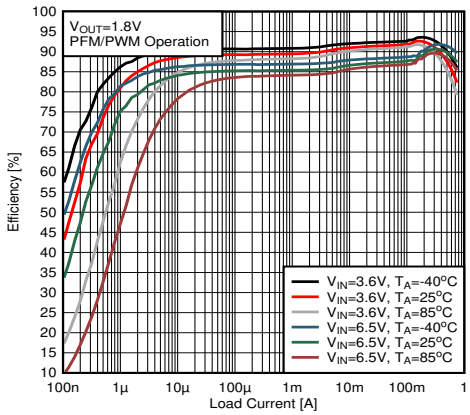
R_{SET} = 15.8 kΩ to GND

図 15. Efficiency Power Save Mode
V_{OUT} = 1.2 V



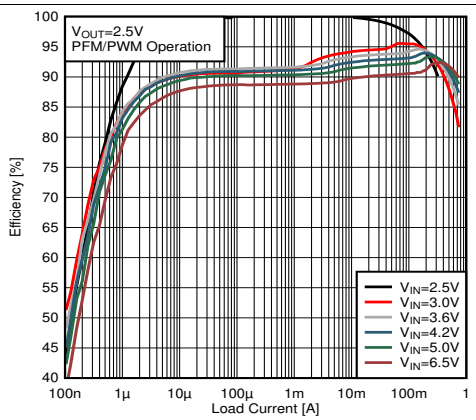
R_{SET} = GND

図 16. Efficiency Power Save Mode
V_{OUT} = 1.8 V



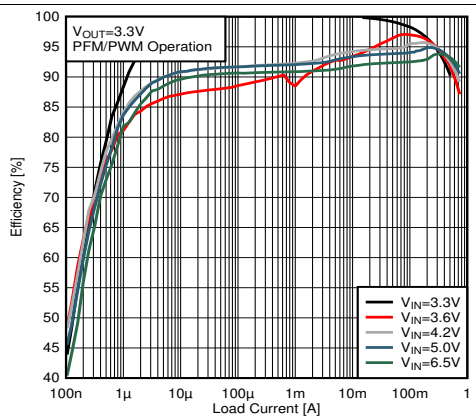
R_{SET} = GND

図 17. Efficiency Power Save Mode
V_{OUT} = 1.8 V



R_{SET} = 11.5 kΩ to GND

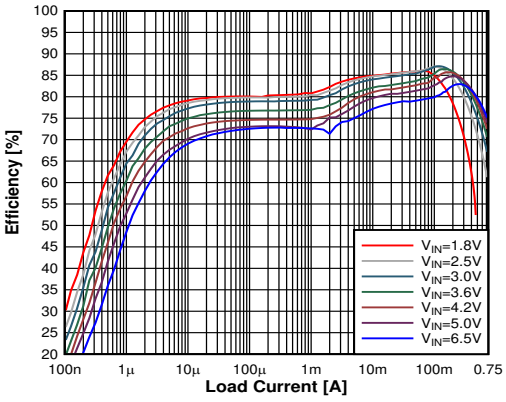
図 18. Efficiency Power Save Mode
V_{OUT} = 2.5 V



R_{SET} = 267 kΩ to GND

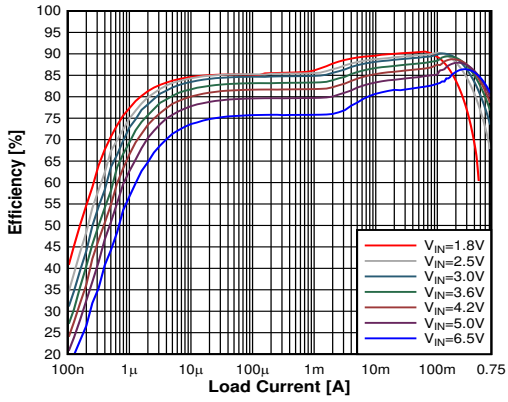
図 19. Efficiency Power Save Mode
V_{OUT} = 3.3 V

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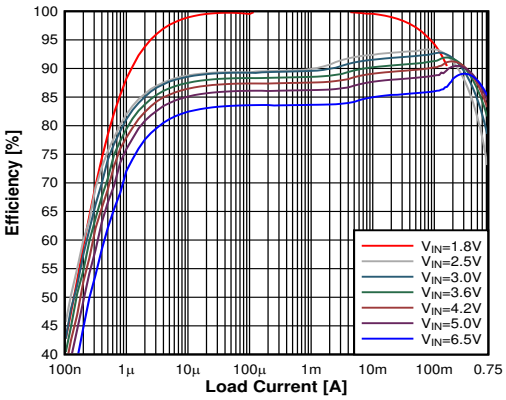
R_{SET} = GND

図 20. Efficiency Power Save Mode
V_{OUT} = 0.8 V for the DGR device



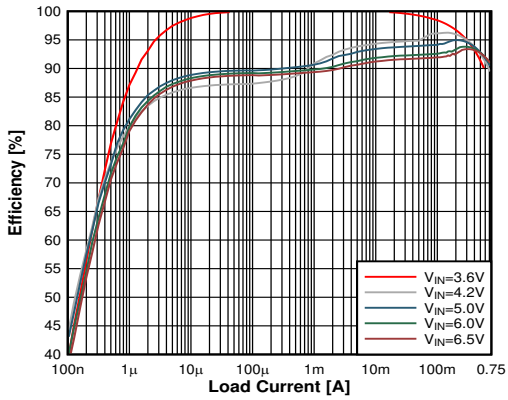
R_{SET} = GND

図 21. Efficiency Power Save Mode
V_{OUT} = 1.2 V for the DGR device



R_{SET} = GND

図 22. Efficiency Power Save Mode
V_{OUT} = 1.8 V for the DGR device



R_{SET} = 267 kΩ to GND

図 23. Efficiency Power Save Mode
V_{OUT} = 3.6 V for the DGR device

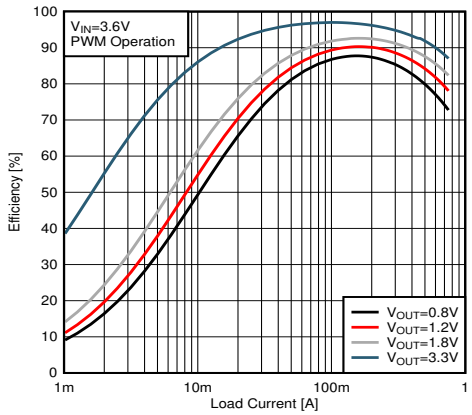
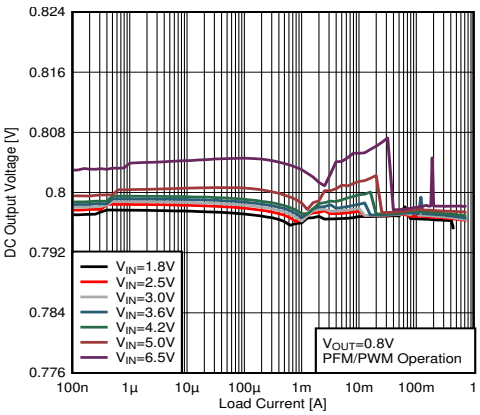


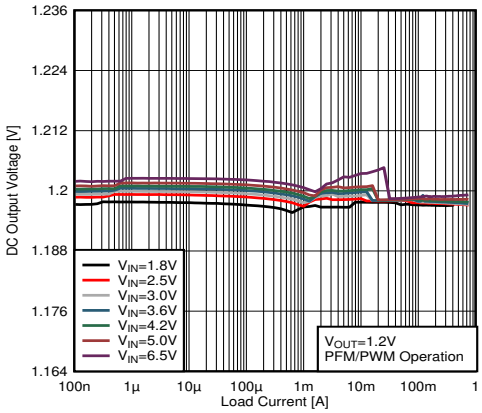
図 24. Efficiency Forced PWM Mode
V_{OUT} = 0.8 V / 1.2 V / 1.8 V / 3.3 V



R_{SET} = GND

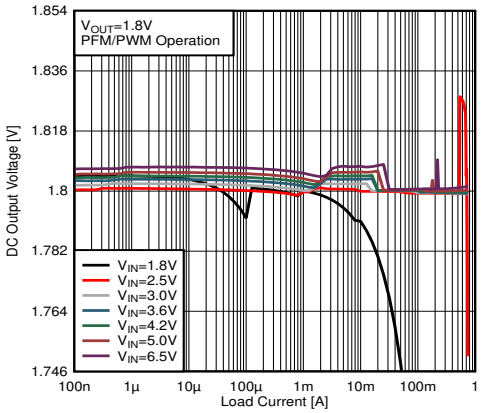
図 25. Output Voltage versus Load Current
V_{OUT} = 0.8 V

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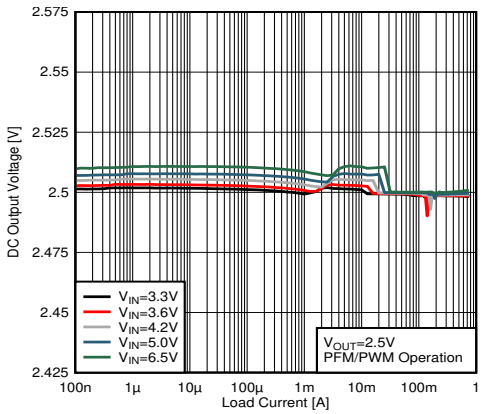
R_{SET} = 15.8k Ω to GND

図 26. Output Voltage versus Load Current
V_{OUT} = 1.2 V



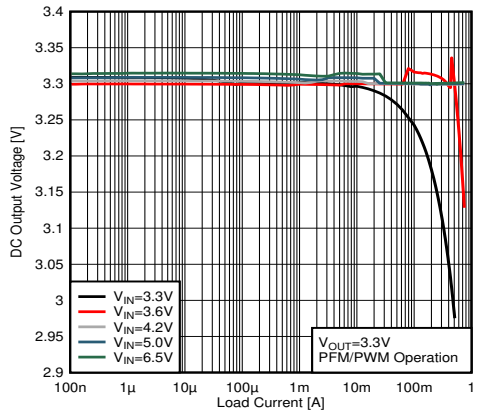
R_{SET} = GND

図 27. Output Voltage versus Load Current
V_{OUT} = 1.8 V



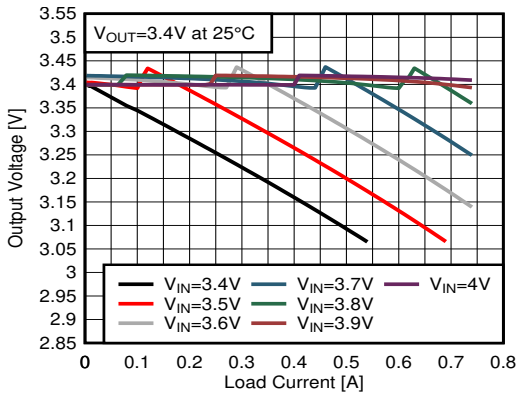
R_{SET} = 11.5 kΩ to GND

図 28. Output Voltage versus Load Current
V_{OUT} = 2.5 V



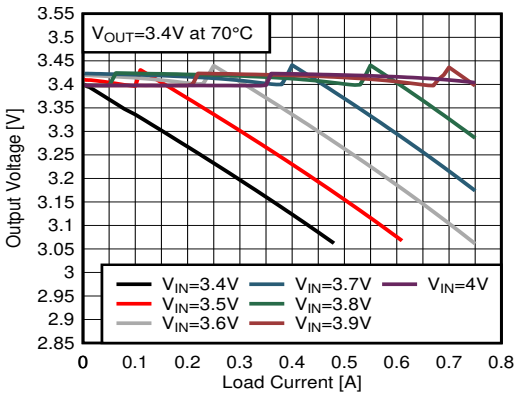
R_{SET} = 267 kΩ to GND

図 29. Output Voltage versus Load Current
V_{OUT} = 3.3 V



R_{SET} = GND

図 30. Output Voltage versus Load Current
V_{OUT} = 3.4 V



R_{SET} = GND

図 31. Output Voltage versus Load Current
V_{OUT} = 3.4 V

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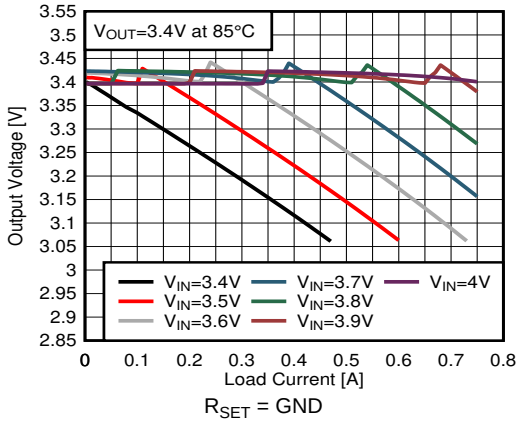


図 32. Output Voltage versus Load Current
V_{OUT} = 3.4 V

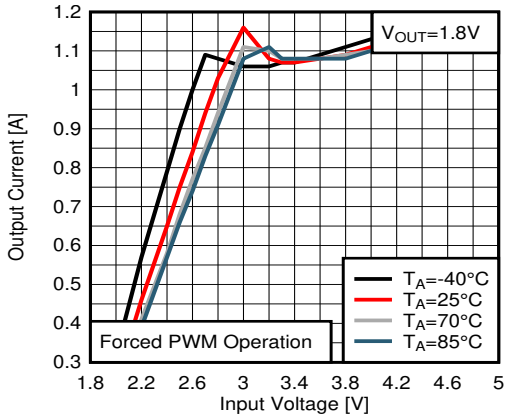


図 33. Maximum Output Current versus Input Voltage
V_{OUT} = 1.8 V

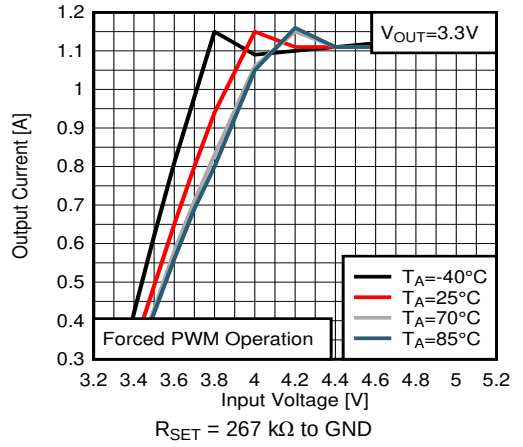


図 34. Maximum Output Current versus Input Voltage
V_{OUT} = 3.3 V

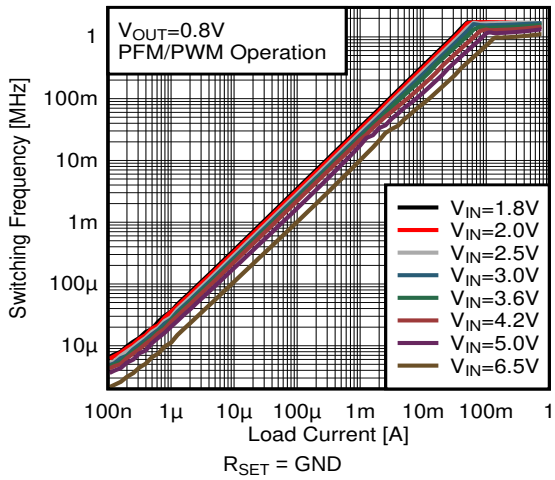


図 35. Switching Frequency versus Load Current
V_{OUT} = 0.8 V

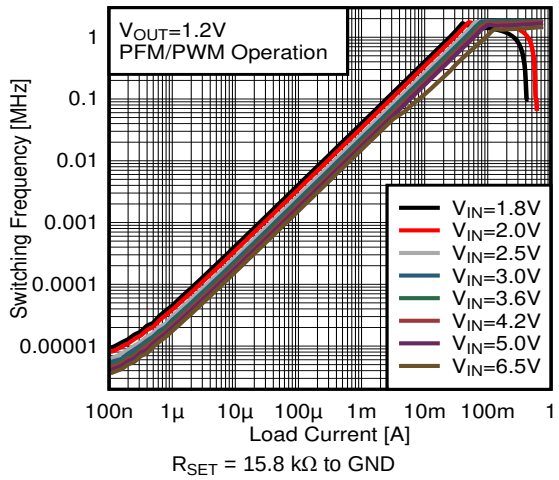


図 36. Switching Frequency versus Load Current
V_{OUT} = 1.2 V

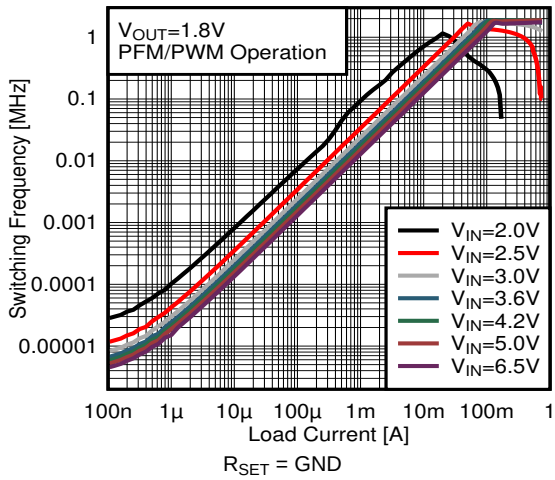
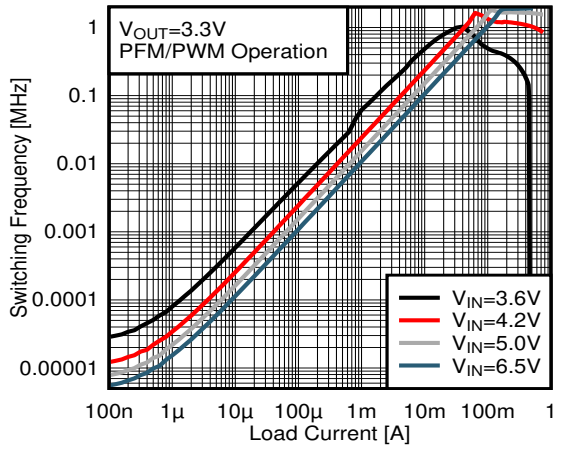


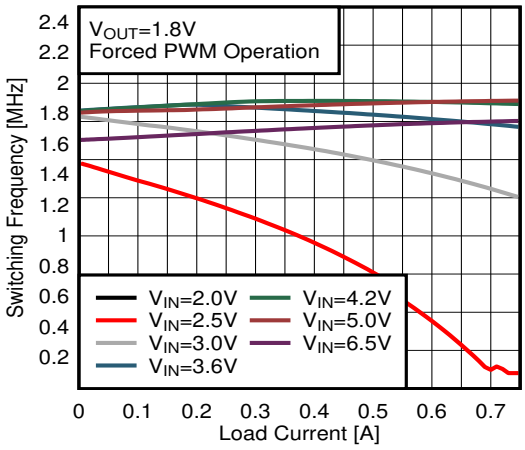
図 37. Switching Frequency versus Load Current
V_{OUT} = 1.8 V

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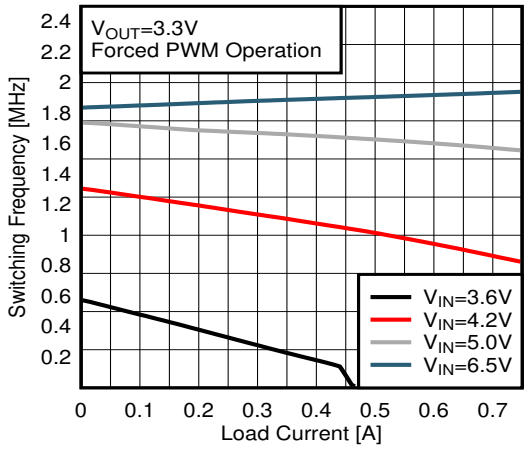
R_{SET} = 267 kΩ to GND

図 38. Switching Frequency versus Load Current
V_{OUT} = 3.3 V



R_{SET} = GND

図 39. Switching Frequency versus Load Current
V_{OUT} = 1.8 V



R_{SET} = 267 kΩ to GND

図 40. Switching Frequency versus Load Current
V_{OUT} = 3.3 V

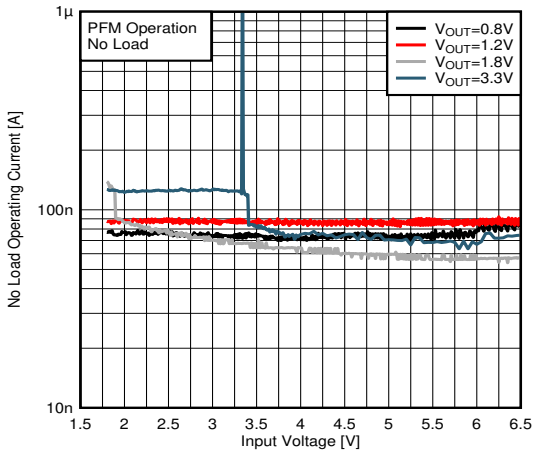


図 41. No Load Operating Current versus Input Voltage

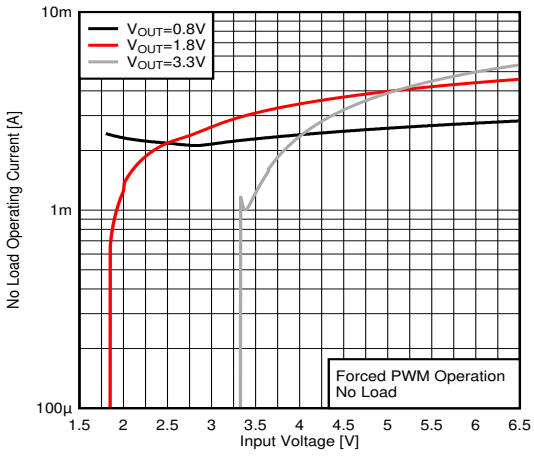
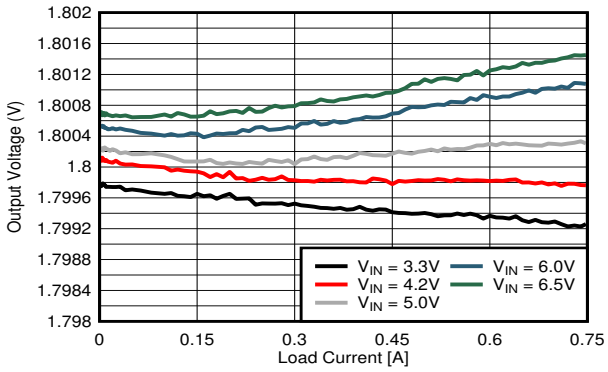


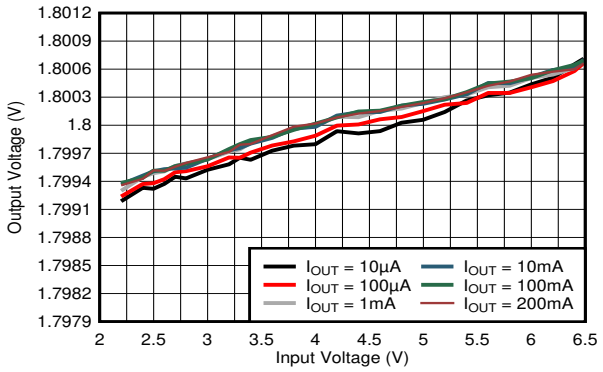
図 42. No Load Operating Current versus Input Voltage



EN = VIN　　MODE = HIGH

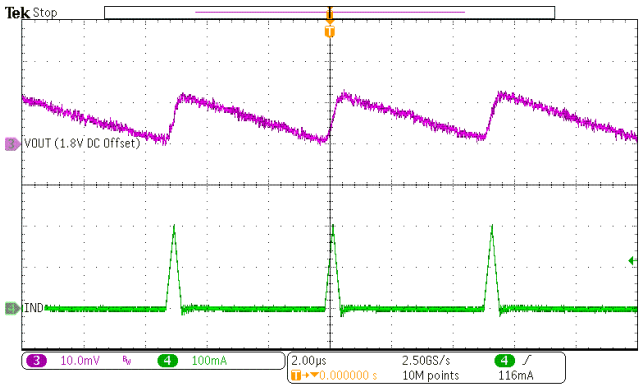
図 43. Output Voltage Accuracy (Load Regulation)

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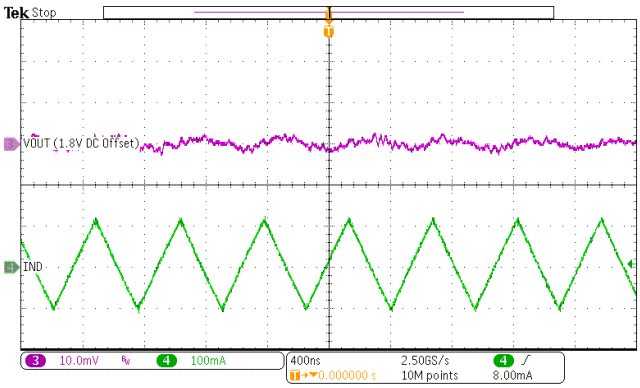
EN = VIN　　MODE = HIGH

図 44. Output Voltage Accuracy (Line Regulation)



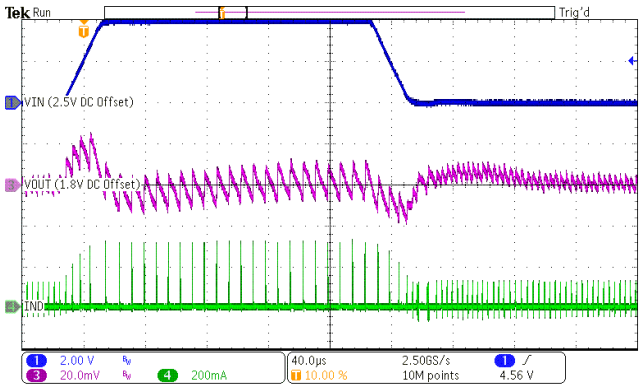
V_{OUT} = 1.8 V　　I_{OUT} = 10 mA

図 45. Output Voltage Ripple, PFM Operation



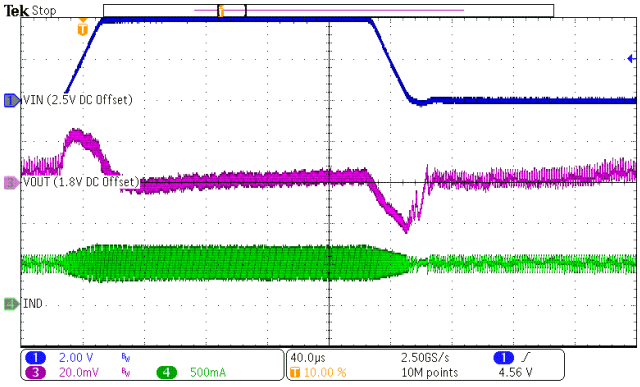
V_{OUT} = 1.8 V
MODE = HIGH　　I_{OUT} = 10 mA

図 46. Output Voltage Ripple, PWM Operation



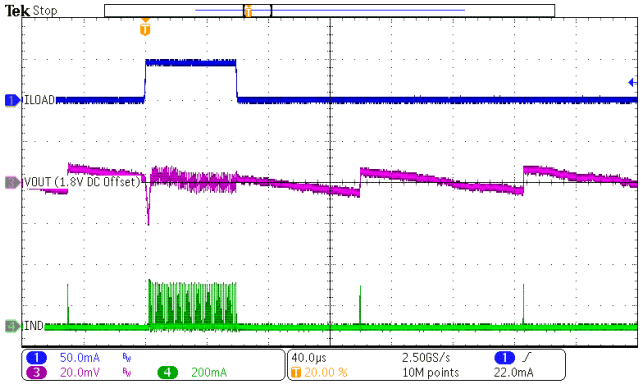
V_{OUT} = 1.8 V
rise/fall time = 20 µs　　V_{IN} = 2.5 V to 6.5 V
I_{OUT} = 10 mA

図 47. Line Transient PFM Mode



V_{OUT} = 1.8 V
rise/fall time = 20 µs　　V_{IN} = 2.5 V to 6.5 V
I_{OUT} = 500 mA

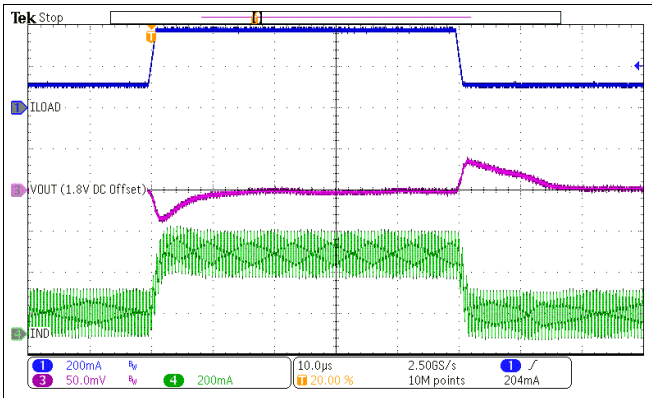
図 48. Line Transient PWM Mode



V_{OUT} = 1.8 V
rise/fall time < 1 µs　　V_{IN} = 3.6 V
I_{OUT} = 125 µA to 50 mA

図 49. Load Transient PFM Mode

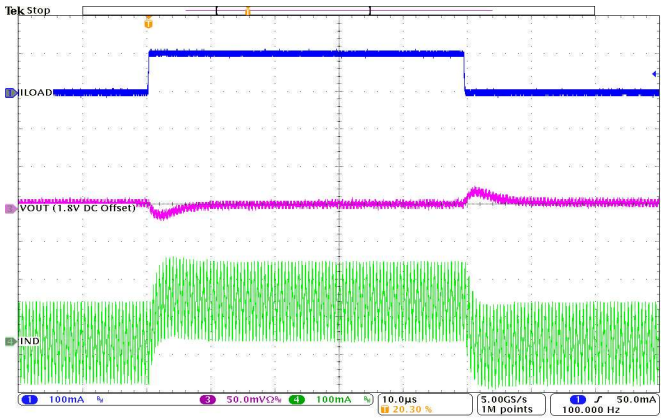
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V_{OUT} = 1.8 V
rise/fall time < 1 µs

V_{IN} = 3.6 V
I_{OUT} = 125 mA to 375 mA

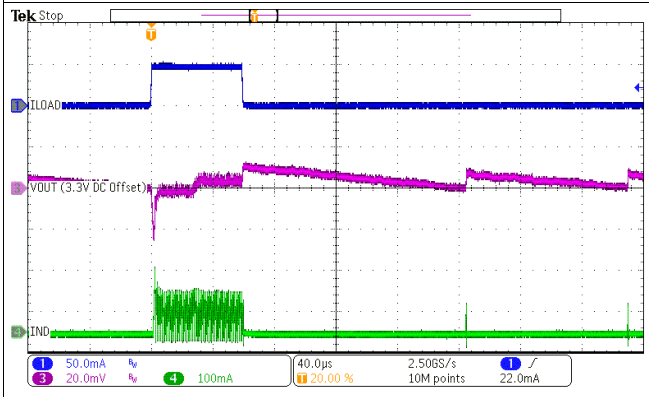
図 50. Load Transient PFM/PWM Mode



V_{OUT} = 1.8 V
rise/fall time < 1 µs

V_{IN} = 3.6 V
I_{OUT} = 0 A to 100 mA

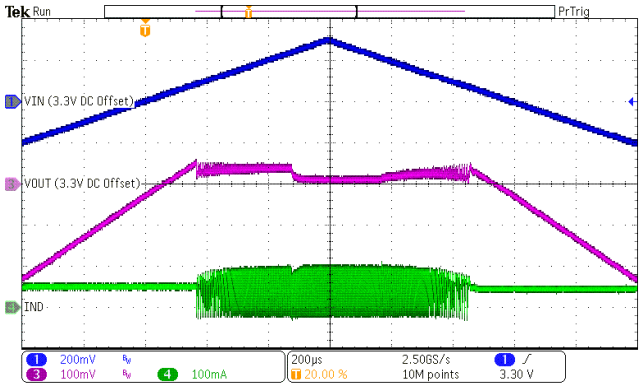
図 51. Load Transient PWM Mode from No load



V_{OUT} = 3.3 V
rise/fall time < 1 µs

V_{IN} = 3.6 V
I_{OUT} = 75 µA to 50 mA

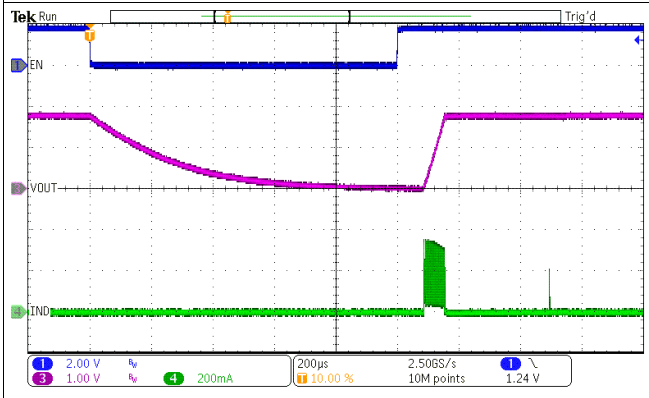
図 52. Load Transient PFM Mode



V_{OUT} = 3.3 V

V_{IN} = 3.1 V to 3.6 V
I_{OUT} = 50 mA

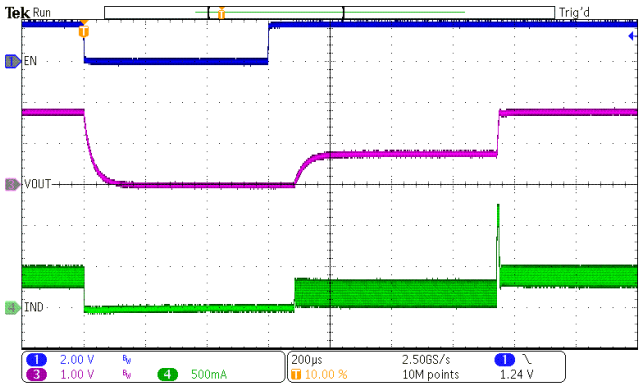
図 53. 100% Mode Entry/Exit Operation



V_{OUT} = 1.8 V
Turned on by EN input

V_{IN} = 3.6 V
I_{OUT} = 0 mA

図 54. Start-up/Shutdown into No Load

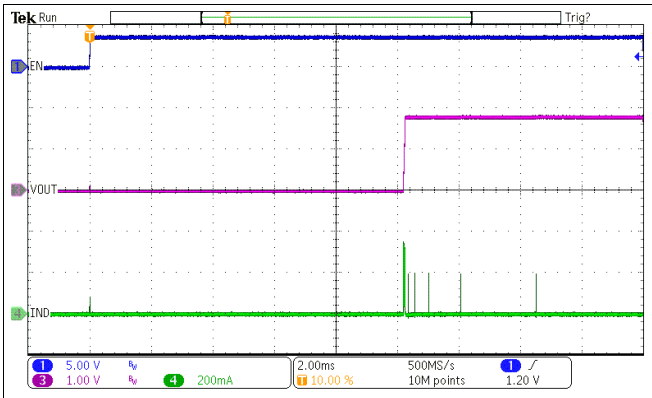


V_{OUT} = 1.8 V
Turned on by EN input

V_{IN} = 3.6 V
I_{OUT} = 400 mA
R_{LOAD} = 4.5 Ω

図 55. Start-up/Shutdown into Load

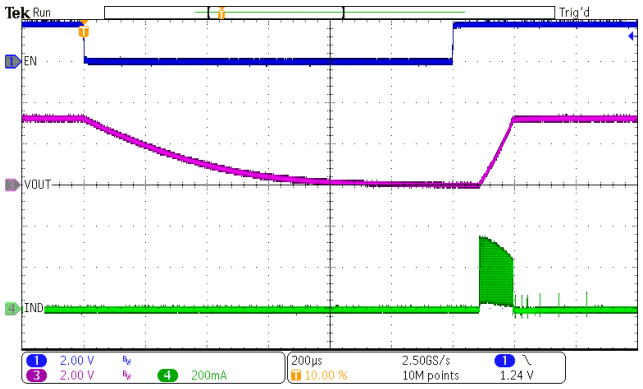
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V_{OUT} = 1.8 V
V_{IN} rising from 0 V to 3.6 V

EN = V_{IN}
I_{OUT} = 0 mA

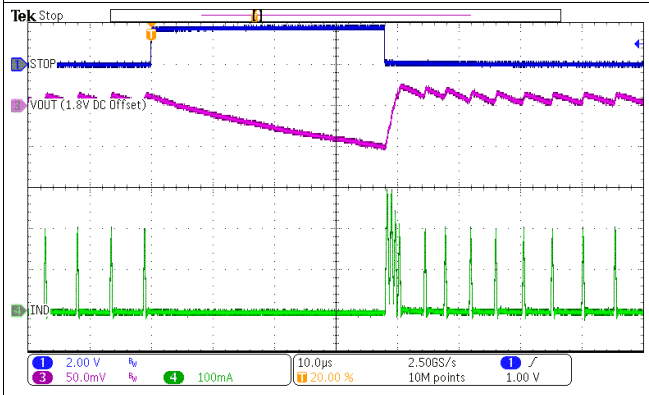
図 56. Start-up/Shutdown into No Load



V_{OUT} = 3.3 V
Turned on by EN input

V_{IN} = 3.6 V
I_{OUT} = 0 mA

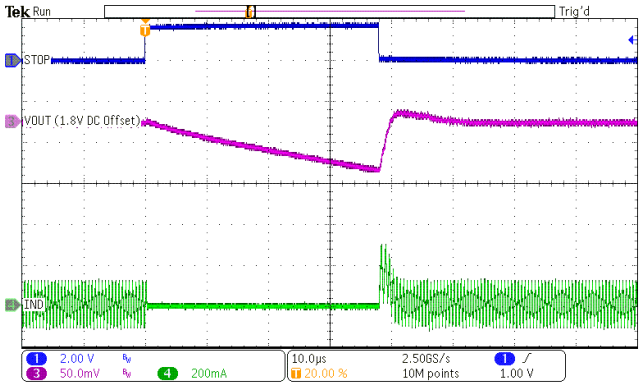
図 57. Start-up/Shutdown into No Load



V_{OUT} = 1.8 V
PFM Operation

V_{IN} = 3.6 V
I_{OUT} = 10 mA

図 58. STOP Mode Operation



V_{OUT} = 1.8 V
PWM Operation

V_{IN} = 3.6 V
I_{OUT} = 10 mA

図 59. STOP Mode Operation

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9.3 System Example

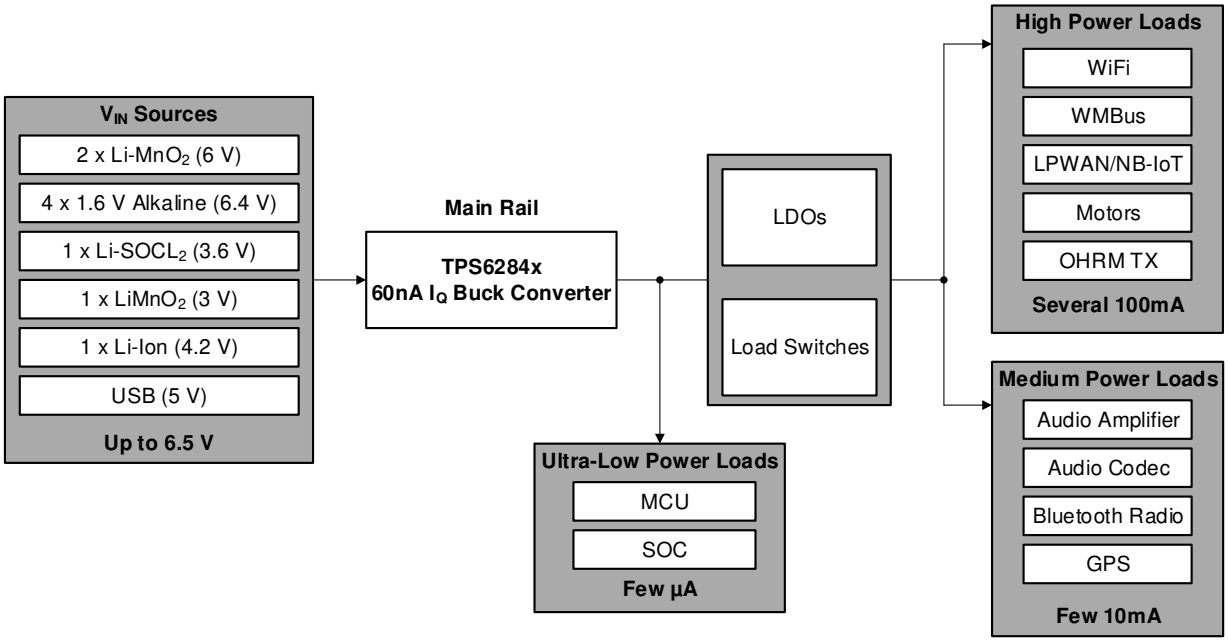


図 60. The Broad Range of Input Voltage Sources and Various Power Loads that TPS6284x Can Support

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62840.

11 Layout

11.1 Layout Guidelines

The TPS62840 pinout has been optimized to enable a single layer PCB routing of the device and its critical passive components such as C_{IN}, C_{OUT}, and L.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

11.2 Layout Example

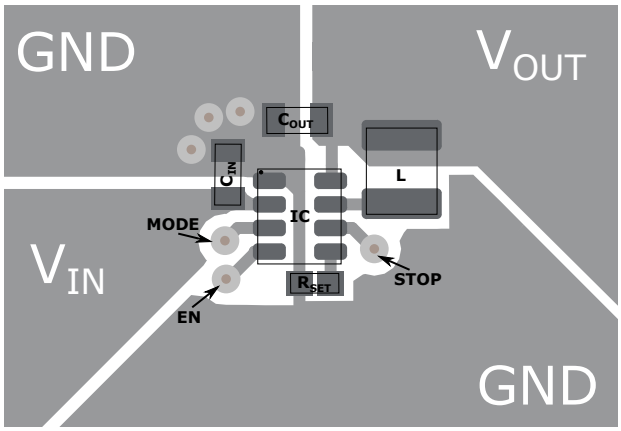


図 61. Recommended PCB Layout
DLC Package

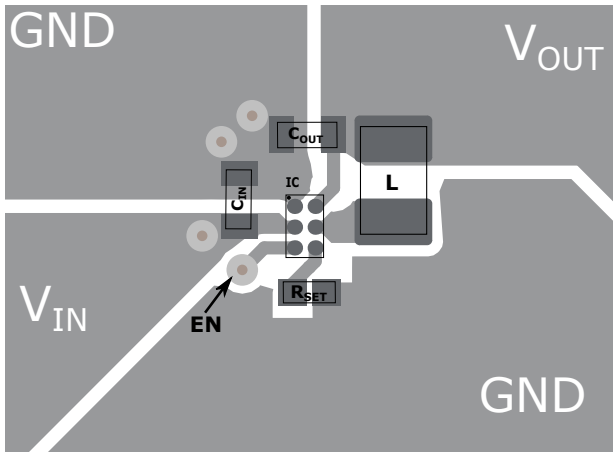


図 62. Recommended PCB Layout
YBG Package

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Layout Example (continued)

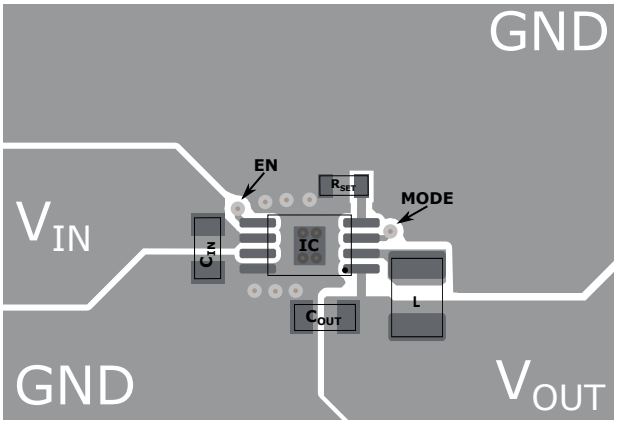


図 63. Recommended PCB Layout
DGR Package

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

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12.4 静電気放電に関する注意事項



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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62840DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	E5	Samples
TPS62840YBGR	ACTIVE	DSBGA	YBG	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	62840	Samples
TPS62841DGRR	ACTIVE	HVSSOP	DGR	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T841R	Samples
TPS62841DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	E9	Samples
TPS62841YBGR	ACTIVE	DSBGA	YBG	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	62841	Samples
TPS62842DGRR	ACTIVE	HVSSOP	DGR	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T842R	Samples
TPS62849DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	FF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

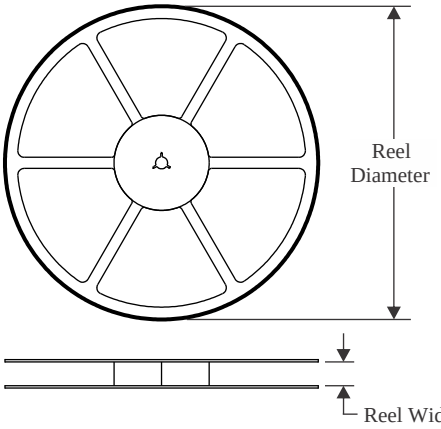
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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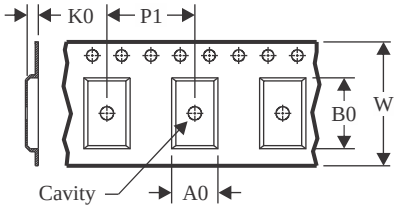
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

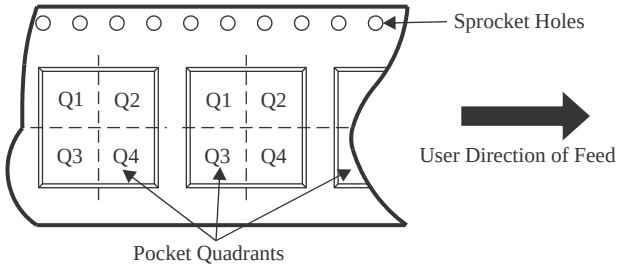


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

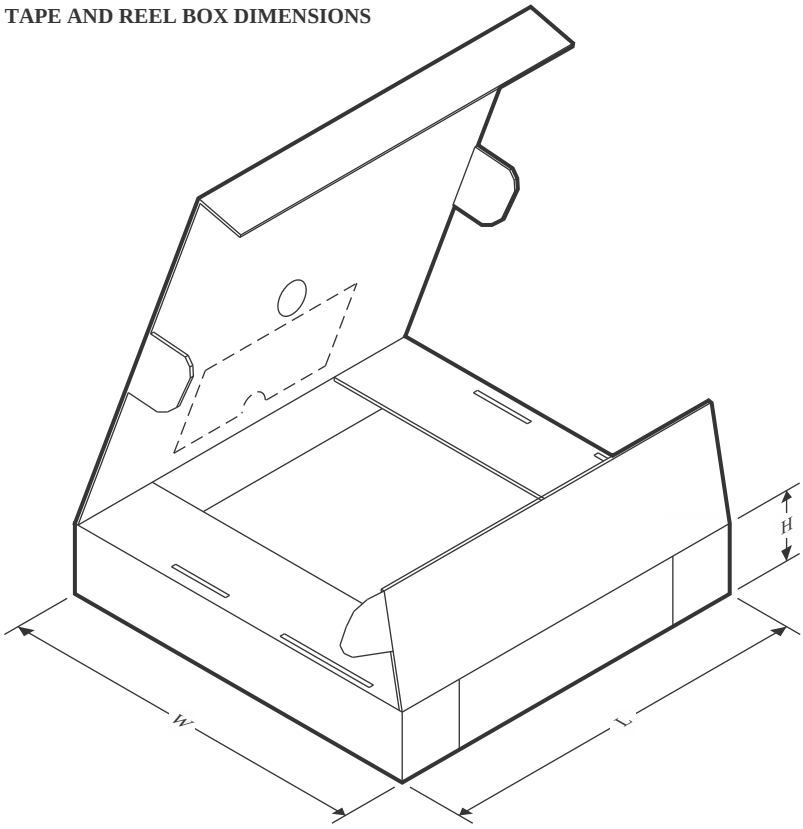
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62840DLCR	VSON-HR	DLC	8	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62840YBGR	DSBGA	YBG	6	3000	180.0	8.4	1.14	1.64	0.59	4.0	8.0	Q1
TPS62841DGRR	HVSSOP	DGR	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62841YBGR	DSBGA	YBG	6	3000	180.0	8.4	1.14	1.64	0.59	4.0	8.0	Q1
TPS62842DGRR	HVSSOP	DGR	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



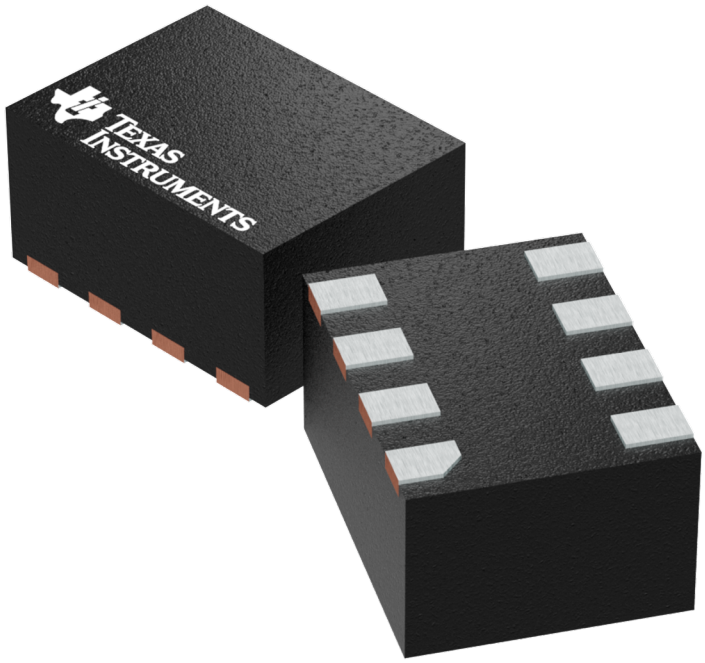
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62840DLCR	VSON-HR	DLC	8	3000	182.0	182.0	20.0
TPS62840YBGR	DSBGA	YBG	6	3000	182.0	182.0	20.0
TPS62841DGRR	HVSSOP	DGR	8	2500	366.0	364.0	50.0
TPS62841YBGR	DSBGA	YBG	6	3000	182.0	182.0	20.0
TPS62842DGRR	HVSSOP	DGR	8	2500	366.0	364.0	50.0

DLC 8 VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

2.0 x 1.5 mm, 0.5 mm pitch



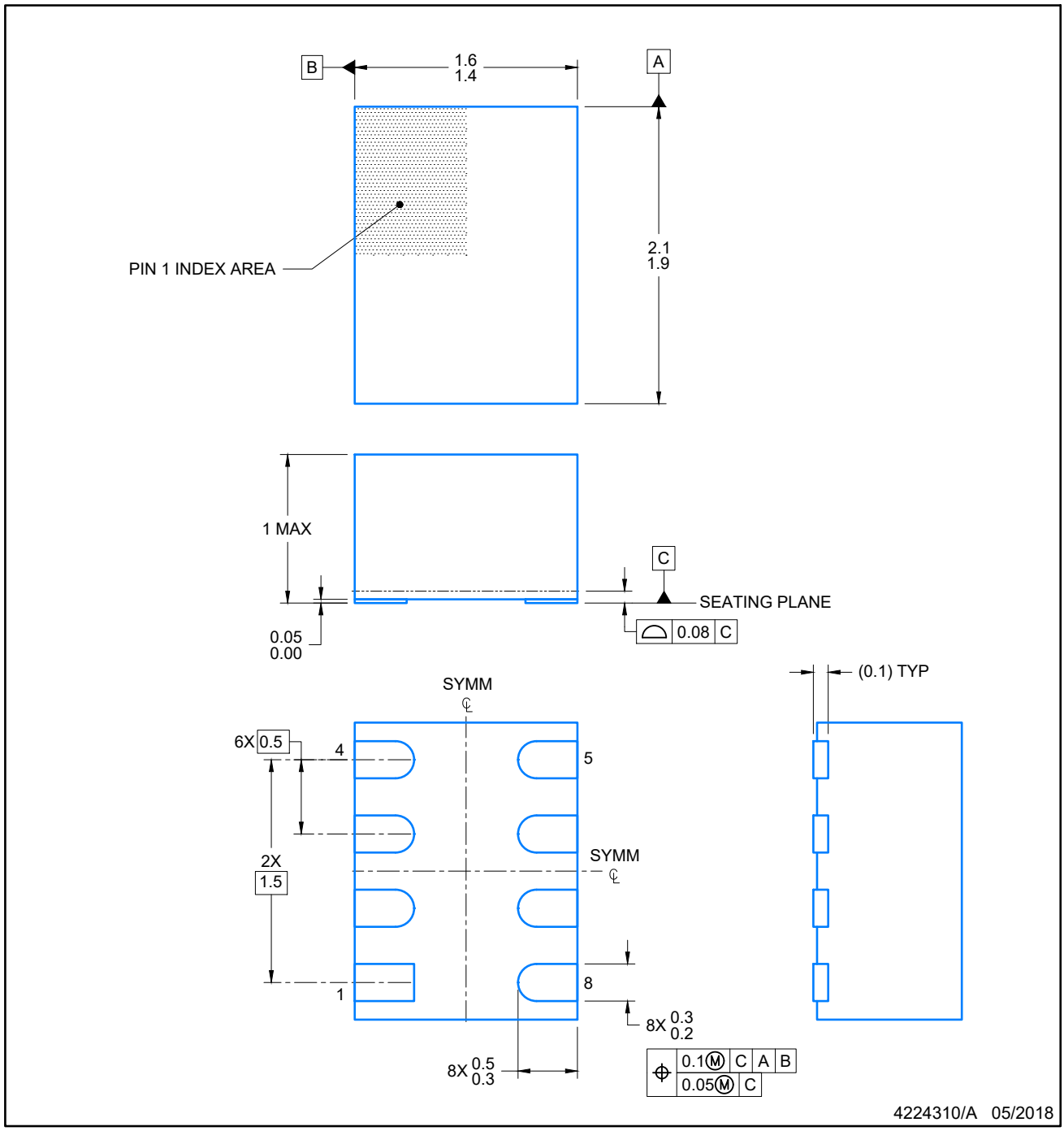
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DLC0008B

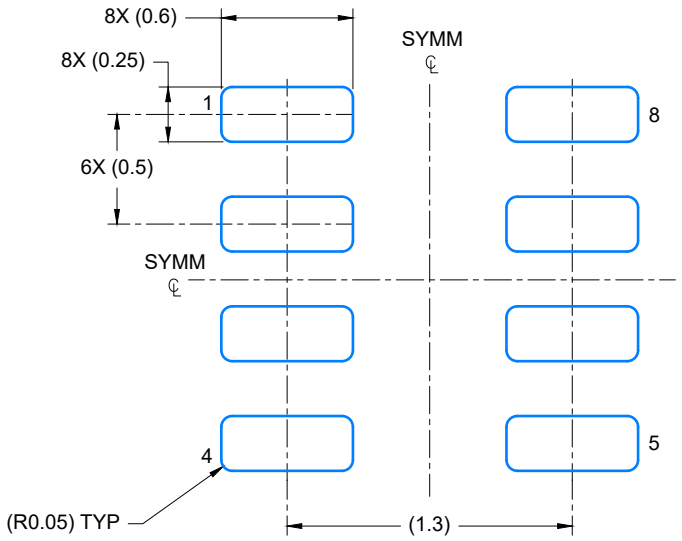
VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

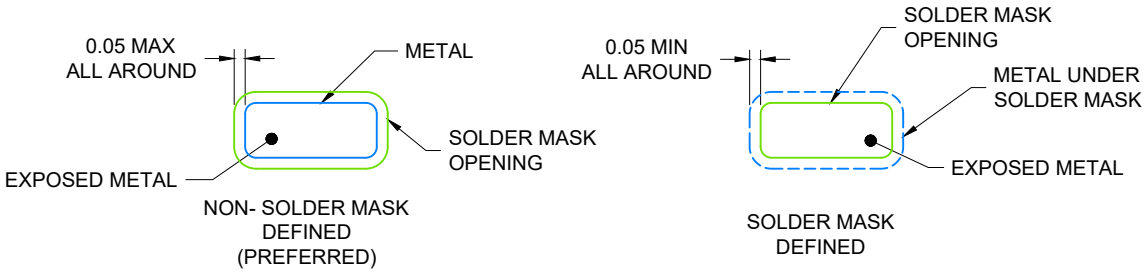


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

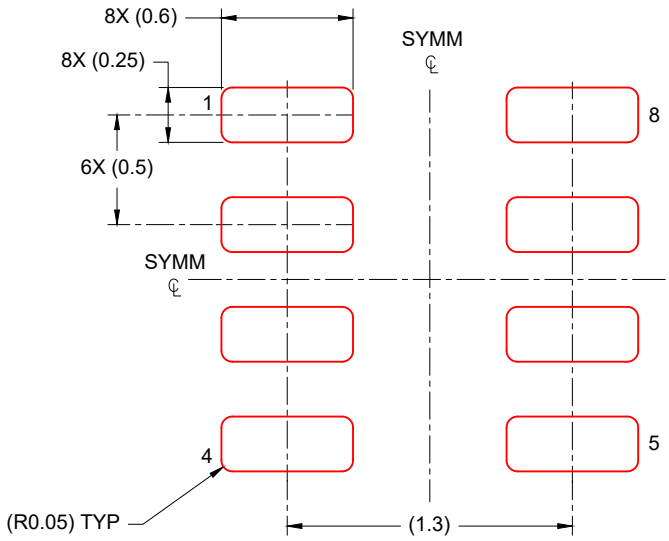


SOLDER MASK DETAILS

4224310/A 05/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224310/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

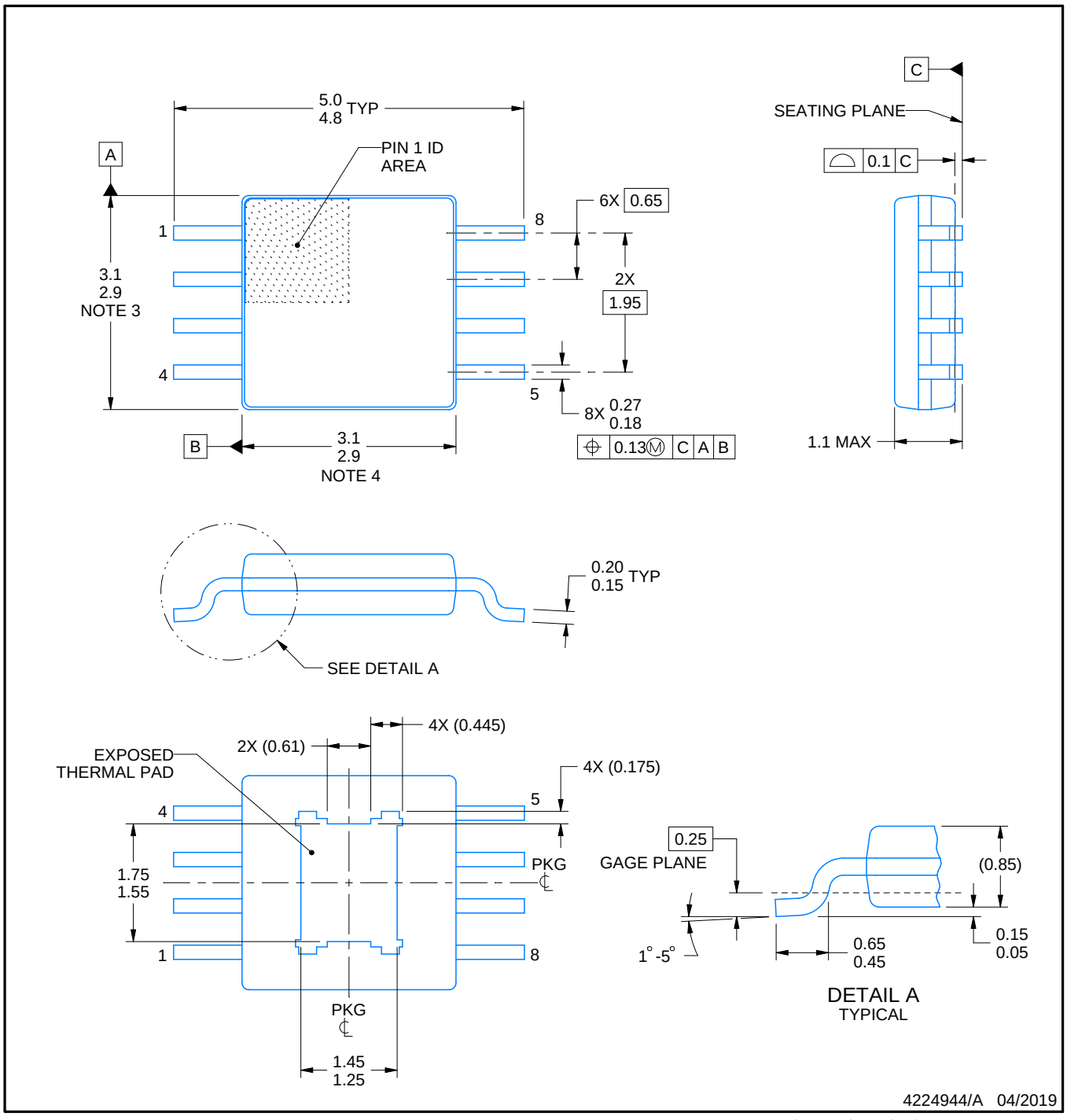
PACKAGE OUTLINE

DGR0008A



VSSOP PowerPAD™ - 1.1 mm max height

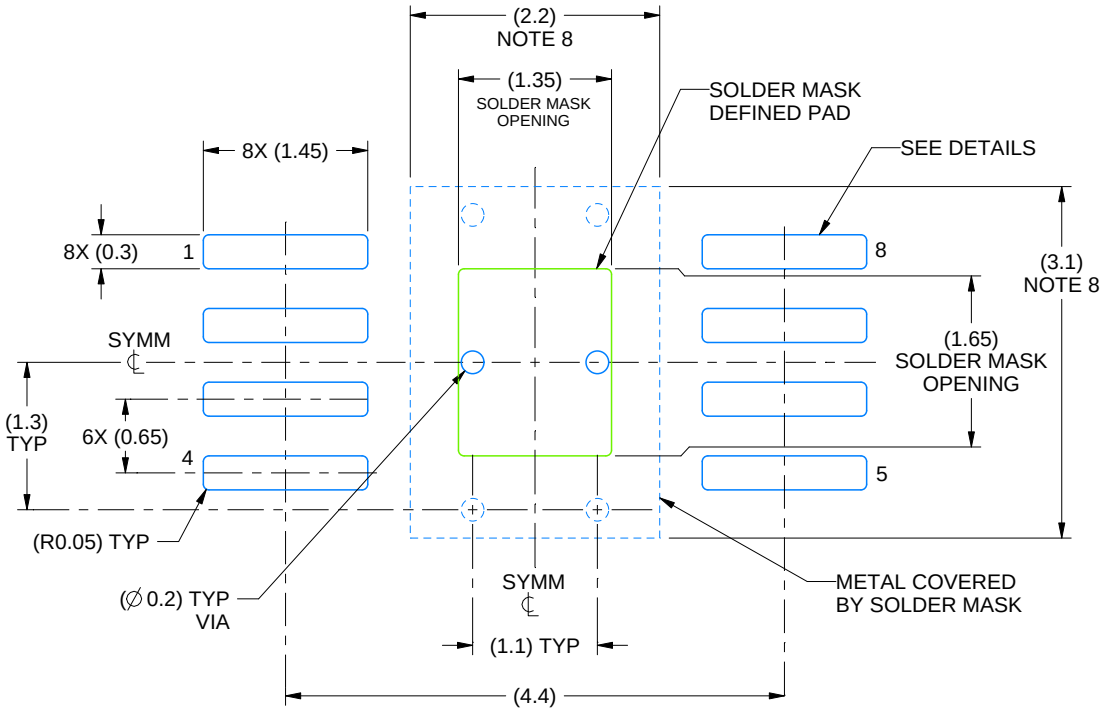
PLASTIC SMALL OUTLINE



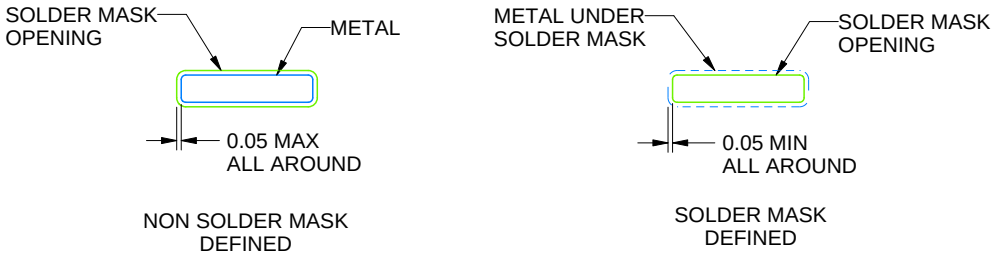
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.3 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

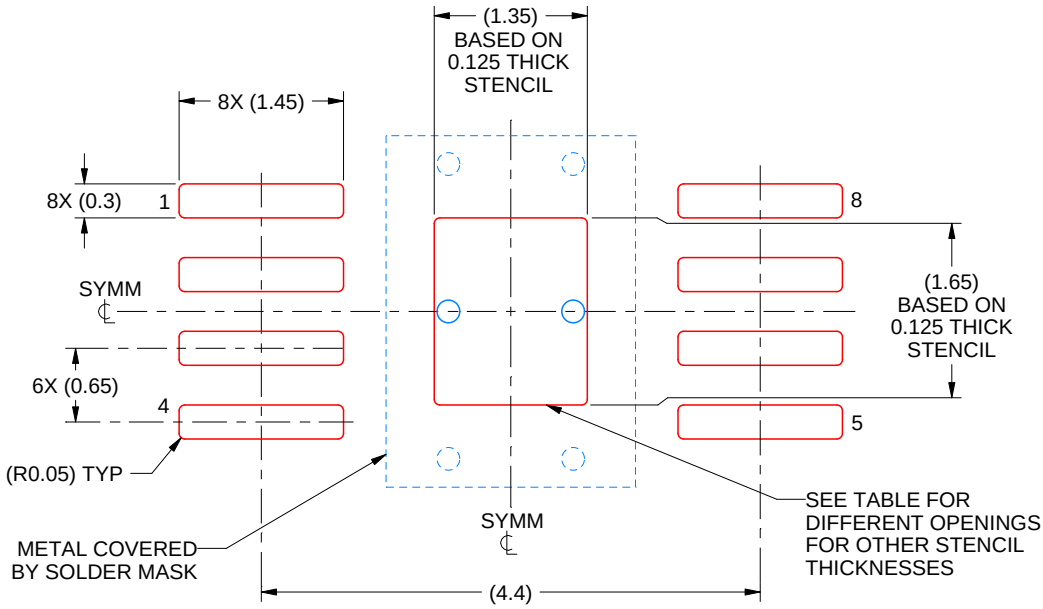


SOLDER MASK DETAILS

4224944/A 04/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.51 X 1.84
0.125	1.35 X 1.65 (SHOWN)
0.150	1.23 X 1.51
0.175	1.14 X 1.39

4224944/A 04/2019

NOTES: (continued)

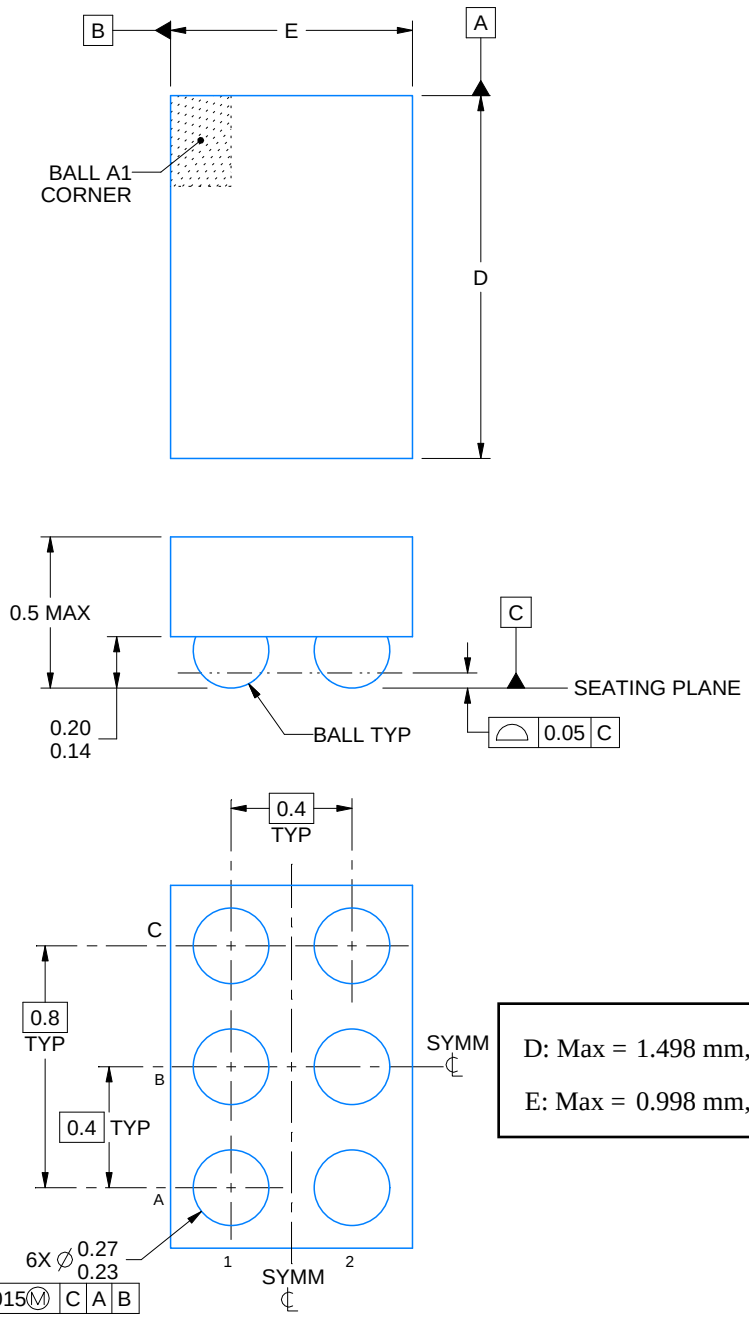
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4224328/A 05/2018

NOTES:

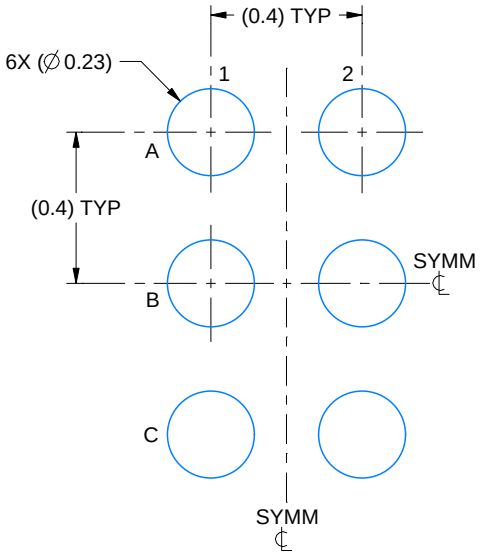
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

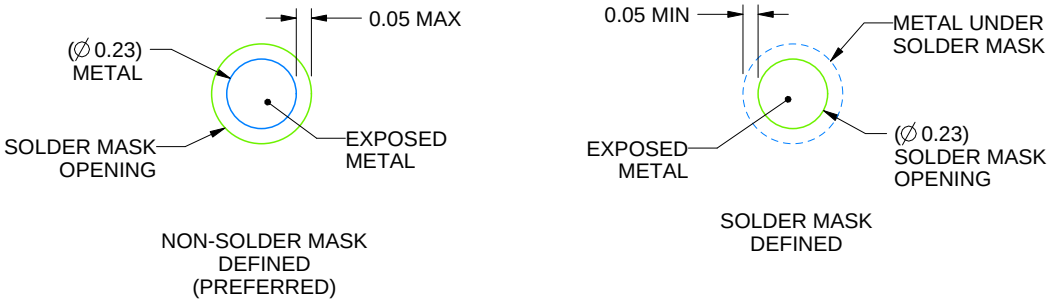
YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4224328/A 05/2018

NOTES: (continued)

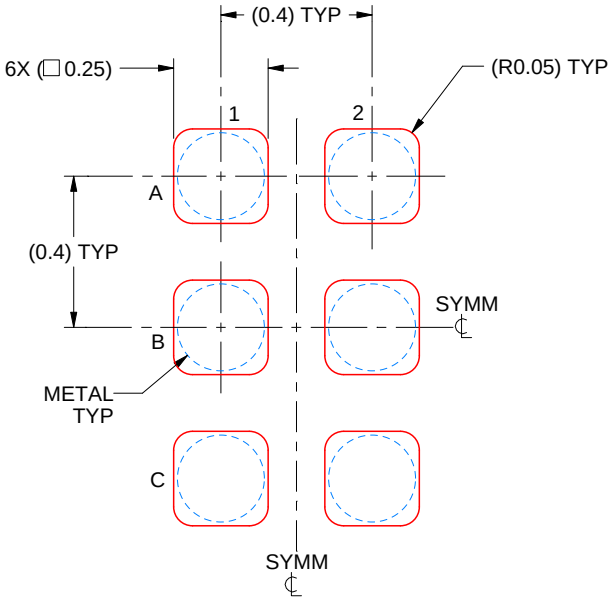
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4224328/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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