System Design Considerations when Upgrading from JESD204B to JESD204C

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ABSTRACT

The purpose of this paper is to highlight the major differences between the JESD204B and JESD204C revisions of Serial Interface Standard for Data Converters. Users of a JESD204-compatible system can apply this knowledge when evaluating the physical layers, link layers, and transport layers of the two revisions. Based on the differences highlighted in this paper and the evaluation results, the user can then make an informed decision when choosing the best standard revision for their systems.

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1   Introduction

The revision C of the Serial Interface for Data Converters, or JESD204C, was completed on December 2017. It offered new possibilities for higher throughput and higher density serial link standard when connecting between data converters and logic devices (that is FPGA/ASICs). With emergence of technologies such as the 5G telecom standard challenging the industry with the need for wider bandwidth and higher components density, system developers are often tempted to adopt the JESD204C as the way moving forward.

The purpose of this application report is to help decide whether to upgrade every system developer's unique project and to highlight the difference between the JESD204 revision B and revision C. This application report also equips system developers with the knowledge needed to analyze each feature to see if the current system and future projects are worthy of the upgrade. The intended audience for this document is the system developers who are planning on using the JESD204 protocol, and are evaluating the trade-offs between the two revisions. Hopefully, this document can help the developers make an informed decision when choosing the JESD204 revisions.

2   Terminologies

- J-RX: JESD204 receiver
  - FPGA/ASIC in ADC link
  - DAC in DAC link
- J-TX: JESD204 transmitter
  - ADC in ADC link
  - FPGA/ASIC in DAC link
- Logic Devices: Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuits (ASIC)

3   Assumed Knowledge

1. The user understands common JESD204 abbreviations, such as LMFS. Refer to TI training link for additional information.
   - https://training.ti.com/high-speed-signal-chain-university
2. The user understands the basic difference between each JESD204 layers: SERDES PHY, Link Layer, and Transport Layer.

4   Major Changes: Three Supported Encoding Options

The first and major change in the revision C is the support for 64B/66B encoding similar to the updated 10G Fiber Channel and 10G Gigabit Ethernet standard. The revision still maintains backward compatibility of 8B/10B, as well as the support of 64B/80B to maintain a proper "gearbox" ratio of the data converter clocking setup. The 64B/66B now has a coding efficiency of close to 97%, as opposed to the 80% coding efficiency of the 8B/10B coding and the 64B/80B coding.

4.1   *What Does This Mean for System Developers?*

System developers now push for higher data rates of the data converters without necessarily increasing the SERDES interface rate significantly. Table 1 compares the SERDES rate difference for a typical data converter setup with one lane supporting one pair of I/Q sample stream (LMFS of 12410 for one data converter). Each I or Q sample stream is a typical telecom operating rate of 491.52 MSPS.

Table 1. SERDES Rate Difference Between the Encoding Options

ENCODING OPTION	EFFECTIVE BIT RATE (BEFORE ENCODING) INTO ONE LANE	EFFECTIVE BIT RATE (AFTER ENCODING) INTO ONE LANE	RATIO OF SERDES RATE 491.52 MSPS DATA CONVERTER RATE
8B/10B	2x16bitsx491.52 MSPS = 15.72864 Gbps	15.72864 Gbps × 10/8 = 19.6608 Gbps	40
64B/66B	Same	15.72864 Gbps × 66/64 = 16.22016 Gbps	33

System developers can draw some conclusions from Table 1:

1. The 64B/66B encoding option reduced the SERDES rate by roughly 17.5%. The SERDES rate reduction can be sufficient enough to allow the bundle of a slower rate SERDES IP class to the FPGA/ASIC or data converter devices while delivering the same throughput as 8B/10B encoding option.

2. The ratio of the SERDES rate and the data converter rate (that is the baseband rate) implies the device clocking and clocking ratio setup of the SERDES PHY and the digital logics in the signal chain (that is the FIRs, digital mixers, and numerically controlled oscillators). The 8B/10B option provides a ratio with flexible common denominators for the clock divider setup. This is not necessarily true for the 64B/66B option, and the actual FPGA/ASIC firmware or data converter design needs to have a proper gearbox setup to accommodate such ratio.

4.2   Things to Consider

1. There are certain high ranges of the SERDES interface rate where 8B/10B is no longer recommended, and there are certain low ranges of the SERDES interface rate where 64B/66B and 64B/80B are not recommended. See Table 4 of the JESD204C document for details. The example shown in Table 1 has the 8B/10B option at 19.6608 Gbps, which is not recommended by the JESD204C standard. This is mainly due to the 8B/10B encoding not having sufficient coding spectral richness for the SERDES equalization at the higher rate to properly adapt without additional care. However, some developers still prefer the 8B/10B option due to the dedicated link establishment period in the handshaking protocol. See Section 6 for details.

Table 2. Supported Link Layers Versus Data Rate[1]

DATA RATE (DR) (Gbps)	8B/10B	64B/66B	64B/80B
DR <= 6.375	Required	Not recommended	Not recommended
6.375 < DR <= 12.5	Required	Recommended	Optional
12.5 < DR <= 16	Optional	Required	Optional
16 < DR <= 32	Not recommended	Required	Optional

[1]   Table 4 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

2. Moving to a higher SERDES rate for 8B/10B encoding beyond the JESD204 standard recommendation is possible. There are a few ASIC, FPGA, and data converters IP that support such higher rate. The main limitation is the SERDES PHY receivers DFE adaptation. Typically, moving to a higher SERDES rate requires an increasing number of DFE taps needing adaptation. The fixed handshaking K28.5 characters during the initial link establishment do not provide the sufficient spectral richness for the adaptation, and hence can cause instability in link establishments. This is especially a concern during the initial ASIC/FPGA/data converter link training where the handshaking protocols and SERDES PHY receivers adaptation occur at the same time. Engineers need to review the initialization sequence of each device carefully to ensure the SERDES PHY receivers have sufficient DFE training time and do not overlap with the handshaking protocol time.

3. If the developers need to upgrade their system for higher data throughput, they can increase the number of JESD204 lanes. If the system has no additional lanes available, the effective JESD204 throughput rate has to increase. Staying in 8B/10B increases the SERDES rate. Upgrading to 64B/66B decreases the SERDES rate, and the user needs to either add additional development to support the 64B/66B link protocol or purchase additional JESD204C IP for the FPGA/ASIC. The developer needs to consider the overall cost and effort of: 1) increasing the number of JESD204 lanes, 2) increasing in SERDES rate, and 3) JESD204C protocol upgrade or purchase of the new IP.

5   Physical Layer Specification: Additional Classifications to Address Different JESD204 Channel Properties

In most of the JESD204B interface bring-up scenarios, the majority of the challenges arise from the basic link protocols such as code group synchronization error (mis-handling of K28.5 handshaking signal), frame/multi-frame errors (mis-configuration of the K value and internal clocking), and basic release buffer overrun (non-optimized release buffer for the given link). Although other typical errors such as 8B/10B not-in-table error or 8B/10B disparity error can arise within the encoding and decoding process within the link layer, the system developer needs to also look into the physical layer impact to the link quality.

The JESD204 committee re-classified the former JESD204B physical layer into Class B and added a separate Class C specification. The exact specification can be found in Table 12 of the JESD204C specification.

Table 3. Device Classification[1]

DEVICE CLASS CATEGORY	DEVICE CLASS	SUPPORTED DATA INTERFACE
B	B-3	The 3.125 Gbps (max) data interface
	B-6	The 6.375 Gbps (max) data interface
	B-12	The 12.5 Gbps (max) data interface
C	C-S	The C-S (short) class 32 Gbps (max) data interface
	C-M	The C-M (medium) class 32 Gbps (max) data interface
	C-R	The C-R (reflective) class 32 Gbps (max) data interface

[1]   Table 12 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

The following is a summary of the two specifications:

1. The Class B (former JESD204B physical layer specification) category minimum rate is 312.5 Mbps. The maximum rate supported are different for B-3, B-6, and B-12. This is the former JESD204B standard for up to 12.5 Gbps interface rate.

2. The Class C (newly addition to the JESD204C) category minimum rate is 6.375 Gbps. Each class can support a maximum of 32 Gbps. Each class has different transmission channel characteristics of short reach, medium reach, and reflective.

Class C introduced several SERDES implementation recommendations for each of the specified channel qualities such as short reach (C-S), medium reach (C-M), or highly reflective (C-R). The primary method to categorize these channel qualities are channel length and insertion loss profile of the channel medium, as highlighted in Figure 24 of the JESD204C standard.
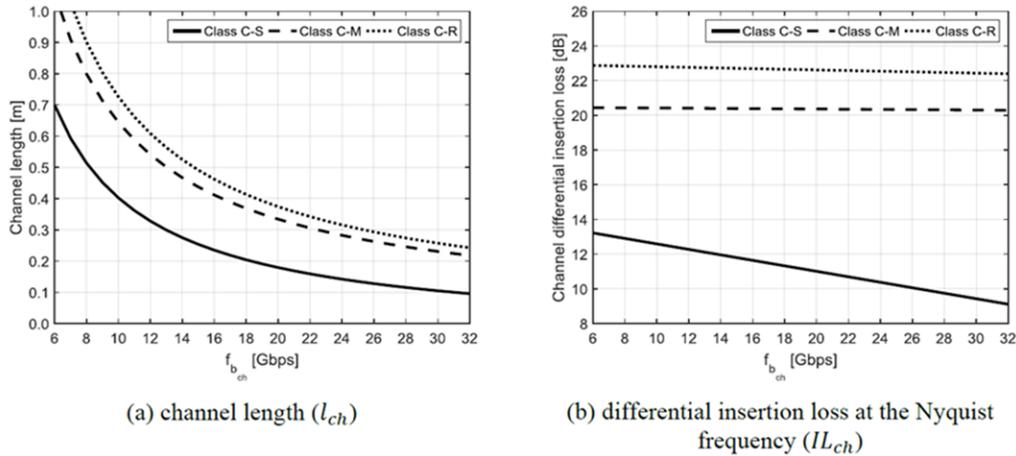
(a) channel length (l_{ch})   (b) differential insertion loss at the Nyquist frequency (IL_{ch})

Figure 1. Category C Channel Characteristics as a Function of a Channel Data Rate [1]

Each category has a specific SERDES transmitter FFE, SERDES receiver CTLE, or DFE taps recommendations, as highlighted in Table 21 of the JESD204C standard.

Table 4. Category C Device Features[1]

CLASS	RELATIVE POWER	TRANSMITTER FFE	RECEIVER CTLE	RECEIVER DFE TAPS	COMPARABLE CHANNEL
C-S	Low	3 taps 9.5 dB	6 dB	0	OIF-CEI 03.1 28G-SR
C-M	Medium		9 dB	3	OIF-CEI 03.1 28G-MR
C-R	High		12 dB	14	OIF-CEI 03.1 25G-LR

[1]   Table 21 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

Perhaps the most significant difference between the JESD204B and JESD204C standard is the recommendations of crosstalk specifications and the inclusion of equalization as means to qualify and quantify the link performance.

1. Category C classification also includes crosstalk specifications for near-end crosstalk power sum (PSNEXT) and far-end crosstalk power sum (PSFEXT). See section 5.2.9.4 of the JESD204C standard for details.

2. The former JESD204B and JESD204C Category B only specifies the eye masks necessary at the transmitter output and receiver input. The measurement point of the eye masks are located near the DUT pins, and do not include additional equalization benefits added by the SERDES transmitter and receiver blocks. Moreover, there are no specific requirements on transmitter architecture (emphasis, de-emphasis, or FIR) and receiver architecture (CTLE and/or DFE). The standard only references OIF-CEI specifications and also lists eye diagram requirements.

3. The JESD204C-specified channel operation margin (JCOM) for the Category C allows the user to budget the entire link budget as a whole, which also includes transmitter architecture and receiver architecture. Refer to section 5.2 of the JESD204C standard for details. This means that the equalization from both the SERDES transmitters and receivers can be included in the link performance benchmark.

5.1   What Does This Mean for a System Developer?

1. With the inclusion of JCOM as means to quantify and qualify link performance, the SERDES transmitter and receiver equalization benefits are now part of the parameters of benchmark. Potentially, the measured eye at the pin of the SERDES receiver input can be closed and deemed unacceptable for the former specification, but the link performance can still pass with the current specification due to the equalization process. Basically, the evaluation of the equalized eye diagram is acceptable for the link performance.

2. Crosstalk is now a benchmark figure for the JESD204 link. The crosstalk benchmark is a function of

[1]   Figure 24 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

the channel medium classification, and the system designer needs to pay additional attention on the channel medium selection, trace routing, and overall component placement strategies to meet crosstalk performance.

5.2 Things to Consider

1. Overall, the addition of JCOM is to evaluate the budget for the actual die-to-die performance including the following:
   - Package model
   - PCB traces
   - SERDES transmitter FIR
   - SERDES receiver CTLE/DFE setup
   - Another set of crosstalk modeling for the victim and aggressor in the package model and PCB traces setup
2. The fundamentals of JCOM is based on frequency domain analysis with time domain conversion. It can still have additional limitations compared to the actual time domain simulators like the IBIS AMI model, which can provide better statistics such as eye diagram performance after receiver equalization. Texas Instruments recommends consultation with simulation tools vendors for details.
3. Regardless of the simulation tool of choice, the bench level testing still requires tools at the SERDES IP level to evaluate the actual eye height and bit error statistics. System engineers must consider the tools available for the FPGA/ASIC/data converter SERDES IP. Typically, basic functions such as eye height (after the CTLE/DFE at the SERDES receiver) and a basic PRBS pattern generator and verifier for statistical bit error analysis must be available for bench level testing.

6 Link Layer: Difference in Handshaking Protocol

As with all the serial link communication, the JESD204 has an initial handshaking protocol to ensure mutual understanding of the J-TX and J-RX before the serial data streaming. The JESD204C specification retains the former JESD204B handshaking protocol for the 8B/10B coding to ensure backward compatibility. Moreover, the JESD204C includes a new set of handshaking protocols for the 64B/66B and 64B/80B encoding that can further simplify the bring-up process as additional smarts are added to the J-RX.
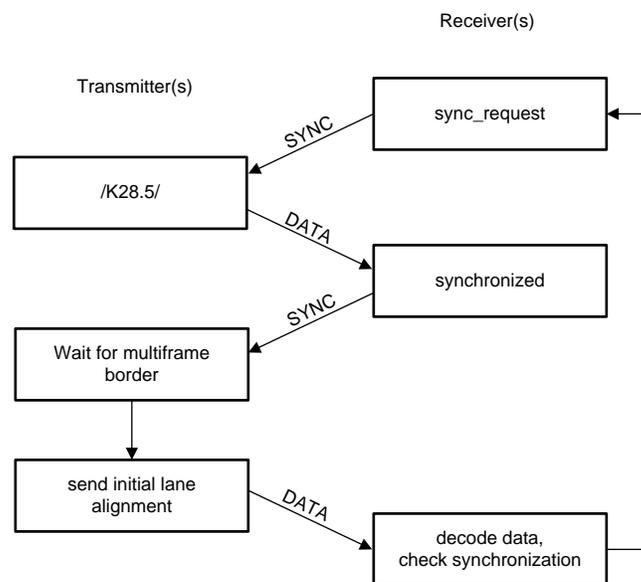
Figure 2. Synchronization Process for Subclasses 1 and 2 [2]

[2] Figure 90 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

To understand the differences in the handshaking protocol between the coding options, first revisit the 8B/10B option. The best diagram that illustrates this is Figure 90 of the JESD204C document that describes the synchronization process. In the diagram, you can see the transition of different stages within the handshaking protocol. The J-RX is designed to have all the smarts in the handshaking protocol. It initially sends the synchronization request (sync_request) via either a hardware-based ~SYNC signal or a software-based ~SYNC signal. This starts the code group synchronization stage. After receiving the ~SYNC signal, the J-TX sends the K28.5 comma characters for the synchronization. The J-RX then indicates that it is indeed synchronized through a transitioned sync_request state and waits for additional checks such as the initial lane alignment sequence. Finally, the J-TX starts sending the actual payload to complete the process, assuming the J-RX does not send an additional sync_request. If at this stage, the J-RX sends another sync_request signal, then there are errors in the handshaking process, and the J-RX state machine repeats the entire process again. [3]

The handshaking protocol for the 64B/66B and 64B/80B encoding is basically a new architecture when compared to the 8B/10B option. One of the primary highlights for the 64B/66B and 64B/80B handshaking protocol is that the J-TX inserts periodic keywords for the J-RX to recognize (as opposed to the one time handshaking synchronization signal of the 8B/10B at the initial handshaking stage). Moreover, the J-RX is essentially smarter and can self-synchronize to the periodic keywords and establish their own link. It is also able to re-establish its own link again without changing the J-TX transmit protocol (assuming the source of link error is not from the J-TX itself and can be self corrected within the JESD204 frame work). The following are details about the new handshake architecture:

1. The 2-bit sync headers are now the hand-shaking code for the link establishment. This is inserted periodically with pre-defined patterns, depending on the usage of cyclic redundancy check (CRC) and forward error correction (FEC). This is one of the major changes in 64B/66B and 64B/80B encoding when compared to a dedicated code group synchronization stage of K28.5 characters in the 8B/10B encoding.

2. The 64B/66B and 64B/80B J-TX continuously transmit the blocks of data (that is the multi-block and extended multi-block) with the 2-bit sync header. The occurrence of the pilot signal insertion is dependent on the usage of the CRC and FEC.

3. The 64B/66B and 64B/80B specifications do not require the physical handshaking signal from the 64B/66B and 64B/80B J-RX because the J-RX is now smart enough to recognize the 2-bit sync headers and establish their own link without feeding the handshaking request to the 64B/66B and 64B/80B J-TX. This is also to accommodate the potential usage of the software-based synchronization signal. [4]

In summary, the 8B/10B encoding has a dedicated handshaking period, whereas the 64B/66B and 64B/80B have a periodic sync header for the J-RX to recognize and self-train to the sync header. The details of the 64B/66B and 64B/80B encoding and decoding process can be illustrated in Figure 67 and Figure 69 of the JESD204C document. The following is the encoding process:

1. Gather eight octets of data from transport layer.

2. Go through scrambler to randomize the stream.

3. Go through CRC or FEC process.

4. Go through sync header insertion. With 64B/80B encoding, extra fill bits are added.

5. Go through gearbox to adjust the rate between data in the transport layer and the ratio of 64B/66B or 64B/80B encoding clock rate.

The following outlines the decoding process:

1. The bit stream is received.

2. The gearbox is used to adjust various clock rate ratios of both the encoding rate and the actual data rate.

3. Block Sync extracts sync header stream to achieve block, multi-block, and end of multi-block synchronization.

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[3] In the former JESD204B document, the better illustration is Figure 5 for J-RX elastic buffer release diagram. Prudent readers can compare the figure with the updated version in JESD204C document and notice the JESD204C figure has the ~SYNC signal removed. This is due to the optional software SYNC option being available in the JESD204C.

[4] The JESD204C document does not specify the ways the J-TX can know the moment the J-RX achieved synchronization. The document also does not specify the data payload requirement of the J-TX before and after the J-RX synchronization. The controlling process can be on a layer higher than the JESD204C such as the application layer.

4. Go through extraction of data and eliminate fill bits.

5. Go through sync header extraction process. The sync header stream contains command channel, CRC, or FEC information.

   a. FEC can be used to both detect and correct an error.

   b. CRC can detect an error and flag alarm to the alarm block.

6. Go through the descrambler process for the data stream without the sync header and fill bit pairs.
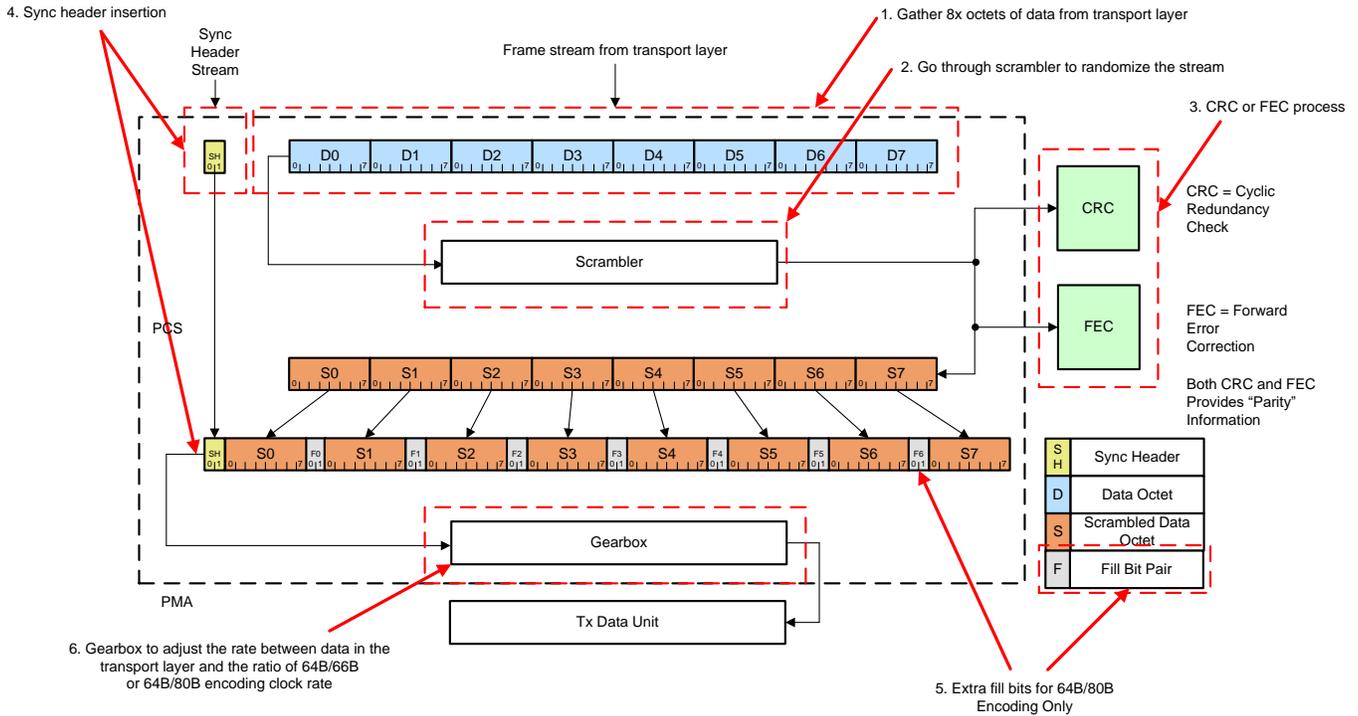
7. Data to be passed to transport layer for processing.

Figure 3. 64B/66B and 64B/80B Encoding Process [5]
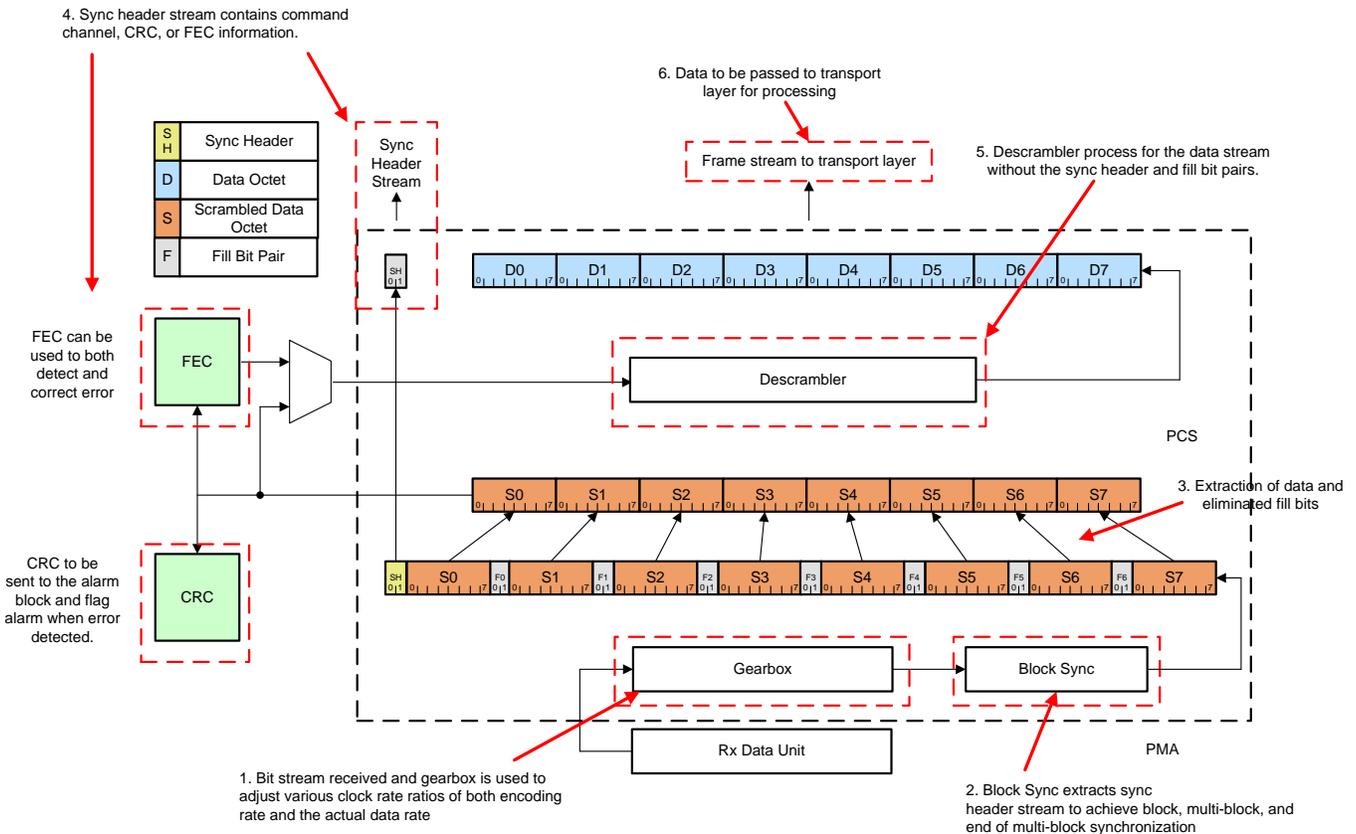
Figure 4. 64B/66B and 64B/80B Decoding Process [6]

6.1 What Does This Mean to System Developers?

1. If the FPGA/ASIC development is based on the JESD204B and the system needs to be migrated to the 64B/66B or 64B/80B encoding option, then the system developer needs to develop a new IP based on the new link layer of the JESD204C 64B/66B and 64B/80B encoding. The new handshaking protocol of the 64B/66B and 64B/80B encoding is not based on the 8B/10B encoding, but rather a new architecture.

2. The 64B/66B and 64B/80B encoding link layer option does not require a handshaking signal such as the ~SYNC. The JESD204C document does not specify the J-TX data requirement before and after the actual J-RX link establishment. The system developer may need to add an additional control layer (via hardware or software) on top of the JESD204C layer in the system to handle the transitional stage before and after the J-RX establishment. Moreover, an alert signal from the J-RX must be routed to indicate link establishment and link error. The following are examples of additional handling processes.

   a. Besides the link layer level, the SERDES receiver in the J-RX physical layer requires CTLE and DFE adaptation process. The CTLE and DFE adaptation process requires the J-TX to send out quasi-random signals such as PRBS or sufficiently random traffic signals from the modem. It is important for the J-RX to communicate properly, perhaps via a higher level host, to the J-TX so the J-TX can send proper training patterns to the J-RX CTLE and DFE adaptation.

   b. In applications where the J-RX is the digital-to-analog converter (DAC) in the transmitter signal chain, the J-TX may need to send zeros for certain periods of time after the J-RX link establishment and before the actual transmission. This is to potentially flush out the random patterns in the DAC digital chain occurred during system bring-up. System developers need to set a period of time (after the training signal for CTLE and DFE adaptation) to send streams of zeros to flush out the DAC digital chain before the actual transmission to the rest of the transmitter chain (that is the pre-amp, power amplifiers, and antenna). The amount of time is typically greater than the latency of the DAC data path.

[6] Figure 69 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

c. The 8B/10B scrambler is a 15th order and self-synchronous. In some conditions such as the baseband data being long streams of zeros, the scrambler outputs initial scrambled data and then a repetitive copy of the data. This condition can cause electromagnetic interference (EMI) or maladaptation of the CTLE and DFE. A typical example is in systems where the signals are time gated (that is the time domain duplex or TDD systems). One way to fix this issue is to re-insert a periodic seeding signal to excite the scrambler again. For example, in a typical telecommunications system, this is the periodic pilot signals in between the data frames. The data streaming within the 64B/66B and 64B/80B encoding are scrambled by a 58th order scrambler and also self-synchronous. The chance of repetitive data for a 58th order scrambler is significantly lower by the design of the updated scrambler scheme, but it is still possible. The system developer needs to evaluate the baseband signal characteristic and use the documents scrambler model to decide if the periodic seeding signal is necessary to mitigate risks of the EMI and CTLE/DFE maladaptation.

3. Some developers still prefer dedicated handshaking protocols and proper sync_request signals, such as ~SYNC, to indicate link establishment. The dedicated handshaking period allows the developer to plan the SERDES equalization training and the other system bring-up to flow better. Moreover, in applications where a DAC in a transmitter chain is used, the sync_request signal can provide deterministic gating of the signal when the JESD204 link is down. Such deterministic gating of the signal can be critical for the transmitter chain to prevent erroneous signal from propagating to the rest of the signal chain, and possibly over the air. In these cases, the JESD204 8B/10B encoding is a more suitable option.

4. Table 1 highlights the importance of the gearbox ratio. The SERDES-to-data converter ratio for 8B/10B is 40, while the ratio for 64B/66B is 33. When selecting between the two encoding options, the developers need to consider the necessary clocks and reference clocks generation for various IP cores. The utility of the 64B/66B encoding can introduce additional restrictions. While 64B/80B encoding provides the same compatibility as the 8B/10B encoding, it does not provide the same efficient encoding as the 64B/66B option.

6.2 Things to Consider

1. The sync header stream provides the pilot signal insertion for the identification of the block and extends the multi-block. Moreover, the stream provides error detection capability (both CRC and FEC) and error correction capability (only FEC).

2. In the 8B/10B encoding scheme, the running disparity error and code error (that is the data not in 8B/10B decoding table) are found almost immediately after data reception.

3. In 64B/66B or 64B/80B, the CRC or FEC error check is done to find bit or burst errors. The CRC or FEC error can be detected only 2048 bits after the wrong data is received. The reason for the 2048 bit delay is that for the error detected of the first multi-block, the CRC, or FEC of the block is transmitted along with the next multi-block.

7 Deterministic Latency

The deterministic latency frame work and requirements of the JESD204C remain similar to the JESD204B standard. The ultimate goal to achieve deterministic latency can be best described in Figure 5 of the JESD204C document. Note that even though the figure is describing the operation in 8B/10B encoding, the same principle of the buffer release can be applied in 64B/66B and 64B/80B encoding conditions. The following is a summary of the steps necessary to achieve deterministic latency.
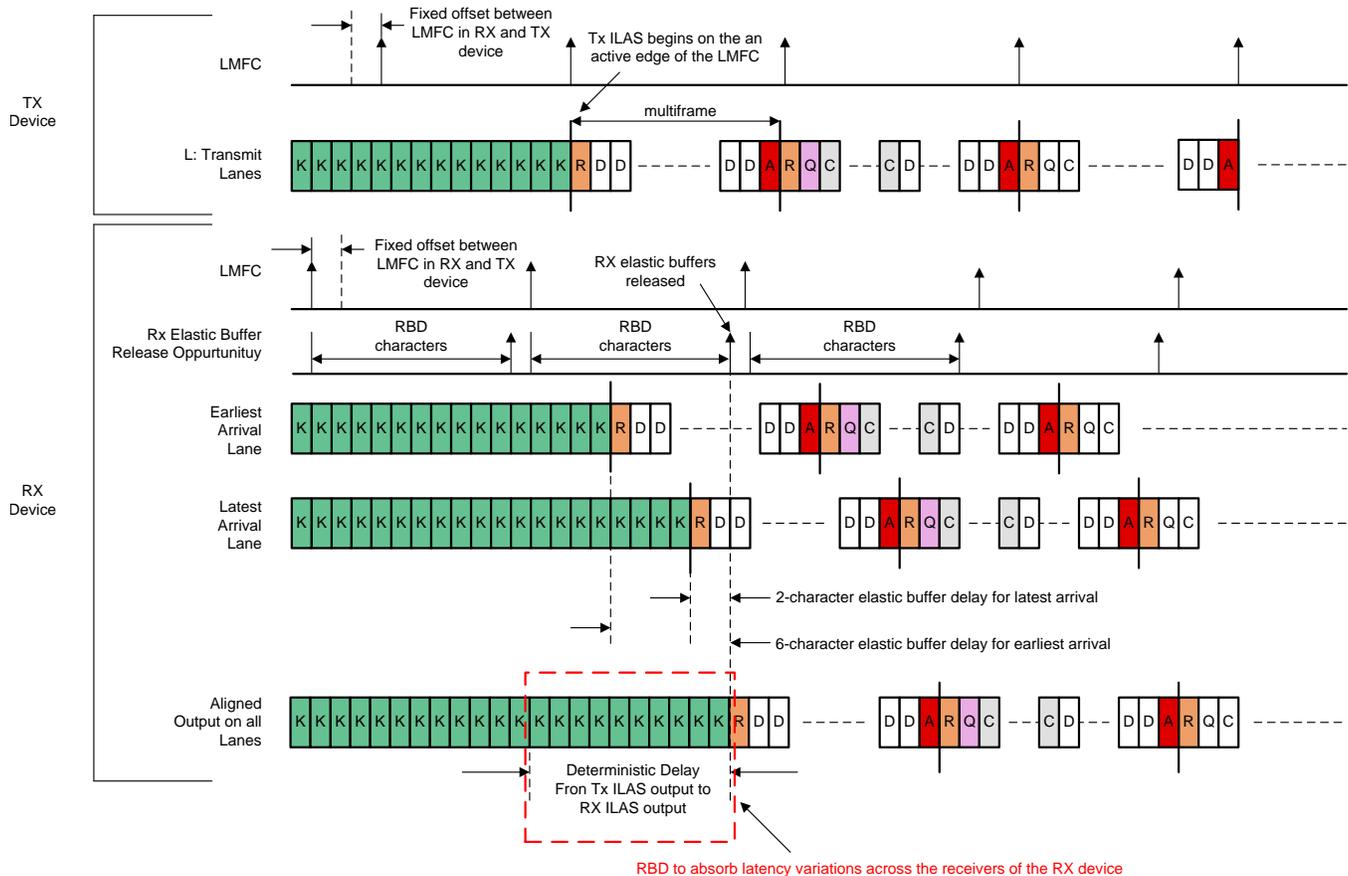
Figure 5. Timing Diagram Illustrating the RX Elastic Buffer Release Opportunity in a JESD204C 8B/10B System [7]

1. System designers set the length of a multi-frame (8B/10B) or extended multi-block (64B/66B) to be larger than the maximum possible delay variations of the J-RX lanes across the link.

2. The buffer size of the J-RX lanes of the link must also be larger than the delay variation to absorb the delay at the J-RX lanes. Once the time stamps of each lane have been received by all the J-RX lanes, the buffer is released. Basically, the buffer absorbs the latency difference among received data in the J-RX lanes.

3. Each lane has its own buffer. The earlier arrival lanes use more of the buffer, while the late arrival lanes use less of the buffer. Upon the receipt of the time stamp signal, all the buffers are released at the same time.

4. The release point can be fine-tuned by the system designers. The release point adjustment basically moves the release point away from the "uncertainty" region.

A few new things that are introduced in the JESD204C that can improve the deterministic latency setup are the following:

1. RBD (release buffer delay) is now defined as adjustment steps instead of fixed frame cycles in the JESD204B 8B/10B coding.

2. The maximum number of frames per multi-frame (K) is now increased from 32 to 256. This indicates that longer buffer in the J-RX IP must be implemented (basically re-use the buffers for the 64B/66B encoding IP for the 8B/10B option).

Note that even though the principle of the release buffer delay and the operation of the buffer to achieve deterministic latency is the same amongst the three encoding options, there are some differences in the definition that the system developers must know. These are the time stamps indicators for the buffers to release:

[7] Figure 5 of JESD204C Document. Copyright JEDEC. Reproduced with permission by JEDEC.

1. 8B/10B link: The difference between the times of the earliest lane and latest lane for the bit transition between the last /K/ character to the first bit data or the start of the initial lane alignment sequence.

2. 64B/66B or 64B/80B link: The difference between the times of the earliest lane and latest lane for the bit transition in the sync header of the first block in a multi-block.

Moreover, there are complete revisions of the skew budget. Section 4.3 of the JESD204C specification includes a detailed analysis and design implementation recommendation. Keep the following directional difference definition in mind when interpreting the specifications:

1. Transit Direction: Specification is for the generated skew.

2. Receive Direction: Specification is for the skew tolerance.

7.1 *Things to Consider*

1. For the 8B/10B encoding option, the setting of K (number of frames in the multi-frame) must be set to the minimum if the lowest link latency is required.

2. For the 64B/66B or 64B/80B, the setting of E (number of multi-block in the extended multi-block) must be set to the minimum if the lowest link latency is required. [8]

3. Choosing the smallest value of K in 8B/10B encoding or smallest value of E in 64B/66B or 64B/80B encoding also improves re-link time if the link re-establishment occurs.

4. Typically, the digital design of the JESD204 core is a function of the multi-frame clock (K) or extended multi-block clock (E). Smaller K or smaller E requires a faster digital processing clock, which translates to faster processing rate of digital designs. Even though the lower bound of K or E value is specified as one in the JESD204C standard, the actual lower bound is set by the logic design of the logic devices and data converters.

5. The value of K or E is a factor for the SYSREF frequency. Deterministic latency requires SYSREF as a time stamp for the logic devices and data converters synchronization.

8 ~SYNC (SYNC REQUEST) Signal Differences

8.1 *8B/10B Coding Option Upgrades*

For the 8B/10B option, the handshaking keyword is the K28.5 character for the initial link synchronization, and the DC coupled handshaking request (or synchronization request) is the ~SYNC signal. There are additional keywords such as K28.7 for the purpose of frame alignment checks. These options remain within the standard for the JESD204C 8B/10B option.

There are a few upgrades from the JESD204B standard:

1. The DC coupled ~SYNC signal can now be optionally software-based via serial communication interface, such as SPI. For example, the host can write a register within J-TX and J-RX to start the synchronization request and also ask the J-TX to issue K28.5 characters. Upon the completion of the synchronization request, the host can then stop the synchronization request and start the data streaming. This option was not fully defined and cannot ensure device deterministic latency between different link establishments.

2. Hardware-based ~SYNC signals now have timing adjustment capability in case the JESD204C device needs to work with an older generation JESD204B-only device.

3. ~SYNC generation and ~SYNC detection clocks added for the 8B/10B link layer only. These can be separate clocks, but it is also possible to reuse another clock with adjustment delays and pulse extension.

4. The pulse width for the ~SYNC for the Sync Request (five Frames and nine octets minimum) and Error Reporting (two Frames Minimum) must allow for adjustment steps for skew and JESD204B backward compatibility.

Due to the nature of the sync header structure for the 64B/66B and 64B/80B coding, the use of SYNC signal is no longer necessary.

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[8] A block contains eight octets of data. A multi-block contains 32 blocks. An extended multi-block contains number E of multi-blocks.

8.2 What Does This Mean to System Developers?

1. Tuning the RBD delay in adjustment steps with respect to frame clock (or multi-block clock) and larger defined J-RX buffer size provide finer control of the delay release point for system developers. This is especially important when system developers are adjusting the delay for multiple data converters to achieve multi-device synchronization.

2. With the inclusion of 64B/66B and 64B/80B encoding, the J-RX buffer size increases with a longer, extended multi-block length. This also increased the buffer size in 8B/10B encoding mode, which allowed the number of multi-frames (K) to increase from 32 to 256 total. The increase in buffer size allowed better tolerance to higher delay variation in the JESD204C system.

3. Since the ~SYNC requirement is removed from the encoding options and also the nature of the encoding definition, the implementation of the JESD204C over fiber can be realized. In the previous 8B/10B encoding option, the delivery of the DC coupled ~SYNC signal has always been a concern.

9 Conclusions

The JESD204C offers more efficient coding schemes, higher throughput rate with more specific physical layer definition, smarter handshaking protocol in the link layer with backwards compatibility with the former standard, and adjustment delay steps in systems requiring deterministic latency and multi-devices synchronization. While all of these features bring out the best of the next generation communications systems, system designers now have the knowledge to also evaluate the impact of upgrading to the JESD204C when compared to staying with the JESD204B.

Regardless of the final choice of the JESD204 standard, Texas Instruments offers a broad portfolio of JESD204B and JESD204C data converters and radio transceivers for many communication system designs. Visit www.ti.com for additional information and also training materials regarding the JESD204 standards.

10 References

- JESD204C Standard – JEDEC, December 2017
- SerDes Design Part 5: Channel Operating Margin, a Powerful Compliance Tool

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