

# Basic Calculation of an Inverting Buck-Boost Power Stage

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## ABSTRACT

This application note provides basic formulas that you need to design the power stage of an inverting buck-boost converter. The premise is that the power switch is integrated in the IC and the rectification is done by a diode (non-synchronous power stage). It provides all the formulas and considerations that you need to select the external power components such as the inductor, the diode, and the input and output capacitors. As the internal switch current capability is limited it will also provide an estimation to judge whether the load current can meet the IC specification.

Preconditions for the design:

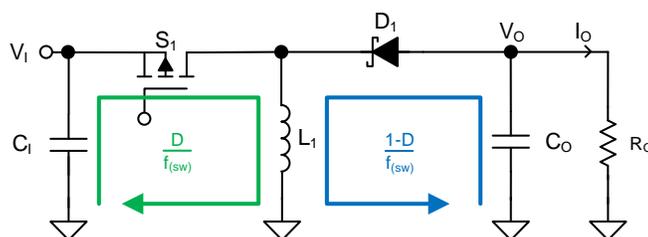
- Basic understanding of the functionality, refer to this [TI Training](#)
- *Continuous-Conduction-Mode* (CCM) consideration
- Large signal consideration
- Integrated switch
- Non-synchronous converter
- Basic understanding of the [DC Bias Effect of Ceramic Capacitors](#)

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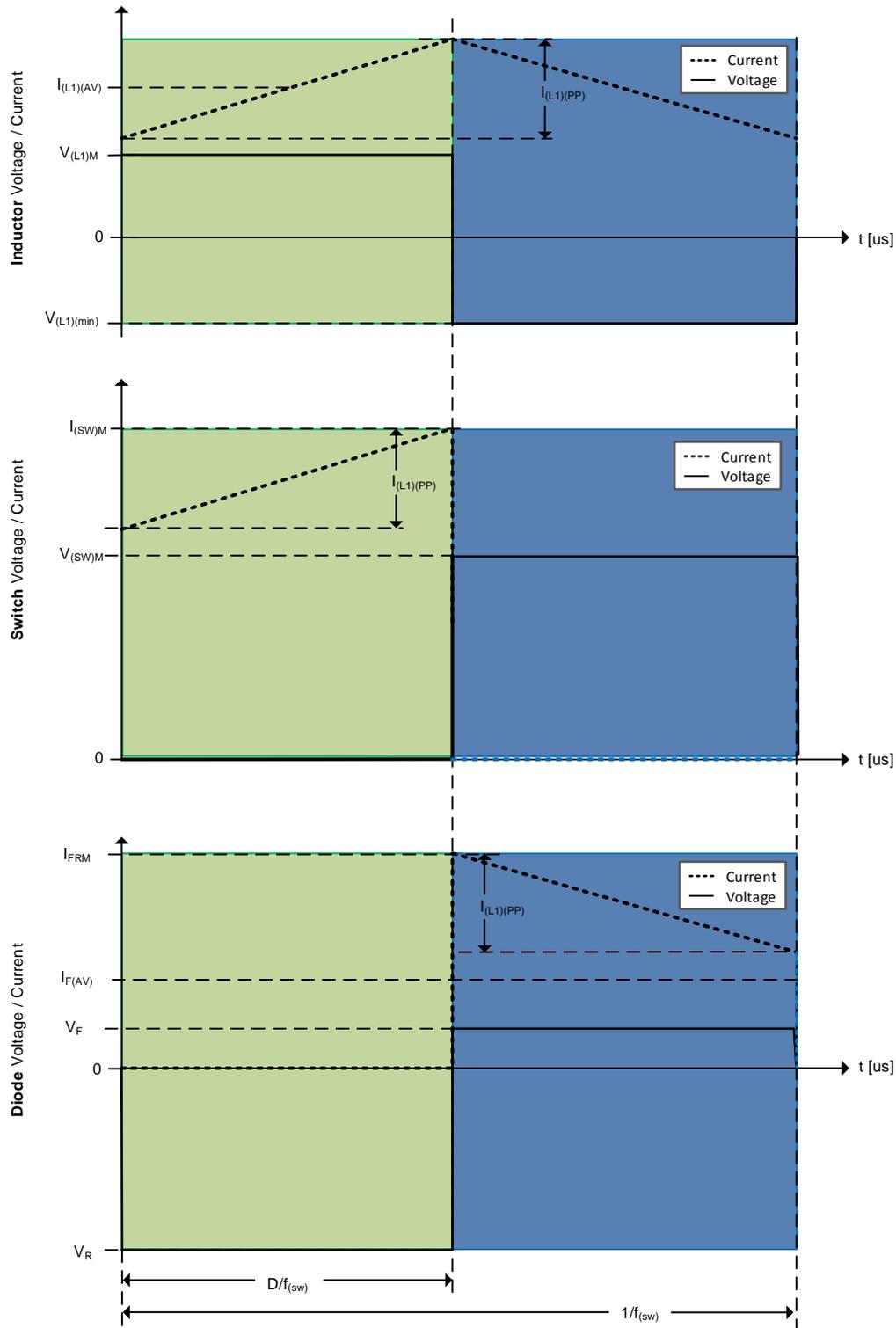
## 1 Basic Configuration of the Power Stage

[Figure 1](#) shows the simplified schematic of an inverting buck-boost power stage. This topology is a so-called flyback topology where the energy is transferred to the output when switch S1 is open.



**Figure 1. Simplified Schematic of an Inverting Buck-Boost Stage**

The following waveforms describe the time characteristics of the necessary currents and voltages. These values are considered in this application note.



**Figure 2. Simplified Waveforms of an Inverting Buck-Boost Stage**

In order to design each external component and to analyze the IC capabilities, the following parameters must be prepared:

**Table 1. Design Parameters**

Description	Parameter	Unit
Input voltage range	$V_{I(\min)}$ to $V_{IM}$	V
Output voltage	$V_O$	V
Maximum average output current	$I_{OM}$	A
Forward voltage drop of the rectifier diode	$V_F$	V
Allowed inductor current ripple	$I_{(L1)(PP)}$	mA
Recommended Inductance Range (data sheet)	L1	μH
Minimum switching current limit of internal switch S1 (data sheet)	$I_{(SW)(\min)(lim)}$	A
Switching frequency of the internal switch S1 (data sheet)	$f_{(SW)}$	MHz

As for all inductive converters one of the essential formulas is the steady state duty cycle. This can be derived from the inductor volt-second balance and the capacitor charge balance. For a robust design it is recommended to calculate the worst-case scenario. For the inverting buck-boost this means the **maximum duty cycle D** present at the minimum input voltage. It is specified as:

$$D = \frac{-V_O + V_F}{-V_O + V_F + V_{I(\min)}} \quad (1)$$

Rearranging [Equation 1](#) provides the **DC conversion ratio  $V_O / V_I$** :

$$\frac{V_O}{V_I} = \frac{-D}{1-D} \quad (2)$$

## 2 Check the Internal Switch S1

In the first step it is important to evaluate if the internal switch S1 can withstand the output current requirement of the application. The minimum switching current limit  $I_{(SW)(\min)(lim)}$  of the internal switch S1 of the chosen converter must be higher or equal to the **maximum switching current  $I_{(SW)M}$**  that is defined as:

$$I_{(SW)M} = (I_{OM} \times \frac{V_{I(\min)} + V_F - V_O}{V_{I(\min)}}) + (\frac{I_{(L1)(PP)}}{2}) \quad (3)$$

It is also possible to calculate the **maximum output current  $I_{OM}$**  that the converter can achieve by rearranging [Equation 3](#), as:

$$I_{OM} = (I_{(SW)(\min)(lim)} + \frac{I_{(L1)(PP)}}{2}) (\frac{V_{I(\min)}}{V_{I(\min)} + V_F - V_O}) \quad (4)$$

The **maximum voltage stress that the switch must withstand is  $V_{(SW)M}$**  and can be calculated with:

$$V_{(SW)M} = V_{IM} + V_F - V_O \quad (5)$$

## 3 Select the Inductor

The next step is to select the required inductance. If the inductance range is not limited by the IC you can estimate the required inductance based on the well-known differential equation:

$$L1 = \frac{V_I D}{I_{(L1)(PP)} f_{(SW)}} \quad (6)$$

The **average inductor current  $I_{(L1)(AV)}$**  is calculated by:

$$I_{(L1)(AV)} = \frac{I_O}{1-D} \quad (7)$$

However, most of the converters are already optimized for specific inductance ranges which are described in the data sheet. In this case, use the recommended value and calculate the **inductor current ripple**  $I_{(L1)(PP)}$  which is a rearrangement of [Equation 6](#):

$$I_{(L1)(PP)} = \frac{V_{I(min)} D}{f_{(SW)} L_1} \quad (8)$$

The **maximum inductor current**  $I_{(L1)M}$  is the sum of the average component and the half of the peak-to-peak inductor current ripple and is as well the maximum switch current shown in [Equation 3](#).

$$I_{(L1)M} = I_{(SW)M} = I_{(L1)(AVG)} + \frac{I_{(L1)(PP)}}{2} \quad (9)$$

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**NOTE:** The inductor must always have a higher current rating than [Equation 3](#) as the inductance decreases with increased current. As a general guideline, the saturation current of the inductance shall be:  $I_{(L1)(sat)} \geq 1.2 \times I_{(L1)M}$

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As soon as switch S1 opens the energy is transferred to the output.

This means that the output voltage flies back to the switching node and the **voltage across the inductance**  $V_{(L1)}$  becomes the output voltage minus the voltage drop of the diode:  $V_{(L1)M} = V_O - V_F$ .

Vice versa, the **maximum voltage**  $V_{(L1)M}$  is defined as the maximum output voltage minus the voltage drop of the diode.

## 4 Select the Rectifier Diode

For selecting the appropriate diode, consider that it needs to withstand the following stress parameters:

1. Average current:  $I_{F(AV)} = I_{OM}$
2. Maximum peak current:  $I_{FRM} = I_{(SW)M}$
3. Maximum DC reverse voltage:  $V_R = V_O - V_{I(min)}$
4. Power dissipation:  $P_D = I_{OM} \times V_F$

Generally, TI recommends using Schottky diodes for inductive low- to middle-power DC/DC converters. This is due to the low forward voltage drop which leads to higher efficiency.

## 5 Select the Capacitors

In the inverting buck-boost topology, the input and the output currents are pulsed. The choice of the input and output capacitances is therefore crucial to ensure stable performance. When choosing capacitors, take into account that the capacitance of ceramic capacitors decreases with its applied voltage, also called the [DC Bias Effect](#).

### 5.1 Input Capacitors

The input capacitance is required to hold up the input voltage during the time when the energy is decreasing in the inductor ( $(1 - D) / f_{(SW)}$ ). If the input voltage drop shall not be bigger than  $V_{I(PP)}$ , the minimum effective value for this capacitor  $C_{I(min)}$  can be estimated with:

$$C_{I(min)} = \frac{I_{(L1)(AVG)} \times D}{f_{(SW)} \times [V_{I(PP)} - (I_{(L1)(PP)} \times ESR_{CI})]} \quad (10)$$

Be aware that most converters already provide the minimum input capacitance requirements in the data sheet.

[Equation 10](#) implies that higher equivalent series resistance of the capacitor (ESR) increases the input voltage drop. TI recommends using low ESR capacitors ( $< 10 \text{ m}\Omega$ ), also referenced in [Section 5.2](#).

## 5.2 Output Capacitors

Since the output current is discontinuous as well, the output capacitor is required to supply the energy to the load during the time when energy is increasing in the inductor ( $D / f_{(SW)}$ ). If the converter is internally compensated, use the recommended values of inductance and output capacitors in the data sheet.

Estimate the **output voltage ripple**  $V_{O(PP)}$  with the following equation:

$$V_{O(PP)} = \frac{I_O D}{f_{(SW)} C_O} + \left( \frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{C_O} \quad (11)$$

If the converter is externally compensated, estimate the **minimum required capacitance**  $C_{O(min)}$  at an output voltage ripple requirement of  $V_{O(PP)}$ , given by:

$$C_{O(min)} = \frac{I_O \times D}{f_{(SW)} \times \left[ V_{O(PP)} - \left( \frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{C_O} \right]} \quad (12)$$

This formula implies that higher equivalent series resistance of the capacitor (ESR) increases the output voltage drop. TI recommends using low ESR capacitors ( $< 10 \text{ m}\Omega$ ), also refer to the following NOTE.

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**NOTE:** In general, TI recommends using ceramic capacitors due to their low ESR ( $< 10 \text{ m}\Omega$ ).

However, ceramic capacitors have some disadvantages that must be considered thoroughly. The following list emphasizes these disadvantages, for detailed information refer to [Murata](#):

- Capacitance decreases with increased voltage (DC bias effect)
  - Capacitance decreases with decreased voltage rating
  - Capacitance decreases with decreased package size
  - Capacitance decreases with increased temperature
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## 5.3 Note About Discontinuous Conduction Mode (DCM)

In the presented inverting buck-boost power stage, the converter could enter DCM operation due to the rectification diode D1 that only allows current to flow in one direction. If the load is so small that the inductor ripple current reaches zero, the switching node voltage becomes negative and the diode is in reverse direction. At this point for a certain time of the switching cycle, the converter will not provide current to the output which leads to different calculations and considerations.

This application note does not intend to provide the procedure to design a DCM converter.

However, be aware that such topology can enter DCM when the load is sufficiently small. The critical conduction current means the point when the converter enters DCM. This can be calculated by:

$$I_{O(DCM)} \leq \frac{I_{(L1)(PP)} \times (1-D)}{2} \quad (13)$$

or

$$I_{O(DCM)} \leq \frac{V_I^2 \times (V_F - V_O)}{(2 \times f_{SW} \times L1) \times (V_I + V_F - V_O)^2} \quad (14)$$

## 6 Summary of all Equations and an Application Example

The following chapter makes an exemplary calculation of the discussed formulas. The TPS65131 device is chosen for the consideration of the switch.

In the following tables all necessary parameters are shown as described in [Table 1](#) and [Table 2](#) will summarize all equations and exemplary calculations.

**Table 2. Application Example - Parameters With TPS65131**

Description	Parameter
Input voltage range	$V_{I(\min)} = 2.7 \text{ V}$ to $V_{IM} = 5.5 \text{ V}$ ; $V_I = 3.3 \text{ V}$
Output voltage	$V_O = -10 \text{ V}$
Maximum average output current	$I_{OM} = 100 \text{ mA}$
Forward voltage drop of the rectifier diode	$V_F = 0.5 \text{ V}$
Allowed inductor current ripple	Use recommended inductance value $L1 = 4.7 \mu\text{H}$
Input voltage ripple	$V_{I(\text{PP})} = 5\%$ of $V_{IM} = 275 \text{ mV}$
Output voltage ripple	$V_{O(\text{PP})} = 0.1\%$ of $V_O = 10 \text{ mV}$
Equivalent Series Resistor (ESR)	$\text{ESR}_{Cl} = \text{ESR}_{Co} = 5 \text{ m}\Omega$
Minimum switching current limit of internal switch S1 (datasheet)	$I_{(\text{SW})(\min)(\text{lim})} = 1.8 \text{ A}$
Switching frequency of the internal switch S1 (datasheet)	$f_{(\text{SW})} = 1.25 \text{ MHz}$

**Table 3. Inverting Buck-Boost Calculations**

Parameter Description [#]	Formula	Example with TPS65131
Maximum Duty Cycle	$D = \frac{-V_O + V_F}{-V_O + V_F + V_{I(\min)}}$	$D = \frac{-(-10 \text{ V}) + 0.5 \text{ V}}{-(-10 \text{ V}) + 0.5 \text{ V} + 2.7 \text{ V}} = 0.795$
DC Conversion Ratio	$\frac{V_O}{V_I} = \frac{-D}{1-D}$	$\frac{V_O}{V_I} = \frac{-0.795}{1-0.795} = -3.878$
Maximum Peak Switch Current	$I_{(\text{SW})M} = (I_{OM} \times \frac{V_{I(\min)} + V_F - V_O}{V_{I(\min)}}) + (\frac{I_{(L1)(\text{PP})}}{2})$	$I_{(\text{SW})M} = (0.1 \text{ A} \times \frac{2.7 \text{ V} + 0.5 \text{ V} - (-10 \text{ V})}{2.7 \text{ V}}) + (\frac{365 \text{ mA}}{2}) = 671 \text{ mA}$
Maximum Output Current	$I_{OM} = (I_{(\text{SW})(\min)(\text{lim})} + \frac{I_{(L1)(\text{PP})}}{2}) \times (\frac{V_{I(\min)}}{V_{I(\min)} + V_F - V_O})$	$I_{OM} = (1.8 \text{ A} + \frac{365 \text{ mA}}{2}) \times (\frac{2.7 \text{ V}}{2.7 \text{ V} + 0.5 \text{ V} - (-10 \text{ V})}) = 405 \text{ mA}$
Maximum Peak Switch Voltage	$V_{(\text{SW})M} = V_{IM} + V_F - V_O$	$V_{(\text{SW})M} = 5.5 \text{ V} + 0.5 \text{ V} - (-10 \text{ V}) = 16 \text{ V}$
Inductance	$L1 = \frac{V_I D}{I_{(L1)(\text{PP})} f_{(\text{SW})}}$	Data sheet Recommendation: $L1 = 4.7 \mu\text{H}$
Average Inductor Current	$I_{(L1)(\text{AV})} = \frac{I_O}{1-D}$	$I_{(L1)(\text{AV})} = \frac{0.1 \text{ A}}{1-0.795} = 0.488 \text{ A}$
Maximum Inductor Current	$I_{(L1)M} = I_{(\text{SW})M} = I_{(L1)(\text{AVG})} + \frac{I_{(L1)(\text{PP})}}{2}$	$I_{(L1)M} = 488 \text{ mA} + \frac{365 \text{ mA}}{2} = 671 \text{ mA}$
Inductor Current Ripple	$I_{(L1)(\text{PP})} = \frac{V_{I(\min)} D}{f_{(\text{SW})} L1}$	$I_{(L1)(\text{PP})} = \frac{(2.7 \text{ V}) \times (0.795)}{1.25 \text{ MHz} \times 4.7 \mu\text{H}} = 365 \text{ mA}$
Inductor Saturation Current	$I_{(L1)(\text{sat})} > 1.2 \times I_{(\text{SW})M}$	$I_{(L1)(\text{sat})} > 805 \text{ mA}$
Diode Forward Current	$I_{F(\text{AVG})} = I_{OM}$	$I_{F(\text{AVG})} = 100 \text{ mA}$
Maximum Diode Peak Current	$I_{FRM} = I_{(\text{SW})M}$	$I_{FRM} = 671 \text{ mA}$

**Table 3. Inverting Buck-Boost Calculations (continued)**

Parameter Description [#]	Formula	Example with TPS65131
Maximum Diode DC Reverse Voltage	$V_{RM} = V_O - V_{IM}$	$V_{RM} = -15.5 \text{ V}$
Minimum Input Capacitance	$C_{I(\min)} = \frac{I_{(L1)(AVG)} \times D}{f_{(SW)} \times [V_{I(PP)} - (I_{(L1)(PP)} \times ESR_{CI})]}$	$C_{I(\min)} = \frac{(488 \text{ mA}) \times (0.795)}{1.25 \text{ MHz} \times [(0.05) \times (2.7 \text{ V}) - (365 \text{ mA}) \times (8 \text{ m}\Omega)]} = 2.3 \mu\text{F}$
Minimum Output Capacitance	$C_{O(\min)} = \frac{I_O \times D}{f_{(SW)} \times \left[ V_{O(PP)} - \left( \frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO} \right]}$	$C_{O(\min)} = \frac{(100 \text{ mA}) \times (0.795)}{1.25 \text{ MHz} \times \left[ 0.001 \times (-10 \text{ V}) - \frac{100 \text{ mA}}{1-0.795} + \left( \frac{365 \text{ mA}}{2} \times 5 \text{ m}\Omega \right) \right]} = 9.6 \mu\text{F}$
Output Voltage Ripple	$V_{O(PP)} = \frac{I_O D}{f_{(SW)} C_O} + \left( \frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO}$	Requirement $V_{O(PP)} = 10 \text{ mV}$
Critical Conduction Current	$I_{O(DCM)} \leq \frac{V_I^2 \times (V_F - V_O)}{(2 \times f_{SW} \times L1) \times (V_I + V_F - V_O)^2}$	$I_{O(DCM)} \leq \frac{2.7 \text{ V}^2 \times (0.5 \text{ V} - (-10 \text{ V}))}{(2 \times 1.25 \text{ MHz} \times 4.7 \mu\text{H}) \times (2.7 \text{ V} + 0.5 \text{ V} - (-10 \text{ V}))^2} = 37.4 \text{ mA}$

The presented calculations can be verified graphically with the [Power Stage Designer Tool](#). The following cutouts of this tool will show the results of the given example from [Table 2](#).

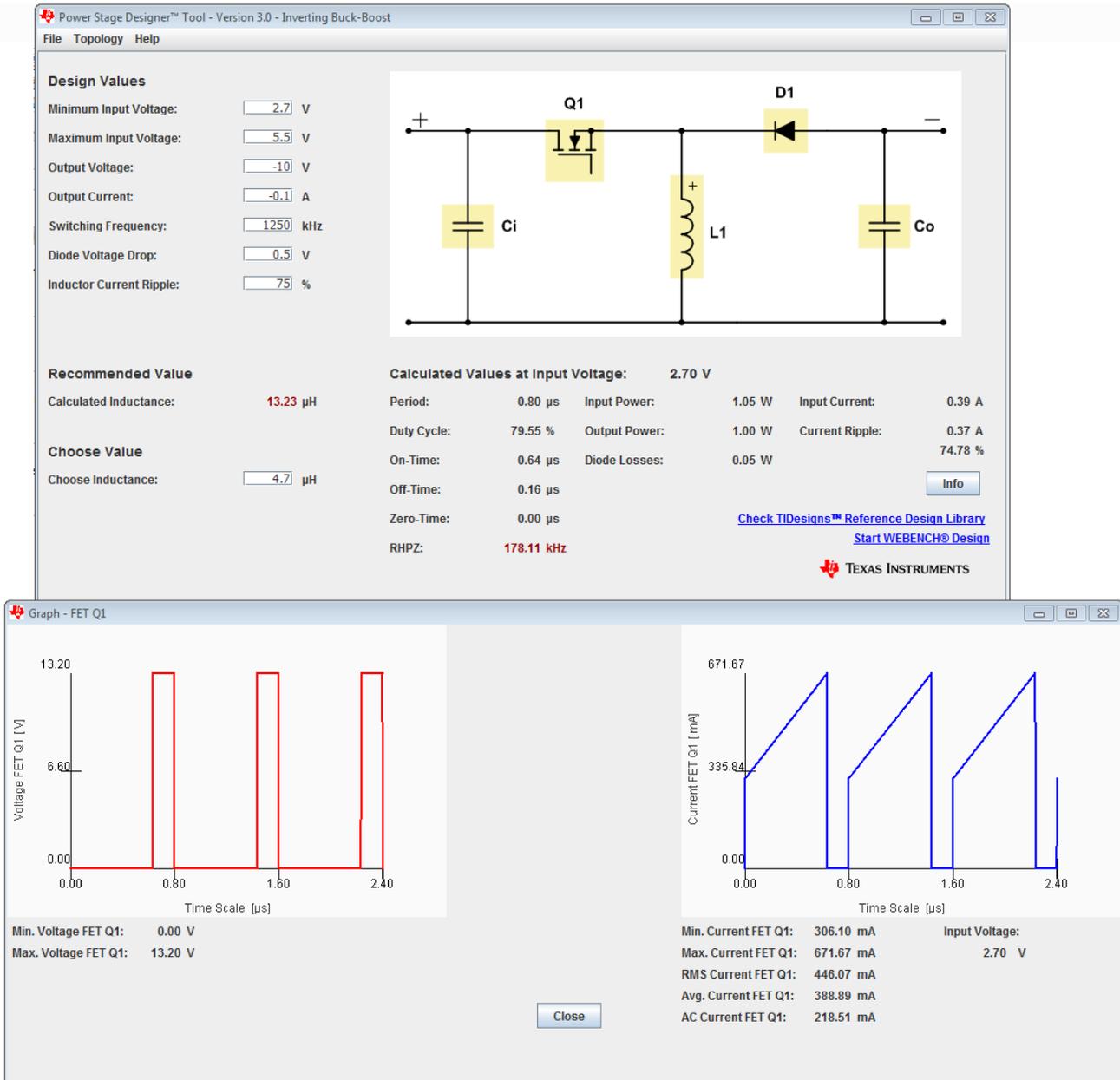


Figure 3. Screenshot of Power Stage Designer Tool (Version 3.0)

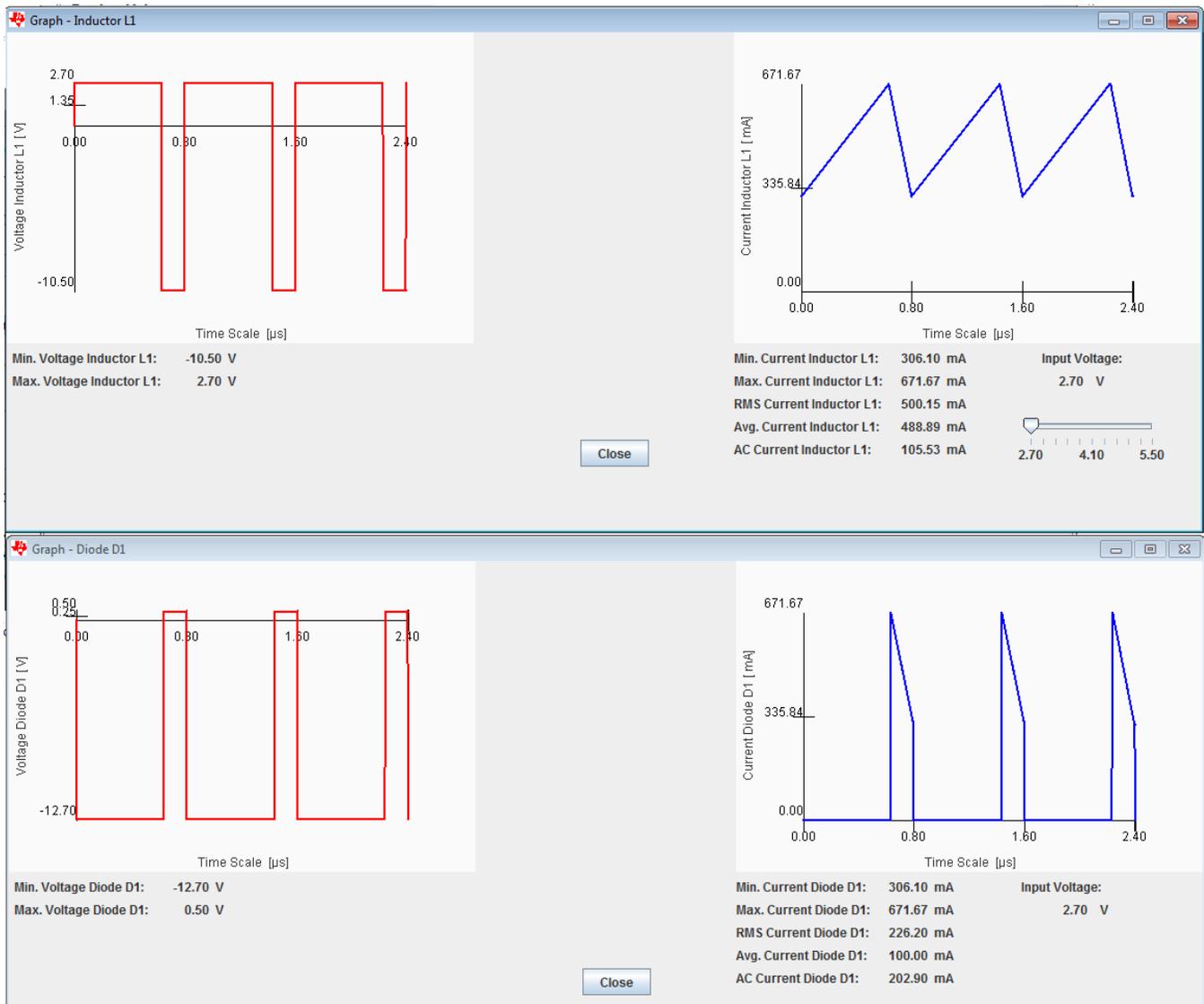


Figure 4. Screenshot of Power Stage Designer Tool (Version 3.0)

## 7 References

1. *Power Topologies Handbook* (Markus Zehendner, Matthias Ullmann), ([SLYU036](#))
2. [Power Stage Designer Tool – Version 3.0](#)
3. *TPS6513x Positive and Negative Output DC-DC Converter* data sheet ([SLVS493](#))
4. Writing Guidelines according to JESD99C
5. Basic Calculation of a Boost Converter's Power Stage ([SLVA372](#))
6. Basic Calculation of a Buck Converter's Power Stage ([SLVA477](#))

### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2017) to A Revision	Page
• Corrections made to equations 11 and 12. ....	5
• Corrections made to the <i>Minimum Output Capacitance</i> and <i>Output Voltage Ripple</i> formulas in the <i>Inverting Buck-Boost Calculations</i> table. ....	7

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