Modeling the output impedance of an op amp for stability analysis

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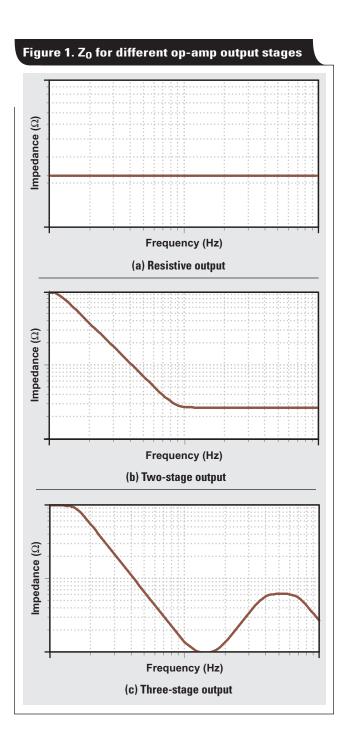
Introduction

The interaction between the output stage of an operational amplifier (op amp) and capacitive loads can impact the stability of the circuit. Throughout the industry, op-amp output-stage requirements have changed greatly since their original creation. Classic output stages with the class-AB common-emitter bipolar junction transistor (BJT) have now been replaced with common-collector BJT and common-drain complementary metal-oxide semiconductor (CMOS) devices. Both of these technologies enable rail-torail output voltages for single-supply and battery-powered applications.

A result of changing these output-stage structures is that the op-amp open-loop output impedance (Z_0) changed from the largely resistive behavior of early BJT op amps to a frequency-dependent Z_0 that features capacitive, resistive, and inductive portions. Proper understanding of Z_0 over frequency is crucial for the understanding of loop gain, bandwidth, and stability analysis. This article develops a passive-component model of the Z_0 curve for a three-stage op amp. This enables a deeper understanding of the different regions of a modern op-amp Z_0 curve that will simplify op-amp stability analysis when designing circuits.

Op-amp output impedance

Output stages with the classic common-emitter BJTs feature flat resistive Z_0 curves as shown in Figure 1a. Many CMOS rail-to-rail output amplifiers feature two-stage Z_0 curves (Figure 1b). Three-stage BJT and CMOS-output topologies that create rail-to-rail outputs while achieving open-loop gains greater than 120 dB, often feature the three-stage Z_0 curve shown in Figure 1c. The Z_0 curves shown here should not be confused with the closed-loop output impedance (Z_{OUT}) curves that are also shown in op-amp data sheets.



The test circuit to measure the open-loop output impedance of op amps in circuit-simulation programs (SPICE) is shown in Figure 2. The circuit uses a very large 1-TH inductor (L_T) and a 1-TF capacitor (C_T) as the feedback components. The L_T inductor provides a closed-loop unitygain feedback path at very low frequencies near DC to define the circuit operating point, while opening the feedback loop for AC. This allows for an open-loop measurement of the output impedance for all frequencies of interest. The C_T capacitor is open at DC and then connects the inverting input to the same potential as the non-inverting input for all frequencies of interest. A current source can then be injected directly into the output while measuring the output voltage, V_{OUT} . The voltage probe on the output will be equal to Z_0 in dB. The results must be converted from dB to a logarithmic scale in V/A to obtain Z_0 in Ω .

Calculating Z₀ curve values

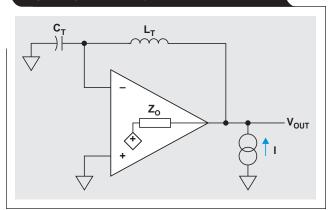
The $Z_{\rm O}$ simulation results for a typical three-stage op amp are shown in Figure 3. While each op amp will have different magnitudes of output impedance, the shape shown in this curve will typically exist.

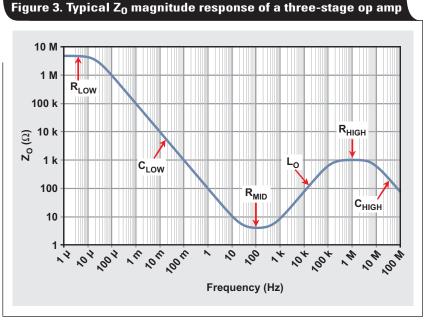
The resistive, capacitive, and inductive portions of the Z_O curve from Figure 3 have been labeled to develop a more intuitive understanding of the Z_O behavior over frequency. Resistive regions are the easiest to identify as the flat regions of the curve. A three-stage output impedance typically has three resistive regions marked as R_{LOW} , R_{MID} , and R_{HIGH} . Capacitive regions result in an equivalent –20-dB/decade decrease in Z_O with frequency as shown in the regions marked C_{LOW} and C_{HIGH} . The inductive region causes an equivalent 20-dB/decade increase in Z_O over frequency as shown in the L_O region of the curve.

The values of the resistive regions of the curve can be read directly from the flat regions of the curve. Table 1 shows the resistive values from the curve in Figure 3.

Designator	Value	Units
R _{LOW}	4.87	MΩ
R _{MID}	4.09	Ω
R _{HIGH}	1.03	kΩ

Figure 2. Simulation circuit for open-loop output impedance (Z₀)





The inductance and capacitance equations, Equations 1 and 2, can be used to calculate the values in those regions of the curve.

$$Z_{\rm C}(f) = \frac{1}{2\pi f \times C} \text{ or } C = \frac{1}{2\pi f \times Z_{\rm C}(f)}$$
(1)

$$Z_{L}(f) = 2\pi f \times L \text{ or } L = \frac{Z_{L}(f)}{2\pi f}$$
(2)

Depending on the shape of the Z_0 magnitude, it can be difficult to determine the correct frequency and impedance values to use in the calculations. This is especially true if there is little separation between the R, L, and C regions. The best frequency to use for the impedance

calculations is the frequency as a logarithmic scale that is in the middle of the poles and zeroes, which define the component's region of operation. The Z_0 phase-response curve shown in Figure 4 can be used to determine the location of the poles and zeros by identifying frequencies that correspond to $\pm 45^{\circ}$ phase shifts. A pole will have -45° of phase-shift from the initial value at the pole frequency, while a zero will have $+45^{\circ}$ of phase-shift from the initial value at the zero frequency.

The poles and zeros are marked in Figure 4 and their frequencies are listed in Table 2.

Table 2. Frequencies of the poles and zeros from the Z_0 phase curve shown in Figure 4

Name	Value	Units
f _{P1}	20.77	μHz
f _{Z1}	24.74	Hz
f _{Z2}	492.73	Hz
f _{P2}	143.33	kHz
f _{P3}	7.68	MHz

To calculate the value for the C_{LOW} region, first determine the average frequency (f_{C_LOW}) between the pole and zero frequencies that define the capacitive region, f_{P1} and f_{Z1} , using Equation 3.

$$f_{C_LOW} = \sqrt{f_{P1} \times f_{Z1}} = \sqrt{20.77 \,\mu Hz \times 24.74 \,Hz}$$
 (3)
= 22.67 mHz

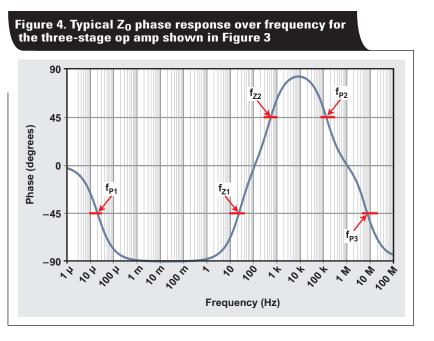
The impedance of the curve at 22.67 mHz, $Z_{C_LOW}(f_{C_LOW})$, is equal to 4.47 k Ω . Equation 4 uses these values to calculate the 1.57 mF value of C_{LOW} .

$$Z_{C_{LOW}}(f_{C_{LOW}}) = \frac{1}{2\pi f_{C_{LOW}} \times C_{LOW}}$$

or
$$C_{LOW} = \frac{1}{2\pi f_{C_{LOW}} \times Z_{C_{LOW}}(f_{C_{LOW}})}$$

$$= \frac{1}{2\pi \times 22.67 \text{ mHz} \times 4472 \Omega} = 1.57 \text{ mF}$$
(4)

The middle frequency for the $L_{\rm O}$ inductance calculation $(f_{\rm Lo})$ can be calculated in a similar way using $f_{\rm Z2}$ and $f_{\rm P2}$ (Equation 3). With a $f_{\rm Lo}$ of 8.403 Hz, the impedance is equal to 64.94 Ω , which can be used with $f_{\rm Lo}$ to calculate the $L_{\rm O}$ inductance (Equation 5).



$$\begin{split} f_{Lo} &= \sqrt{f_{Z2}} \times f_{P2} = \sqrt{492.73 \,\text{Hz}} \times 143.33 \,\text{kHz} = 8,403 \,\text{Hz} \\ Z_{Lo}(f_{Lo}) &= 2\pi f_{Lo} \times L_{O} \\ \text{or} & (5) \\ L_{O} &= \frac{Z_{LO}(f_{LO})}{2\pi f_{LO}} = \frac{64.94 \,\Omega}{2\pi \times 8,403 \,\text{Hz}} = 1.23 \,\text{mH} \end{split}$$

The zero associated with C_{HIGH} is typically outside of the frequency range included in a Z_O curve and, therefore, is unknown. C_{HIGH} can be calculated using the impedance at the maximum frequency shown in the graph (100 MHz) and adjusted later if required. Slight inaccuracies in the value of C_{HIGH} are not as critical as some of the other values because the C_{HIGH} region is typically outside of the op-amp's bandwidth. The values calculated from the Z_O curve shown in Figure 3 are listed in Table 3.

Table 3. Values for all regions of the Z₀ curve

Designator	Value	Units
R _{LOW}	4.87	MΩ
CLOW	1.57	mF
R _{MID}	4.09	Ω
L ₀	1.23	mH
R _{HIGH}	1.03	kΩ
C _{HIGH}	20.14	pF

Lines representing the calculated passive R, L, and C impedances have been overlaid on the original Z_O curve in Figure 5. The impedance lines lay directly over the respective portions of the Z_O curve, confirming that the component value calculations are accurate.

Passive-component Z_0 model of the three-stage op amp

A passive model of the three-stage op-amp $\rm Z_O$ curve using the calculated R, L, and C values is shown in Figure 6. Note that there are many ways to represent and model op-amp $\rm Z_O$ curves. Depending on the type of simulation being run, other methods may work better. However, the passive model presented here makes it easier to gain an intuitive understanding of the $\rm Z_O$ curve, which is critical for stability analysis.

While the component names and values from the calculations can be identified in the passive model, the arrangement of the components requires explanation. First, keep in a capacitors are open circuits at DC. Therefore, th path through the passive model can be identified as the series path through R_{LOW} and L_{O} , labeled as the first stage in Figure 6. The second stage, C_{LOW} and R_{MID} , are in parallel with R_{LOW} . When the impedance of C_{LOW} begins to encroach upon the value of R_{LOW} , the output impedance will decrease. The impedance stops decreasing once the impedance of C_{LOW} drops below the value of the series R_{MID} resistance.

Once the impedance of the L_O inductor increases above the level of R_{MID} , the curve will increase. The curve continues to increase until the impedance reaches the R_{HIGH} resistance in the third stage, which is in parallel with the first two stages. The C_{DAMP} capacitor is required to prevent R_{HIGH} from interfering with the Z_O curve at low frequencies. C_{DAMP} will be selected such that the R, L, C circuit formed from R_{HIGH} , L_O , and C_{DAMP} has a

damping factor (ζ) greater than one, which prevents undesired peaking in the Z_O curve. The C_{HIGH} impedance in the fourth stage is in parallel with the entire model and will cause the curve to decrease at high frequencies once its impedance is lower than the R_{HIGH} resistance. The R_{VHIGH} resistance is included to flatten the curve back to a known resistance at frequencies much higher than the bandwidth of the op amp. Its value is not critical because it will have an effect well outside of the bandwidths of interest.

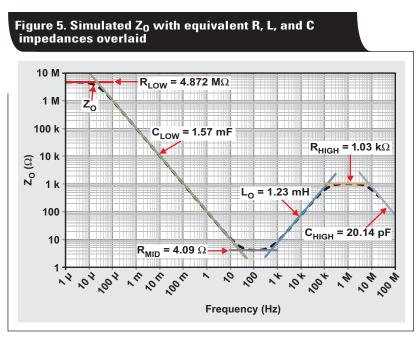
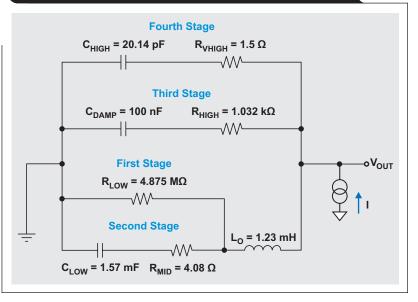


Figure 6. A passive-component Z₀ model for a typical three-stage op amp



Verifying the passive model

The simulation results of the passive model are compared to the original simulated results from the full op-amp transistor-level model in Figure 7. As expected from the calculations, the passive-model output impedance lies directly on top of the results of the op-amp transistor-level model simulation.

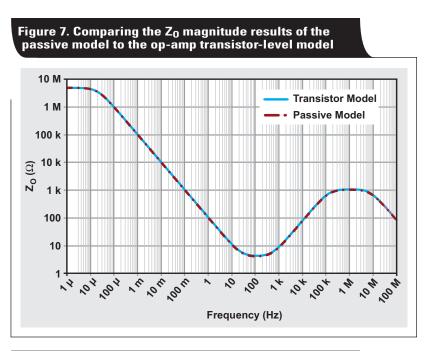
A comparison of the phase results from the passive model and the op-amp transistor-level model are shown in Figure 8. Comparing the phase results is often a more rigorous verification because slight deviations in the magnitude are often easier to identify in the phase response. The passive-model results once again lie directly on top of the results for the op-amp transistor-level model simulated. This confirms that the passive model presented here is an accurate representation of the Z_0 curve of a typical three-stage op amp.

Conclusion

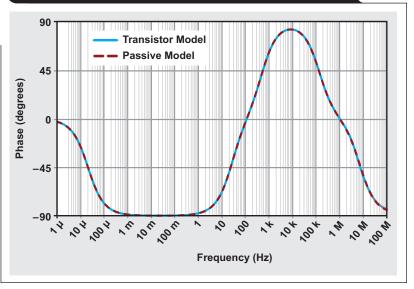
Op-amp output stages have evolved from classic BJT output stages with resistive output impedances to the RLC three-stage output impedances found in many rail-to-rail output stages with high open-loop gain. To help develop a more intuitive understanding of these output impedance structures, a model of an example op-amp output impedance was created out of passive components. The passive model helped to intuitively determine what effects output loading have on the circuit performance in the different regions of the curve. The results for this passive model exactly matched the results from the original op-amp transistor-level simulation model. This proved that the passive RLC model is an accurate representation of the three-stage output impedance that can be used for stability analysis.

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