Migrating From TMS320C6416 to TMS320TCI100

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ABSTRACT

This application report describes issues of interest related to migration from the TMS320C6416 to the TMS320TCI100 device. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the *TMS320C6414, TMS320C6415, TMS320C6416 Fixed-Point Digital Signal Processors Data Sheet* (SPRS146F or later), the *TMS320TCI100 Fixed-Point Digital Signal Processor Data Sheet* (SPRS218), and the *TMS320C6000 Peripherals Reference Guide* (SPRU190) and associated *Manual Update Sheet* (SPRZ122).

Migration issues from the C6416 to TCI100 are indicated with the following symbols:

S Means software modification is required.

H Means hardware modification is required.

D Means the C6416 and TCI100 devices are different (usually due to added features or enhancements on the TCI100 device), but no modification is necessary for migration (i.e., different but compatible).

These symbols are included at the beginning of each section.

C6416:

Unless otherwise noted, the information contained in the C6416 data sheet (see section 7, *References*) should be considered Production Data.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necesarily include testing of all parameters.

TCI100:

Unless otherwise noted, the information contained in the TCI100 data sheet (see section 7, *References*) should be considered Product Preview.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Contents

List of Tables

1 Core Power [H]

The core voltage of the TCI100 is 1.1 V with 5% tolerance (1.2 V with 3% tolerance for high-performance operation); reduced from 1.2 V and 1.4 V, respectively, on the C6416. In systems where the TCI100 replaces the C6416, the power supply circuit on the board must be modified to support this change. Table 1 shows the relationship between operating voltages, frequencies, and CV_{DD} tolerances supported on the TCI100 device. The DV_{DD} (I/O voltage) is unchanged (3.3 V ±5%).

Table 1. Voltages, Frequencies, and CV_{DD} Tolerances on the TCI100 Device

CV_{DD}	Tolerance	Max. Frequency
1.2V	±3%	720 Mhz
1.1V	±5%	600 Mhz

2 Device Identification (ID)

The TMS320TCI100 device is a new product. The JTAG (BSDL) ID and Silicon Revision ID are different than other TMS320C64x DSP devices.

Table 2 identifies the JTAG (BSDL) ID differences between the C6416 and TCI100.

Table 2. JTAG (BSDL) ID for TCI100

Device	JGAG (BSDL) ID			
	Variant	Part Number	Manufacturer	LSB
TCI100	0000	0000000010000001	00000010111	1
C6416 (Rev. 1.1)	0010	0000000001110000	00000010111	1

Table 3 identifies the Silicon Revision ID differences between the C6416/15/14 and TCI100.

Table 3. Silicon Revision ID for TCI100

Device	Silicon Revision ID (0x01B00200)	
	Turbo ID [20]	Revision ID [19:16]
TCI100	1	0000
C6416 (Silicon Rev. 1.1)	0	0010
C6415 (Silicon Rev. 1.1)	0	0010
C6414 (Silicon Rev. 1.1)	0	0010

3 Package and Pins [H D]

The physical dimensions and pin out of the package used for TCI100are the same as those on the C6416. Some modifications can be made to the package that are transparent to the user. These changes (e.g., different substrate) may affect the thermal characteristics of the package; see the *TMS320TCI100 Fixed-Point Digital Signal Processor Data Sheet* (SPRS218).

3.1 External Terminators [H D]

TCI100 input/output (I/O) buffers have been modified for the new 0.09-μm manufacturing process and have different output impedance than those of the C6416. For boards designed with the C6416, termination resistor values need to be recalculated and changed if necessary.

4 PLL/CPU Clock [H]

PLL configuration options on TCI100 are the same as were available on C6416.

For a board using C6416 with CLKMODE [1:0] set to 10b, using a 50-MHz CLKIN would result in a 600-MHz CPU clock. For the TCI100 to maintain a CPU frequency of 600 MHz, no changes to the board are necessary, since the CLKMODE [1:0] pins remain at 10b. With the 50-MHz CLKIN, the x12 PLL mode still results in 600 MHz. In order to achieve the maximum frequency of 720 MHz, CLKIN needs to be increased to 60 MHz.

Table 4 shows the changes in PLL modes when transferring from C6416 to TCI100.

Table 4. Changes in PLL Modes When Transferring From C6416 to TCI100

C6416				
PLL MODE	**CLKIN (Min.)**	**CLKIN (Max.)**	**CPU CLK (Min.)**	**CPU_CLK (Max.)**
6	30	75	180	450
12	30	60	360	720
TCI100				
6	42	75	252	450
12	42	60	504	720

5 System Reset [D]

There is minor modification in the reset logic of the TCI100 that will cause system reset to extend by approximately 16070 CPU cycles. This delay occurs after the device is powered on, and device reset, /RESET, goes inactive. The device will not be fully out of reset and initialized until after the 16070P (P=1/CPU) delay, and the “host boot” should not proceed until the 16070P delay has elapsed.

In addition to the previous difference, when the device has been powered up and the PLL is in a stable state, when device reset, /RESET, goes active it will cause the PLL to reset. This requires that the device reset, /RESET, be held for 250μs to give the PLL time to stabilize. This is different than the 6416 where the /RESET pulse needed to be only 10P (P=1/CPU) since the PLL was already stable and not reset by the device reset going active.

These two items result in the compatibility of the TCI100 relative to 6416 during and a relatively short time after reset is not 100%.

NOTE: Cycle compatibility after the 16070 cycles is 100%.

6 I/O Timing [D S]

The TCI100 has the same AC characteristics for I/O timings as the timings of the C6416 (600 MHz and below). When the CPU/X option is used for peripheral clocking, the relative timing to the reference remains the same, but the absolute timing of the I/O could be impacted. This requires reconfiguring the peripheral registers for controlling the timing parameters, depending upon the system requirement. Therefore, overall timing can be recalculated to adjust the cycle-time difference by using the C6416 and TCI100 data sheets (see section 7, *References*).

NOTE: For keeping 600 MHz, there is no change required.

6.1 EMIF

The user should verify the EMIF timings per -6E3, as specified in the C6416 and TCI100 data sheets (see section 7, *References*).

Assuming that the TCI100 is running at 720 MHz, and EMIF at CPU/6 = 120MHz, be aware of the fact that input/output setup times will change, based on EMIF going from a 100-MHz to 120-MHz interface. Input/output hold times will remain the same. As -6E3 timings are ensured up to 133 MHz, the user should not have a problem meeting timing at 120 MHz.

6.2 McBSP

The McBSP is able to operate at a rate of CPU/8, which for the TCI100 at 720 MHz allows for running at McBSP operation of 90 MHz, compared to 75 MHz for the C6416. Any single McBSP can run at 90 MHz, but system-level issues (i.e., EDMA bandwidth and prioritization), which impact the operating frequency of all peripherals, must be considered in multiple McBSP operations.

7 References

1. *TMS320C6416 Fixed-Point Digital Signal Processor Data Sheet* (SPRS146F or later).
2. *TMS320TCI100 Fixed-Point Digital Signal Processor Data Sheet* (SPRS218).
3. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
4. *TMS320C6000 Peripherals Reference Guide − Manual Update Sheet* for SPRU190D (SPRZ122).

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