

- SH01 - TITLE PAGE
- SH02 - SoC MCASP
- SH03 - SoC SERIAL I/O
- SH04 - SoC SD/MMC IF
- SH05 - SoC MLB
- SH06 - SoC ETHERNET/USB
- SH07 - SoC GPMC
- SH08 - SoC DDR EMIF1 INTERFACE
- SH09 - SoC DDR EMIF2 NC
- SH10 - SoC HDMI
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- SH12 - SoC VIDEO PORTS IN
- SH13 - SoC SATA/PCIe INTERFACE
- SH14 - SoC JTAG
- SH15 - SoC CLOCKS
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- SH18 - SoC POWER LV8
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- SH23 - DDR3 EMIF1 TESTPOINTS
- SH24 - DDR3 BANK 1 ECC
- SH25 - DDR3 MEMORY BANK 1
- SH26 - DDR3 MEMORY CAPS BANK 1
- SH27 - DDR TERMINATION BANK 1
- SH28 - MUX A/C QSPI/EMMC/GPMC
- SH29 - MUX B VOUT3/GPMC
- SH30 - MUX B VOUT3/GPMC ADD
- SH31 - MUX D GMPCA
- SH32 - MUX E VIN2
- SH33 - MUX G ENET0/VIN4
- SH34 - MUX H MCASP/VIN6A
- SH35 - MUX J/K/L SERIAL I/O
- SH36 - MEM SPI FLASH
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- SH40 - MEM SD CARD
- SH41 - USB VBUS
- SH42 - USB CONNECTORS
- SH43 - USB FTDI UART
- SH44 - AIC3106
- SH45 - SERDES CLOCK
- SH46 - PCIe CONNECTORS
- SH47 - LCD CONNECTOR
- SH48 - HDMI OUTPUT CONNECTOR
- SH49 - FPD LINK
- SH50 - CAMERA IF
- SH51 - CAN CONNECTORS
- SH52 - I2C EEPROM/TEMP SENSOR
- SH53 - I2C EXPANDER
- SH54 - BOOTSWITCHES
- SH55 - COM8 LEVEL TRANSLATOR
- SH56 - COM8 CONNECTOR
- SH57 - ETHERNET POWER AND RESET
- SH58 - ETHERNET PORT0
- SH59 - ETHERNET PORT1
- SH60 - APPLICATION IF CONN1
- SH61 - APPLICATION IF CONN2
- SH62 - APPLICATION IF CONN3
- SH63 - RESET
- SH64 - POWER INPUT
- SH65 - POWER TPS443351DAP
- SH66 - MISC POWER SWITCHES
- SH67 - PMIC
- SH68 - POWER MONITOR 1
- SH69 - POWER MONITOR 2
- SH70 - DARA
- SH71 - ECN REV B1 TO C

REVISION STATUS OF SHEETS

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SH										
REV										
SH										
REV	D									
SH	71									
REV	C	C	A	C	C	C	D	C	C	C
SH	61	62	63	64	65	66	67	68	69	70
REV	A	C2	A	A	A	A	C	D	D	C
SH	51	52	53	54	55	56	57	58	59	60
REV	A	B	A	A	A	B	A	C	A	B
SH	41	42	43	44	45	46	47	48	49	50
REV	A	D	C	A	A	A	A	A	C	C
SH	31	32	33	34	35	36	37	38	39	40
REV	A	A	B	C	C	A	C	A	C	C
SH	21	22	23	24	25	26	27	28	29	30
REV	D	A	C	C	A	A	A	A	A	D2
SH	11	12	13	14	15	16	17	18	19	20
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SH	1	2	3	4	5	6	7	8	9	10

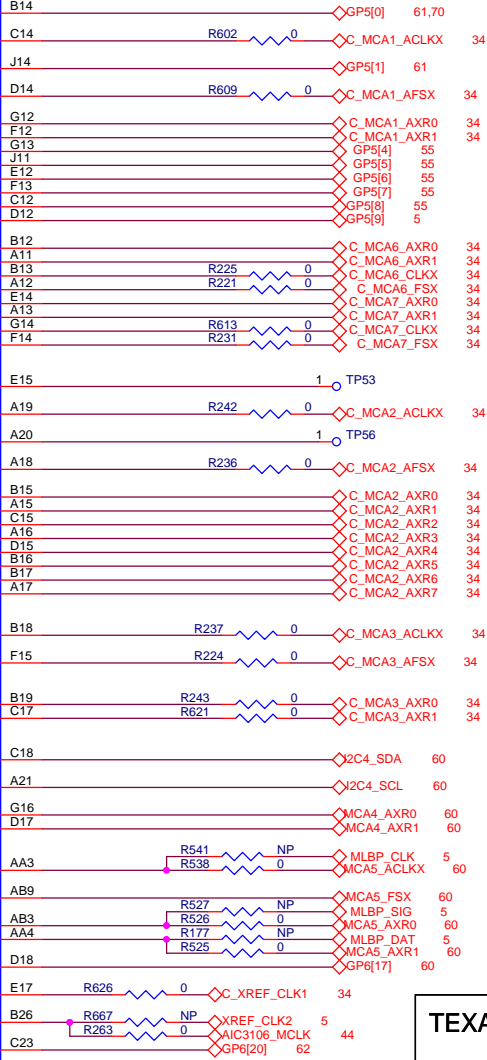
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CHK	DATE
T.W.K.	11/12/2015
ENGR	DATE
J.A.C.	11/12/2015
ENGR-MGR	DATE
J.A.C.	11/12/2015
QA	DATE
C.M.D.	11/12/2015
MFG	DATE
J.A.C.	11/12/2015
RLSE	DATE
J.A.C.	11/12/2015

APPLICATION

TEXAS INSTRUMENTS INCORPORATED		
Title: DRA72x/TA2Ex EVM CPU Board		
Page Contents: TITLE PAGE		
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MCASP1_ACLKR/MCASP7_axr[2]/VOUT2_d[0]/VIN2a_d[0]/i2c4_sda/gpio5_0
 MCASP1_ACLKX/VIN1a_fld0/i2c3_sda/pr2_mdio_mdclk/pr2_pr1_r31[7]/pr2_pr1_pr1_r30[7]/gpio7_31
 MCASP1_FSR/MCASP7_axr[3]/VOUT2_d[1]/VIN2a_d[1]/i2c4_scl/gpio5_1
 MCASP1_FXS/VIN1a_de0/i2c3_scl/pr2_mdio_data/gpio7_30
 MCASP1_AXR00/uart6_rxd/VIN1a_vsnc0/i2c5_sda/pr2_mii0_rxer/pr2_pr1_pr1_r31[8]/pr2_pr1_pr1_r30[8]/gpio5_2
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 MCASP1_AXR02/MCASP6_axr[2]/uart6_ctsn/VOUT2_d[2]/VIN2a_d[2]/gpio5_4
 MCASP1_AXR03/MCASP6_axr[3]/uart6_rtsn/VOUT2_d[3]/VIN2a_d[3]/gpio5_5
 MCASP1_AXR04/MCASP4_axr[2]/VOUT2_d[4]/VIN2a_d[4]/gpio5_6
 MCASP1_AXR05/MCASP4_axr[3]/VOUT2_d[5]/VIN2a_d[5]/gpio5_7
 MCASP1_AXR06/MCASP5_axr[2]/VOUT2_d[6]/VIN2a_d[6]/gpio5_8
 MCASP1_AXR07/MCASP5_axr[3]/VOUT2_d[7]/VIN2a_d[7]/timer4/gpio5_9
 MCASP1_AXR08/MCASP6_axr[0]/spi3_sclk/VIN1a_d[15]/timer5/pr2_mii0_txen/pr2_pr1_pr1_r31[10]/pr2_pr1_pr1_r30[10]/gpio5_10
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 MCASP2_AXR1/VOUT2_d[11]/VIN2a_d[11]
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 MCASP5_AXR1/spi4_cs[0]/uart9_rtsn/uart3_txd/mlb_dat
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 XREF_CLK1/MCASP2_axr[9]/MCASP1_axr[5]/MCASP2_ahclkx/MCASP6_ahclkx/at_clk1/VIN1a_clk0/timer14/pr2_mii1_crs/pr2_pr1_r31[6]
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J6ECO_09Dec2013



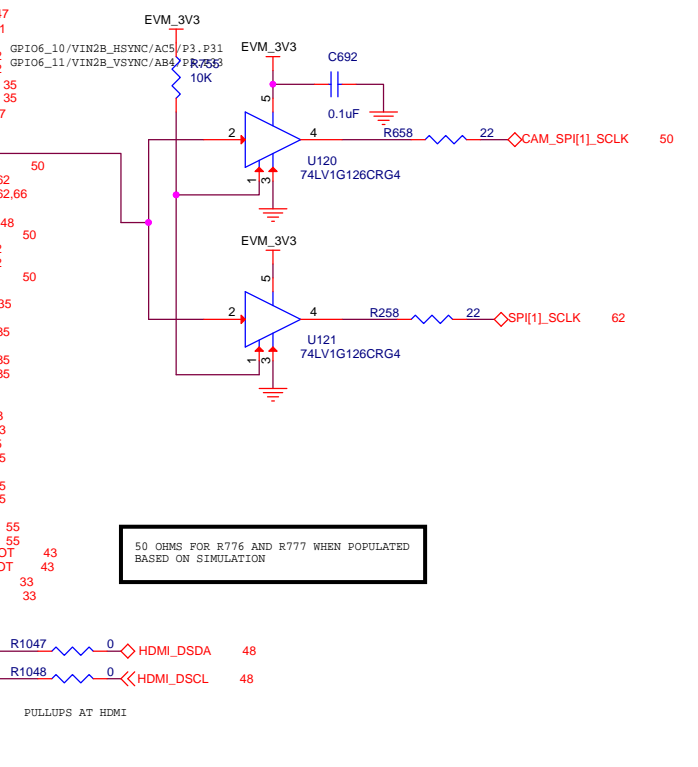
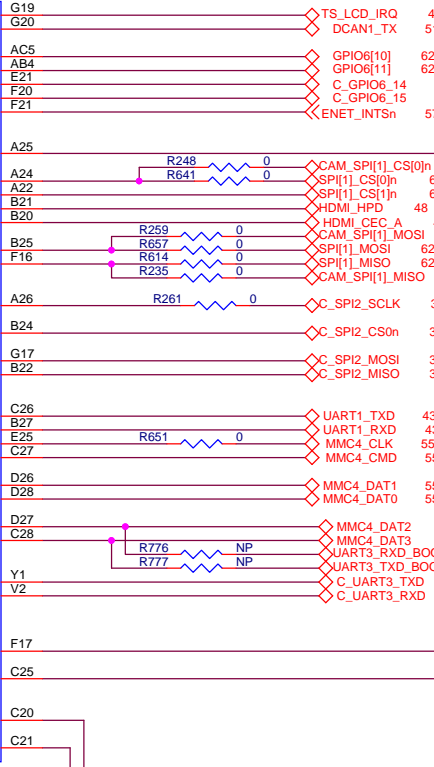
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2AEx EVM CPU Board

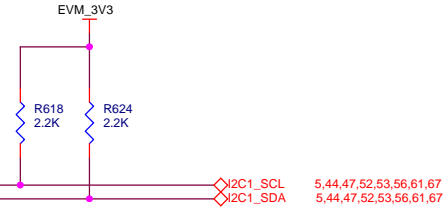
Page Contents: SoC MCASP

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50 OHMS FOR R776 AND R777 WHEN POPULATED
 BASED ON SIMULATION



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Title: DRA72x/TA2A2Ex EVM CPU Board

Page Contents: SoC SERIAL I/O

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TEXAS INSTRUMENTS INCORPORATED

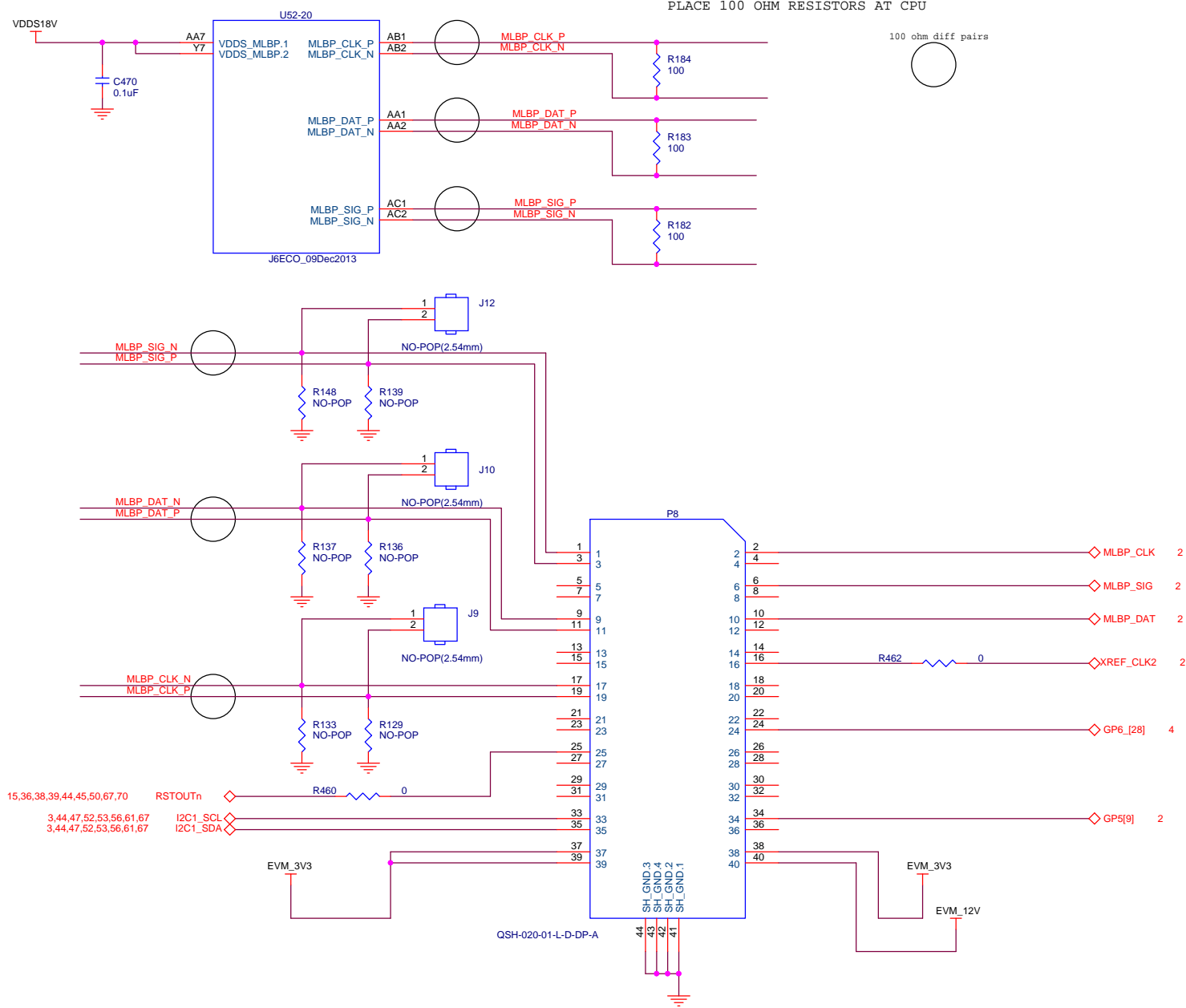
Title: DRA72x/TDA2Ex EVM CPU Board

Page Contents: SoC SD/MMC IF

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PLACE 100 OHM RESISTORS AT CPU

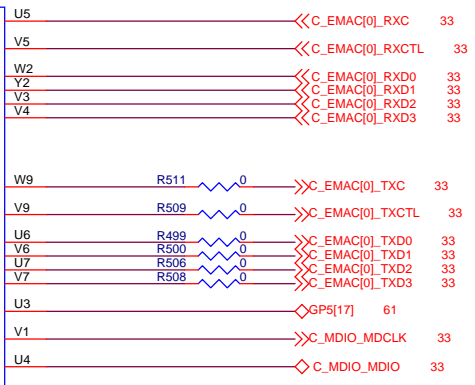


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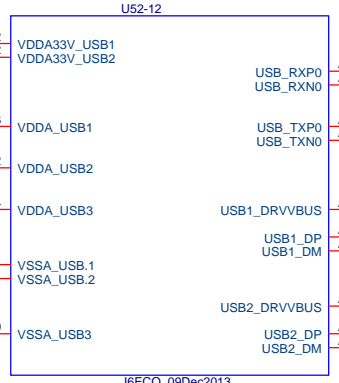
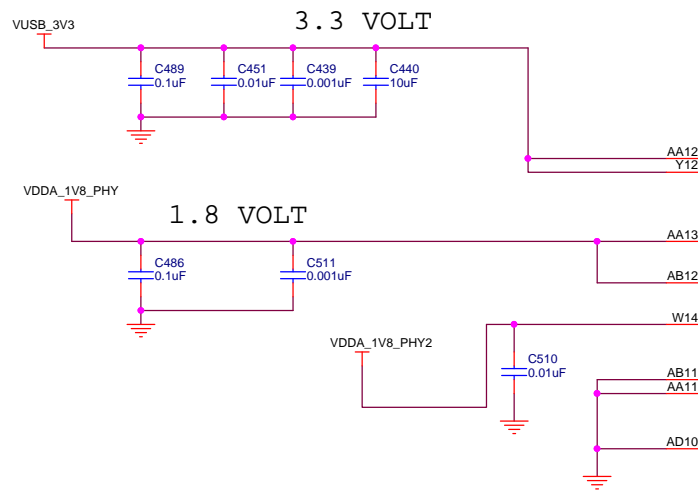
Title: DRA72x/TDA2Ex EVM CPU Board

Page Contents: SoC MLB

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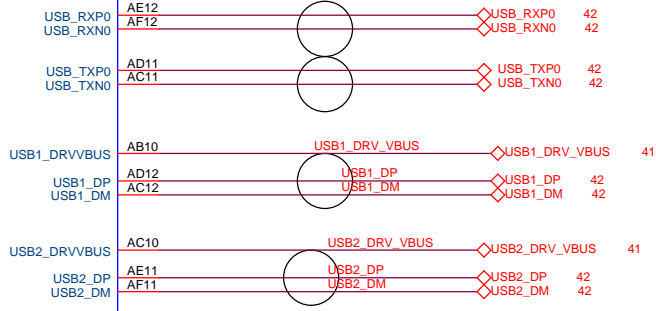


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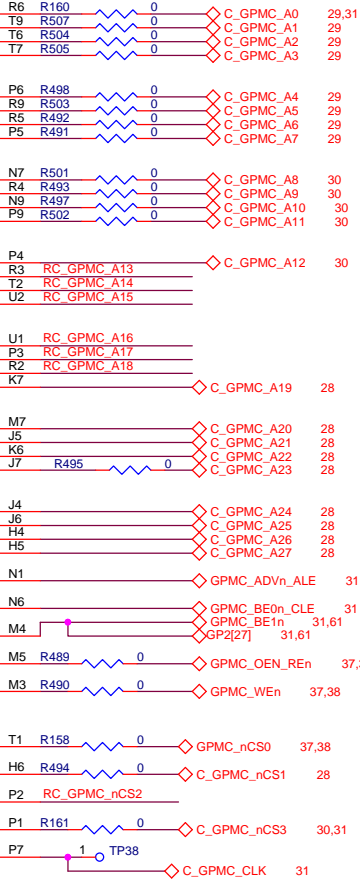
DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



TEXAS INSTRUMENTS INCORPORATED			
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Page Contents: SoC ETHERNET/USB			
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TEXAS INSTRUMENTS INCORPORATED

Title: DRA72z/TA2AEx EVM CPU Board

Page Contents: SoC GPMC

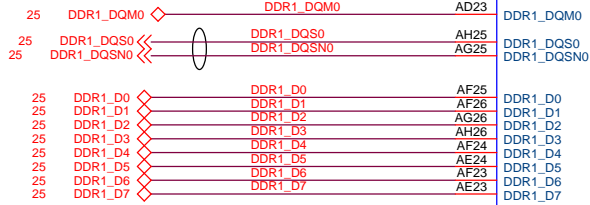
Size: B	DOC NO: 517502	REV: A
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AQSPI PATH IS THE FAST PATH WITH MAX TRACE LENGTH OF 2.75 INCHES. THIS RESISTOR POPULATIONS IS ON BOTH ENDS OF THE NET. THE OTHER END IS THE SPI FLASH U18.

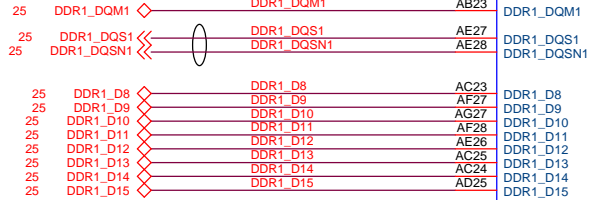
EACH DATA GROUP IS MATCHED WITHIN THE GROUP. SEE PCB GUIDELINES FOR SPECIFIC RULES.

differential pairs 100 ohm
6 places

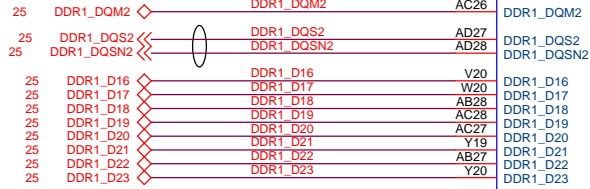
Data Group 0-0



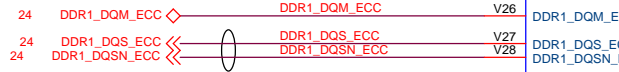
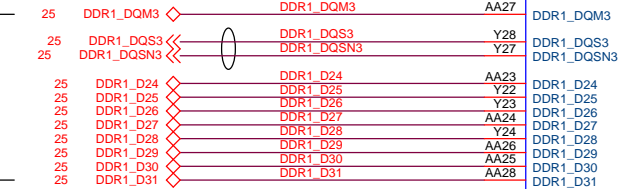
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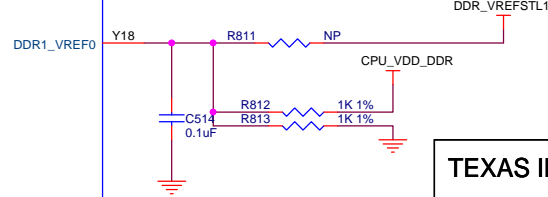
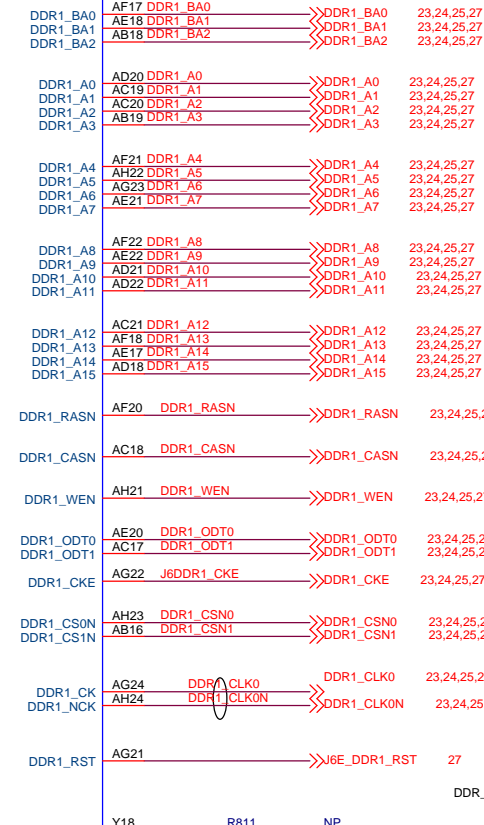
Data Group 0-2



Data Group 0-3



U52-5



TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2AEx EVM CPU Board

Page Contents: SoC DDR EMIF1 INTERFACE

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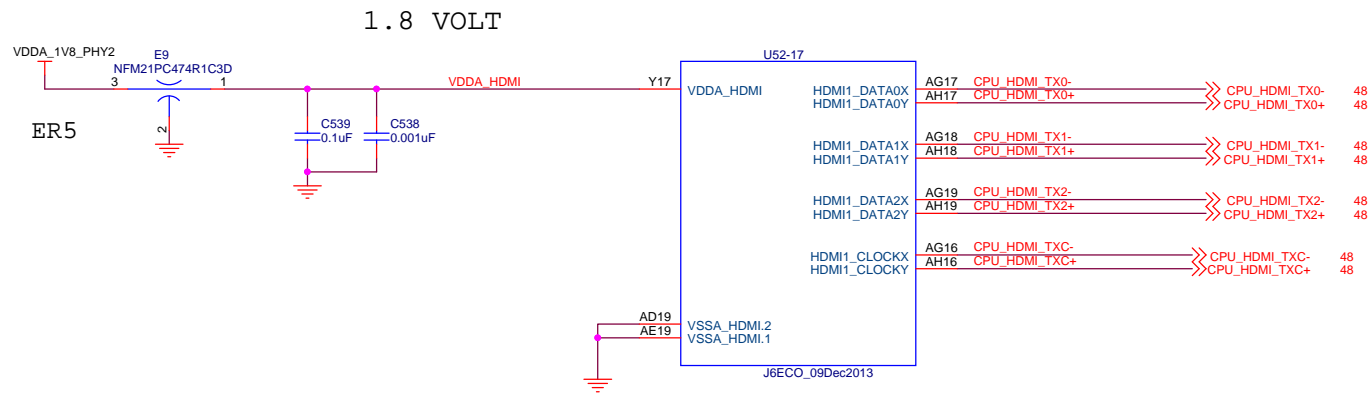
J6ECO_09Dec2013

U52-6

F28	NC_F28		
G28	NC_G28	NC_U23	U23
G27	NC_G27	NC_U27	U27
		NC_U26	U26
E26	NC_E26	NC_R25	R25
G25	NC_G25	NC_R26	R26
F25	NC_F25	NC_R28	R28
F24	NC_F24	NC_R27	R27
F26	NC_F26		
F27	NC_F27		
E27	NC_E27	NC_P23	P23
E28	NC_E28	NC_P22	P22
		NC_P25	P25
		NC_N20	N20
G24	NC_G24		
H27	NC_H27	NC_P27	P27
H28	NC_H28	NC_N27	N27
		NC_N23	N23
		NC_P26	P26
H23	NC_H23		
H25	NC_H25		
H24	NC_H24	NC_N28	N28
H26	NC_H26	NC_T22	T22
G26	NC_G26	NC_R22	R22
J25	NC_J25	NC_U22	U22
J26	NC_J26		
J24	NC_J24		
		NC_T23	T23
K23	NC_K23		
K27	NC_K27	NC_U28	U28
K28	NC_K28		
		NC_U25	U25
L22	NC_L22		
K20	NC_K20	NC_R23	R23
K21	NC_K21		
L23	NC_L23		
L24	NC_L24	NC_U24	U24
J23	NC_J23		
K22	NC_K22		
J20	NC_J20	NC_P24	P24
M22	NC_M22		
M28	NC_M28		
M27	NC_M27	NC_T28	T28
		NC_T27	T27
L27	NC_L27		
L26	NC_L26		
L25	NC_L25		
L28	NC_L28	NC_R24	R24
M23	NC_M23		
M24	NC_M24		
M25	NC_M25	NC_N22	N22
M26	NC_M26		

J6ECO_09Dec2013

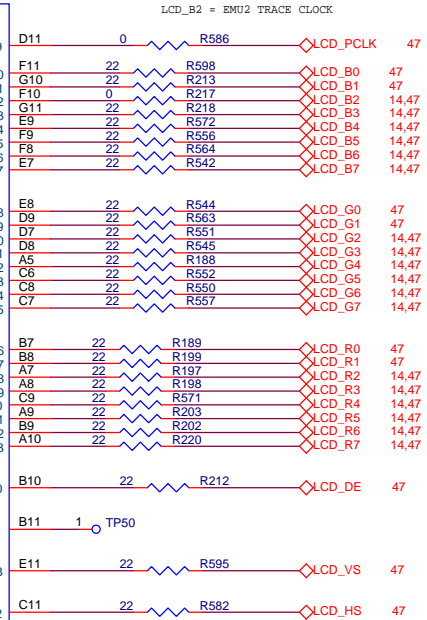
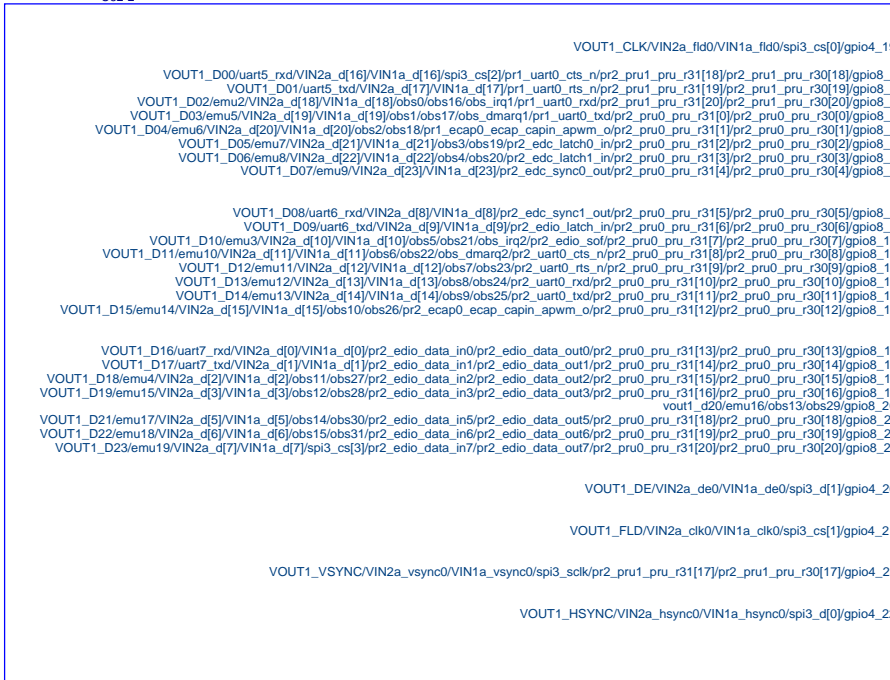
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: SoC DDR EMIF2 NC			
Size: B	DOC NO: 517502	REV: A	
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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: SoC HDMI			
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22 OHM OK FOR LCD AS IT IS NOT GOING THROUGH MIXES.

U52-2



J6ECO_09Dec2013

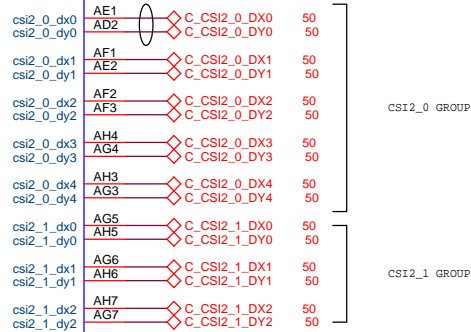
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TDA2Ex EVM CPU Board

Page Contents: SoC VOUT1 PORT LCD

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- NC_AE8
- NC_AD8
- NC_AG8
- NC_AG2
- NC_AF4
- NC_AE3
- NC_AE5
- NC_AE6
- NC_AD3
- NC_AD9
- NC_AF9
- NC_AE9
- NC_AF8



TEXAS INSTRUMENTS INCORPORATED

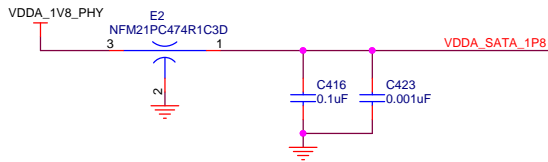
Title: DRA72x/TA2AEx EVM CPU Board

Page Contents: SoC VIDEO PORTS IN

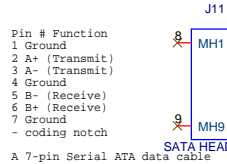
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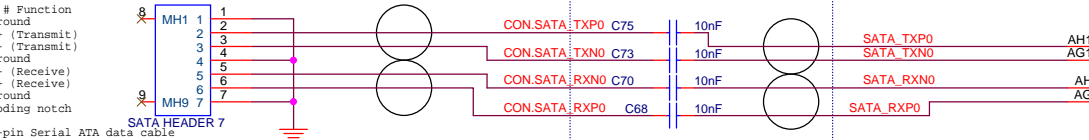
1.8 VOLT



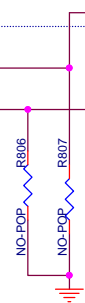
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100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



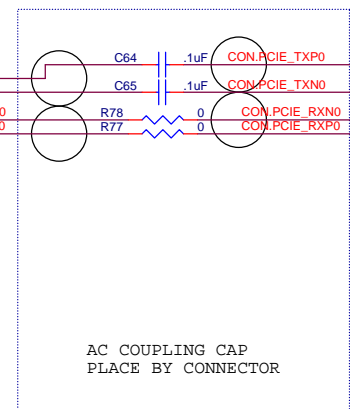
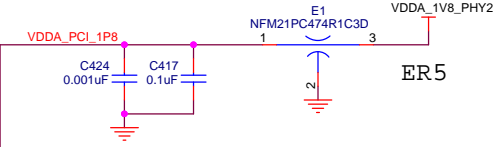
AC COUPLING CAP
PLACE BY CONNECTOR



DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

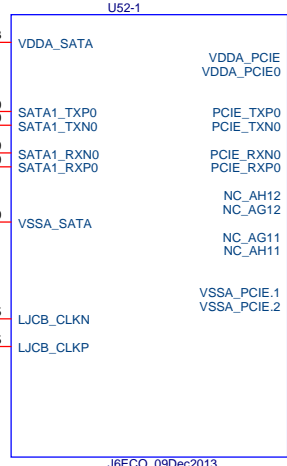


1.8 VOLT



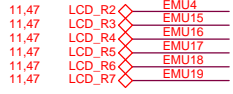
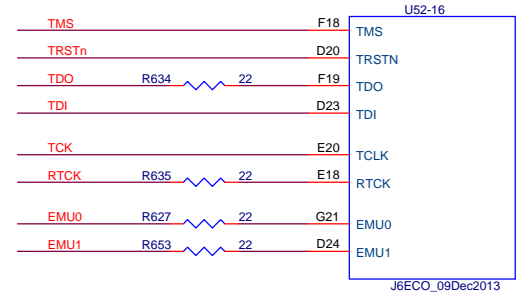
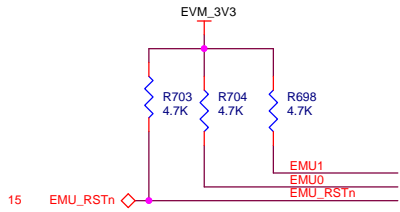
AC COUPLING CAP
PLACE BY CONNECTOR

DIFFERENTIAL PAIR
XXXX OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

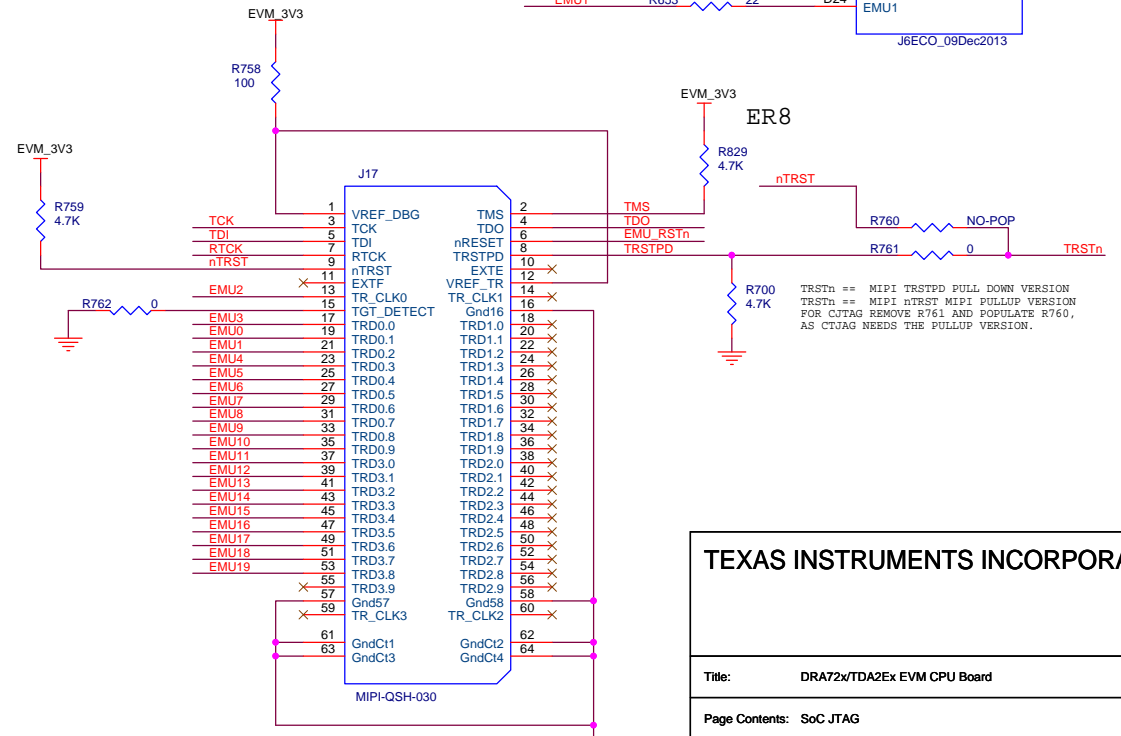


TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: SoC SATA/PCIe INTERFACE			
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EMUX SIGNALS NEED TO ROUTE FROM U52 THROUGH J17/J14 THEN TO LCD. THE TRACE LENGTH RULES FOR THE LCD SIGNALS NEEDS TO BE MAINTAINED.



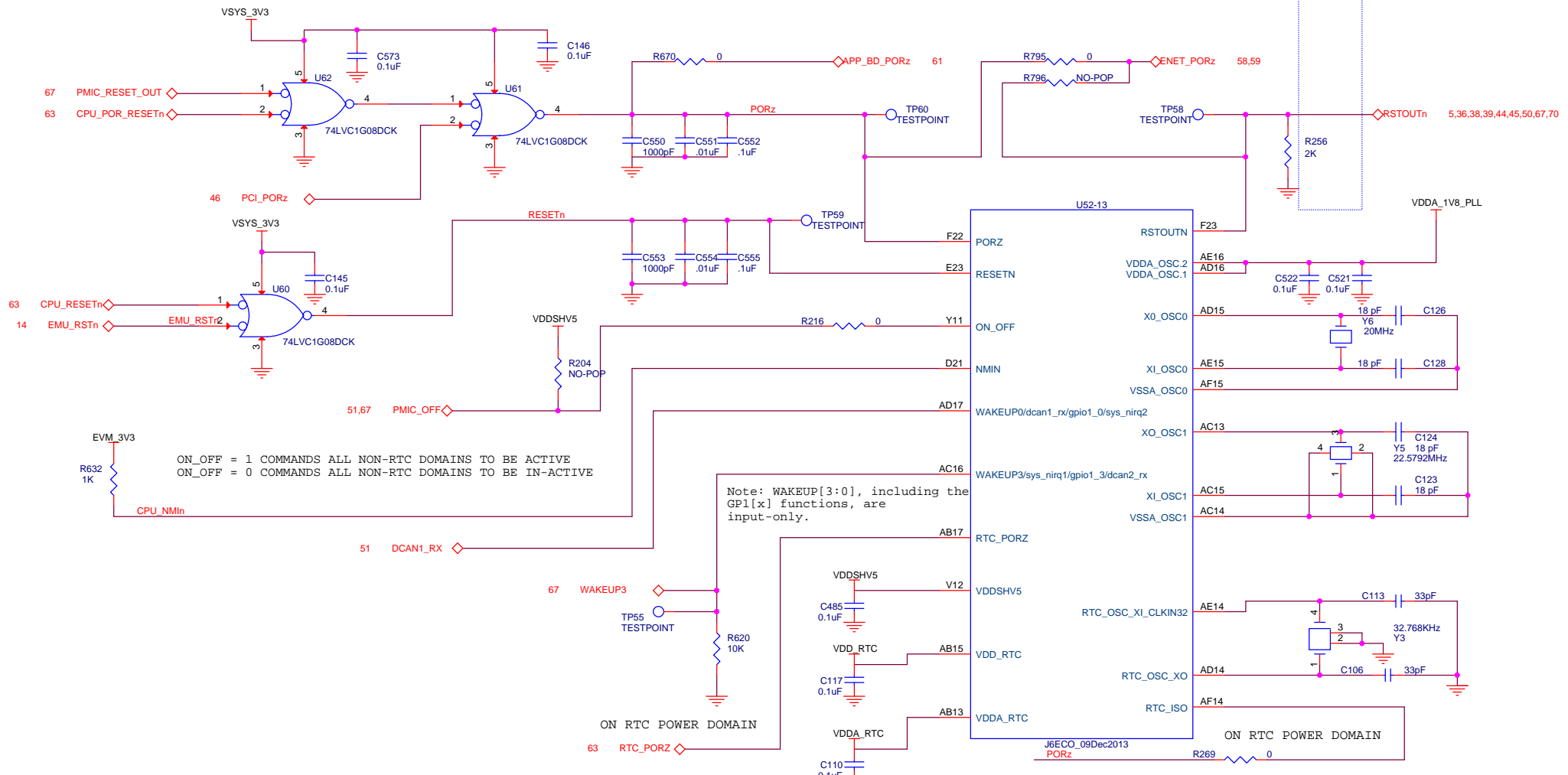
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Title: DRA72x/TDA2Ex EVM CPU Board

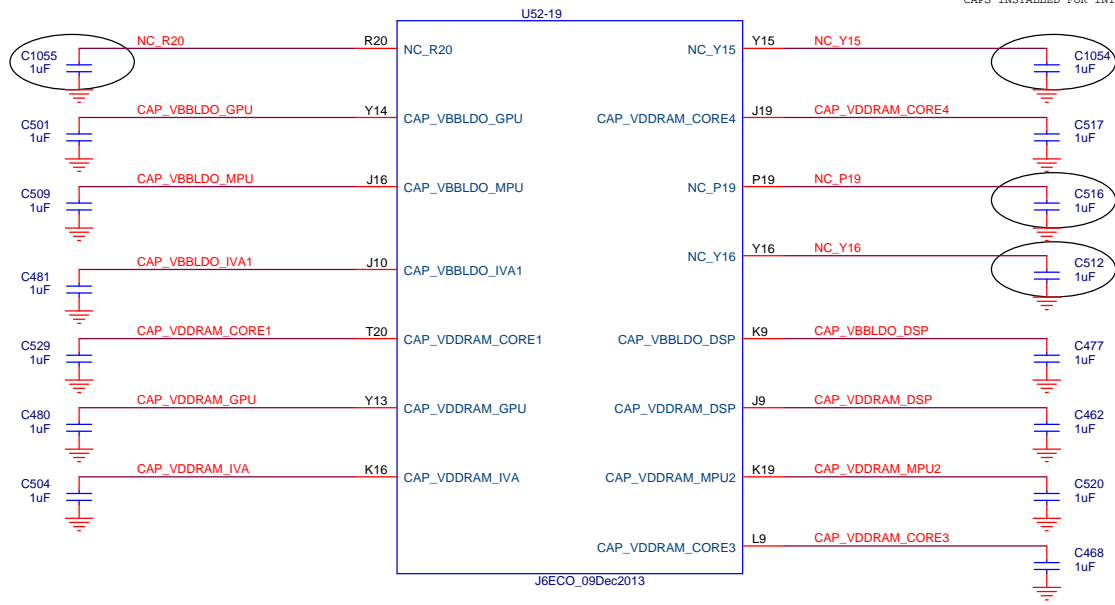
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Size: B	DOC NO: 517502	REV: C
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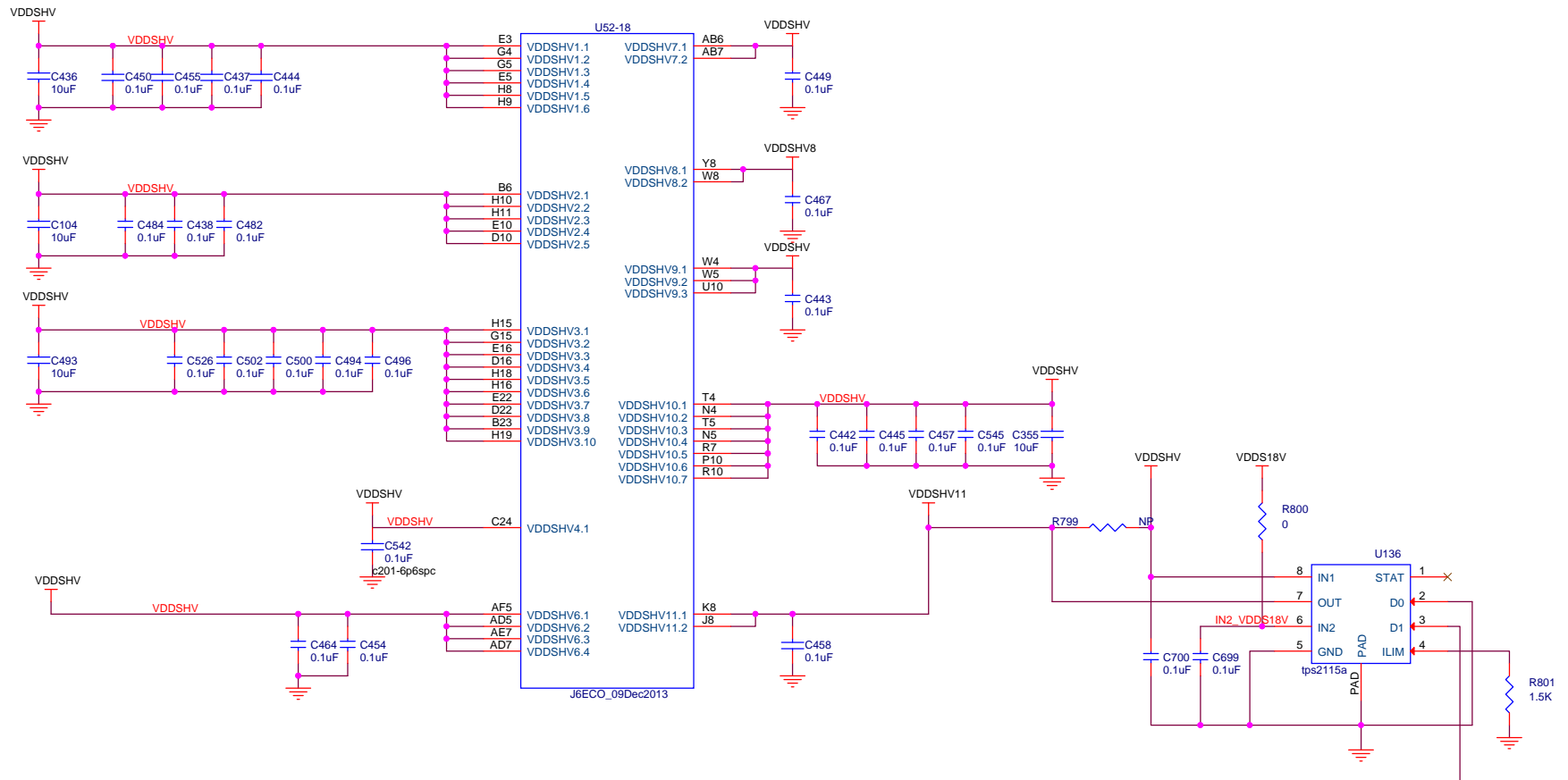
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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2A2Ex EVM CPU Board			
Page Contents: SoC CLOCKS			
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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: SoC INTERNAL LDOS			
Size: B	DOC NO: 517502	REV: A	
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28.53,54 MMC2_SELn

D1=1, IN1 NOR BOOT
D1=0, IN2 eMMC BOOT
BOOT SWITCHES DEFAULT AS PULLUPS. SWITCH
CLOSED IS PULL DOWN TO SELECT FUNCTION.

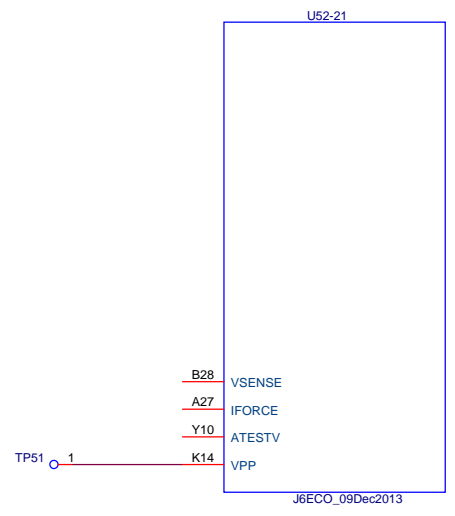
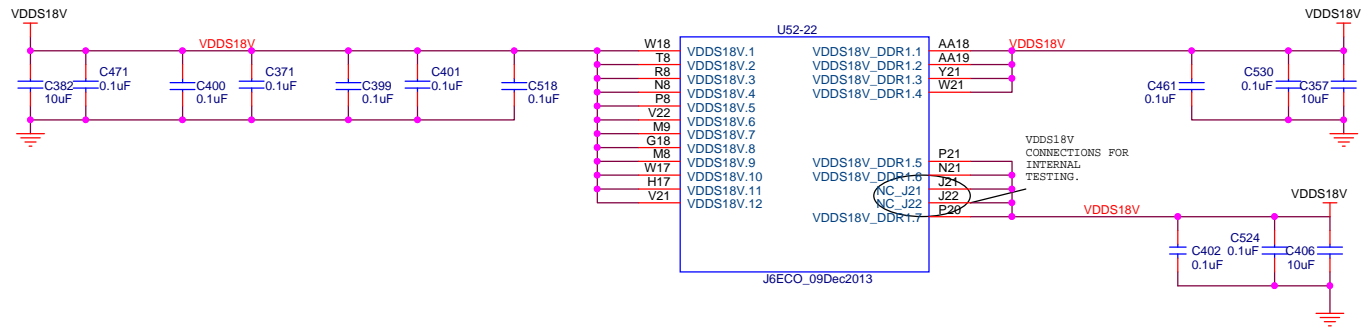
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Title: DRA72x/TA2Ex EVM CPU Board

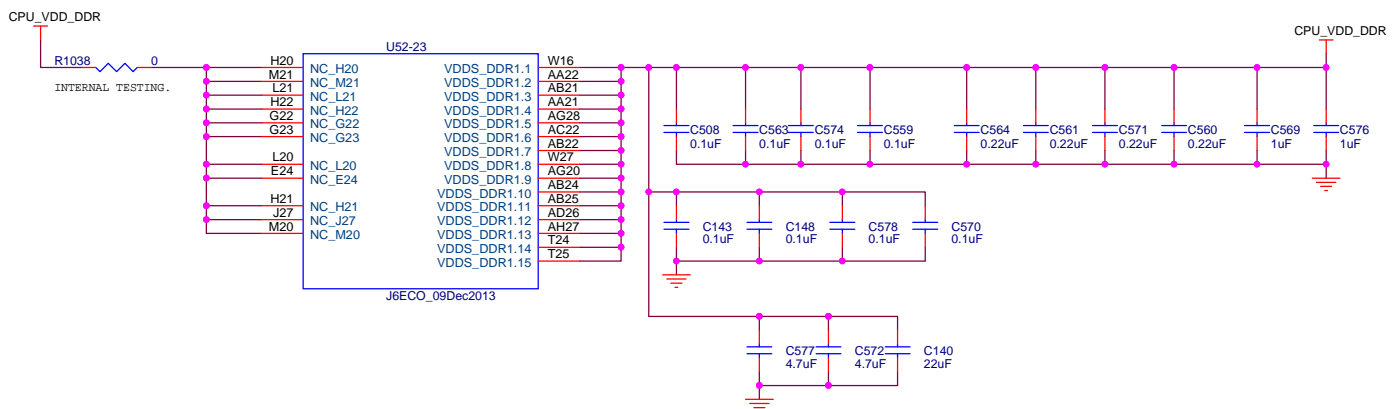
Page Contents: SoC IO POWER

Size: B	DOC NO: 517502	REV: A
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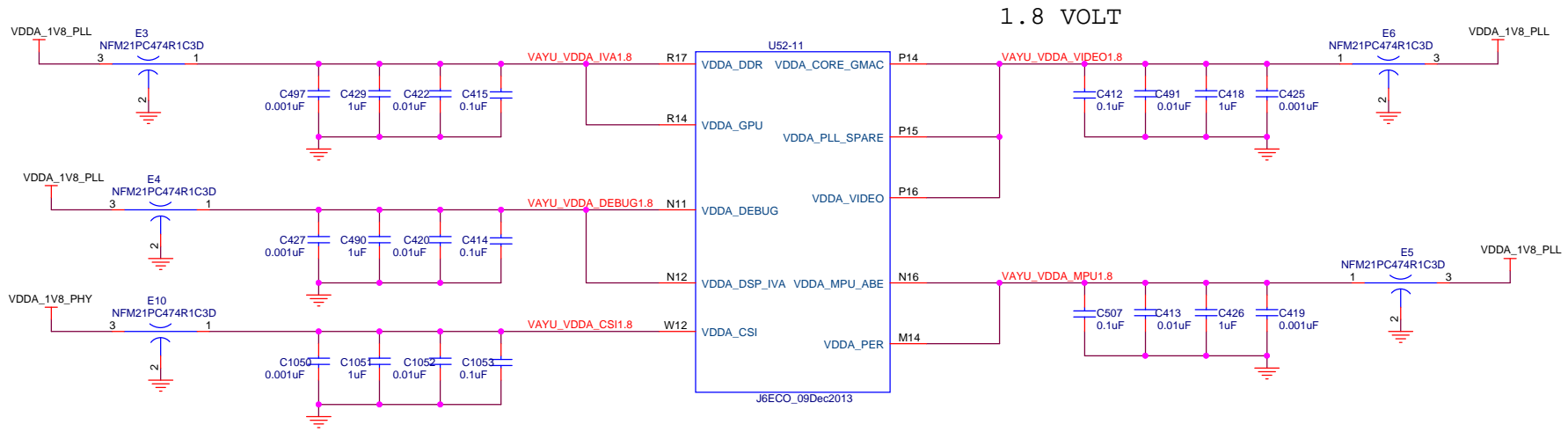
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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: SoC POWER 1V8			
Size: B	DOC NO: 517502	REV: A	
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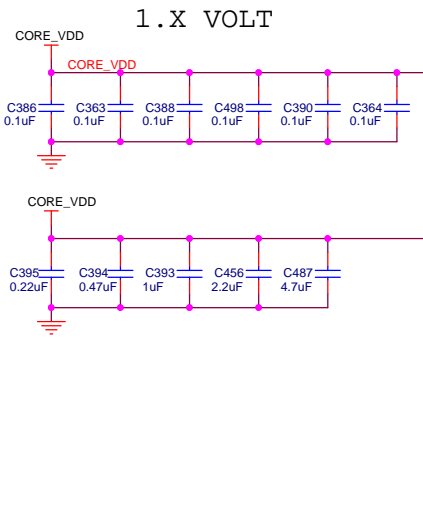


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Title: DRA72x/TDA2Ex EVM CPU Board		
Page Contents: SoC DDR POWER		
Size: B	DOC NO: 517502	REV: A
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1.8 VOLT

TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: SoC 1V8A			
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CAPACITANCE	SIZE
.1uF	0201
.22uF	0201
.47uF	0201
1uF	0201
2.2uF	0402
4.7uF	0402
10uF	0402
22uF	0603

- V8 VDD.1
- HH3 VDD.18
- HH4 VDD.22
- N10 VDD.6
- N13 VDD.16
- P11 VDD.9
- R16 VDD.8
- R19 VDD.26
- T13 VDD.27
- T16 VDD.13
- U8 VDD.25
- U9 VDD.29
- U13 VDD.2
- P12 VDD.3
- VDD.12
- L7 VDD.34
- L8 VDD.15
- J17 VDD.15
- J18 VDD.X1
- P13 VDD.X2
- T19 VDD.X3
- U16 VDD.X7
- V16 VDD.X8
- VDD.X9

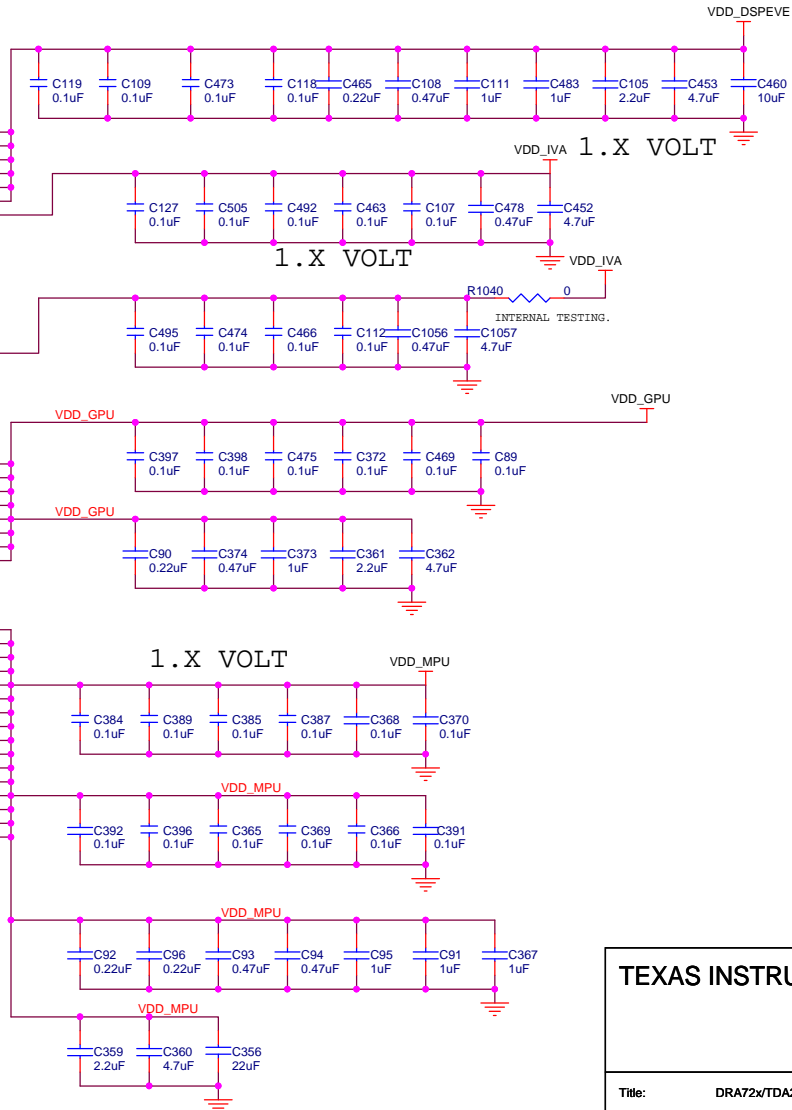
- K10 VDD_DSP1
- K11 VDD_DSP2
- L10 VDD_DSP3
- L11 VDD_DSP4
- M10 VDD_DSP5
- M11 VDD_DSP6
- J13 VDD_IVA1
- K12 VDD_IVA2
- K13 VDD_IVA3
- L12 VDD_IVA4
- M12 VDD_IVA5
- M13 VDD_IVA6

- U18 NC_U18
- U19 NC_U19
- V18 NC_V18
- V19 NC_V19

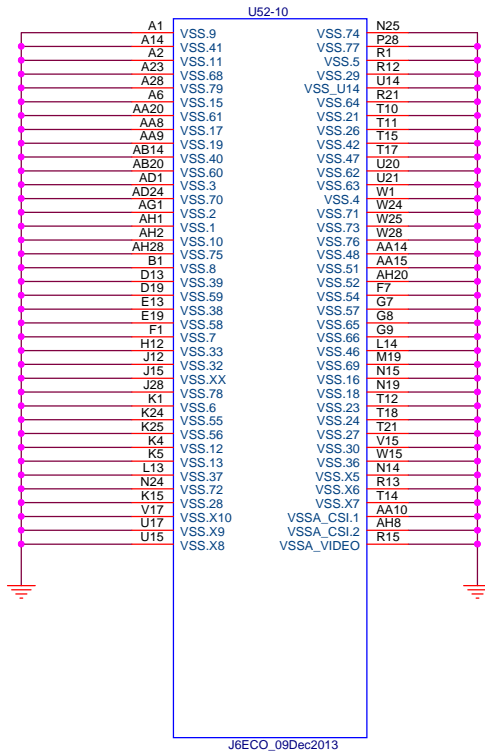
- W10 VDD_GPU.1
- V10 VDD_GPU.2
- V11 VDD_GPU.3
- W11 VDD_GPU.4
- U11 VDD_GPU.5
- U12 VDD_GPU.6
- V14 VDD_GPU.7
- W13 VDD_GPU.8

- N18 VDD_MPU.1
- K18 VDD_MPU.2
- L19 VDD_MPU.3
- N17 VDD_MPU.4
- M17 VDD_MPU.5
- L17 VDD_MPU.6
- M18 VDD_MPU.7
- L18 VDD_MPU.8
- P18 VDD_MPU.9
- K17 VDD_MPU.10
- L15 VDD_MPU.11
- L16 VDD_MPU.12
- M15 VDD_MPU.13
- M16 VDD_MPU.14
- P17 VDD_MPU.15
- R18 VDD_MPU.16

J6ECO_09Dec2013



TEXAS INSTRUMENTS INCORPORATED		
Title: DRA72x/TDA2Ex EVM CPU Board		
Page Contents: SoC CORE POWER		
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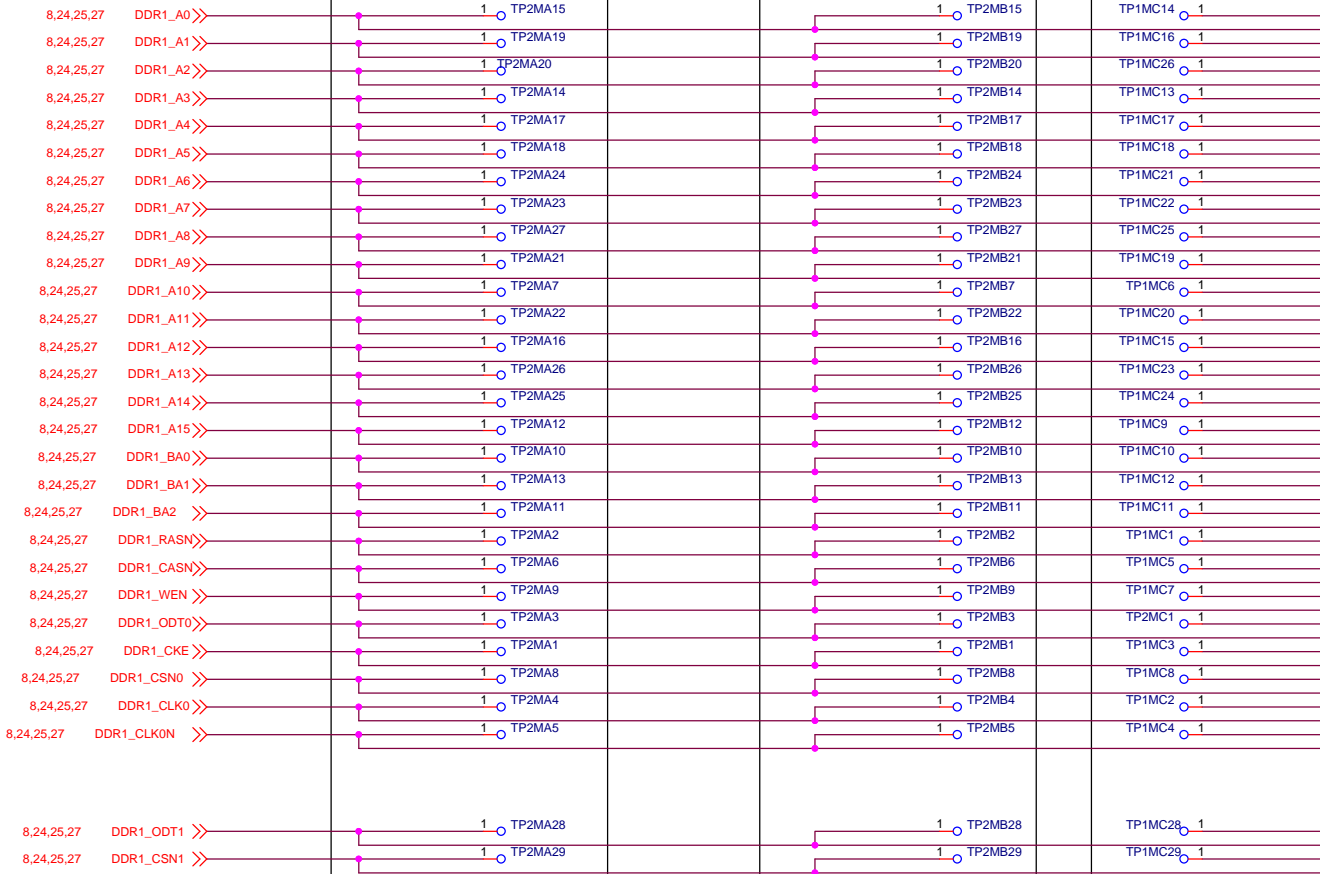


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Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: SoC GROUND PINS			
Size: B	DOC NO: 517502	REV: A	
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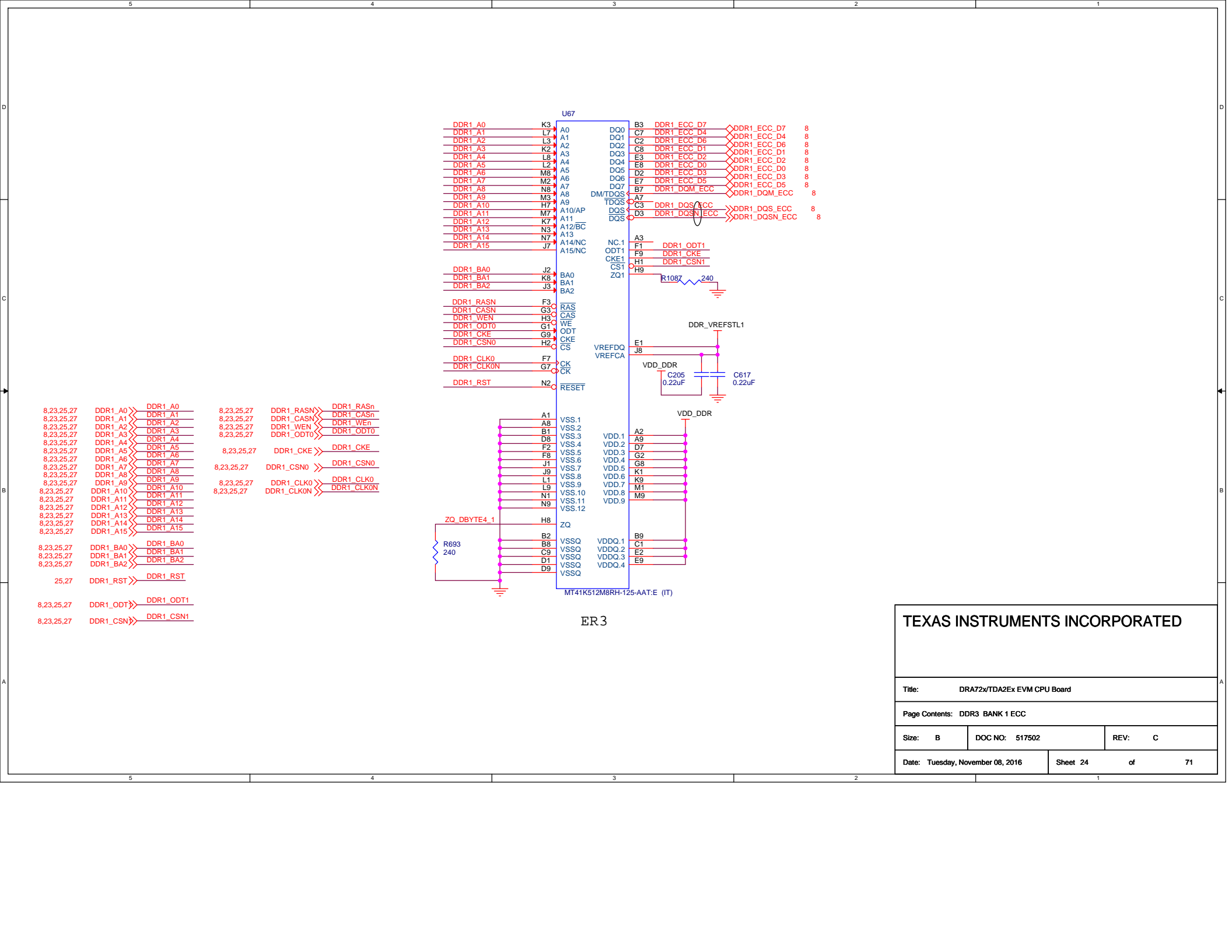
MEMORY 1
MEMORY 2

MEMORY 3
MEMORY 4

ECC

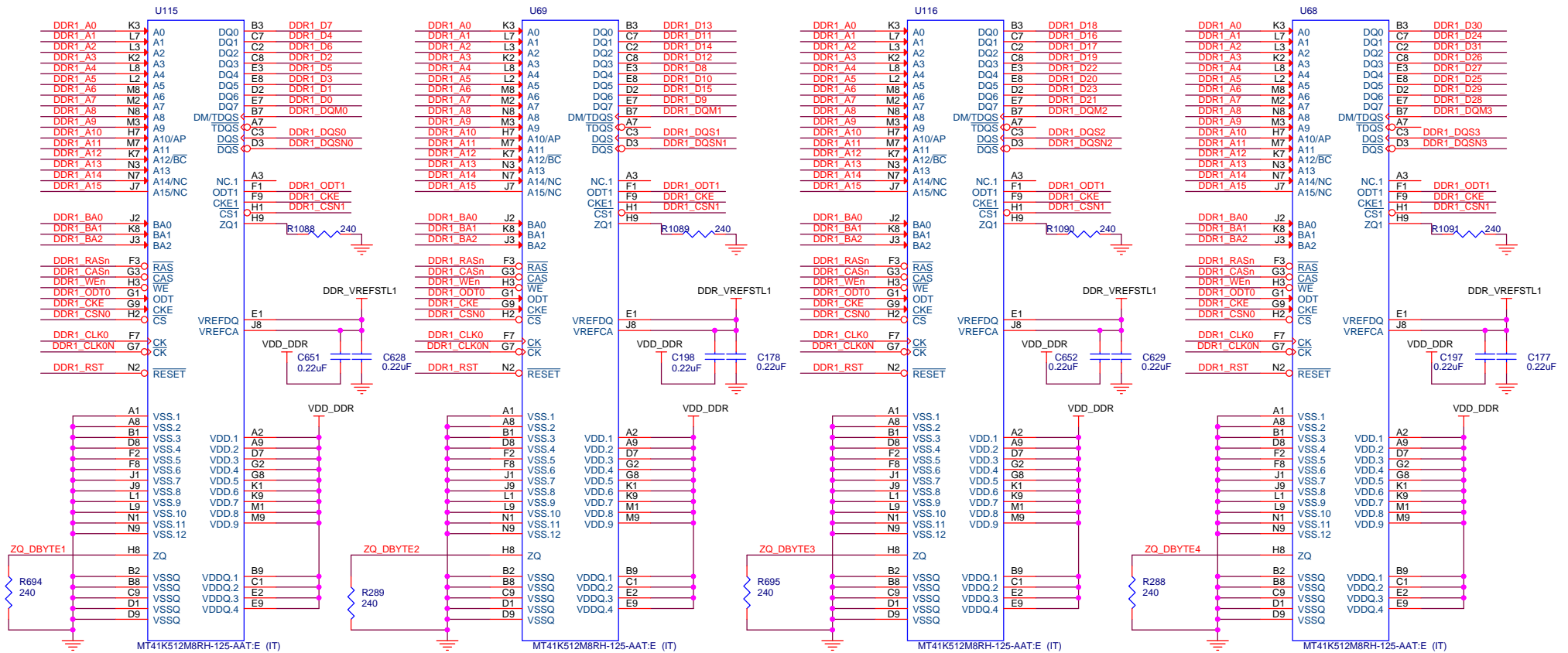


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Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: DDR3 EMIF1 TESTPOINTS			
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- | | | | | | | | |
|------------|-----------|----|-----------|------------|------------|----|------------|
| 8.23.25.27 | DDR1_A0 | >> | DDR1_A0 | 8.23.25.27 | DDR1_RASn | >> | DDR1_RASn |
| 8.23.25.27 | DDR1_A1 | >> | DDR1_A1 | 8.23.25.27 | DDR1_CASn | >> | DDR1_CASn |
| 8.23.25.27 | DDR1_A2 | >> | DDR1_A2 | 8.23.25.27 | DDR1_WEn | >> | DDR1_WEn |
| 8.23.25.27 | DDR1_A3 | >> | DDR1_A3 | 8.23.25.27 | DDR1_ODT0 | >> | DDR1_ODT0 |
| 8.23.25.27 | DDR1_A4 | >> | DDR1_A4 | | | | |
| 8.23.25.27 | DDR1_A5 | >> | DDR1_A5 | 8.23.25.27 | DDR1_CKE | >> | DDR1_CKE |
| 8.23.25.27 | DDR1_A6 | >> | DDR1_A6 | | | | |
| 8.23.25.27 | DDR1_A7 | >> | DDR1_A7 | 8.23.25.27 | DDR1_CSN0 | >> | DDR1_CSN0 |
| 8.23.25.27 | DDR1_A8 | >> | DDR1_A8 | | | | |
| 8.23.25.27 | DDR1_A9 | >> | DDR1_A9 | 8.23.25.27 | DDR1_CLK0 | >> | DDR1_CLK0 |
| 8.23.25.27 | DDR1_A10 | >> | DDR1_A10 | 8.23.25.27 | DDR1_CLKN0 | >> | DDR1_CLKN0 |
| 8.23.25.27 | DDR1_A11 | >> | DDR1_A11 | | | | |
| 8.23.25.27 | DDR1_A12 | >> | DDR1_A12 | | | | |
| 8.23.25.27 | DDR1_A13 | >> | DDR1_A13 | | | | |
| 8.23.25.27 | DDR1_A14 | >> | DDR1_A14 | | | | |
| 8.23.25.27 | DDR1_A15 | >> | DDR1_A15 | | | | |
| 8.23.25.27 | DDR1_BA0 | >> | DDR1_BA0 | | | | |
| 8.23.25.27 | DDR1_BA1 | >> | DDR1_BA1 | | | | |
| 8.23.25.27 | DDR1_BA2 | >> | DDR1_BA2 | | | | |
| 25.27 | DDR1_RST | >> | DDR1_RST | | | | |
| 8.23.25.27 | DDR1_ODT1 | >> | DDR1_ODT1 | | | | |
| 8.23.25.27 | DDR1_CSN1 | >> | DDR1_CSN1 | | | | |

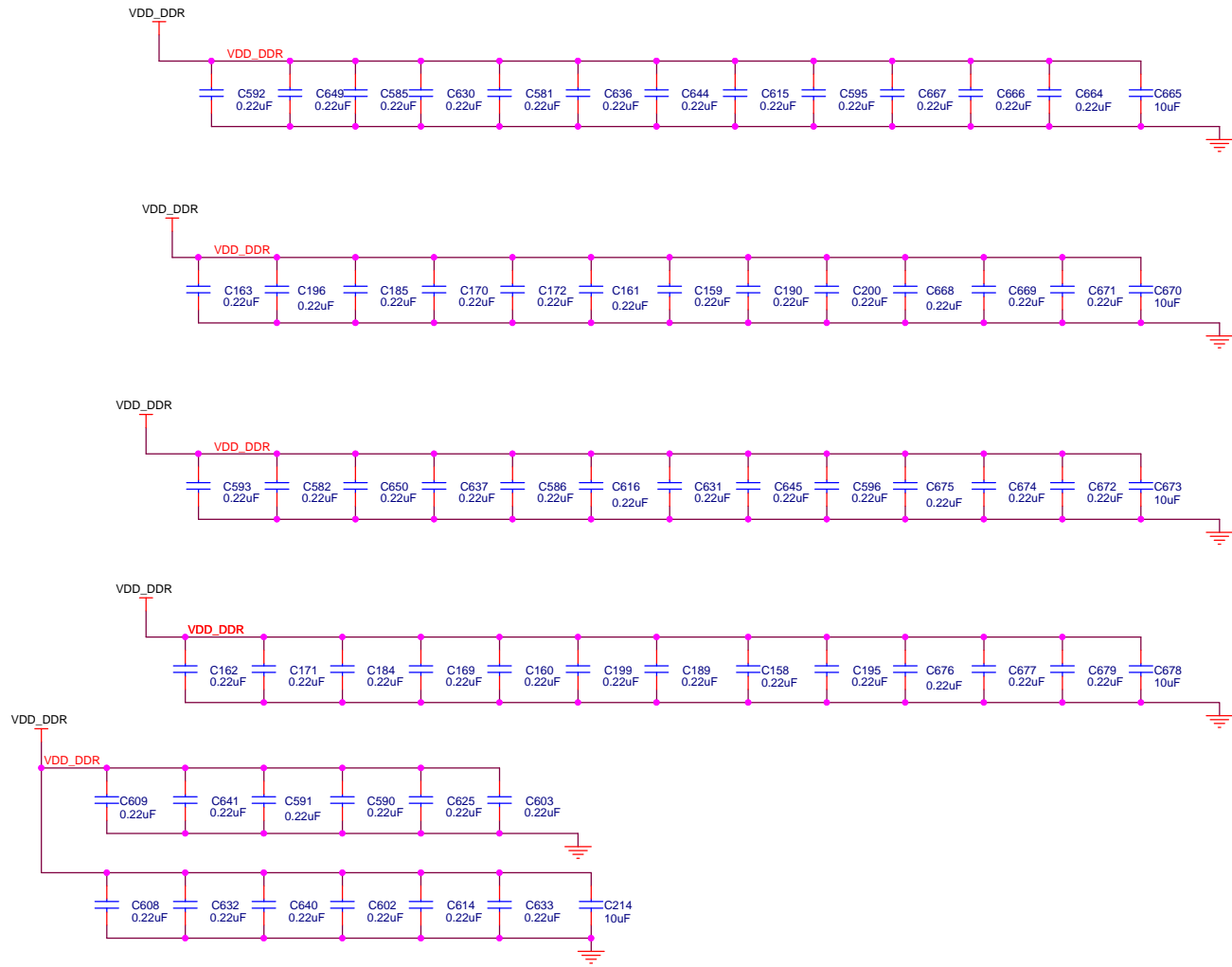
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Title: DRA72x/TA2A2Ex EVM CPU Board			
Page Contents: DDR3 BANK 1 ECC			
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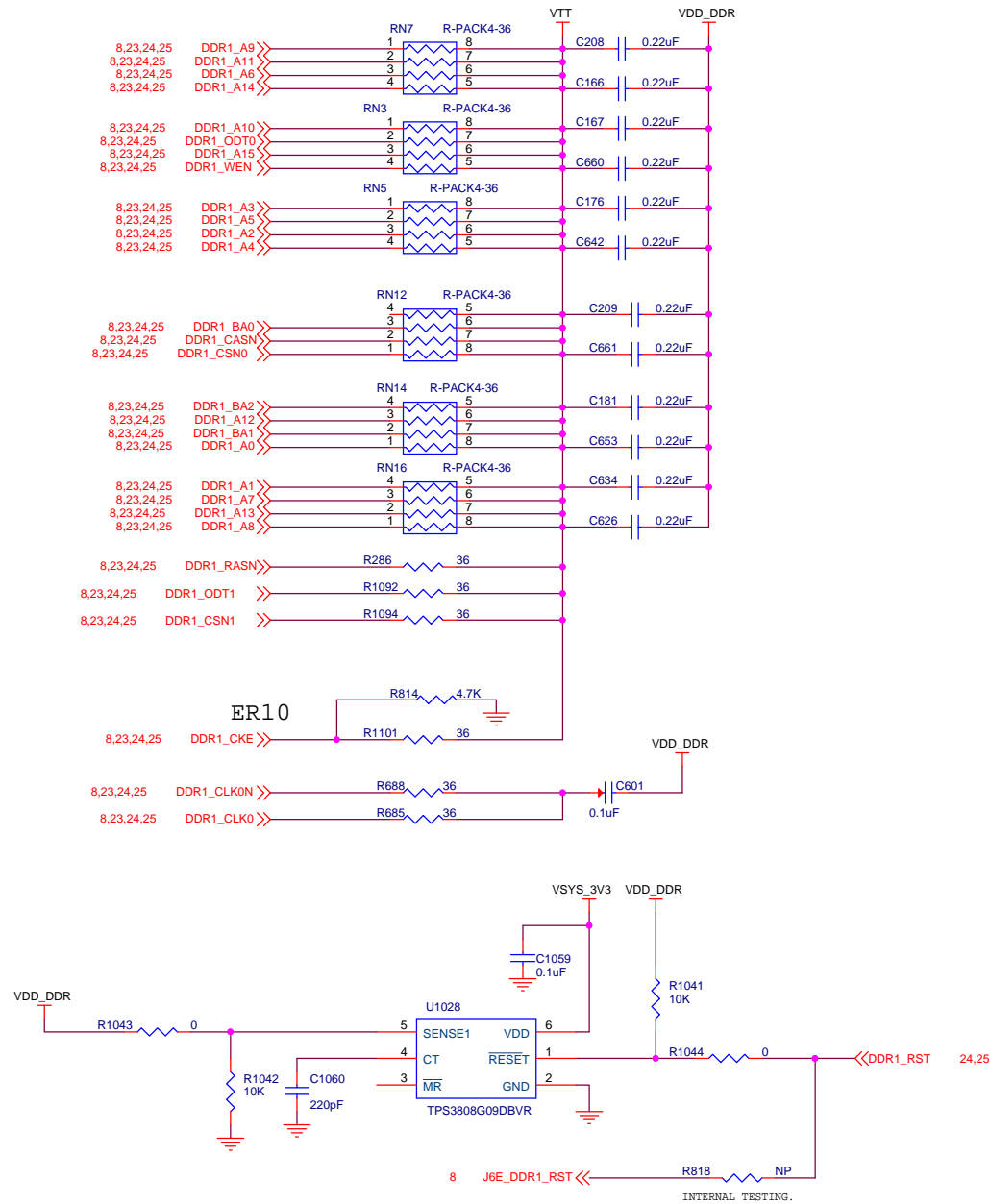
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8.23.24.27	DDR1_A1	DDR1_A1	8.23.24.27	DDR1_CASn	DDR1_WEn	8	DDR1_D1	DDR1_D1	8	DDR1_D17	DDR1_D17
8.23.24.27	DDR1_A2	DDR1_A2	8.23.24.27	DDR1_WEn	DDR1_ODT0	8	DDR1_D2	DDR1_D2	8	DDR1_D18	DDR1_D18
8.23.24.27	DDR1_A3	DDR1_A3	8.23.24.27	DDR1_ODT0		8	DDR1_D3	DDR1_D3	8	DDR1_D19	DDR1_D19
8.23.24.27	DDR1_A4	DDR1_A4		DDR1_CKE	DDR1_CKE	8	DDR1_D4	DDR1_D4	8	DDR1_D20	DDR1_D20
8.23.24.27	DDR1_A5	DDR1_A5	8.23.24.27	DDR1_CSN0	DDR1_CSN0	8	DDR1_D5	DDR1_D5	8	DDR1_D21	DDR1_D21
8.23.24.27	DDR1_A6	DDR1_A6				8	DDR1_D6	DDR1_D6	8	DDR1_D22	DDR1_D22
8.23.24.27	DDR1_A7	DDR1_A7	8.23.24.27	DDR1_CSN0	DDR1_CSN0	8	DDR1_D7	DDR1_D7	8	DDR1_D23	DDR1_D23
8.23.24.27	DDR1_A8	DDR1_A8				8	DDR1_D8	DDR1_D8	8	DDR1_D24	DDR1_D24
8.23.24.27	DDR1_A9	DDR1_A9	8.23.24.27	DDR1_CLK0	DDR1_CLK0	8	DDR1_D9	DDR1_D9	8	DDR1_D25	DDR1_D25
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8.23.24.27	DDR1_A11	DDR1_A11				8	DDR1_D11	DDR1_D11	8	DDR1_D27	DDR1_D27
8.23.24.27	DDR1_A12	DDR1_A12				8	DDR1_D12	DDR1_D12	8	DDR1_D28	DDR1_D28
8.23.24.27	DDR1_A13	DDR1_A13				8	DDR1_D13	DDR1_D13	8	DDR1_D29	DDR1_D29
8.23.24.27	DDR1_A14	DDR1_A14				8	DDR1_D14	DDR1_D14	8	DDR1_D30	DDR1_D30
8.23.24.27	DDR1_A15	DDR1_A15				8	DDR1_D15	DDR1_D15	8	DDR1_D31	DDR1_D31
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8.23.24.27	DDR1_BA2	DDR1_BA2	8.23.24.27			8	DDR1_DQS0n	DDR1_DQS0n	8	DDR1_DQS2n	DDR1_DQS2n
24.27	DDR1_RST	DDR1_RST				8	DDR1_DQM1	DDR1_DQM1	8	DDR1_DQM3	DDR1_DQM3
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ER13

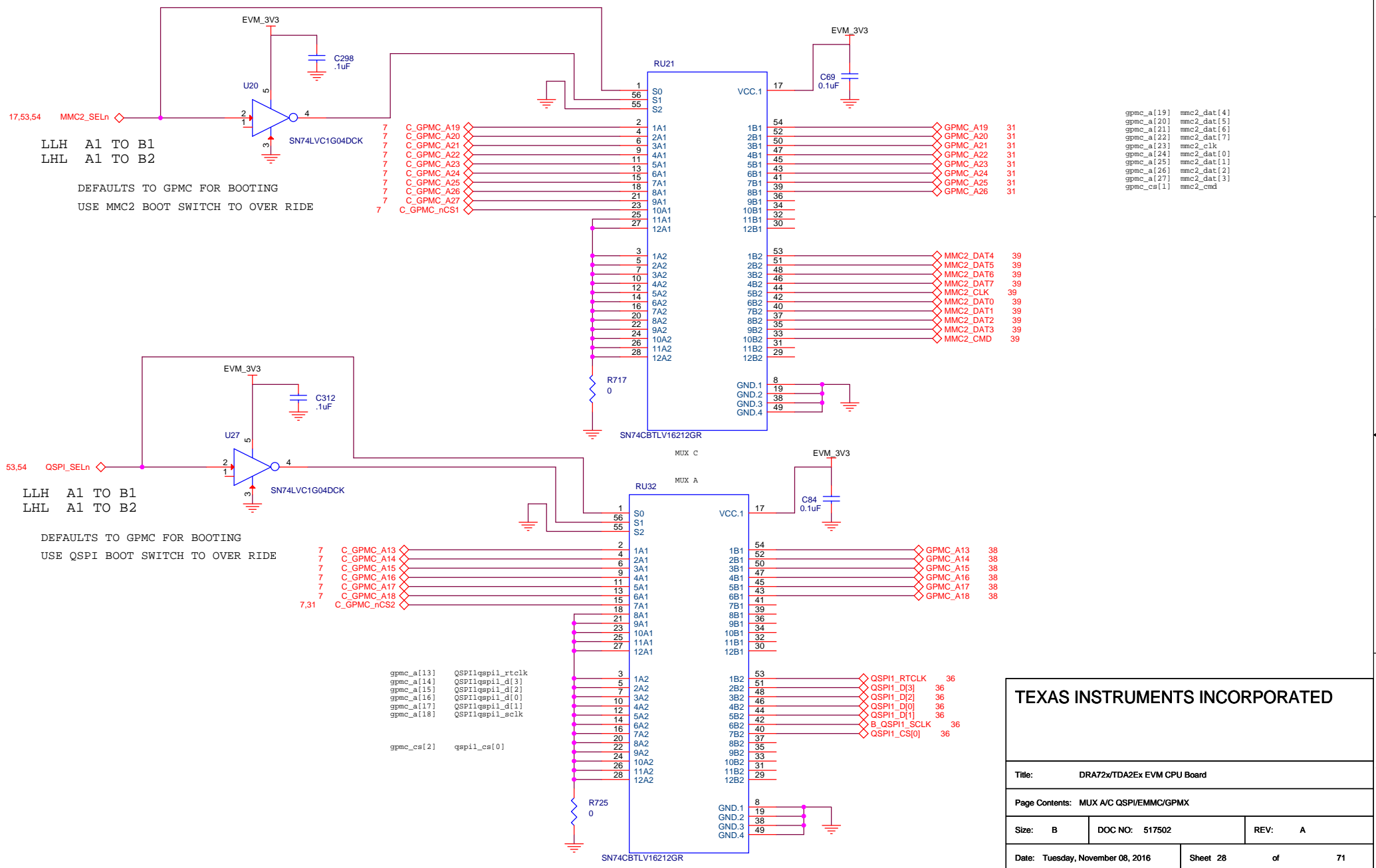
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Title: DRA72z/TA2AEx EVM CPU Board		
Page Contents: DDR3 MEMORY BANK 1		
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Page Contents: DDR3 MEMORY CAPS BANK 1			
Size: B	DOC NO: 517502	REV: A	
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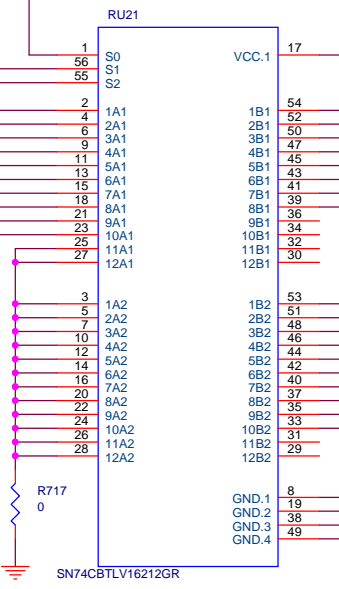
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Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: DDR TERMINATION BANK 1			
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LLH A1 TO B1
LHL A1 TO B2

DEFAULTS TO GPMC FOR BOOTING
USE MMC2 BOOT SWITCH TO OVER RIDE

- 7 C_GPMC_A19
- 7 C_GPMC_A20
- 7 C_GPMC_A21
- 7 C_GPMC_A22
- 7 C_GPMC_A23
- 7 C_GPMC_A24
- 7 C_GPMC_A25
- 7 C_GPMC_A26
- 7 C_GPMC_A27
- 7 C_GPMC_nCS1



- 1B1
- 2B1
- 3B1
- 4B1
- 5B1
- 6B1
- 7B1
- 8B1
- 9B1
- 10B1
- 11B1
- 12B1
- 1B2
- 2B2
- 3B2
- 4B2
- 5B2
- 6B2
- 7B2
- 8B2
- 9B2
- 10B2
- 11B2
- 12B2

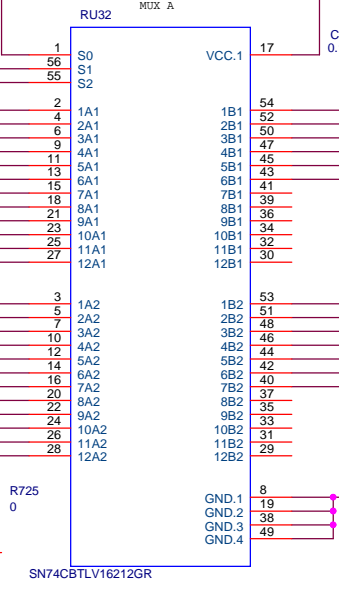
- gpmc_a[19] mmc2_dat[4]
- gpmc_a[20] mmc2_dat[5]
- gpmc_a[21] mmc2_dat[6]
- gpmc_a[22] mmc2_dat[7]
- gpmc_a[23] mmc2_clk
- gpmc_a[24] mmc2_dat[0]
- gpmc_a[25] mmc2_dat[1]
- gpmc_a[26] mmc2_dat[2]
- gpmc_a[27] mmc2_dat[3]
- gpmc_cs[1] mmc2_cmd

- MMC2_DAT4
- MMC2_DAT5
- MMC2_DAT6
- MMC2_DAT7
- MMC2_CLK
- MMC2_DAT0
- MMC2_DAT1
- MMC2_DAT2
- MMC2_DAT3
- MMC2_CMD

LLH A1 TO B1
LHL A1 TO B2

DEFAULTS TO GPMC FOR BOOTING
USE QSPI BOOT SWITCH TO OVER RIDE

- 7 C_GPMC_A13
- 7 C_GPMC_A14
- 7 C_GPMC_A15
- 7 C_GPMC_A16
- 7 C_GPMC_A17
- 7 C_GPMC_A18
- 7 C_GPMC_nCS2



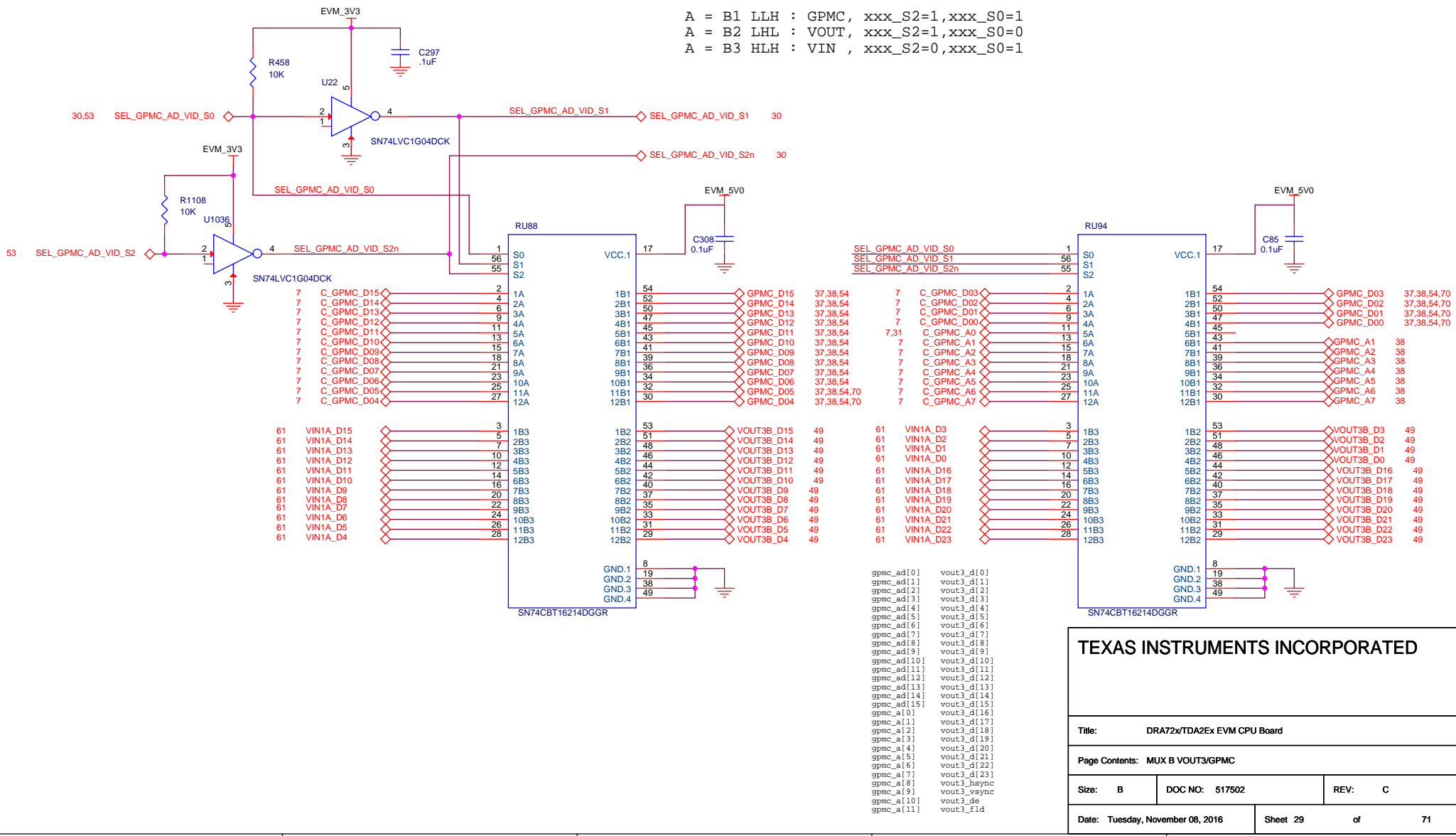
- 1B1
- 2B1
- 3B1
- 4B1
- 5B1
- 6B1
- 7B1
- 8B1
- 9B1
- 10B1
- 11B1
- 12B1
- 1B2
- 2B2
- 3B2
- 4B2
- 5B2
- 6B2
- 7B2
- 8B2
- 9B2
- 10B2
- 11B2
- 12B2

TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: MUX A/C QSPI/EMMC/GPMC			
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DEFAULTS TO GPMC FOR BOOTING

A = B1 LLH : GPMC , xxx_S2=1,xxx_S0=1
 A = B2 LHL : VOUT , xxx_S2=1,xxx_S0=0
 A = B3 HLH : VIN , xxx_S2=0,xxx_S0=1



TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board

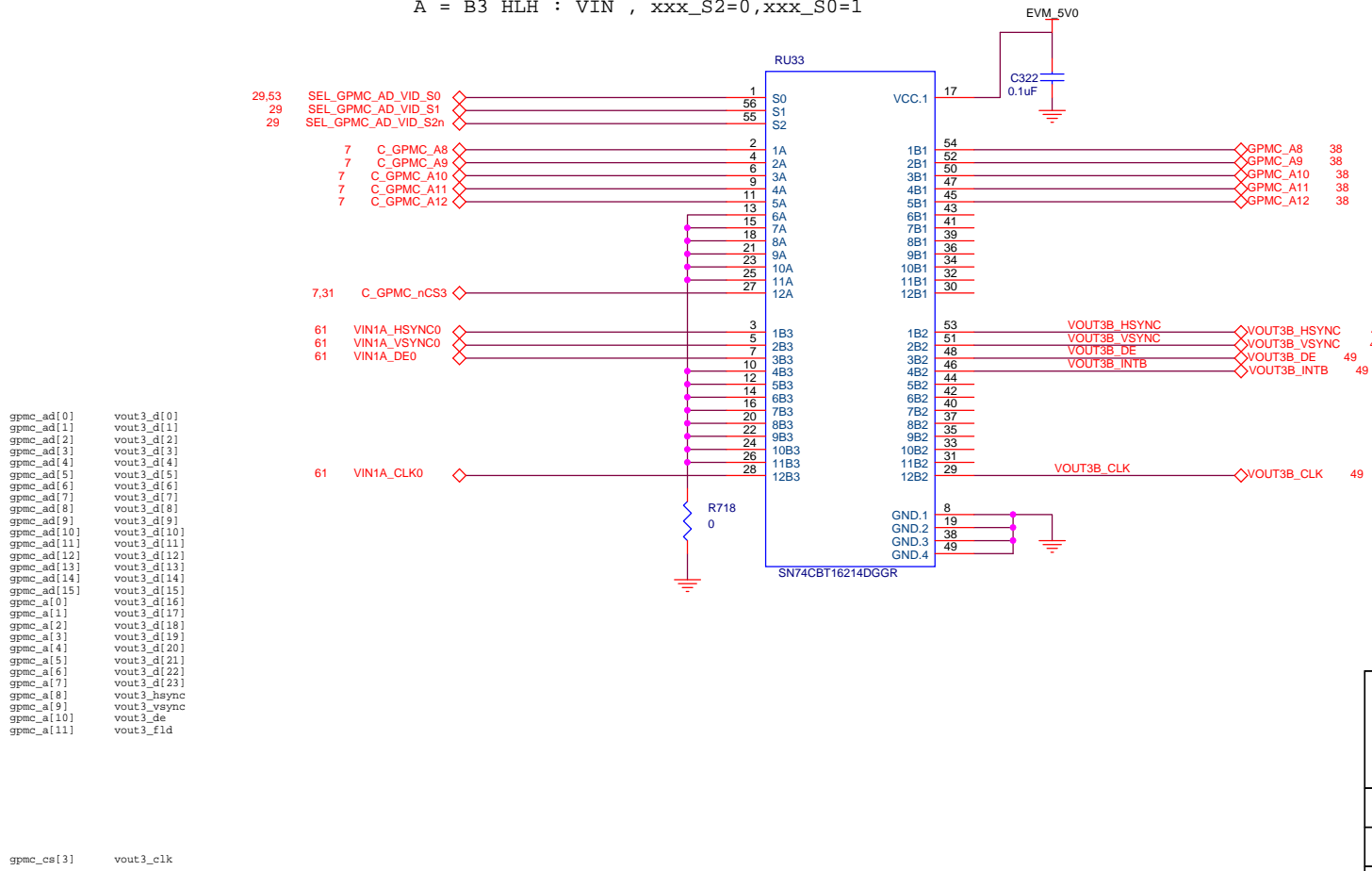
Page Contents: MUX B VOUT3/GPMC

Size: B DOC NO: 517502 REV: C

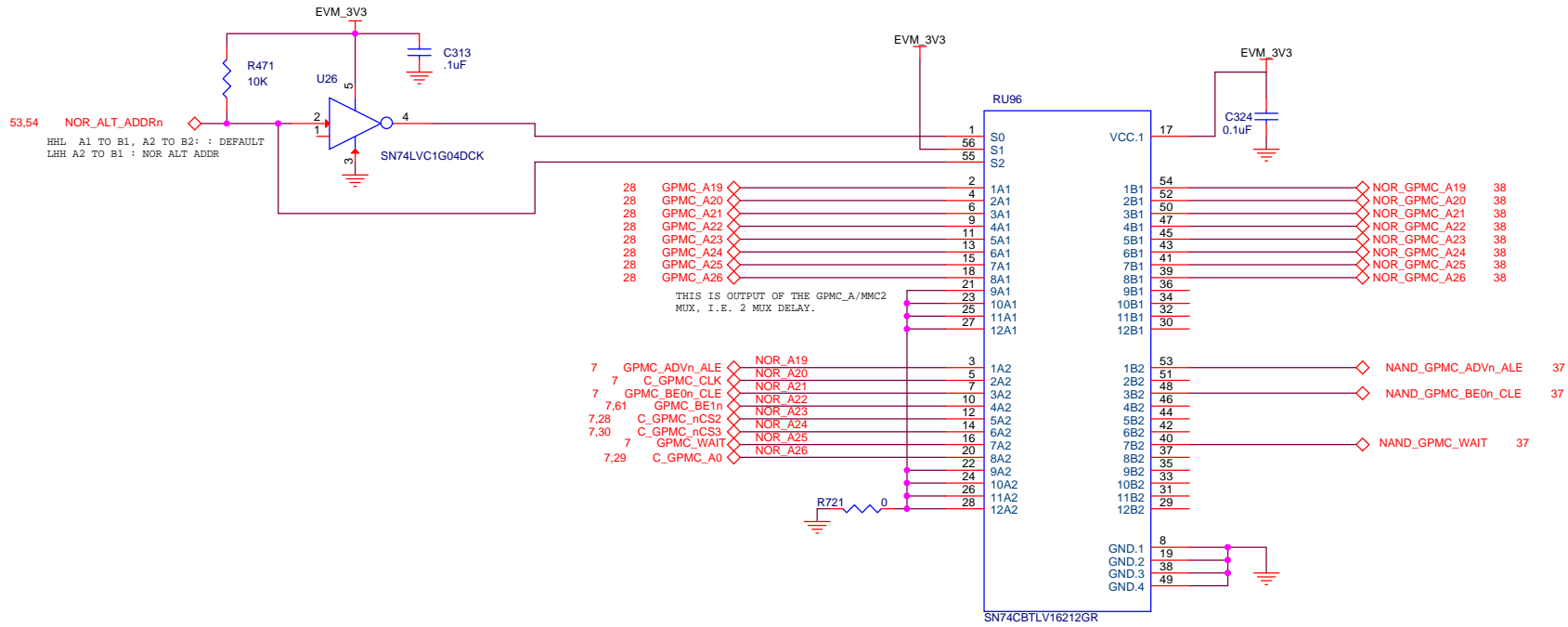
Date: Tuesday, November 08, 2016 Sheet 29 of 71

DEFAULTS TO GPMC FOR BOOTING

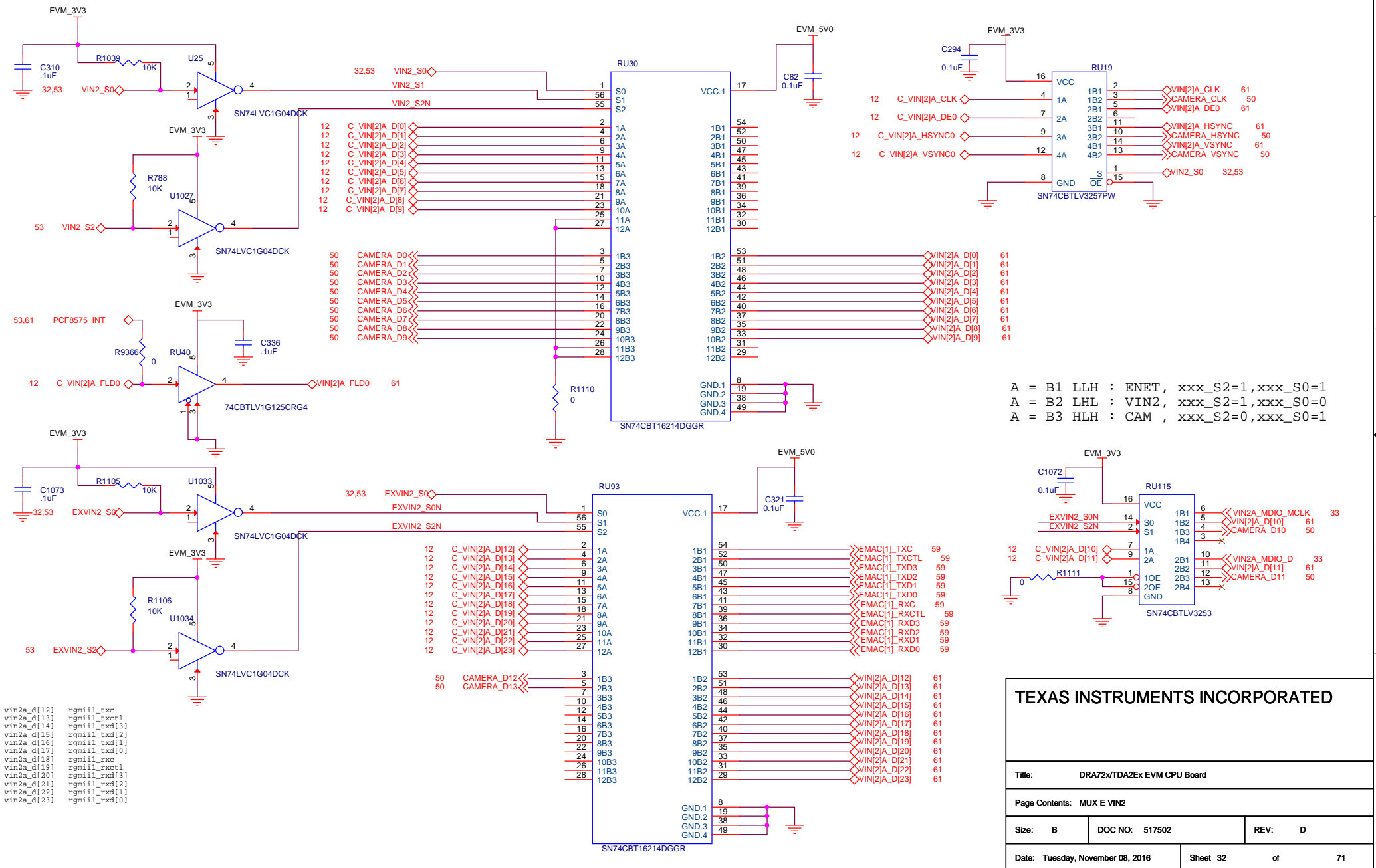
A = B1 LLH : GPMC, xxx_S2=1,xxx_S0=1
 A = B2 LHL : VOUT, xxx_S2=1,xxx_S0=0
 A = B3 HLH : VIN , xxx_S2=0,xxx_S0=1



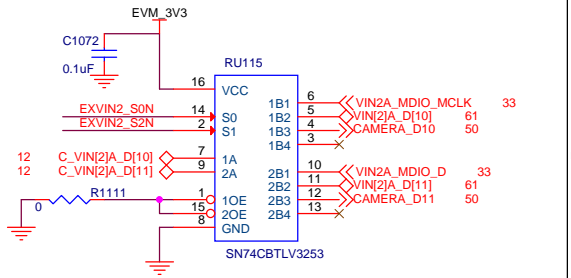
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: MUX B VOUT3/GPMC ADD			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 30	of	71



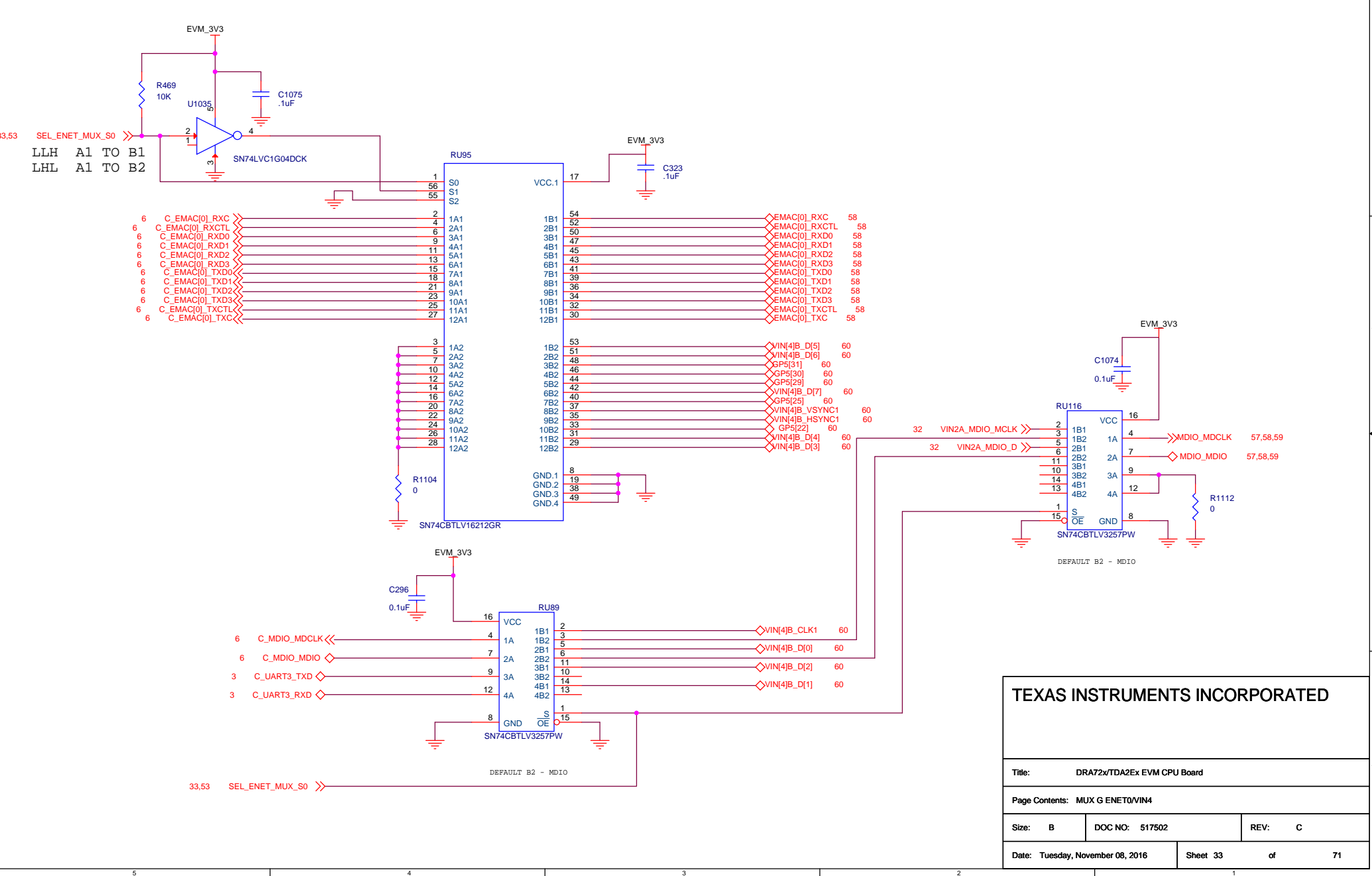
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: MUX D GMPCA			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 31	of	71



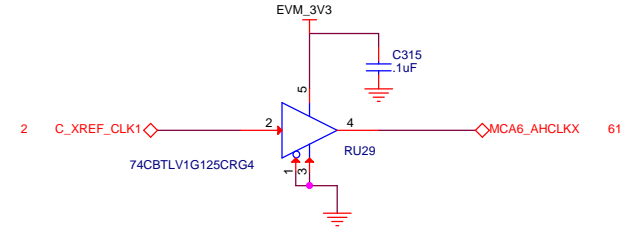
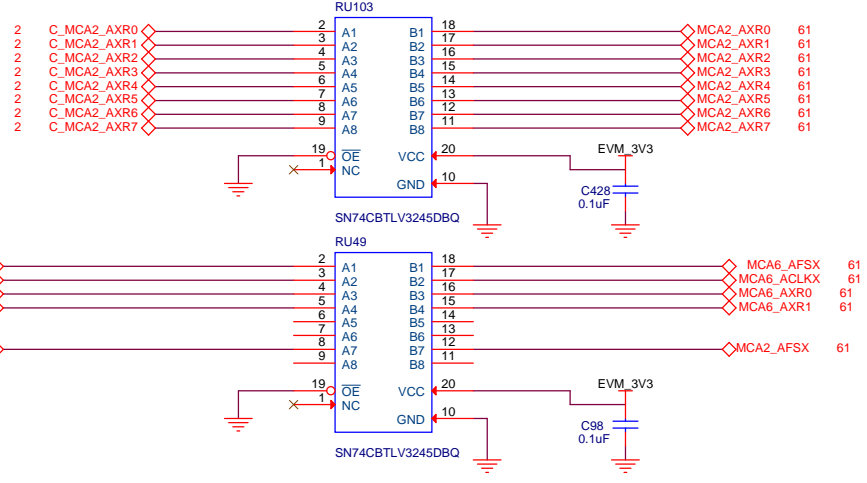
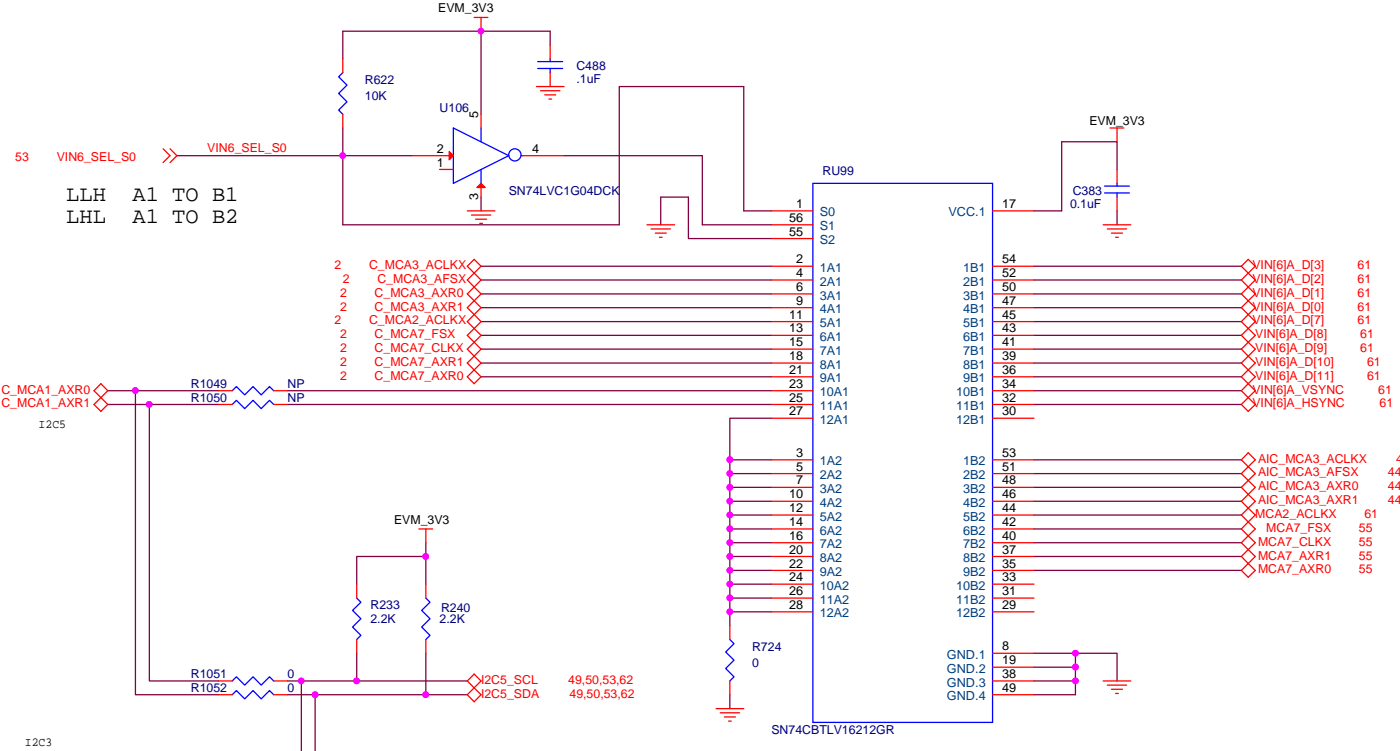
A = B1 LLH : ENET, xxx_S2=1,xxx_S0=1
 A = B2 LHL : VIN2, xxx_S2=1,xxx_S0=0
 A = B3 HLH : CAM , xxx_S2=0,xxx_S0=1



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: MUX E VIN2			
Size: B	DOC NO: 517502	REV: D	
Date: Tuesday, November 08, 2016	Sheet 32	of	71



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: MUX G ENET0/VIN4			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 33	of	71



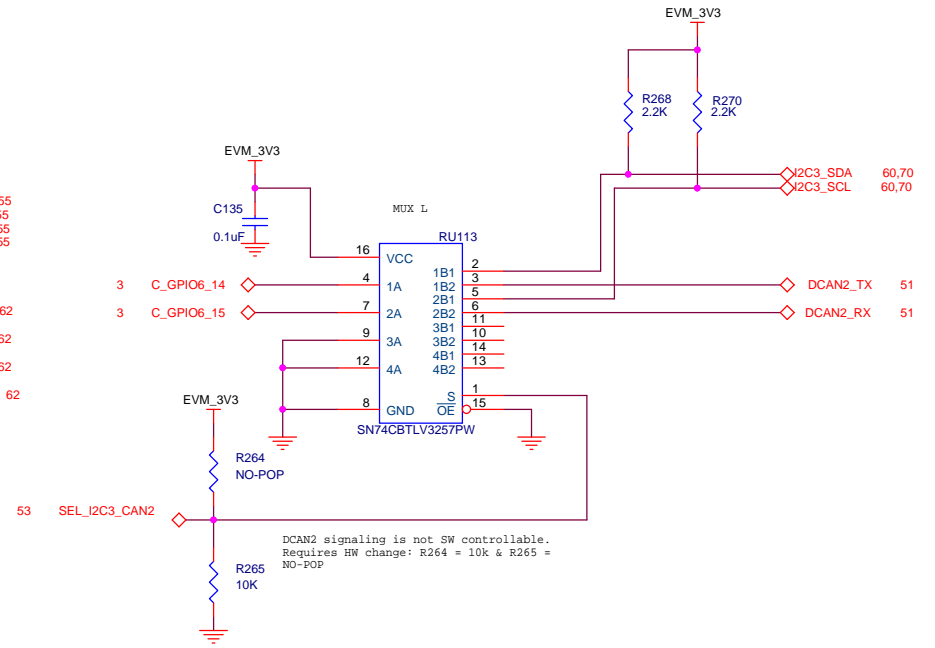
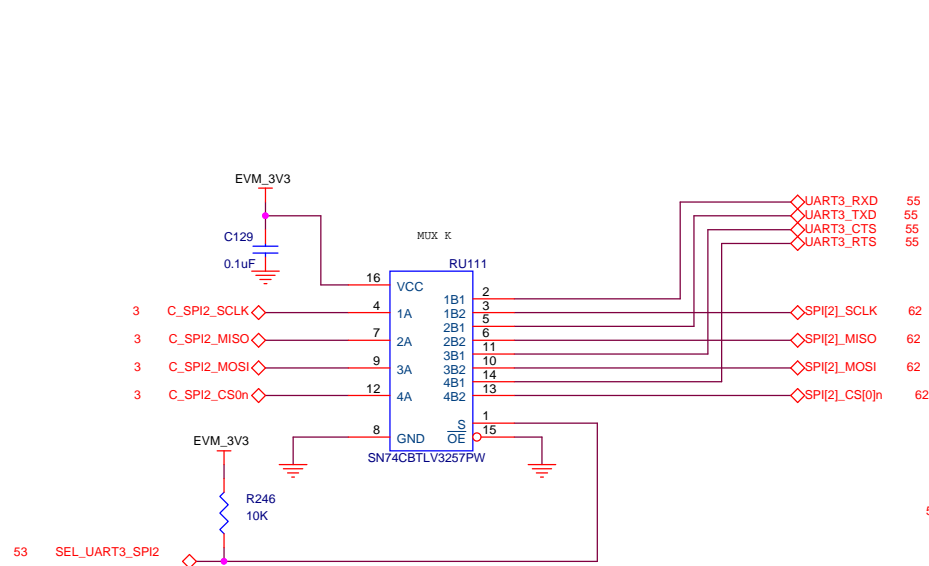
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2AEx EVM CPU Board

Page Contents: MUX H MCASP/VIN6A

Size: B	DOC NO: 517502	REV: A
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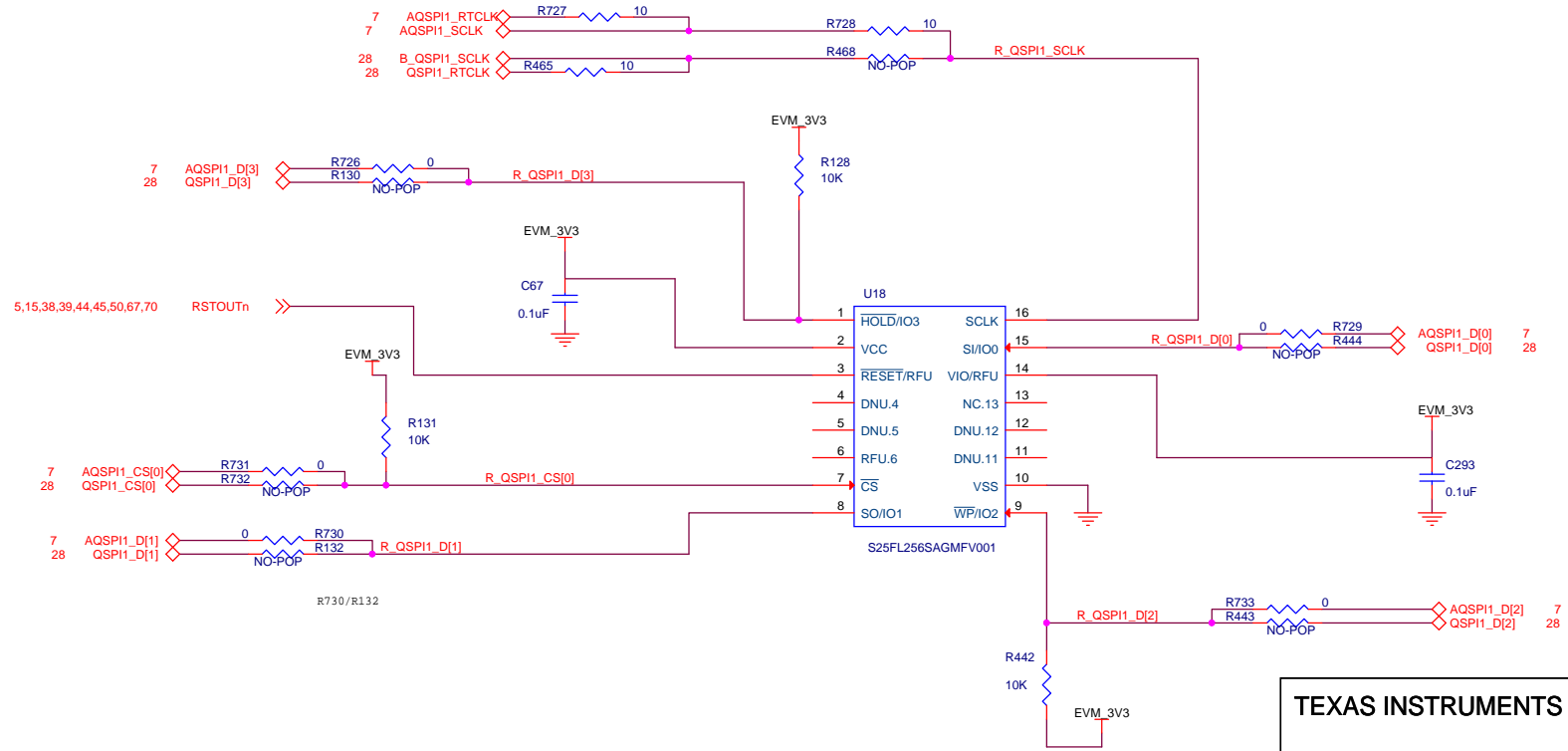
Date: Tuesday, November 08, 2016	Sheet 34 of 71
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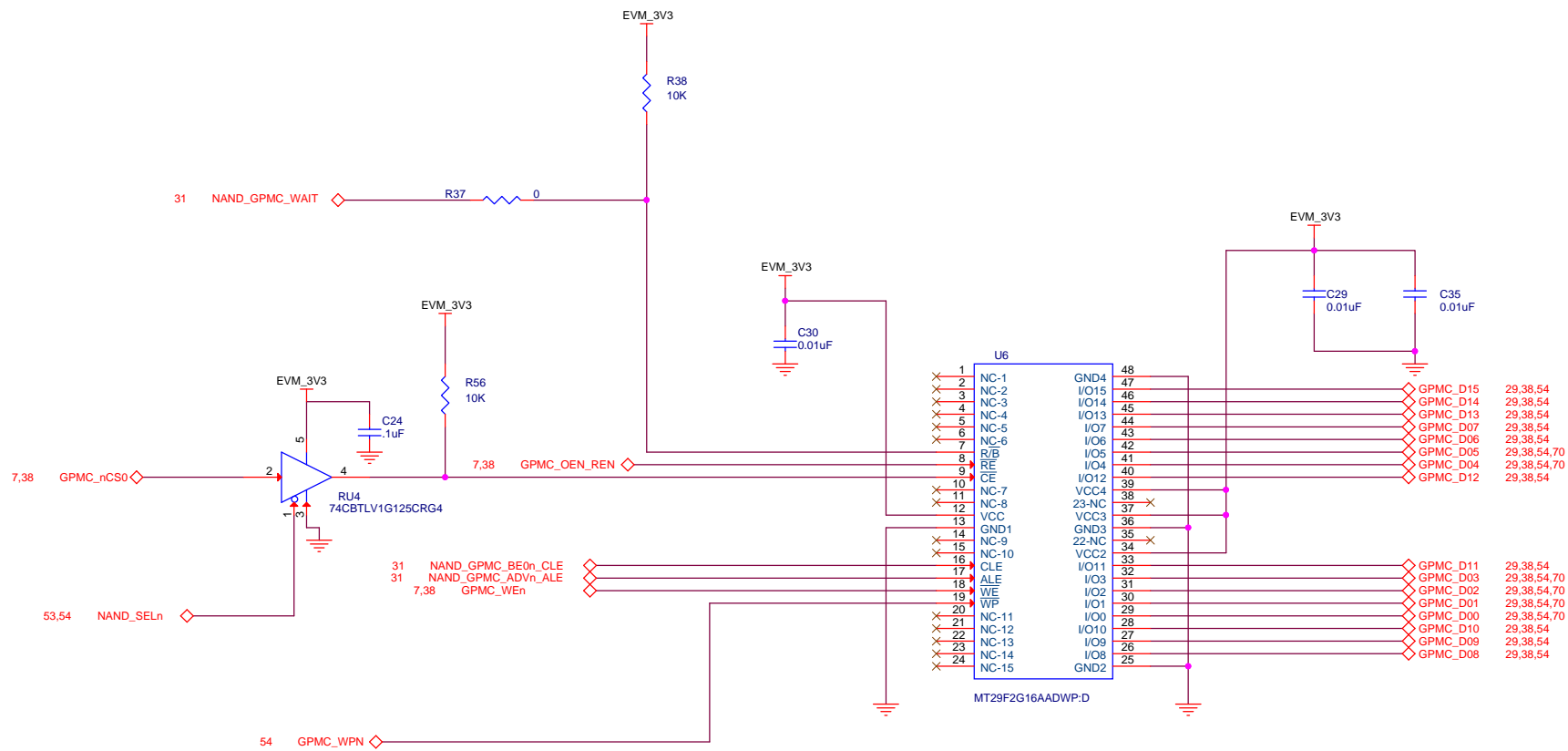
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: MUX J/K/L SERIAL I/O			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 35	of	71

ROUTE THE FOLLOWING SIGNALS AS A GROUP
 WITH A NET LENGTH LESS THEN 2.75
 INCHES AND 60ps OF SKEW. PLACE THE
 DUAL RESISTOR CLOSE TOGETHER NEAR THE
 PIN OF THE FLASH.

AQSP11_SCLK
 AQSP11_RTCLK
 AQSP11_CS[0]
 AQSP11_D[0]
 AQSP11_D[1]
 AQSP11_D[2]
 AQSP11_D[3]



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2A2Ex EVM CPU Board			
Page Contents: MEM SPI FLASH			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 36	of	71



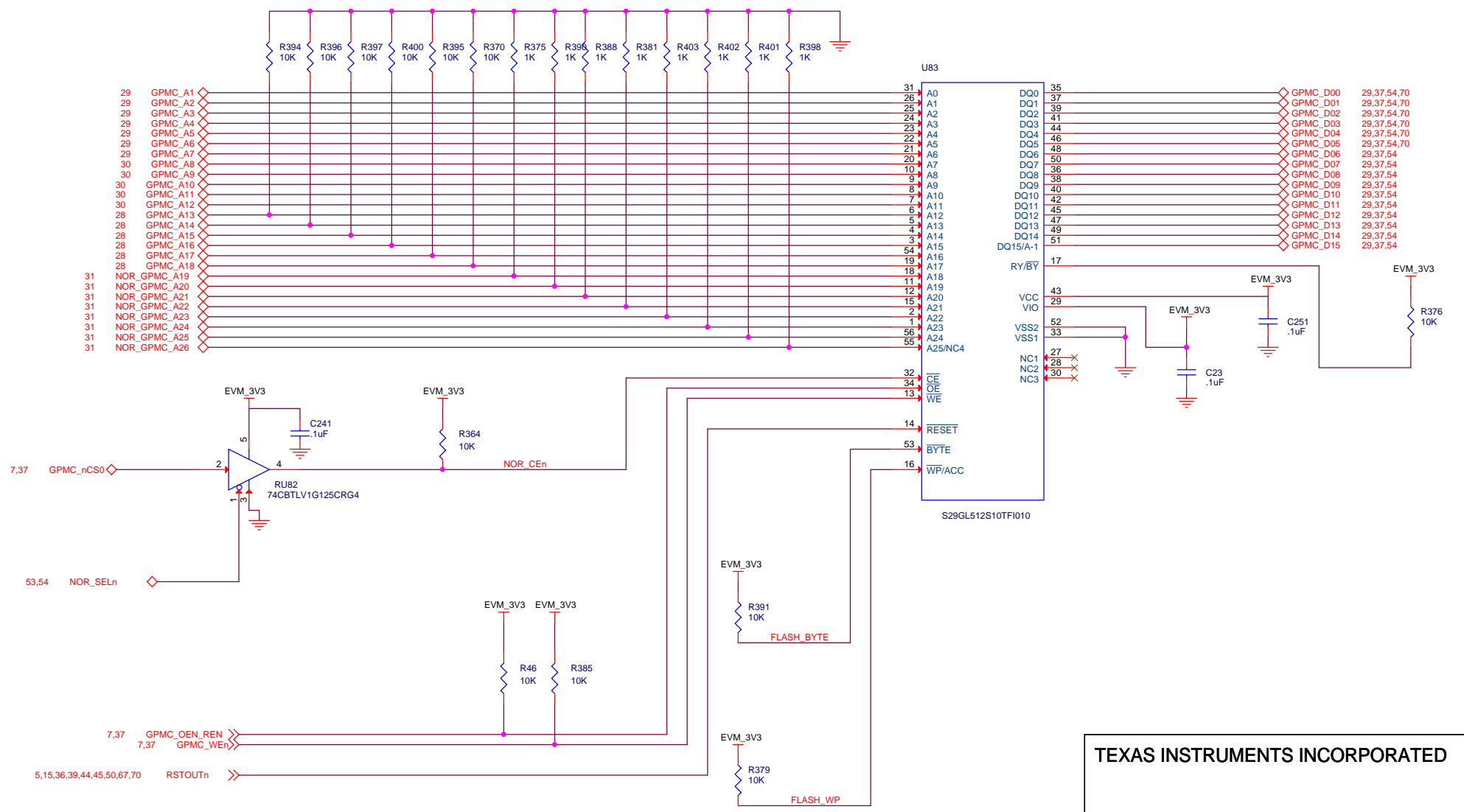
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TDA2Ex EVM CPU Board

Page Contents: MEM NAND FLASH

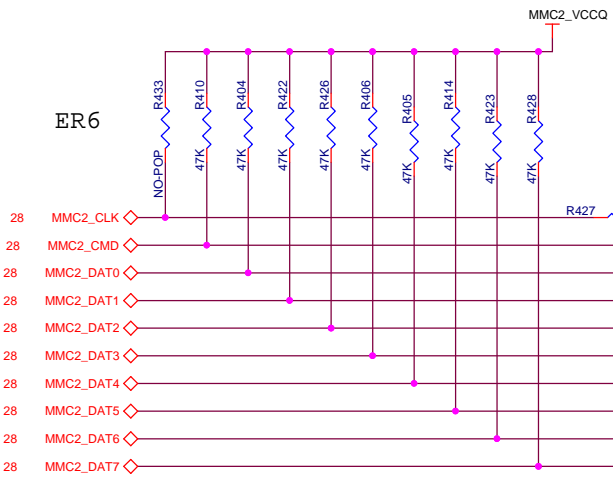
Size: B	DOC NO: 517502	REV: A
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Date: Tuesday, November 08, 2016	Sheet 37	of 71
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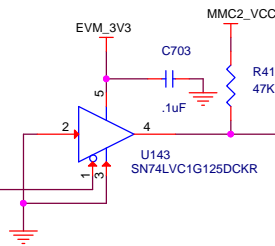
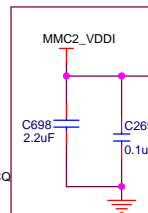


TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: MEM NOR FLASH			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 38	of	71

ER6



- 28 MMC2_CLK
- 28 MMC2_CMD
- 28 MMC2_DAT0
- 28 MMC2_DAT1
- 28 MMC2_DAT2
- 28 MMC2_DAT3
- 28 MMC2_DAT4
- 28 MMC2_DAT5
- 28 MMC2_DAT6
- 28 MMC2_DAT7

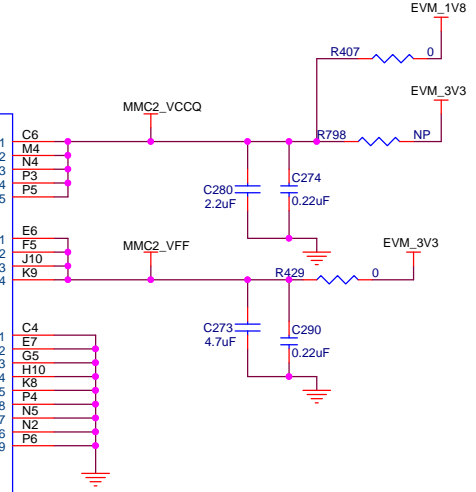


5,15,36,38,44,45,50,67,70

M1	NC.M1	M14	NC.M14
M2	NC.M2	M13	NC.M13
M3	NC.M3	M12	NC.M12
M4	NC.M4	M11	NC.M11
M5	NC.M5	M10	NC.M10
M6	NC.M6	M9	NC.M9
M7	NC.M7	M8	NC.M8
M8	NC.M8	M7	NC.M7
M9	NC.M9	M6	NC.M6
M10	NC.M10	M5	NC.M5
M11	NC.M11	M4	NC.M4
M12	NC.M12	M3	NC.M3
M13	NC.M13	M2	NC.M2
M14	NC.M14	M1	NC.M1
L1	NC.L1	J14	NC.J14
L2	NC.L2	J13	NC.J13
L3	NC.L3	J12	NC.J12
L4	NC.L4	J11	NC.J11
L5	NC.L5	J10	NC.J10
L6	NC.L6	J9	NC.J9
L7	NC.L7	J8	NC.J8
L8	NC.L8	J7	NC.J7
L9	NC.L9	J6	NC.J6
L10	NC.L10	J5	NC.J5
L11	NC.L11	J4	NC.J4
L12	NC.L12	J3	NC.J3
L13	NC.L13	J2	NC.J2
L14	NC.L14	J1	NC.J1
K1	NC.K1	J14	NC.J14
K2	NC.K2	J13	NC.J13
K3	NC.K3	J12	NC.J12
K4	NC.K4	J11	NC.J11
K5	NC.K5	J10	NC.J10
K6	NC.K6	J9	NC.J9
K7	NC.K7	J8	NC.J8
K8	NC.K8	J7	NC.J7
K9	NC.K9	J6	NC.J6
K10	NC.K10	J5	NC.J5
K11	NC.K11	J4	NC.J4
K12	NC.K12	J3	NC.J3
K13	NC.K13	J2	NC.J2
K14	NC.K14	J1	NC.J1
I1	NC.I1	J14	NC.J14
I2	NC.I2	J13	NC.J13
I3	NC.I3	J12	NC.J12
I4	NC.I4	J11	NC.J11
I5	NC.I5	J10	NC.J10
I6	NC.I6	J9	NC.J9
I7	NC.I7	J8	NC.J8
I8	NC.I8	J7	NC.J7
I9	NC.I9	J6	NC.J6
I10	NC.I10	J5	NC.J5
I11	NC.I11	J4	NC.J4
I12	NC.I12	J3	NC.J3
I13	NC.I13	J2	NC.J2
I14	NC.I14	J1	NC.J1
H1	NC.H1	J14	NC.J14
H2	NC.H2	J13	NC.J13
H3	NC.H3	J12	NC.J12
H4	NC.H4	J11	NC.J11
H5	NC.H5	J10	NC.J10
H6	NC.H6	J9	NC.J9
H7	NC.H7	J8	NC.J8
H8	NC.H8	J7	NC.J7
H9	NC.H9	J6	NC.J6
H10	NC.H10	J5	NC.J5
H11	NC.H11	J4	NC.J4
H12	NC.H12	J3	NC.J3
H13	NC.H13	J2	NC.J2
H14	NC.H14	J1	NC.J1
G1	NC.G1	J14	NC.J14
G2	NC.G2	J13	NC.J13
G3	NC.G3	J12	NC.J12
G4	NC.G4	J11	NC.J11
G5	NC.G5	J10	NC.J10
G6	NC.G6	J9	NC.J9
G7	NC.G7	J8	NC.J8
G8	NC.G8	J7	NC.J7
G9	NC.G9	J6	NC.J6
G10	NC.G10	J5	NC.J5
G11	NC.G11	J4	NC.J4
G12	NC.G12	J3	NC.J3
G13	NC.G13	J2	NC.J2
G14	NC.G14	J1	NC.J1
F1	NC.F1	J14	NC.J14
F2	NC.F2	J13	NC.J13
F3	NC.F3	J12	NC.J12
F4	NC.F4	J11	NC.J11
F5	NC.F5	J10	NC.J10
F6	NC.F6	J9	NC.J9
F7	NC.F7	J8	NC.J8
F8	NC.F8	J7	NC.J7
F9	NC.F9	J6	NC.J6
F10	NC.F10	J5	NC.J5
F11	NC.F11	J4	NC.J4
F12	NC.F12	J3	NC.J3
F13	NC.F13	J2	NC.J2
F14	NC.F14	J1	NC.J1
E1	NC.E1	J14	NC.J14
E2	NC.E2	J13	NC.J13
E3	NC.E3	J12	NC.J12
E4	NC.E4	J11	NC.J11
E5	NC.E5	J10	NC.J10
E6	NC.E6	J9	NC.J9
E7	NC.E7	J8	NC.J8
E8	NC.E8	J7	NC.J7
E9	NC.E9	J6	NC.J6
E10	NC.E10	J5	NC.J5
E11	NC.E11	J4	NC.J4
E12	NC.E12	J3	NC.J3
E13	NC.E13	J2	NC.J2
E14	NC.E14	J1	NC.J1
D1	NC.D1	J14	NC.J14
D2	NC.D2	J13	NC.J13
D3	NC.D3	J12	NC.J12
D4	NC.D4	J11	NC.J11
D5	NC.D5	J10	NC.J10
D6	NC.D6	J9	NC.J9
D7	NC.D7	J8	NC.J8
D8	NC.D8	J7	NC.J7
D9	NC.D9	J6	NC.J6
D10	NC.D10	J5	NC.J5
D11	NC.D11	J4	NC.J4
D12	NC.D12	J3	NC.J3
D13	NC.D13	J2	NC.J2
D14	NC.D14	J1	NC.J1
C1	NC.C1	J14	NC.J14
C2	NC.C2	J13	NC.J13
C3	NC.C3	J12	NC.J12
C4	NC.C4	J11	NC.J11
C5	NC.C5	J10	NC.J10
C6	NC.C6	J9	NC.J9
C7	NC.C7	J8	NC.J8
C8	NC.C8	J7	NC.J7
C9	NC.C9	J6	NC.J6
C10	NC.C10	J5	NC.J5
C11	NC.C11	J4	NC.J4
C12	NC.C12	J3	NC.J3
C13	NC.C13	J2	NC.J2
C14	NC.C14	J1	NC.J1
B1	NC.B1	J14	NC.J14
B2	NC.B2	J13	NC.J13
B3	NC.B3	J12	NC.J12
B4	NC.B4	J11	NC.J11
B5	NC.B5	J10	NC.J10
B6	NC.B6	J9	NC.J9
B7	NC.B7	J8	NC.J8
B8	NC.B8	J7	NC.J7
B9	NC.B9	J6	NC.J6
B10	NC.B10	J5	NC.J5
B11	NC.B11	J4	NC.J4
B12	NC.B12	J3	NC.J3
B13	NC.B13	J2	NC.J2
B14	NC.B14	J1	NC.J1
A1	NC.A1	J14	NC.J14
A2	NC.A2	J13	NC.J13
A3	NC.A3	J12	NC.J12
A4	NC.A4	J11	NC.J11
A5	NC.A5	J10	NC.J10
A6	NC.A6	J9	NC.J9
A7	NC.A7	J8	NC.J8
A8	NC.A8	J7	NC.J7
A9	NC.A9	J6	NC.J6
A10	NC.A10	J5	NC.J5
A11	NC.A11	J4	NC.J4
A12	NC.A12	J3	NC.J3
A13	NC.A13	J2	NC.J2
A14	NC.A14	J1	NC.J1
VDD.1	VDD.1	VDD.1	VDD.1
VDD.2	VDD.2	VDD.2	VDD.2
VDD.3	VDD.3	VDD.3	VDD.3
VDD.4	VDD.4	VDD.4	VDD.4
VDD.5	VDD.5	VDD.5	VDD.5
VFF.1	VFF.1	VFF.1	VFF.1
VFF.2	VFF.2	VFF.2	VFF.2
VFF.3	VFF.3	VFF.3	VFF.3
VFF.4	VFF.4	VFF.4	VFF.4
VSS.1	VSS.1	VSS.1	VSS.1
VSS.2	VSS.2	VSS.2	VSS.2
VSS.3	VSS.3	VSS.3	VSS.3
VSS.4	VSS.4	VSS.4	VSS.4
VSS.5	VSS.5	VSS.5	VSS.5
VSS.6	VSS.6	VSS.6	VSS.6
VSS.7	VSS.7	VSS.7	VSS.7
VSS.8	VSS.8	VSS.8	VSS.8
VSS.9	VSS.9	VSS.9	VSS.9

169 WFBGA EXTENDED MOUNTING PADS

DUAL FOOTPRINT 153/169 USES 153 PIN NUMBERS FOR COMPATIBLE PINS.

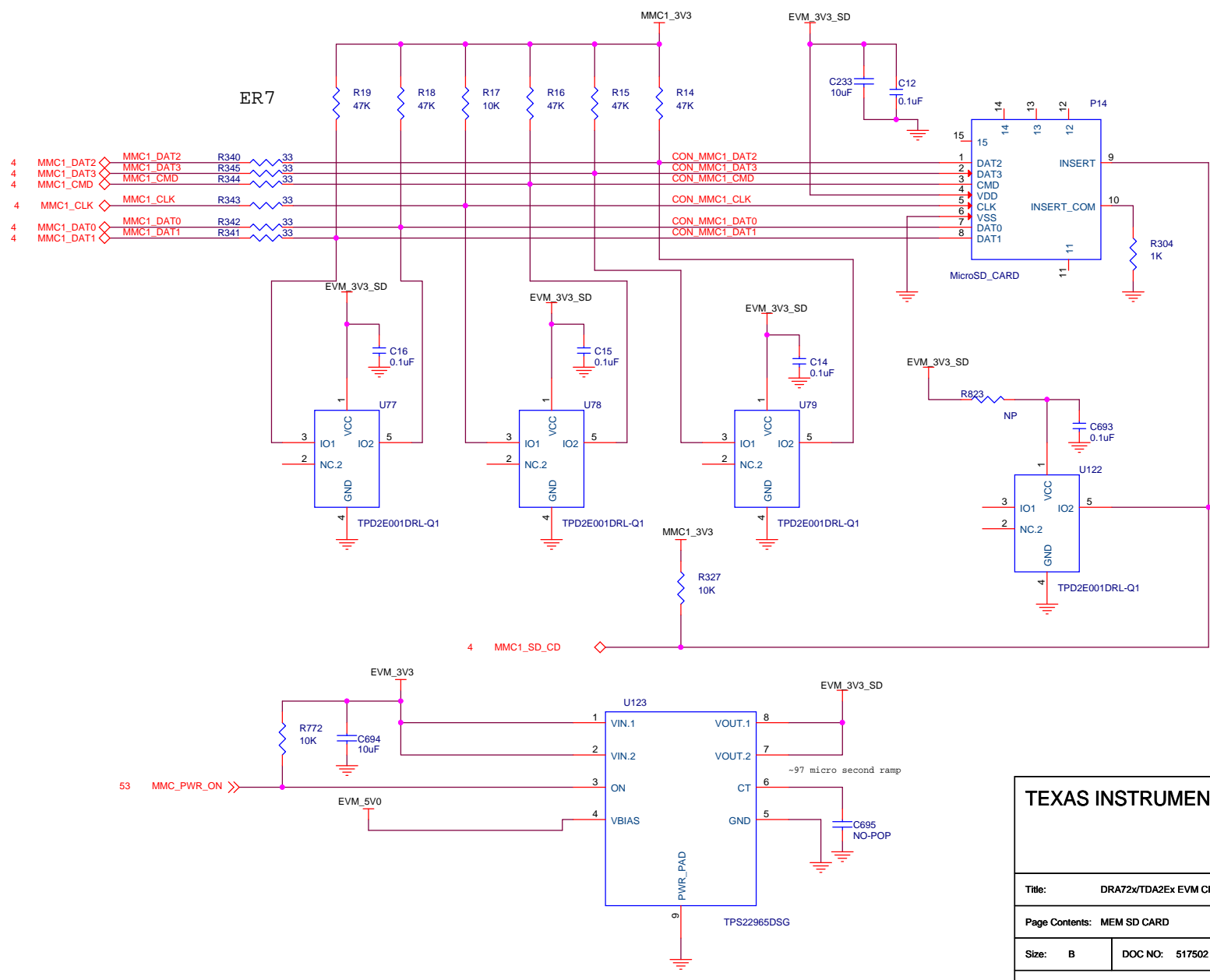


TEXAS INSTRUMENTS INCORPORATED

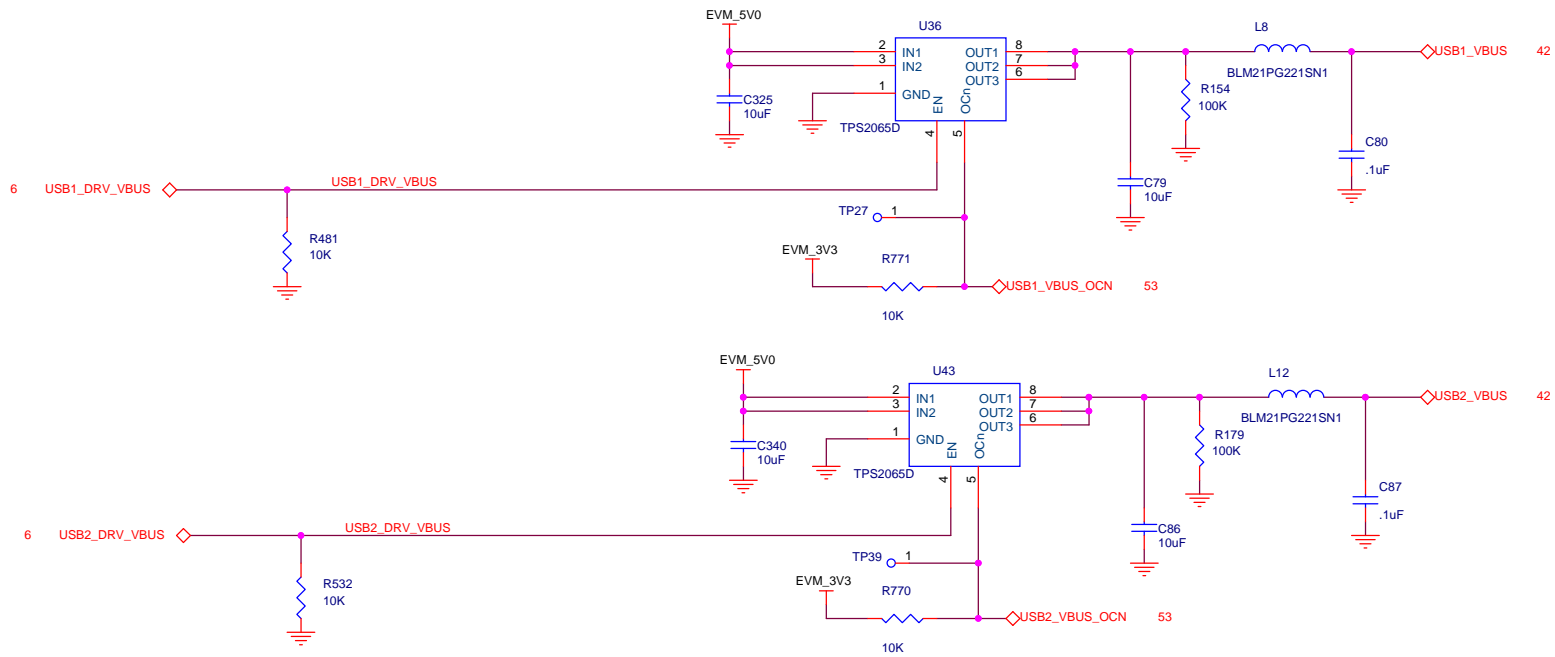
Title: DRA72x/TA2Ex EVM CPU Board

Page Contents: MEM eMMC

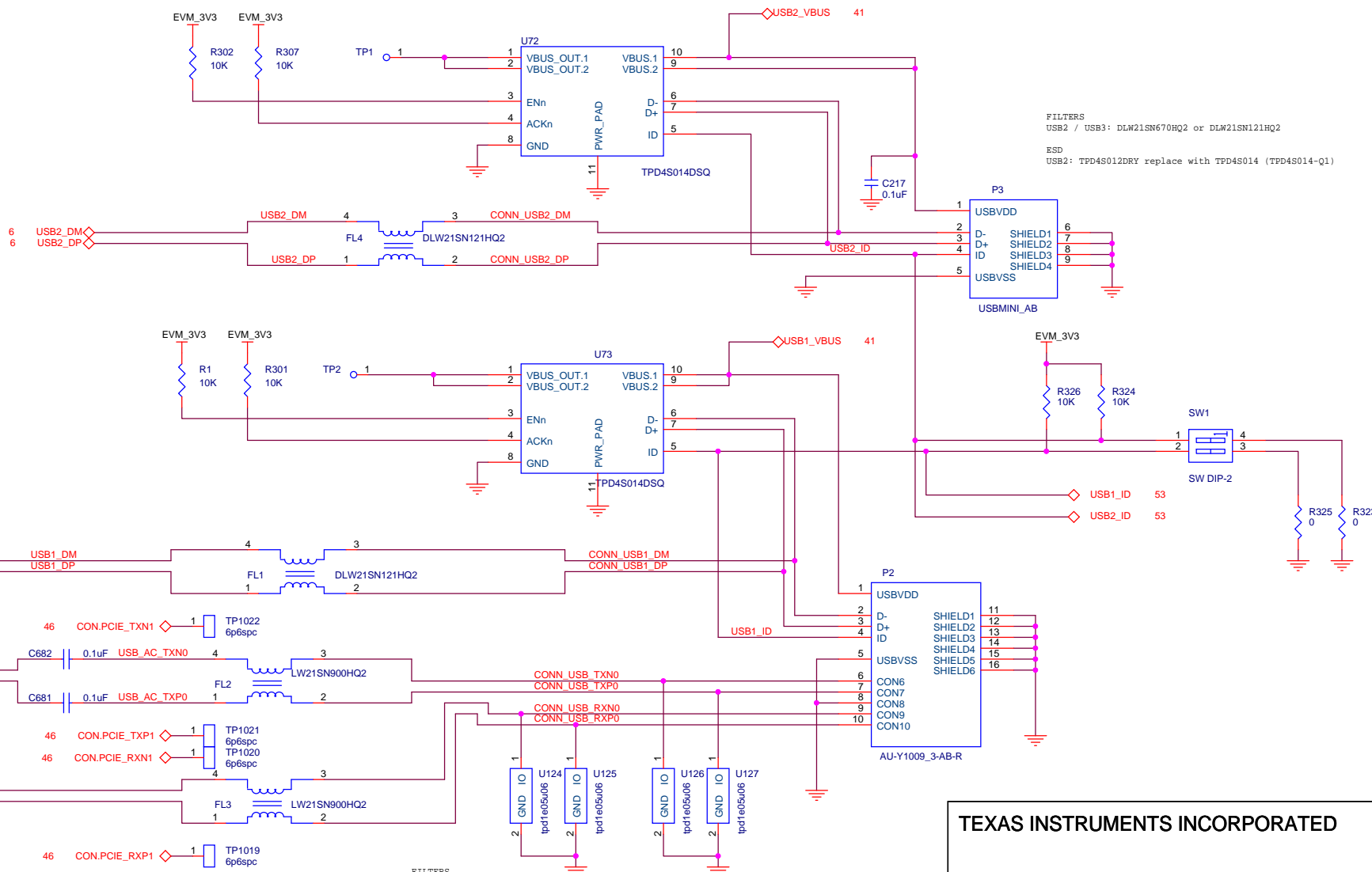
Size: B	DOC NO: 517502	REV: C
Date: Tuesday, November 08, 2016	Sheet 39	of 71



TEXAS INSTRUMENTS INCORPORATED		
Title: DRA72x/TA2Ex EVM CPU Board		
Page Contents: MEM SD CARD		
Size: B	DOC NO: 517502	REV: C
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TEXAS INSTRUMENTS INCORPORATED		
Title: DRA72x/TDA2Ex EVM CPU Board		
Page Contents: USB VBUS		
Size: B	DOC NO: 517502	REV: A
Date: Tuesday, November 08, 2016	Sheet 41	of 71



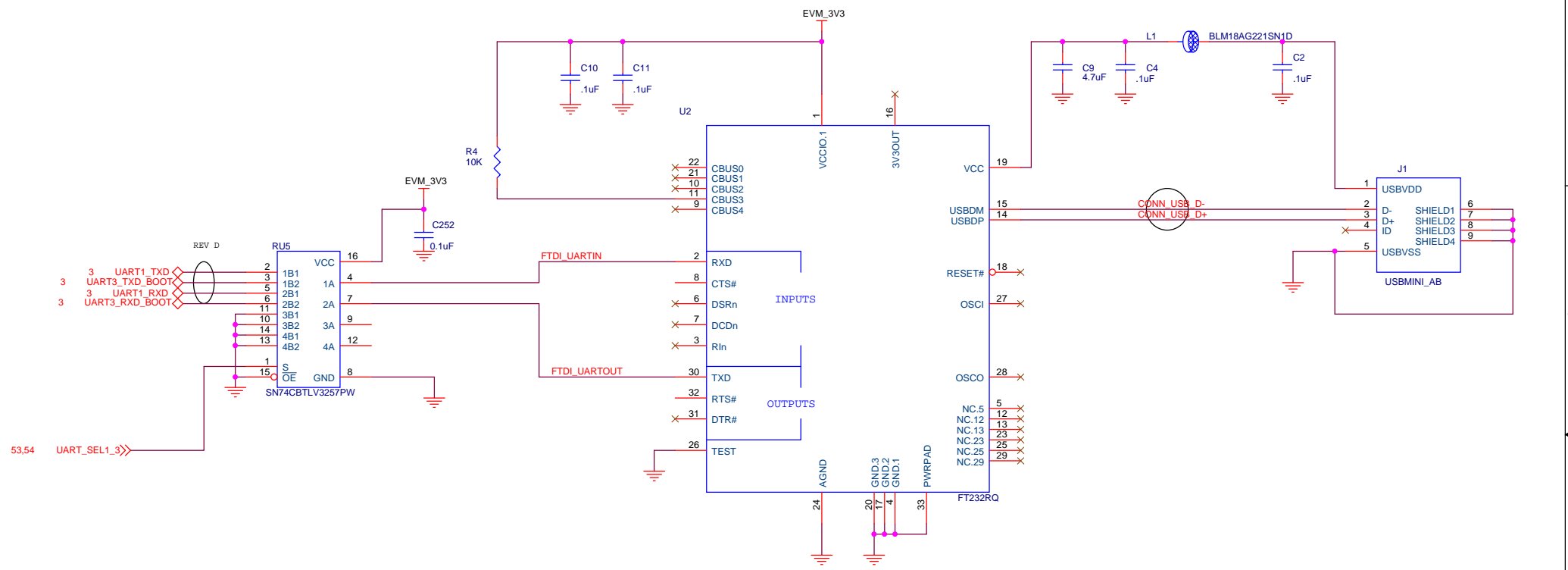
FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2
 ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)

PCIE PADS SHARE PIN 1/4 WITH FL2/3.
 FLx NO-POP, PCIE SIGNALS CAN BE POP
 WITH 0201 OR SOLDER BRIDGE.

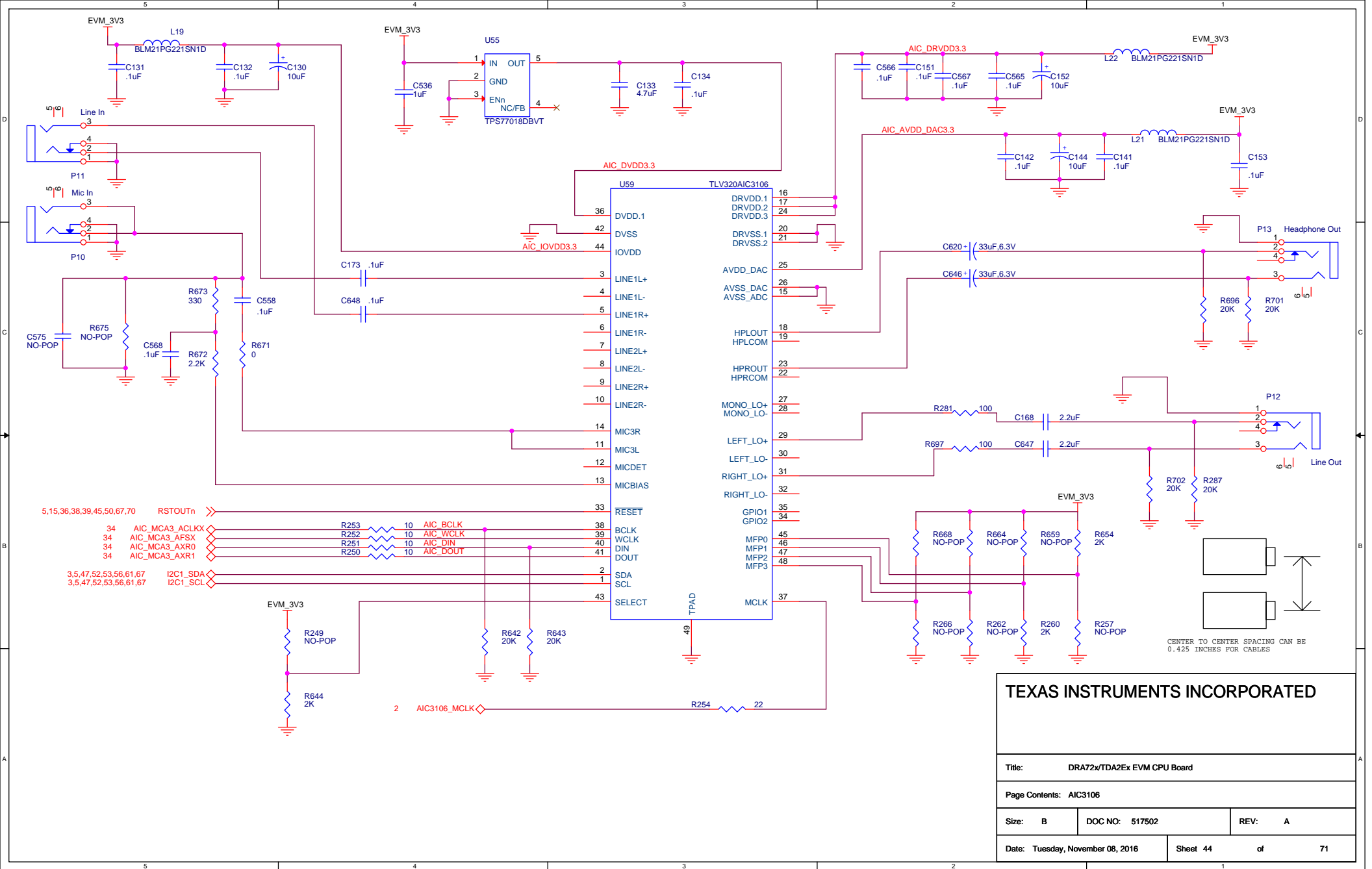
FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2

ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)
 USB3: TPD4EUSB30 replace with two TPD2EUSB30 (TPD2EUSB30-Q1) in drt package

TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Exx EVM CPU Board			
Page Contents: USB CONNECTORS			
Size: B	DOC NO: 517502	REV: B	
Date: Tuesday, November 08, 2016	Sheet 42	of	71



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: USB FTDI UART			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 43	of	71



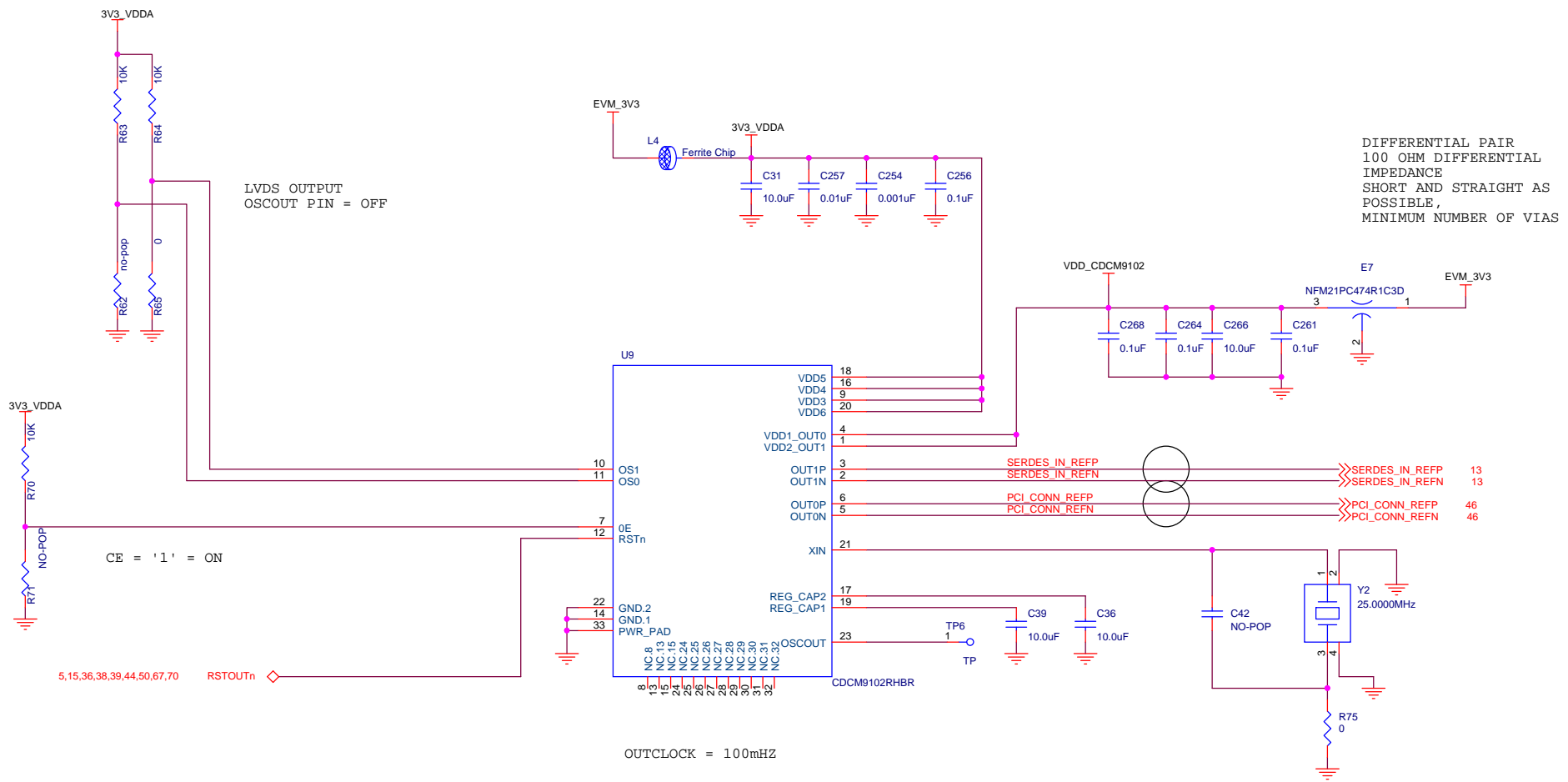
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board

Page Contents: AIC3106

Size: B	DOC NO: 517502	REV: A
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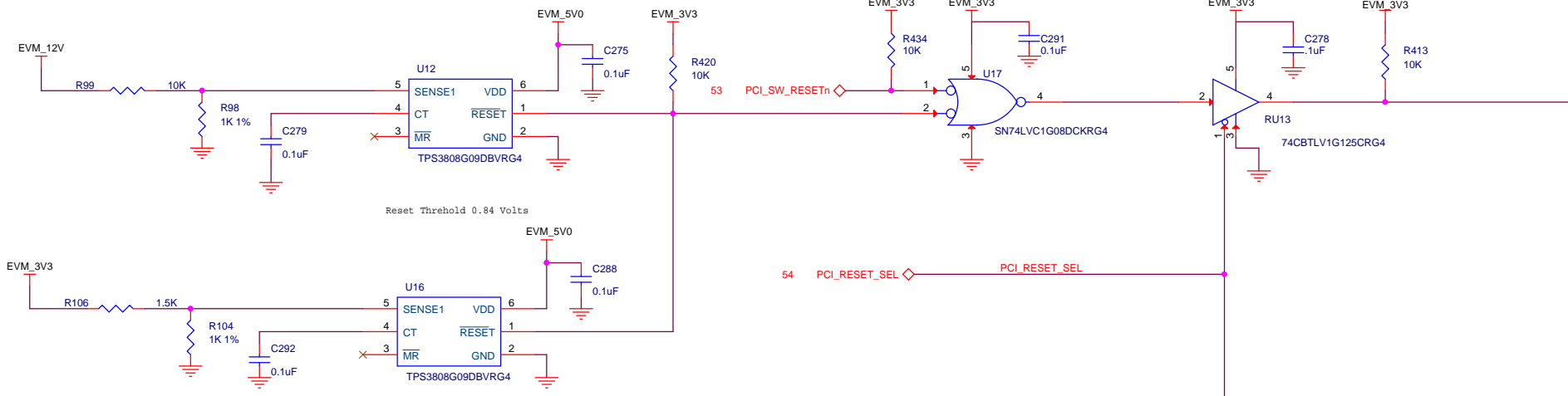
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2AEx EVM CPU Board

Page Contents: SERDES CLOCK

Size: B	DOC NO: 517502	REV: A
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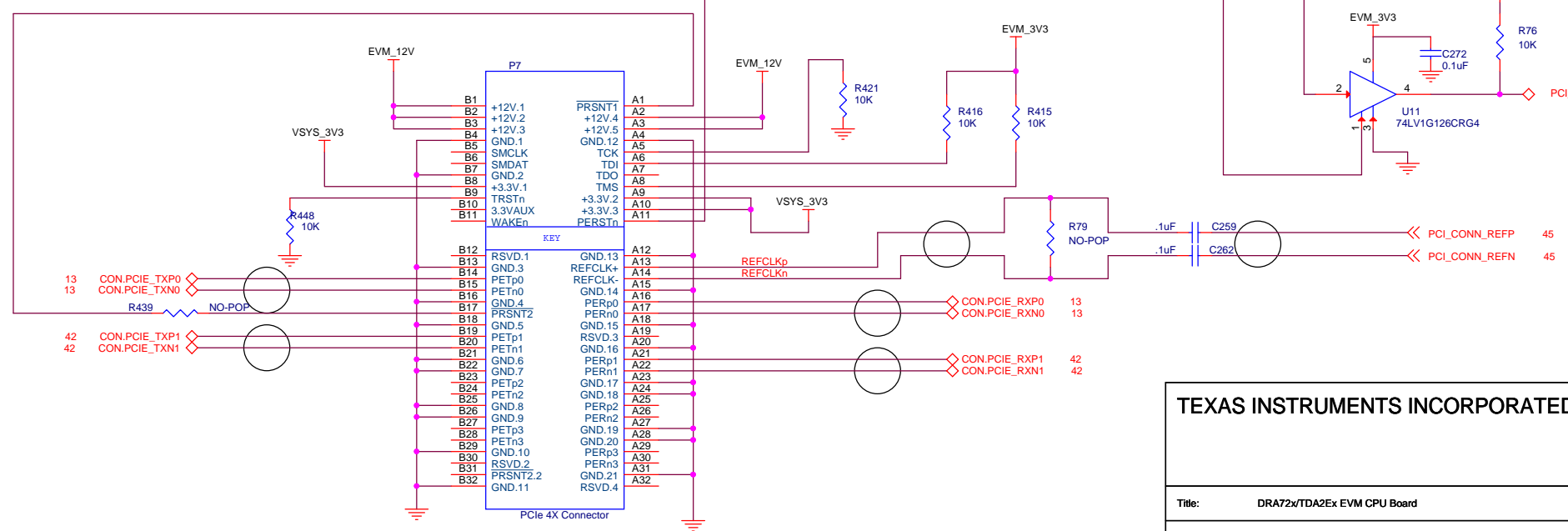
Date: Tuesday, November 08, 2016	Sheet 45 of 71
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Reset Threshold 0.84 Volts

Reset Threshold 0.84 Volts

Connector must be less than 2.25 inches to board edge from key to board edge



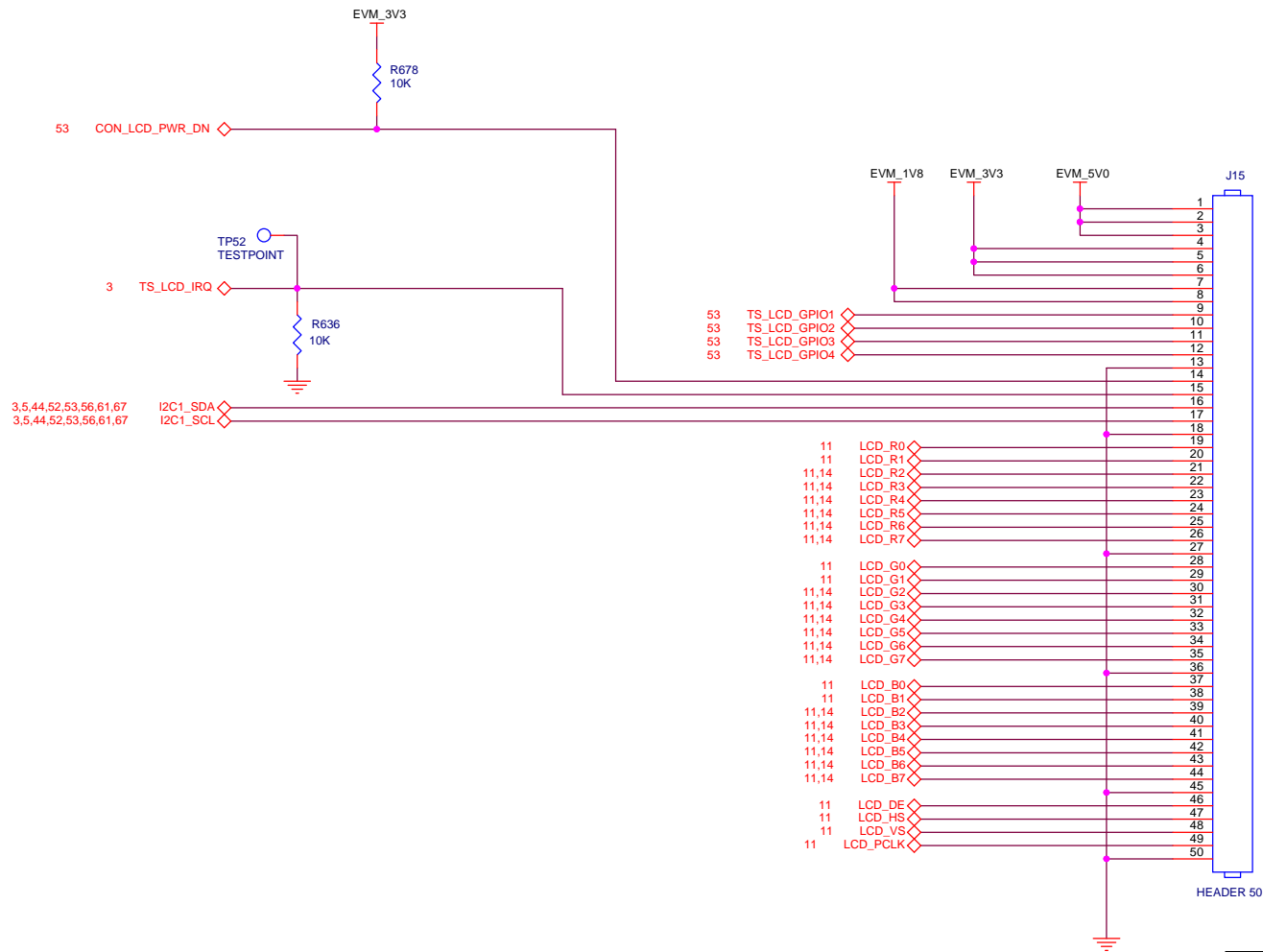
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2AEx EVM CPU Board

Page Contents: PCIe CONNECTORS

Size: B	DOC NO: 517502	REV: B
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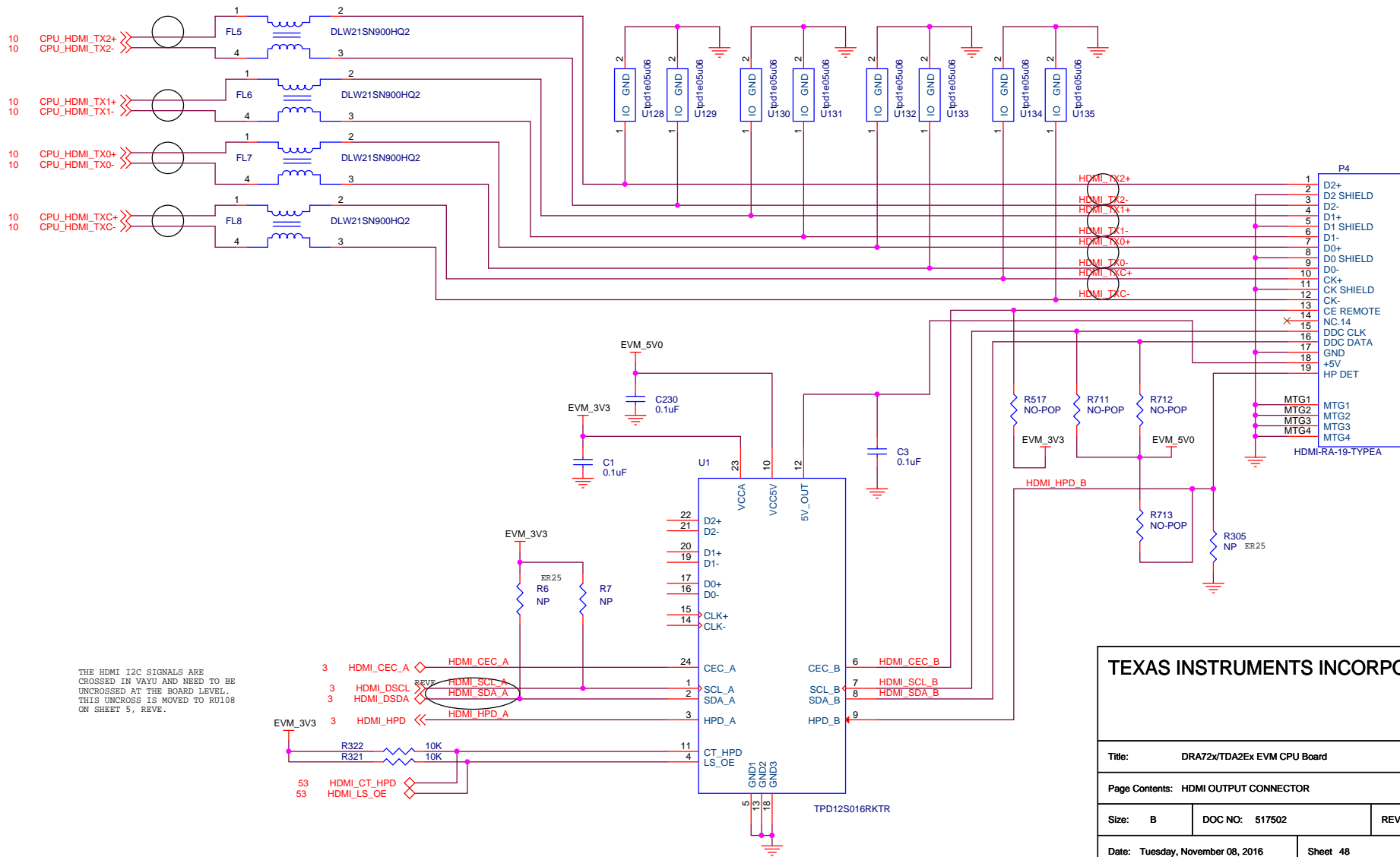
Date: Tuesday, November 08, 2016	Sheet 46	of 71
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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: LCD CONNECTOR			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 47	of	71

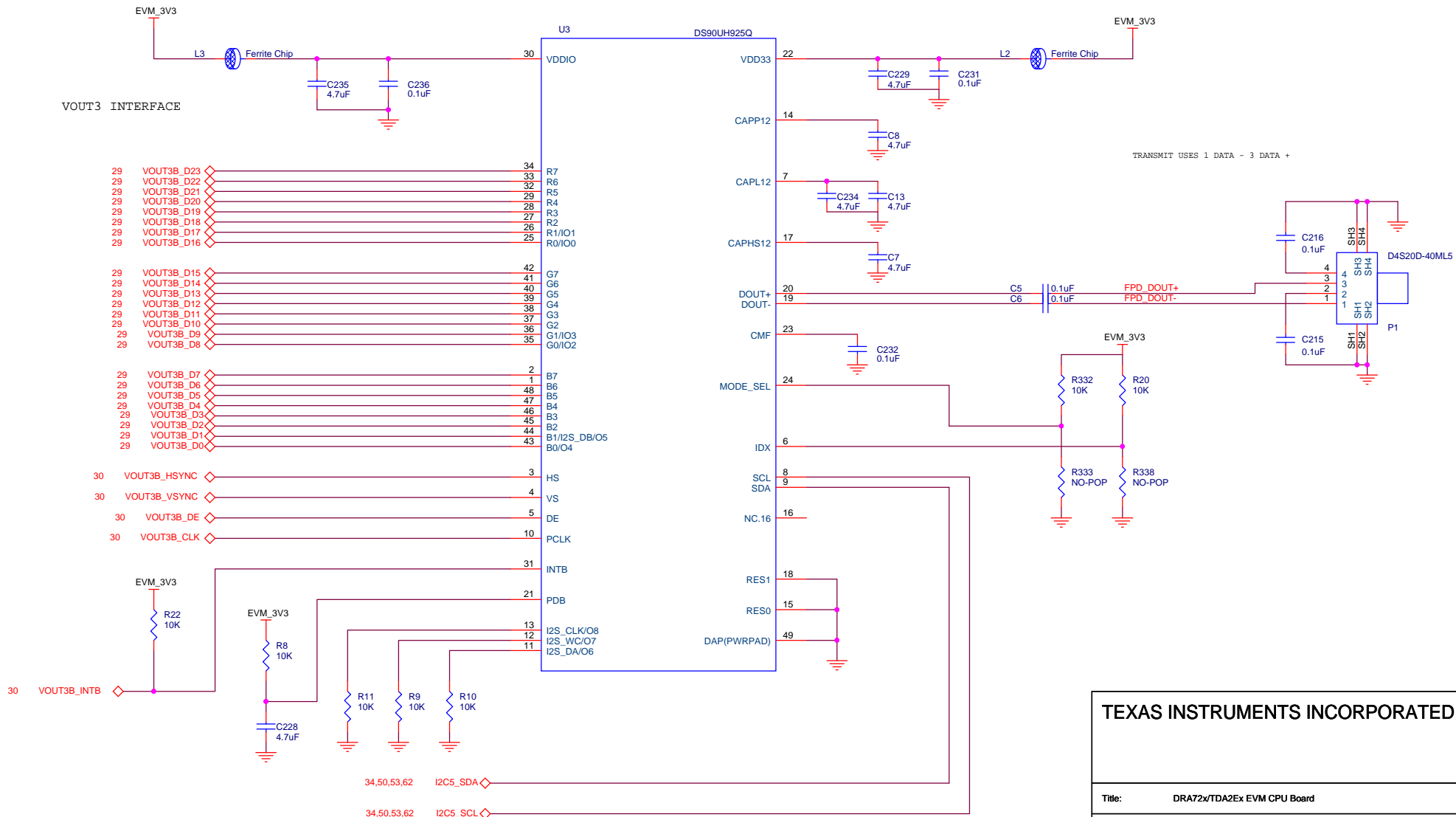
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



THE HDMI I2C SIGNALS ARE
CROSSED IN VAYU AND NEED TO BE
UNCROSSED AT THE BOARD LEVEL.
THIS UNCROSS IS MOVED TO RUI08
ON SHEET 5, REV.

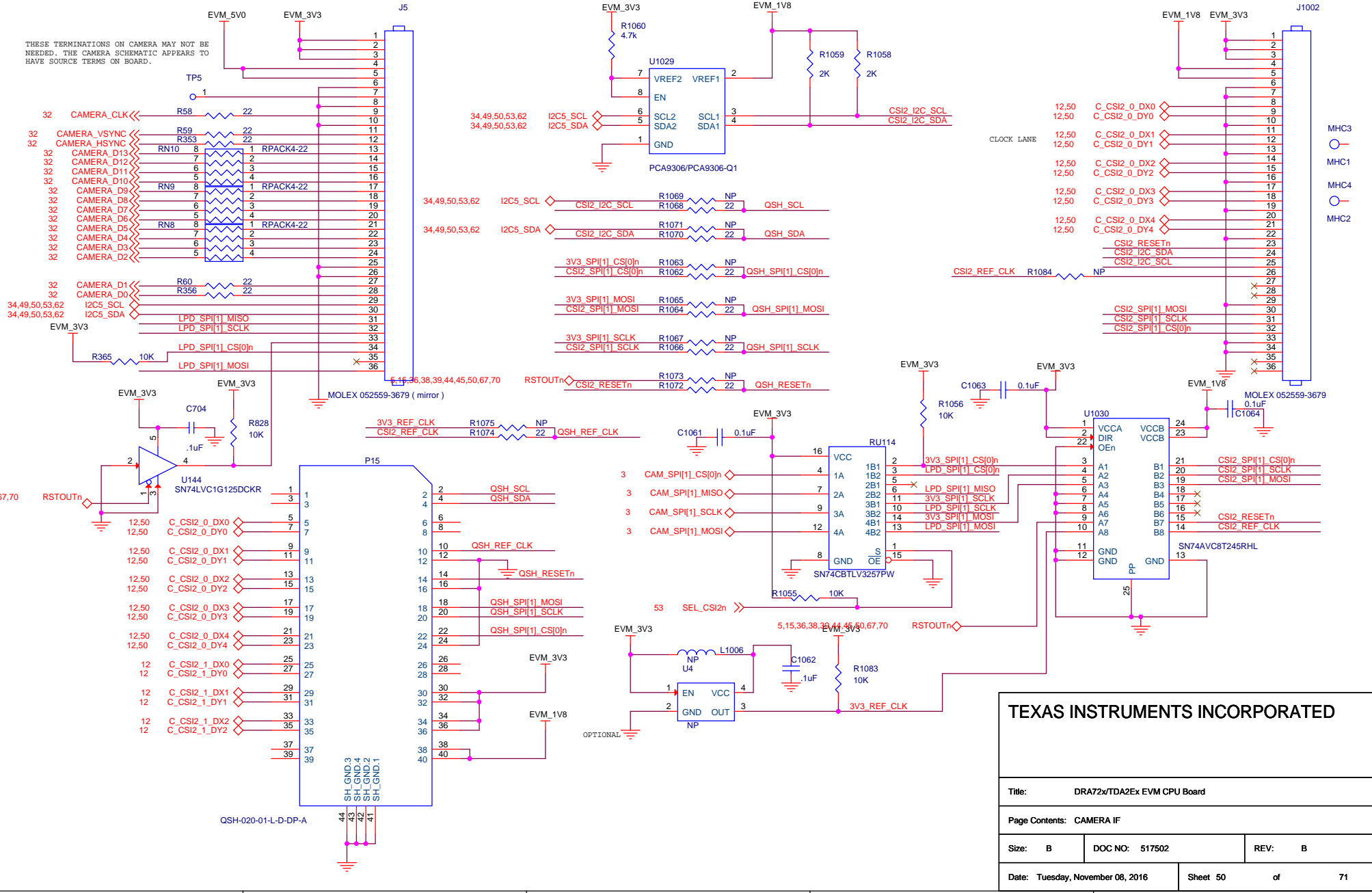
TEXAS INSTRUMENTS INCORPORATED		
Title: DRA72x/TA2Ex EVM CPU Board		
Page Contents: HDMI OUTPUT CONNECTOR		
Size: B	DOC NO: 517502	REV: C
Date: Tuesday, November 08, 2016	Sheet 48	of 71



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: FPD LINK			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 49	of	71

MHC1
MHC1
MHC2
MHC2

THESE TERMINATIONS ON CAMERA MAY NOT BE NEEDED. THE CAMERA SCHEMATIC APPEARS TO HAVE SOURCE TERMS ON BOARD.



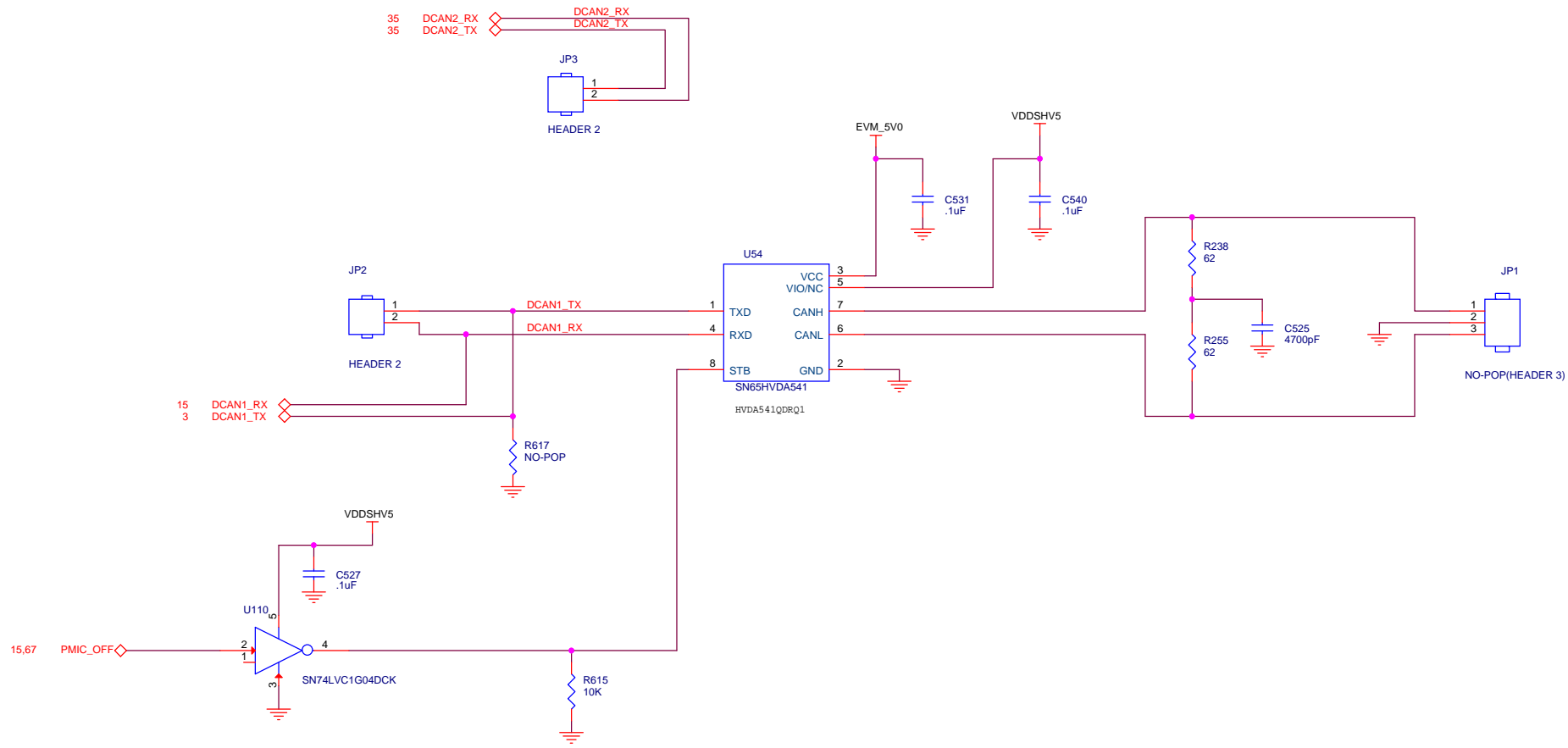
TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board

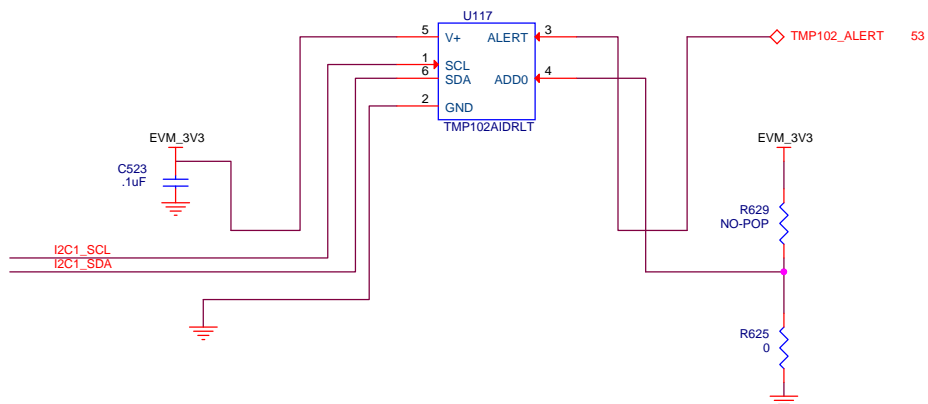
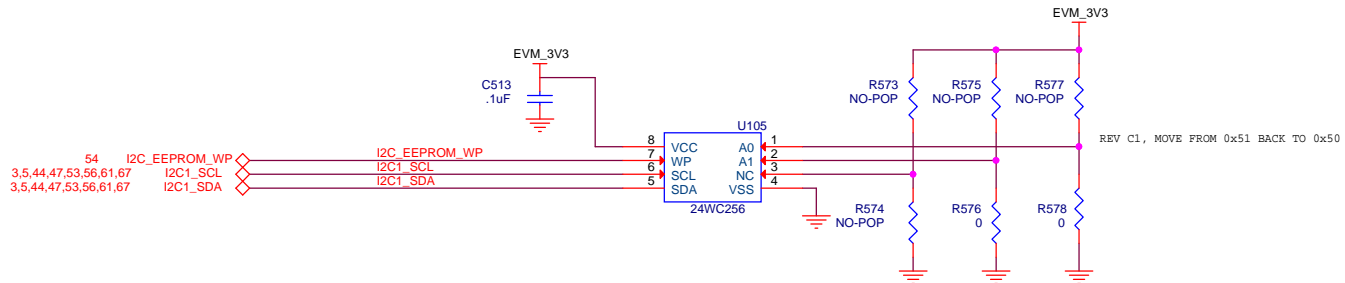
Page Contents: CAMERA IF

Size: B	DOC NO: 517502	REV: B
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Date: Tuesday, November 08, 2016	Sheet 50	of 71
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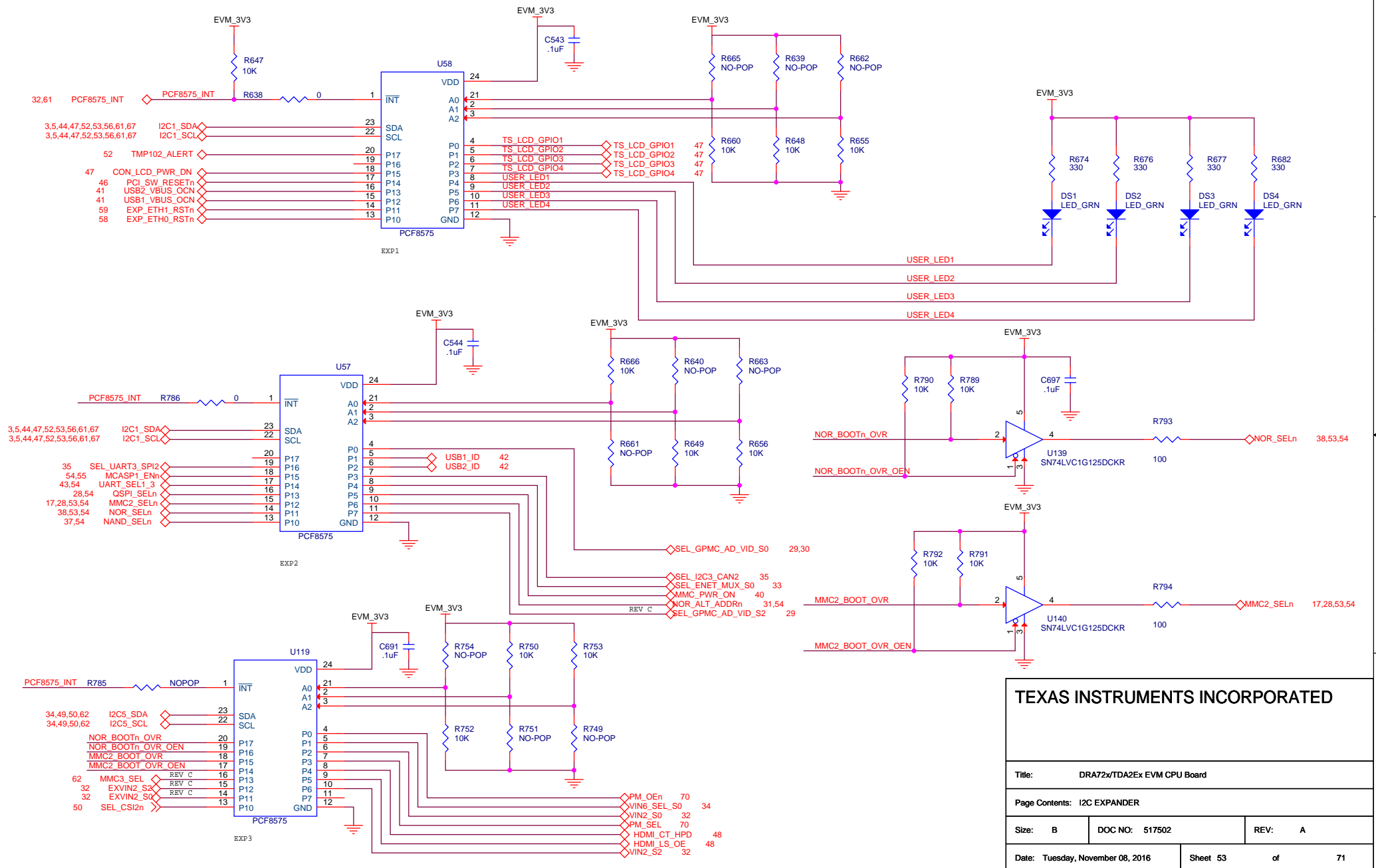


TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: CAN CONNECTORS			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 51	of	71

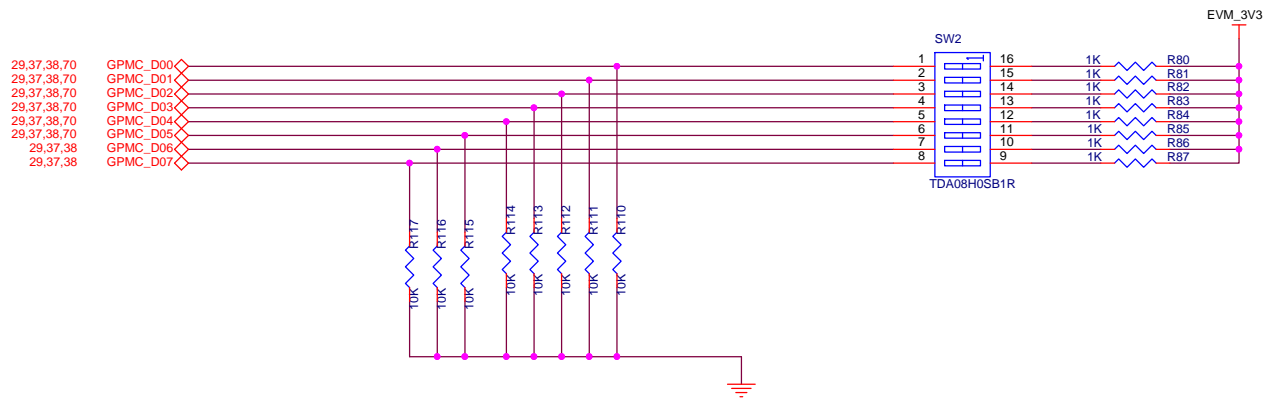


PLACE TEMP SENSOR CLOSE TO PROCESSOR

TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: I2C EEPROM/TEMP SENSOR			
Size: B	DOC NO: 517502	REV: C1	
Date: Tuesday, November 08, 2016	Sheet 52	of	71



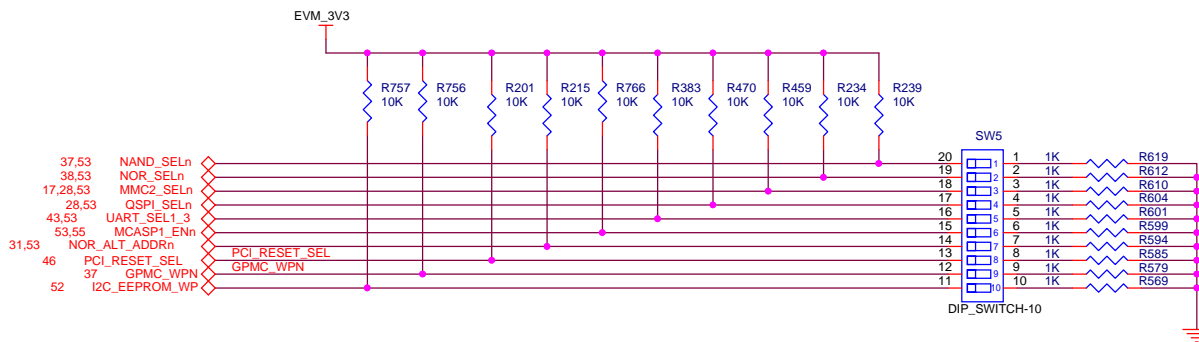
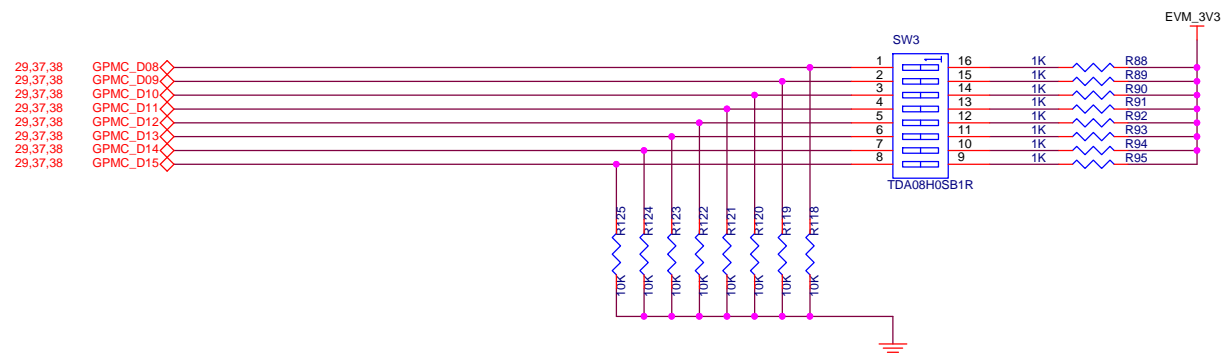
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: I2C EXPANDER			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 53	of	71



MMC2 BOOT PULL UP ON PAGE 23 SET TO LOGIC 0 TO ENABLE MMC2 MUX FOR BOOTING SET TO 1 FOR GPMC BOOTING

QSPI BOOT PULL UP ON PAGE 23 SET TO LOGIC 0 TO ENABLE QSPI MUX FOR BOOTING SET TO 1 FOR GPMC BOOTING

UART SEL1_3 PULL UP ON PAGE 58 SELECTS UART3 MUX INPUT TO BE USART PORT AT MINI_USB A(J1) DURING BOOTING.
MCASP1_ENn MUST BE SET TO LOGIC 1 TO DISABLE COM8. ALSO OTHER MUX NEEDS TO BE IN DEFAULT CONFIGURATION



TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TDA2Ex EVM CPU Board

Page Contents: BOOTSWITCHES

Size: B

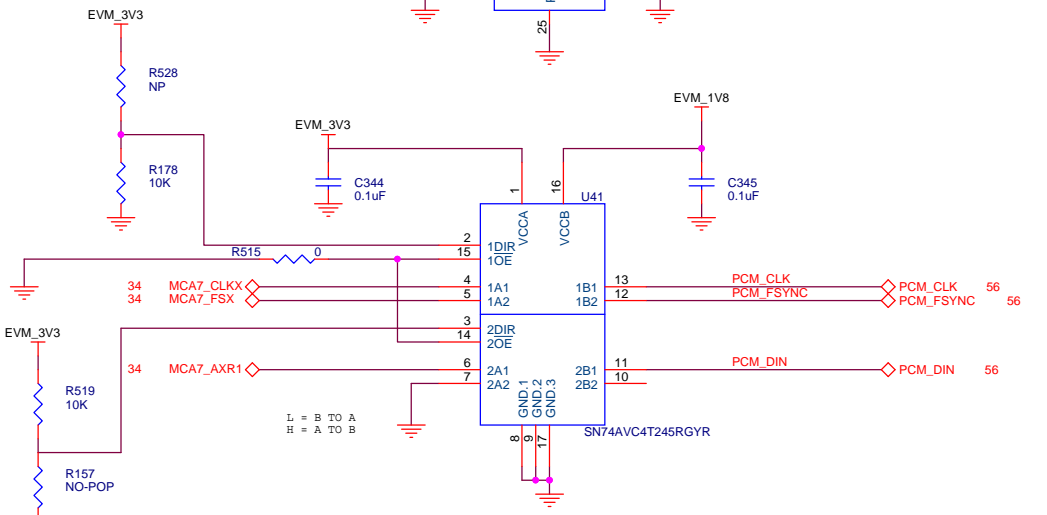
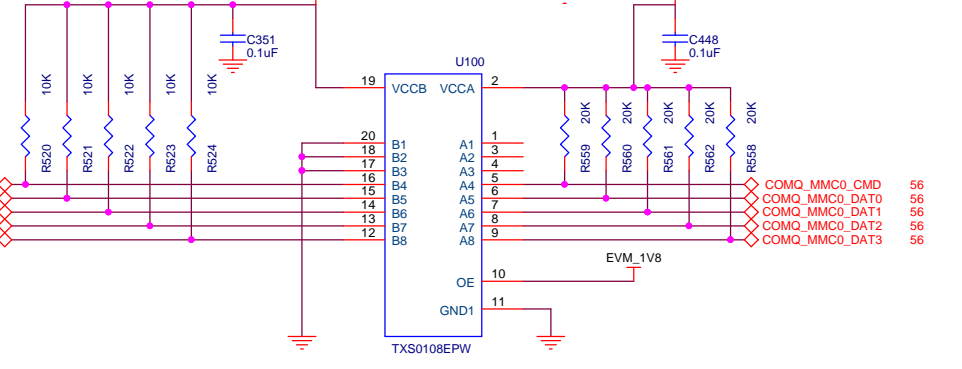
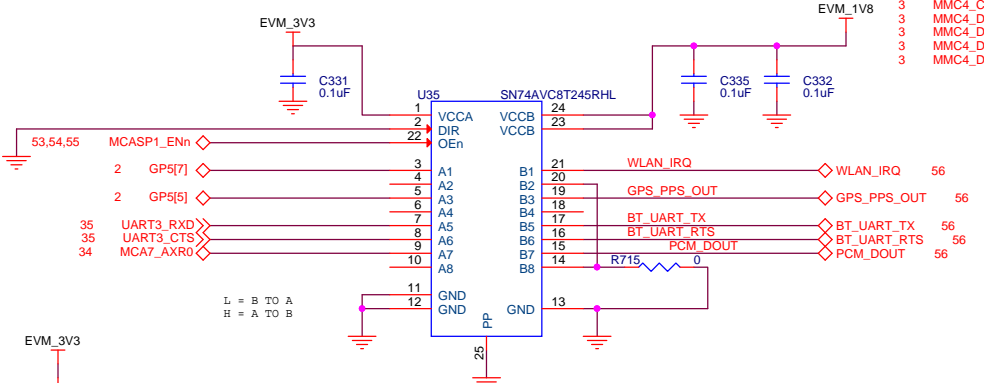
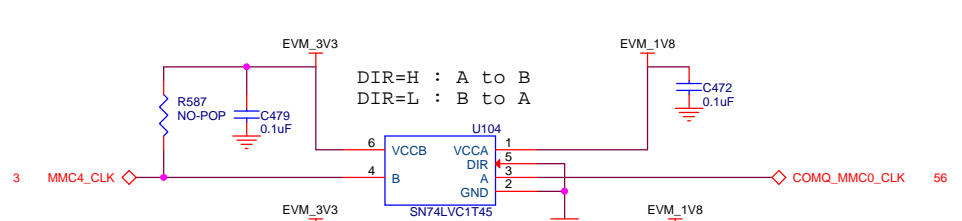
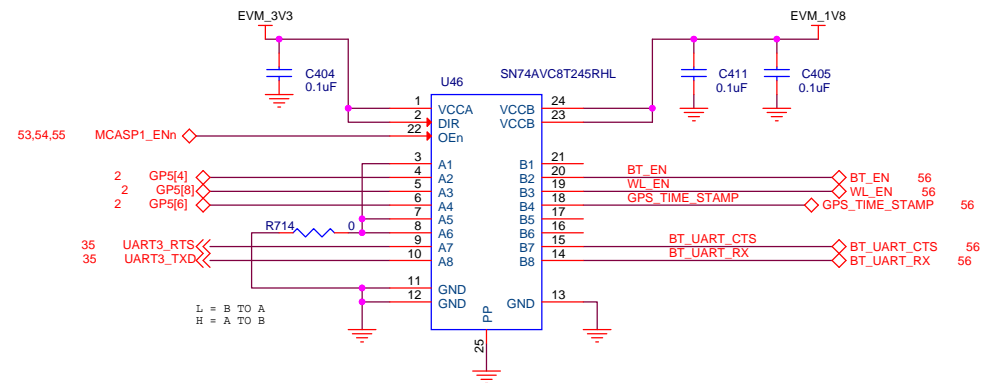
DOC NO: 517502

REV: A

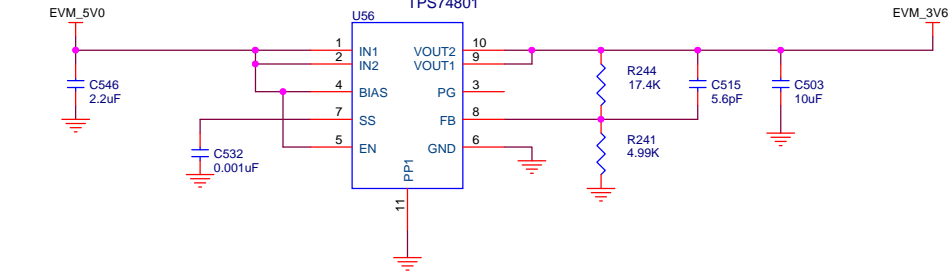
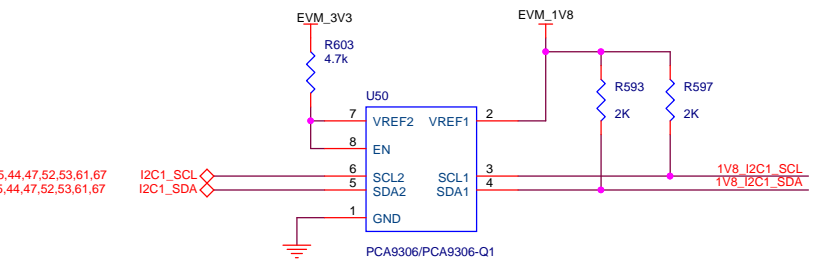
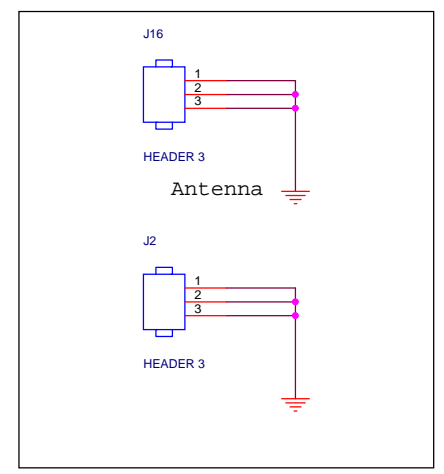
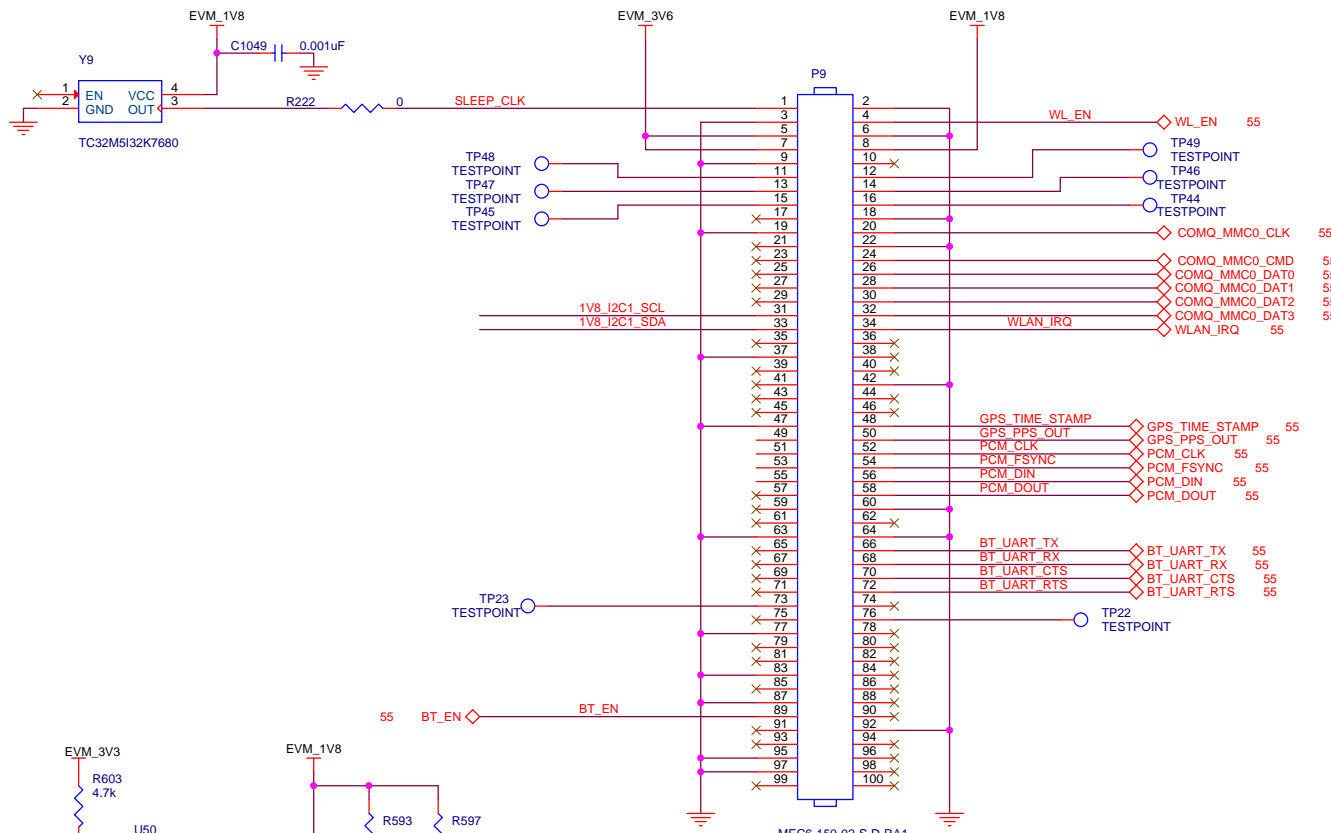
Date: Tuesday, November 08, 2016

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TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: COM8 LEVEL TRANSLATOR			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 55	of	71



$$V_{OUT} = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

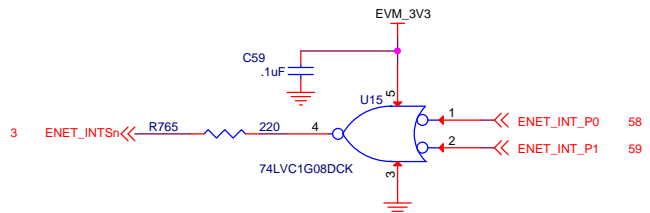
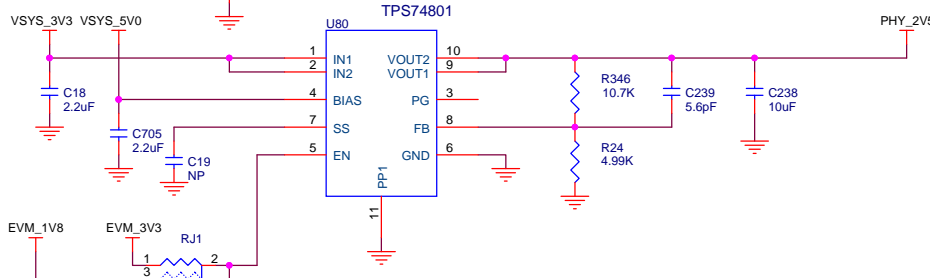
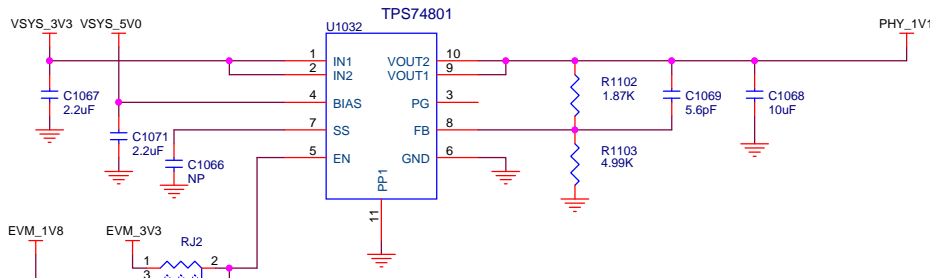
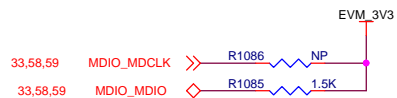
$$3.6 = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

$$4.5 = (1 + (R_{TOP}/R_{BOTTOM}))$$

$$3.5 = ((R_{TOP}/R_{BOTTOM}))$$

$$3.5 R_{BOTTOM} = R_{TOP}$$

TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: COM8 CONNECTOR			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 56	of	71



$$V_{OUT} = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

$$2.5 = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

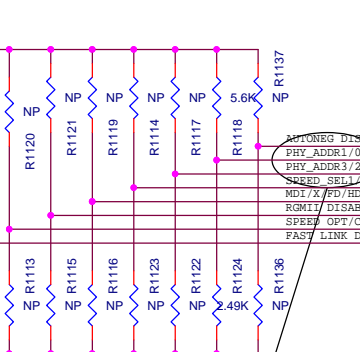
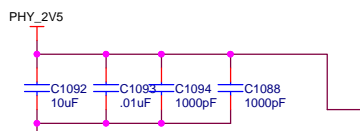
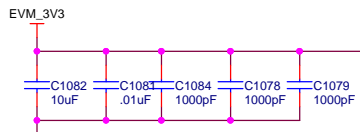
$$2.5 = 0.8 * (1 + (R_{TOP}/4.99K))$$

$$3.125 = (1 + (R_{TOP}/4.99K))$$

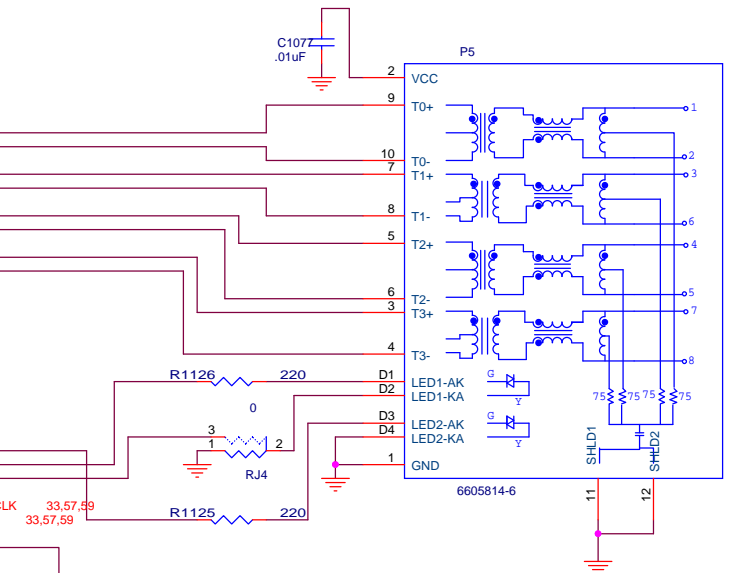
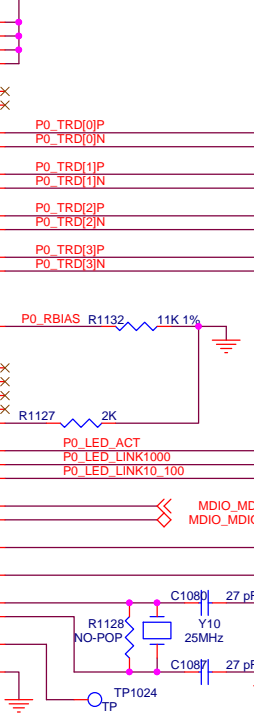
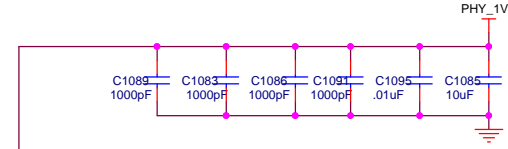
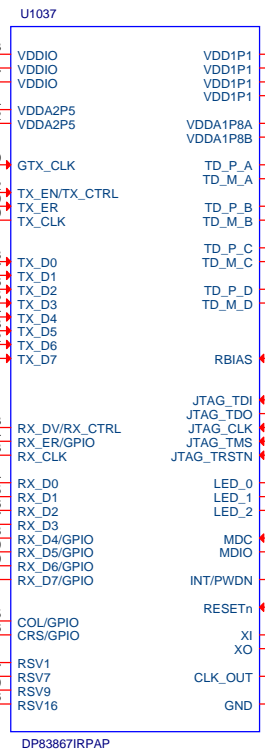
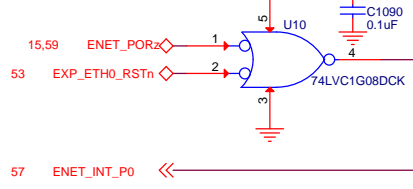
$$2.125 = (R_{TOP}/4.99K)$$

$$10.6K = R_{TOP}$$

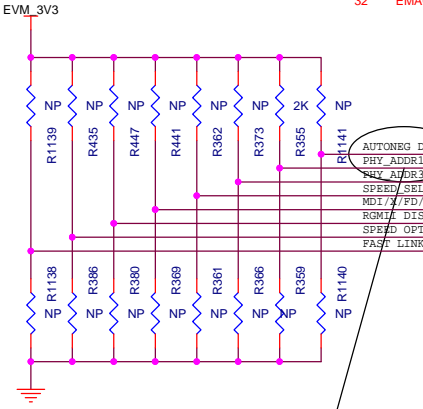
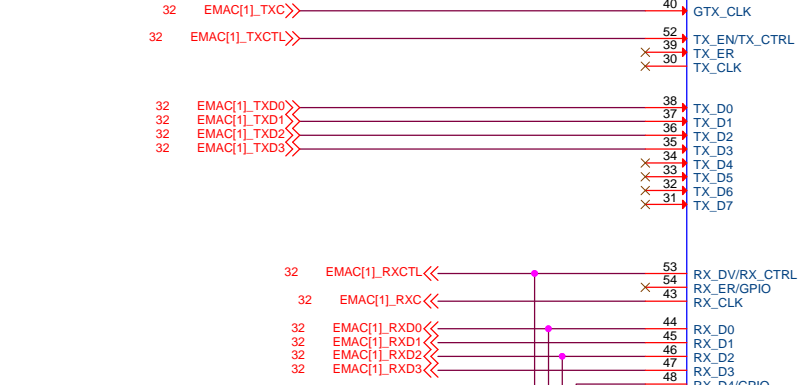
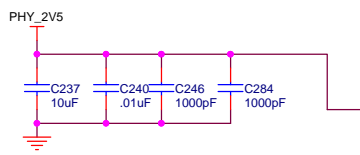
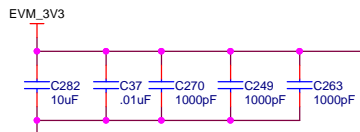
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2A2Ex EVM CPU Board			
Page Contents: ETHERNET POWER AND MISC			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016		Sheet 57	of 71



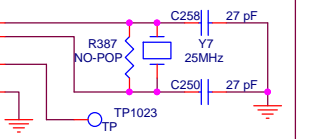
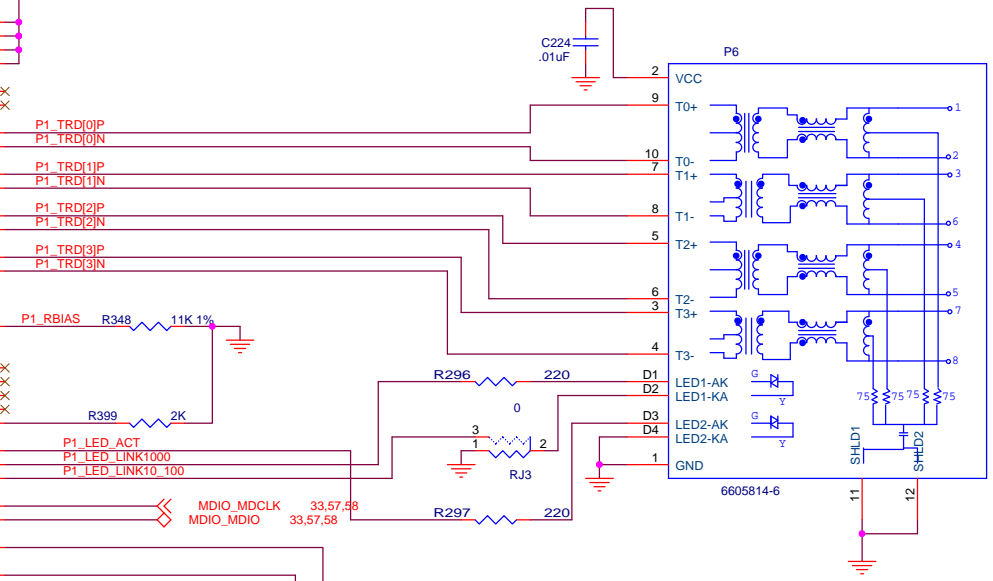
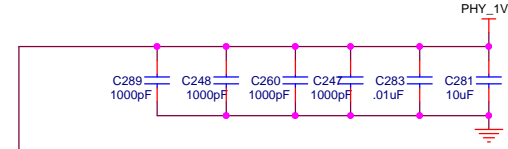
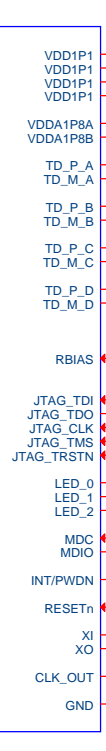
PHY_ADDR 2, TO MATCH VAYU EVM.
 BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY_ADDR 3:0.
 DISABLING SOC PD WILL ALSO CAUSE DIFFERENT SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET. RECOMMEND THAT SOC PD NOT BE DISABLED.



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: ETHERNET PORT0			
Size: B	DOC NO: 517502	REV: D	
Date: Tuesday, November 08, 2016	Sheet 58	of	71

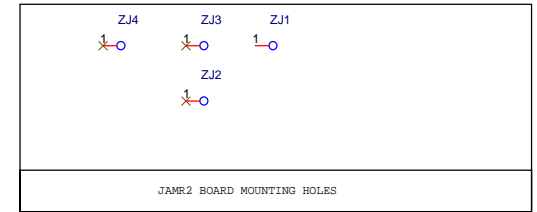
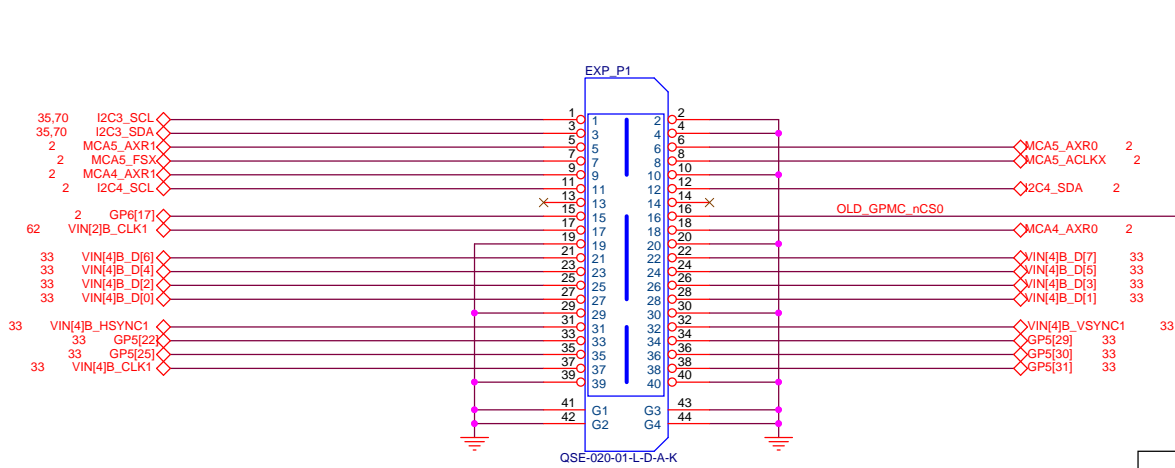


PHY ADDR 3, TO MATCH VAYU EVM.
 BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY ADDR 3:0.
 DISABLING SOC PD WILL ALSO CAUSE DIFFERENT SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET. RECOMMEND THAT SOC PD NOT BE DISABLED.

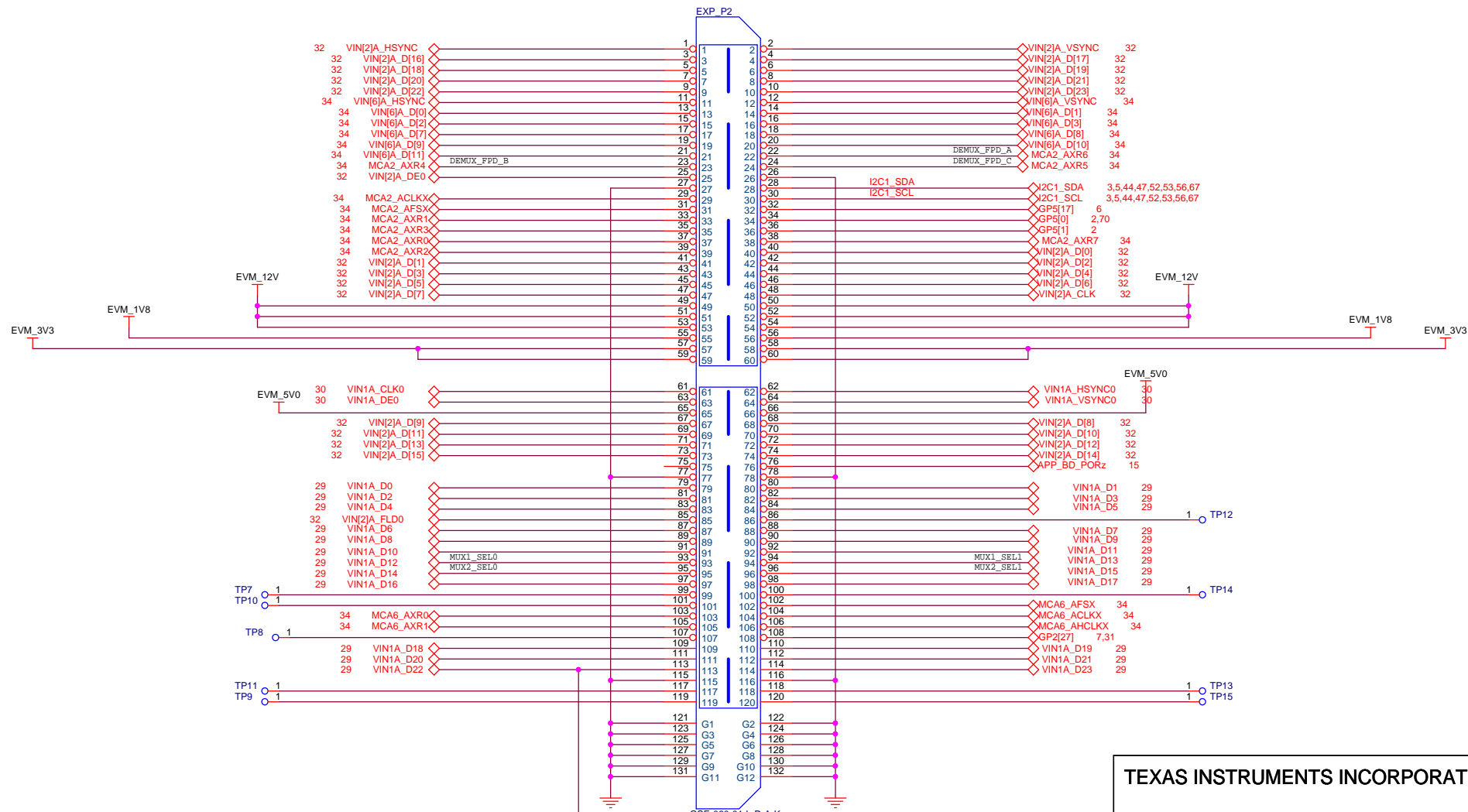


TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: ETHERNET PORT1			
Size: B	DOC NO: 517502	REV: D	
Date: Tuesday, November 08, 2016	Sheet 59	of	71

MMC3_D7/VIN2B_CLK1/AB5/P1.P17

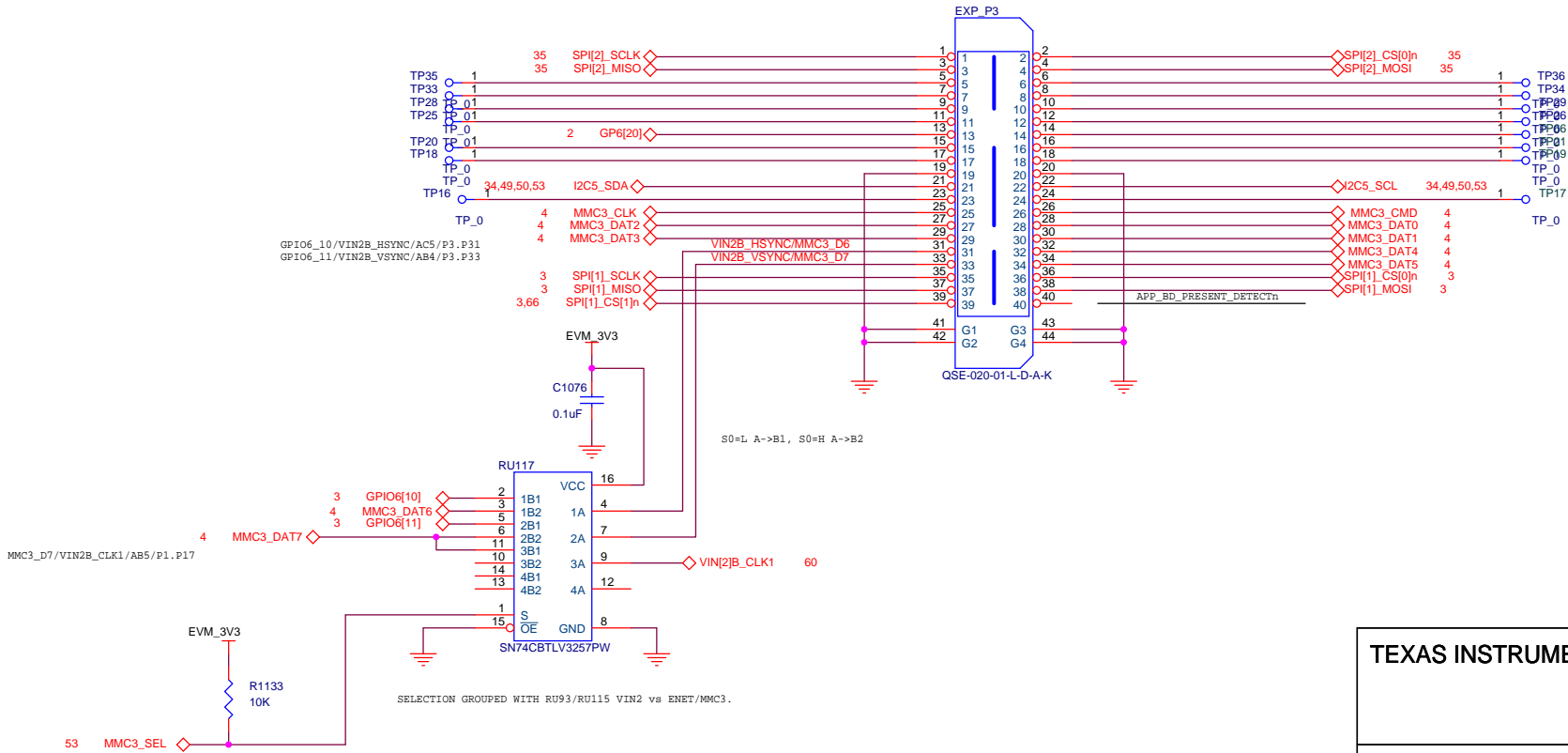


TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: APPLICATION IF CONN1			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 60	of	71

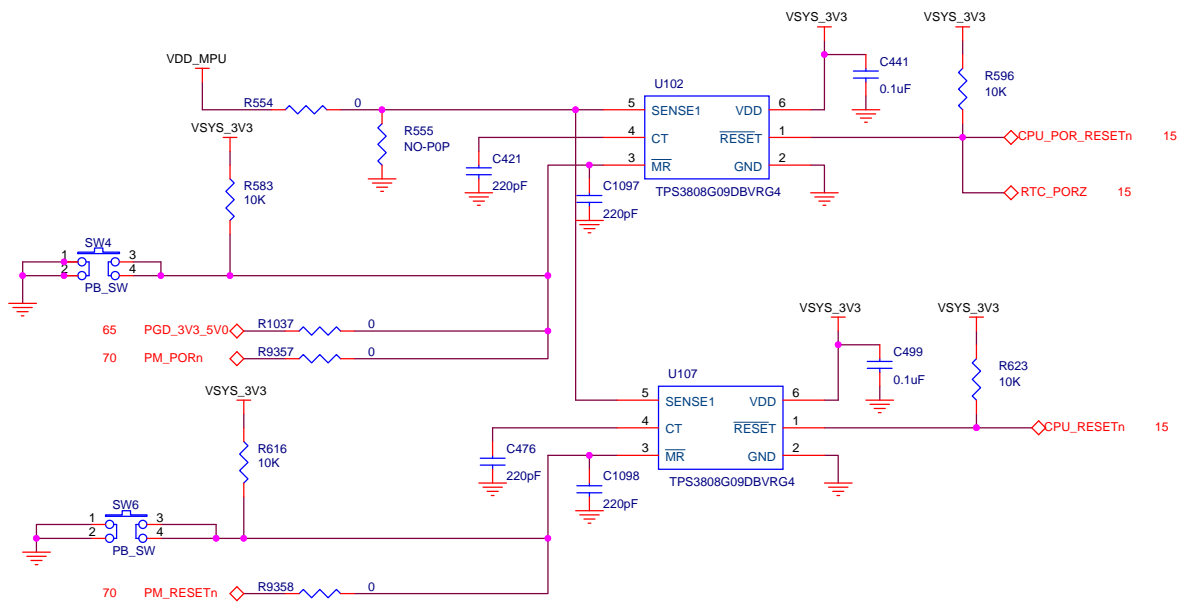


QSE-060-01-L-D-A-K

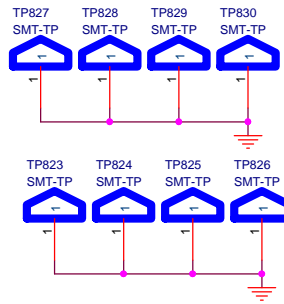
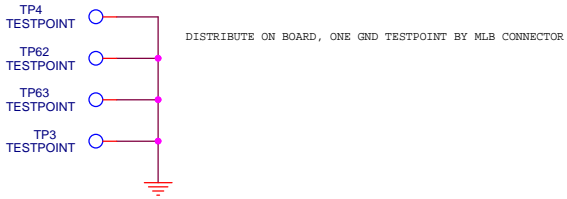
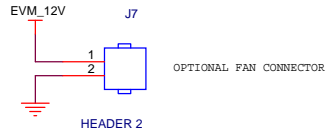
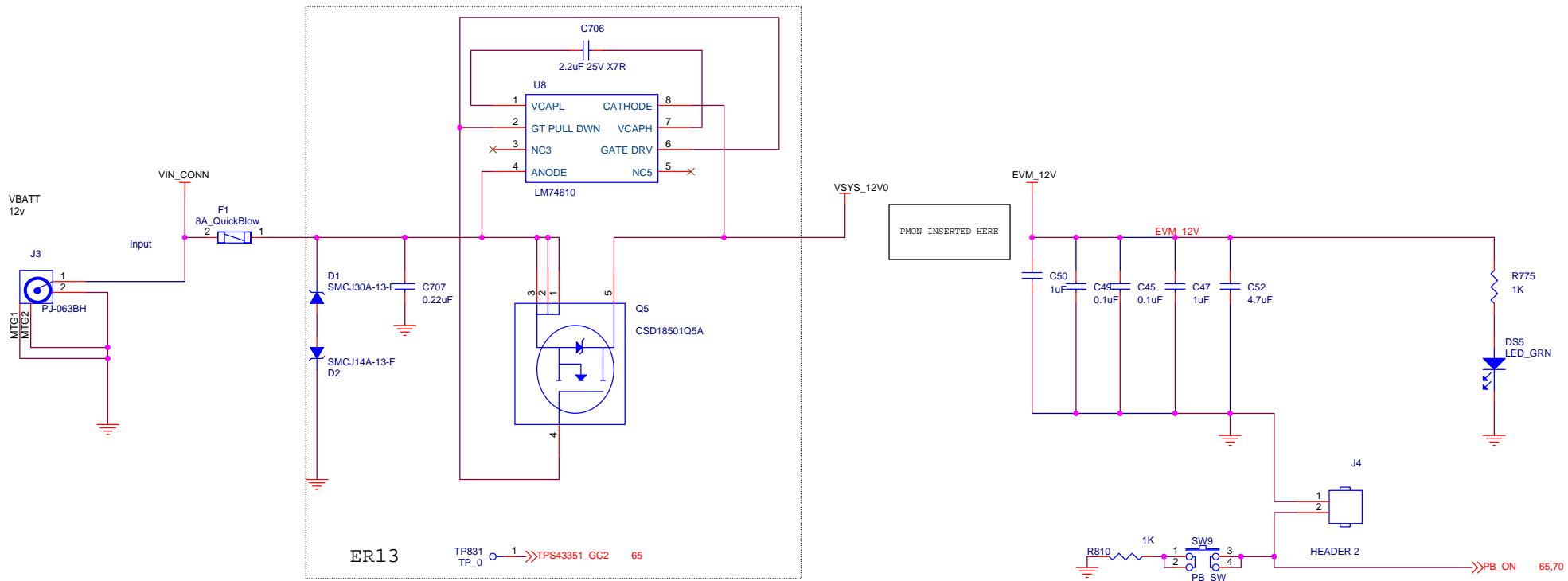
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: APPLICATION IF CONN2			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 61	of 71	



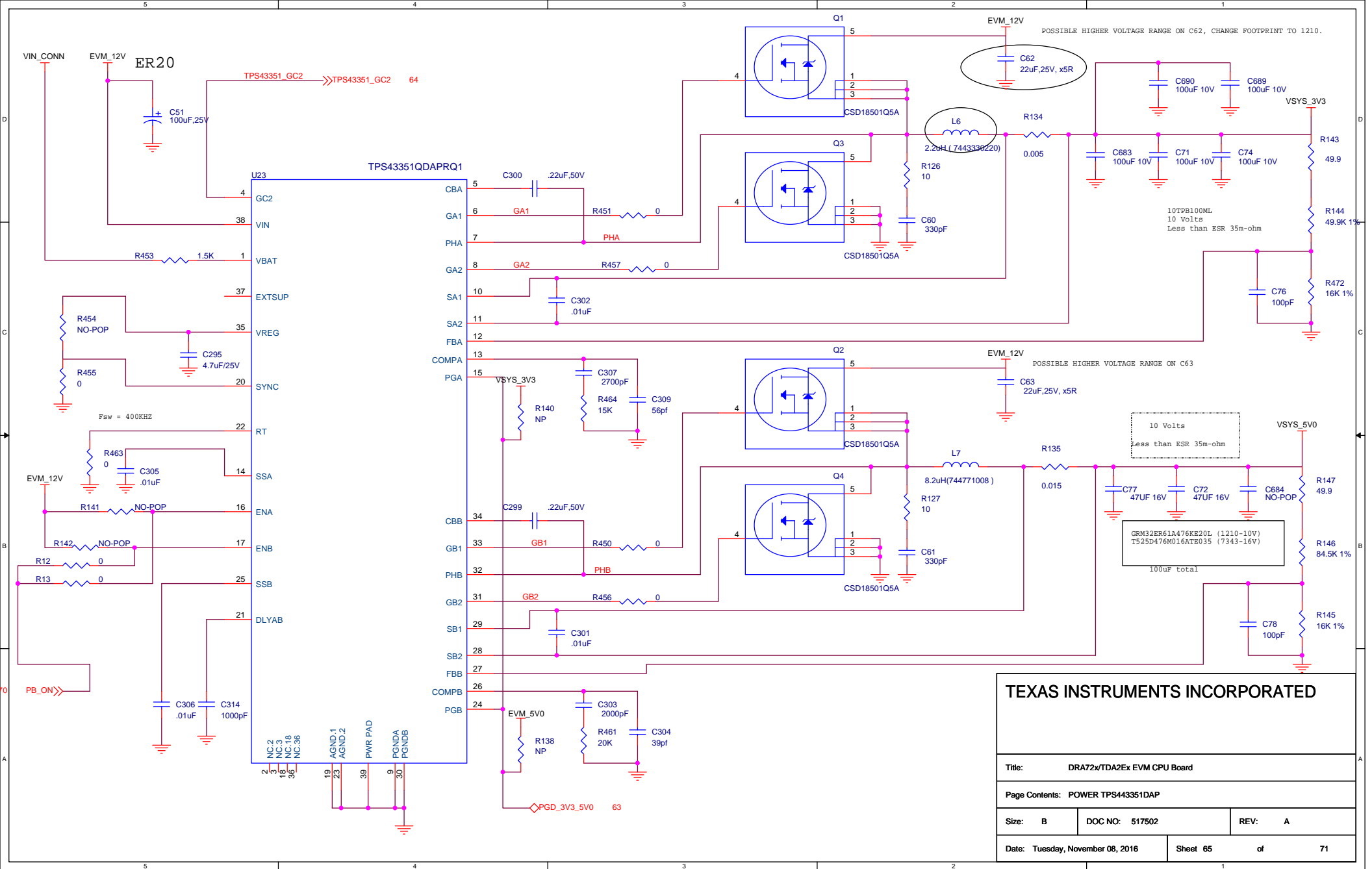
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: APPLICATION IF CONN3			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 62	of	71



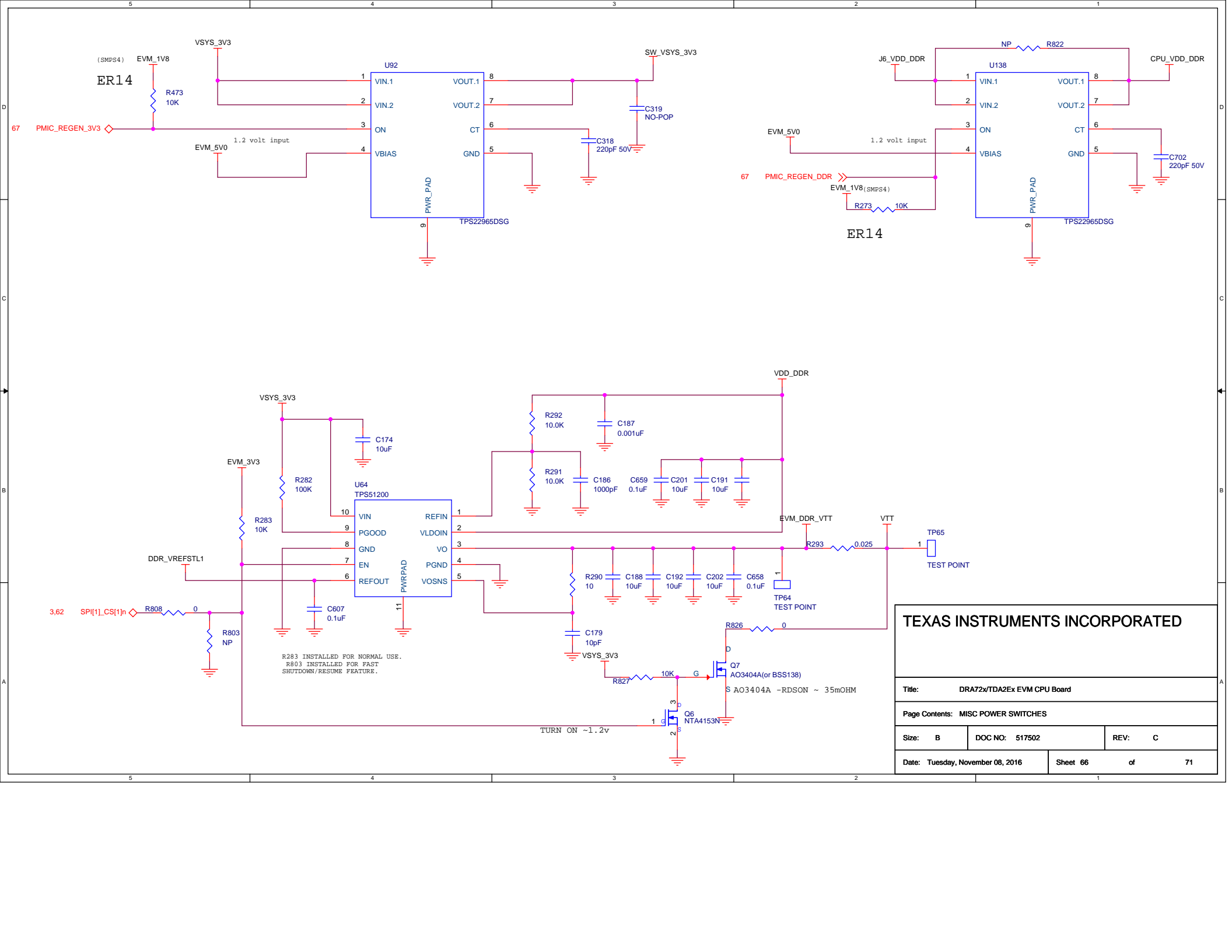
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: RESET			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 63	of	71



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TDA2Ex EVM CPU Board			
Page Contents: POWER INPUT			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 64	of	71



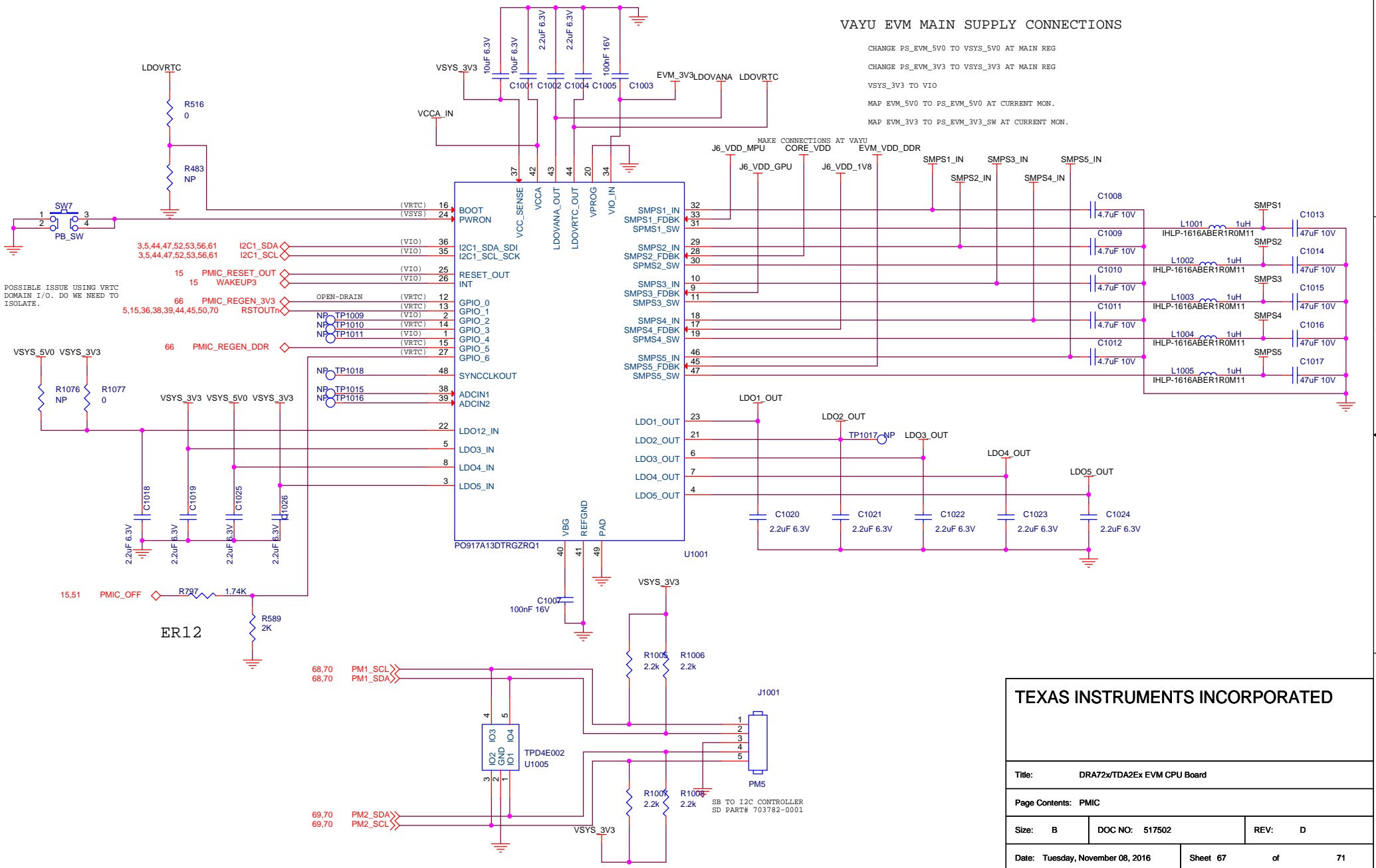
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2Ex EVM CPU Board			
Page Contents: POWER TPS443351DAP			
Size: B	DOC NO: 517502	REV: A	
Date: Tuesday, November 08, 2016	Sheet 65	of	71



TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: MISC POWER SWITCHES			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 66	of	71

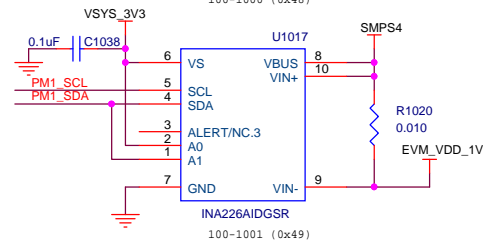
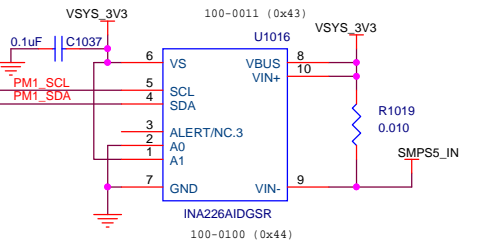
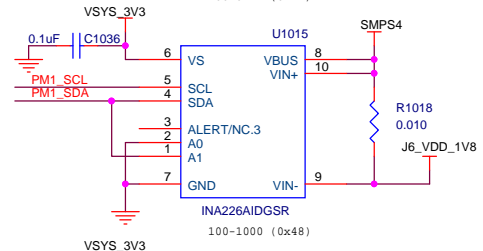
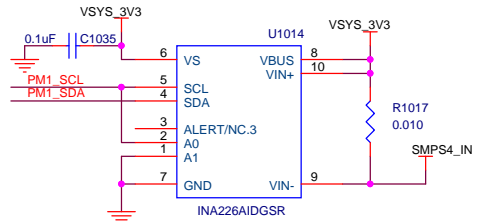
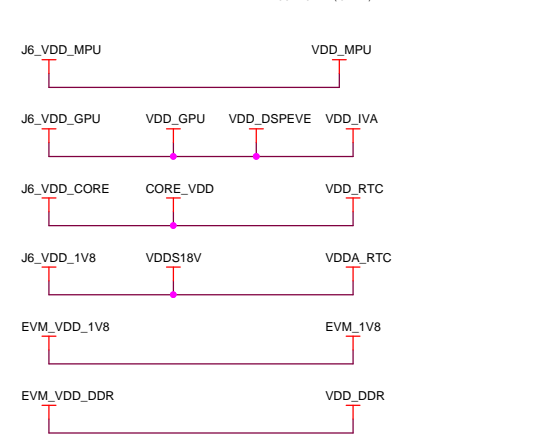
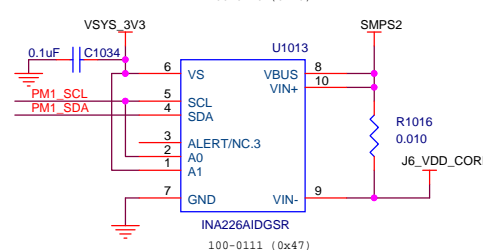
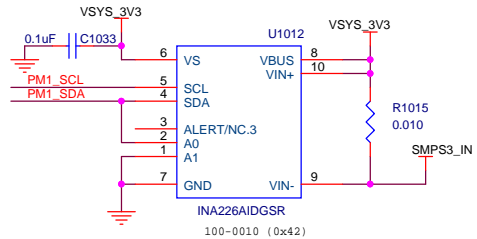
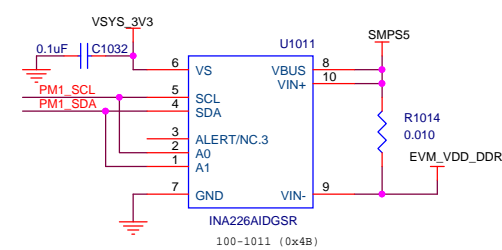
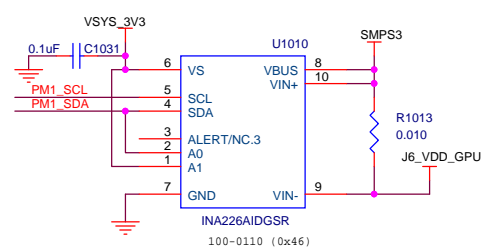
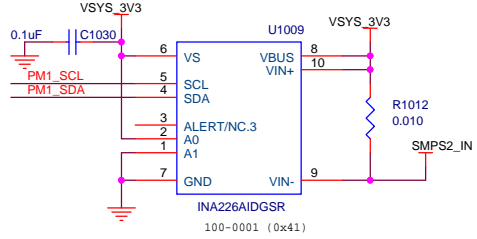
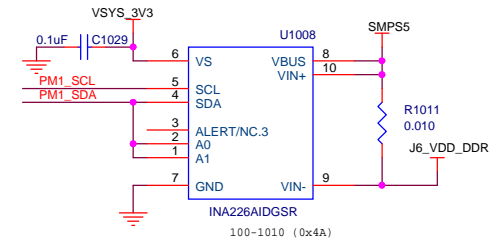
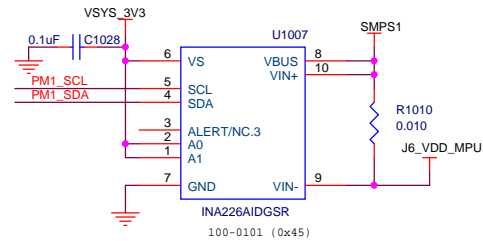
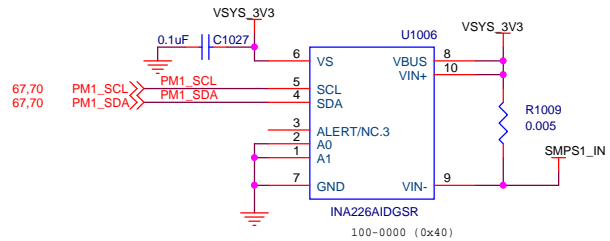
VAYU EVM MAIN SUPPLY CONNECTIONS

CHANGE PS_EVM_5V0 TO VSYS_5V0 AT MAIN REG
 CHANGE PS_EVM_3V3 TO VSYS_3V3 AT MAIN REG
 VSYS_3V3 TO VIO
 MAP EVM_5V0 TO PS_EVM_5V0 AT CURRENT MON.
 MAP EVM_3V3 TO PS_EVM_3V3_SW AT CURRENT MON.



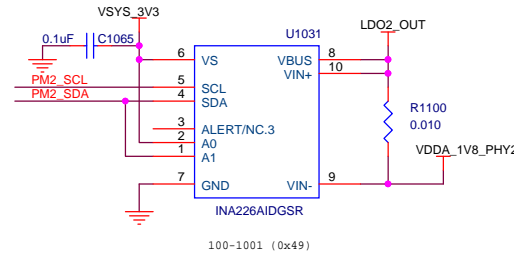
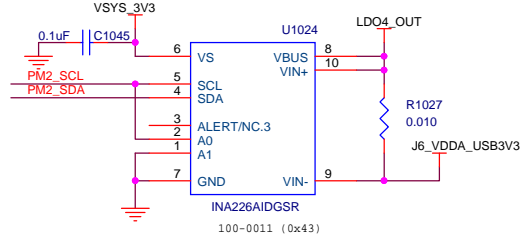
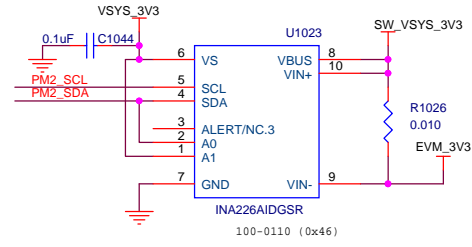
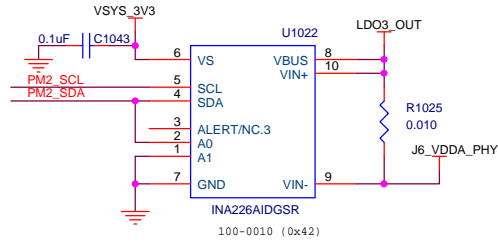
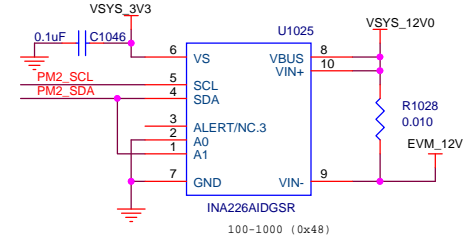
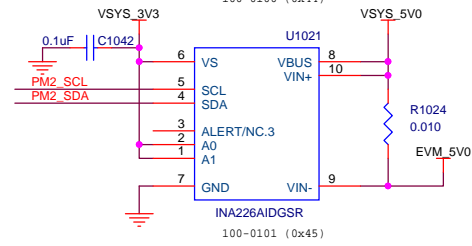
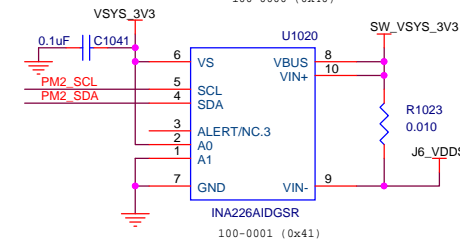
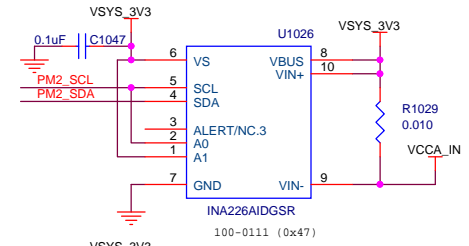
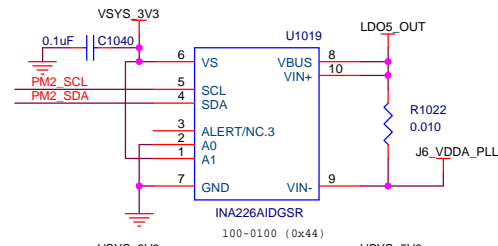
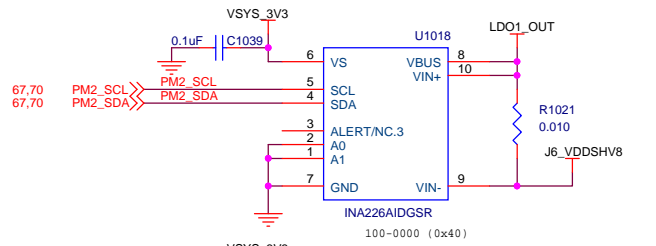
POSSIBLE ISSUE USING VRTC DOMAIN I/O. DO WE NEED TO ISOLATE.

TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: PMIC			
Size: B	DOC NO: 517502	REV: D	
Date: Tuesday, November 08, 2016	Sheet 67	of	71



TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board		
Page Contents: POWER MONITOR 1		
Size: B	DOC NO: 517502	REV: C
Date: Tuesday, November 08, 2016	Sheet 68	of 71



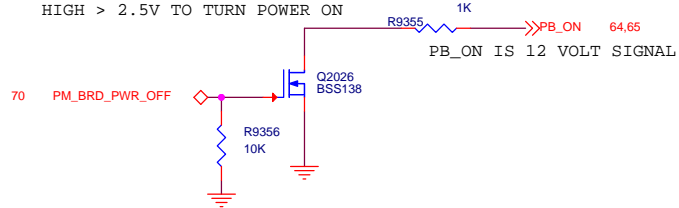
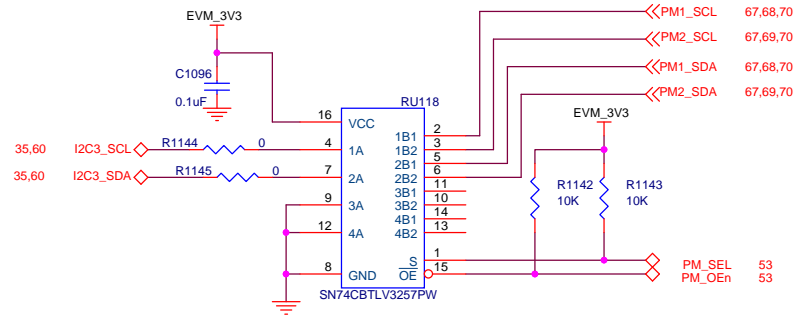
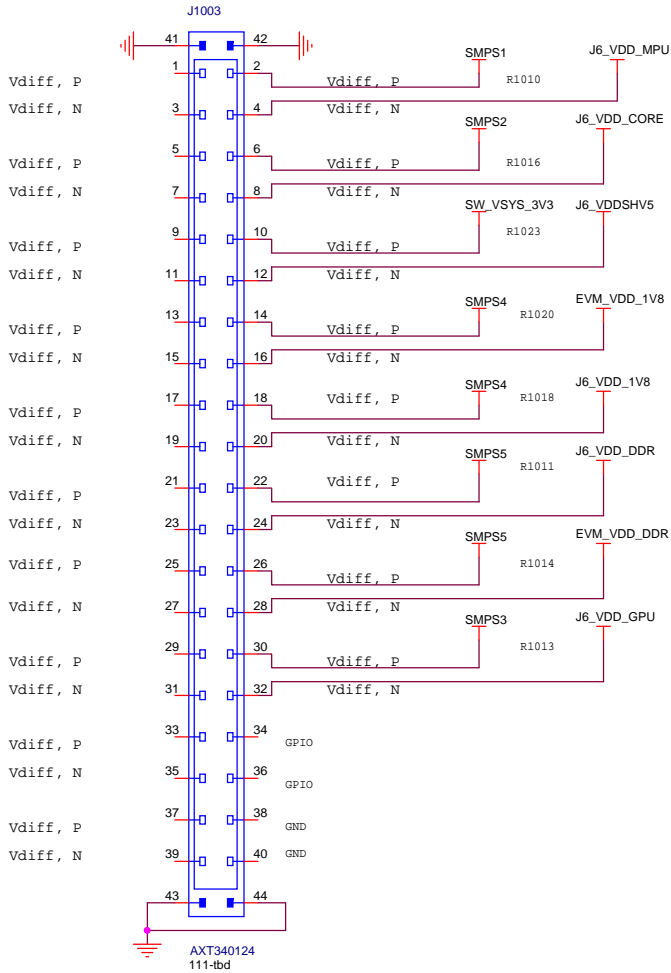
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA72x/TA2AEx EVM CPU Board			
Page Contents: POWER MONITOR 2			
Size: B	DOC NO: 517502	REV: C	
Date: Tuesday, November 08, 2016	Sheet 69	of	71

ER21

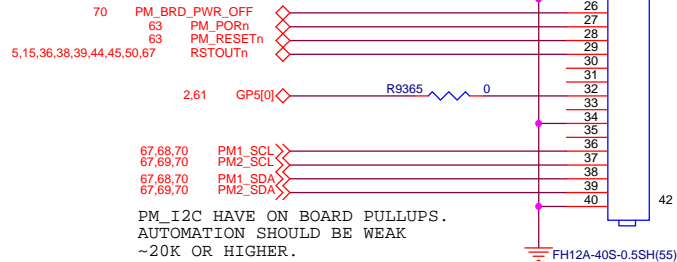
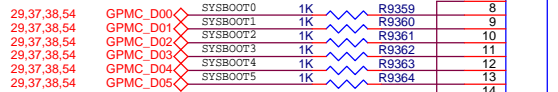
DARA Bd Interface Connector

DARA Bd can be interfaced to conduct more in-depth power measurements.

All Vdiff signal pairs (P & N) shown should be routed as pseudo-Diff Pair segments using min trace widths since these are low voltage sensing nets, not power delivery nets.



BOOT SWITCHES SHOULD BE SET TO OFF FOR PULLDOWNS. AUTOMATION WILL DRIVE HIGH TO OVERRIDE.



ER22

AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

TEXAS INSTRUMENTS INCORPORATED

Title: DRA72x/TA2Ex EVM CPU Board		
Page Contents: POWER MONITOR 1		
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ECN Number 517500-E002
 Date Requested 11/10/2015
 Requester Tony C.
 Approvals Tony C.
 Assembly Number 516680-0001
 Current Assembly Rev B1
 New Assembly Rev C
 Date Implemented 01/06/2016

Implementation notes To many bom changes to list all individually. Diff Rev B1 and C boms for complete details.

Item#	Init Date	Priority	Status	Description
ER1				ASSY FROM B1 TO C ASSY FROM B1 TO C ASSY FROM B1 TO C
ER1				Upgrade J6 ECO Processor to ES 2.0 V52 From 104492-0001R-TI to 104492-0002R-TI
ER3				Create new J6 ECO part # 104492-0002R-TI IC_BGA_J6 ECO PROCESSOR GP_ES2.0 XDR426B8GABC
ER3				Sheet 24, 25 Update memory to 2GB total U115, U116, U68, U69, U67 From 104177-0125R TO 104895-0125R MFA14512A10PH-325-M4 E U10
ER4				Change Boot voltages for MPUICORE to 1.15V
ER5				Sheet 10, 13, 69 VDDA_PHY rail measurements exceeds LDO ratings Create new power net with current monitor LDO2_OUT - VDDA_1V8_PHY2 I2c Address 0x49 ADD C1065, 0 1uF, 101587-1100R ADD R1100, 0.010, 102590-0001R ADD U1031, INA226ADGSR_103928-0001R
ER6				Sheet 39 Update MMC2_DAT10 0JCMD Pullups with 47k R424, R425, R426, R414, R422, R423, R425, R428 From R0402-NOPOP to 101370-4703R R410, R417 From 102145-4993R to 101370-4703R
ER7				Sheet 40 Update SD Data3 0JCMD to 47k R19, R18, R16, R15, R14 From 101370-1003R to 101370-4703R
ER8				Sheet 14 Add pull-up to TMS (silicon does not include PU or PD, so floating) Add R629, 4.7k, 101370-4702R Change R758 From 0 to 100 From 101370-0001R to 101370-1001R This limits current into VREF with LasterBauch adapter plugged in backwards.
ER9				Sheet 66 Investigate Power sequence of ENET MAC (core before IO) Change the 2.5V PHY power sequence to track EVM_3V3 as recommended in not 7.17 of the datasheet Add C785 101030-0220R, 2.2uF Add R11 101370-4702R, 4.7k Add R832, 100642-1073R, 10.7k Change C19 from 102058-1102R to d0402-nopop NOTE: ER9, ER14 AND ER23 ARE UPDATED TO SWITCH TO NEW PHY.
ER10				Sheet 27 Move DDR termination (net DDR2_CKE) to discrete resistor (so can be populated for Suspend to RAM) Add R1101, 36, 102145-3600R

ER11 Fix CS2_0 routing (Reference Layer 9 has split plane)

ER12 Sheet 67
Voltage divider for PMC GPIO_6NSLEEP (1.74k series, 2k pull-down)
Add R589, 2K, 103158-2002R
Add R797, 1.74K, 102145-1742R

ER13 Sheet 64
Update reverse battery protection to TI smart diode solution using LM74610
U6 From 103038-0001R To 104635-0001R
Q5 From 103998-0001R To 104263-0001R
ADD C706 101415-0220R
ADD C707 103895-1220R
ADD D1 101808-0020R
ADD D2 101808-0014R
ADD TR931 TP-18R06-NO-POP

ER14 Sheet 57, 58
Ethernet PHY core 1.5V leakage to 3.3V rail. Use load switch and duplicate power up circuitry used on 3.3V supply so it can be adjusted independently.
ADD C708 00603-NOPOP
C709 100993-1220R
R833 100642-1073R
R12 101370-4702R
U145 104267-0001R
NOTE: ER9, ER14 AND ER23 ARE UPDATED TO SWITCH TO NEW PHY.

ER15 Sheet 68,69
Current measurement R changes to 10mOhm
R1024 Fm. 104445-0001R To 102598-0001R
R1026 Fm. 104445-0001R To 102598-0001R
R1028 Fm. 104297-0002R To 102598-0001R
R1029 Fm. 104444-0005R To 102598-0001R
R1010 Fm. 104445-0001R To 102598-0001R
R1013 Fm. 104445-0001R To 102598-0001R
R1016 Fm. 104297-0002R To 102598-0001R
R1012 Fm. 104444-0005R To 102598-0001R
R1014 Fm. 104444-0005R To 102598-0001R
R1017 Fm. 104444-0005R To 102598-0001R
R1018 Fm. 104444-0005R To 102598-0001R
R1011 Fm. 104444-0005R To 102598-0001R
R1015 Fm. 104444-0005R To 102598-0001R
R1019 Fm. 104444-0005R To 102598-0001R

ER16 PB free marking in silk screen

ER17 FCC marking in silk screen. *For evaluation only, not FCC approved for res

ER18 Sheet 66
REG_EN pullups voltage to SMPS4

ER19 See TI input

ER20 Sheet 66
CS1 change to 25V cap from 16 V on 12 V input
FROM 101290-0102R TO 104700-0102R

ER21 Sheet 70
Add DARA power measurement
J1003 - 104610-0040R

ER22 See TI input

ER23 Sheet 57, 58, 59
Migrate to DR9367R PHY

ER24 NA - UPDATE 7000X TOP LEVELS

ER25 Sheet 48
Remove unneeded pullup/pulldown on HDMI signals. These are included in the TPDI23018R-KTR device
R6, R7 From 101370-2202R to d0402-nopop
R305 From 103158-1003R to d001-nopop

Update Update part body of SN74AVCB245RH devices. Layout only change to improve mfg

ECN Number 517500-E002
 Date Requested 04/28/2016
 Requester Tony C.
 Approvals Tony C.
 Assembly Number 517500-0001
 Current Assembly Rev C1
 New Assembly Rev D
 Date Implemented 5/17/2016

Implementation notes

Item#	Init Date	Priority	Status	Description
1				LOGIC FROM C1 TO D PWB FROM C TO D ASSY FROM C1 TO D
2				Sheet 32 Change R0001 musing, change RU116 TYPE all of EMAC 1 is not muxed through R493 RU115 FROM 101670-0001R TO 101433-0001R FROM SN74CBTLV3257PW TO SN74CBTLV3253
3				Sheet 58 and 59 Remove all series R on RX line to improve routing. Z control can be done in the PHY. REMOVE R1130,R1131,R117,R437,R438,R111
4				Sheet 67 Change PMIC version U1001 FROM 104443-0002R-TI TO 104443-0003R-TI FROM P0917A13DTRGZR01 TO P0917A13DTRGZR01
5				Create new PMIC part # 104443-0003R-TI, P0917A13DTRGZR01
6				Sheet 67 Change PMIC boot mode from low to high R516 FROM r0201-nopop TO 103158-0001R R483 FROM 103158-0001R TO r0201-nopop
6				Sheet 11 Change LCD_PCLK series term for better clock at 100pp R596 From 22 ohm, 103158-2200R to 0 ohm, 103158-0001R

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