DRV2511-Q1 8A車載用、ソレノイドおよび音声コイル用ハプティック・ドライバ

1 特長

- 広い動作電圧範囲(4.5V〜26V)
- 30Vの電圧を処理可能
- 高い電流ドライブ(8Aピーク)
- 低いRDS(on)、完全なHブリッジ出力
- フォルト保護機能内蔵
  - 短絡保護
  - 過熱保護
  - 過電圧および低電圧保護
  - 障害通知
- アナログ入力
- 専用の割り込みピン
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード1: 動作時周囲温度範囲
    - -40℃〜125℃
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC4B

2 アプリケーション

- 電磁気アクチュエータ・ドライバ
  - 音声コイル
  - ソレノイド
- 機械式ボタンの置き換え
- 車載用ハプティック・アプリケーション
  - インフォテインメント
  - 中央コンソール
  - ステアリング・ホイール
  - ドア・パネル
  - シート

3 概要

このDRV2511-Q1デバイスは、大電流のハプティック・ドライバで、ソレノイドや音声コイルなど誘導性の負荷に特化して設計されています。

出力ステージは、完全なHブリッジで構成され、8Aのピーク電流を供給できます。

DRV2511-Q1デバイスは、低電圧誤動作防止、過電流保護、過熱保護などの保護機能を備えています。

このDRV2511-Q1デバイスは車載用に認定済みです。

製品情報(1)

<table>
<thead>
<tr>
<th>型番</th>
<th>パッケージ</th>
<th>本体サイズ(公称)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV2511-Q1</td>
<td>HTSSOP (32)</td>
<td>11 mm x 6.20 mm</td>
</tr>
</tbody>
</table>

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図

(Solenoid/ Voice-Coil)
目次

1 特長................................................................. 1
2 アプリケーション................................................. 1
3 概要................................................................. 1
4 改訂履歴.......................................................... 2
5 Pin Configuration and Functions.......................... 3
6 Specifications.................................................... 4
   6.1 Absolute Maximum Ratings.......................... 4
   6.2 ESD Ratings.................................................. 4
   6.3 Recommended Operating Conditions................ 4
   6.4 Thermal Information...................................... 4
   6.5 Electrical Characteristics............................ 6
   6.6 Switching Characteristics............................. 6
   6.7 Typical Characteristics............................... 7
7 Detailed Description ......................................... 8
   7.1 Overview................................................... 8
   7.2 Functional Block Diagram.............................. 8
7.3 Feature Description........................................... 9
7.4 Device Functional Modes.................................... 11
7.5 Programming.................................................. 11
8 Application and Implementation.......................... 12
   8.1 Application Information............................... 12
   8.2 Typical Applications..................................... 12
9 Power Supply Recommendations............................ 16
10 Layout............................................................ 16
   10.1 Layout Guidelines....................................... 16
   10.2 Layout Example.......................................... 16
11 デバイスおよびドキュメントのサポート.................. 17
   11.1 デバイス・サポート...................................... 17
   11.2 商標....................................................... 17
   11.3 静電気放電に関する注意事項........................... 17
   11.4 Glossary.................................................. 17
12 メカニカル、パッケージ、および注文情報................... 18

4 改訂履歴
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年6月発行のものから更新

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

• 量産データとしてリリース ........................................
5 Pin Configuration and Functions

DAP Package
32-Pin HTSSOP
Top View

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>1, 9, 10, 11, 22, 25, 28</td>
<td>P</td>
</tr>
<tr>
<td>EN</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>INTZ</td>
<td>3</td>
<td>O</td>
</tr>
<tr>
<td>IN+</td>
<td>4</td>
<td>I</td>
</tr>
<tr>
<td>IN-</td>
<td>5</td>
<td>I</td>
</tr>
<tr>
<td>REG</td>
<td>6, 7</td>
<td>P</td>
</tr>
<tr>
<td>GAIN</td>
<td>8</td>
<td>I</td>
</tr>
<tr>
<td>STDBY</td>
<td>12</td>
<td>I</td>
</tr>
<tr>
<td>FS2</td>
<td>13</td>
<td>I</td>
</tr>
<tr>
<td>FS1</td>
<td>14</td>
<td>I</td>
</tr>
<tr>
<td>FS0</td>
<td>15</td>
<td>I</td>
</tr>
<tr>
<td>N/C</td>
<td>16</td>
<td>N/C</td>
</tr>
<tr>
<td>AVDD</td>
<td>17</td>
<td>P</td>
</tr>
<tr>
<td>PVDD</td>
<td>18, 19, 31, 32</td>
<td>P</td>
</tr>
<tr>
<td>BSTN</td>
<td>20, 24</td>
<td>P</td>
</tr>
<tr>
<td>OUT-</td>
<td>21, 23</td>
<td>O</td>
</tr>
<tr>
<td>BSTP</td>
<td>26, 30</td>
<td>P</td>
</tr>
</tbody>
</table>
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT+</td>
<td>O</td>
<td>Positive output.</td>
</tr>
<tr>
<td>Thermal Pad or PowerPAD™</td>
<td>G</td>
<td>Connect to GND for best system performance. If not connected to GND, leave floating.</td>
</tr>
</tbody>
</table>

### 6 Specifications

#### 6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>PVDD, AVDD</td>
<td>−0.3</td>
</tr>
<tr>
<td>Input voltage, $V_i$</td>
<td>IN+, IN−</td>
<td>−0.3</td>
</tr>
<tr>
<td></td>
<td>GAIN</td>
<td>−0.3</td>
</tr>
<tr>
<td></td>
<td>EN</td>
<td>−0.3</td>
</tr>
<tr>
<td>Current</td>
<td>DC current on PVDD, GND, OUT+, OUT−</td>
<td>−8</td>
</tr>
<tr>
<td>Operating free-air temperature, $T_A$</td>
<td>−40</td>
<td>125</td>
</tr>
<tr>
<td>Storage temperature range, $T_{stg}$</td>
<td>−50</td>
<td>150</td>
</tr>
</tbody>
</table>

---

*(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

#### 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins$^{(1)}$</td>
<td>−2000</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins$^{(2)}$</td>
<td>−450</td>
</tr>
</tbody>
</table>

---

*(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

*(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.*

#### 6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage. PVDD, AVDD.</td>
<td>4.5</td>
<td>26</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High-level input voltage. STDBY, EN, FS0, FS1, FS2.</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low-level input voltage. STDBY, EN, FS0, FS1, FS2.</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage. INTZ, $R_{PULL-UP} = 100$ kΩ, PVDD = 26 V.</td>
<td>0.8</td>
<td>50</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High-level input current. STDBY, EN, FS0, FS1, FS2. ($V_i = 2$ V, PVDD = 26 V).</td>
<td>1.65</td>
<td></td>
</tr>
<tr>
<td>$R_L$</td>
<td>Minimum load Impedance.</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$L_o$</td>
<td>Output-filter Inductance.</td>
<td>32.4</td>
<td></td>
</tr>
</tbody>
</table>

#### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>DRV2511-Q1</th>
<th>DAP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>32.4</td>
<td>32 PINS</td>
</tr>
<tr>
<td>$R_{JUC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>17.2</td>
<td></td>
</tr>
</tbody>
</table>

---

*(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.*
## Thermal Information (continued)

<table>
<thead>
<tr>
<th>THERMAL METRIC[^1]</th>
<th>DRV2511-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{UB}$ Junction-to-board thermal resistance</td>
<td>17.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>0.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>17.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>1</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

[^1]: (1)
## 6.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$, $AVCC = PVDD = 12\ \text{V}$, $R_L = 5\ \Omega$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>V_{OS}</td>
<td>$</td>
<td>Output offset voltage (measured differentially) $V_I = 0\ \text{V}$, Gain = 36 dB</td>
<td>1.5</td>
<td>15</td>
</tr>
<tr>
<td>$I_{VDD}$</td>
<td>Quiescent supply current</td>
<td>No load or filter</td>
<td>20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{VDD(SD)}$</td>
<td>Quiescent supply current in shutdown mode</td>
<td>No load or filter</td>
<td>35</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{VDD(STD\ BY)}$</td>
<td>Quiescent supply current in standby mode</td>
<td>No load or filter</td>
<td>11</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$r_{DS(on)}$</td>
<td>Drain-source on-state resistance, measured pin to pin $T_J = 25^\circ\text{C}$</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>mΩ</td>
</tr>
<tr>
<td>$G$</td>
<td>Gain $R_1 = \text{open, } R_2 = 20\ \text{k} \Omega$</td>
<td>25</td>
<td>26</td>
<td>27</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$R_1 = 100\ \text{k} \Omega, R_2 = 20\ \text{k} \Omega$</td>
<td>31</td>
<td>32</td>
<td>33</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$R_1 = 100\ \text{k} \Omega, R_2 = 47\ \text{k} \Omega$</td>
<td>35</td>
<td>36</td>
<td>37</td>
<td>dB</td>
</tr>
<tr>
<td>$V_{REG}$</td>
<td>Regulator voltage</td>
<td>6.4</td>
<td>6.9</td>
<td>7.4</td>
<td>V</td>
</tr>
<tr>
<td>$BW$</td>
<td>Full Power Bandwidth</td>
<td>60</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Output voltage (measured differentially) $\text{Measured at PVDD = 26}\text{V}$</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power supply ripple rejection</td>
<td>200 mVpp ripple at 1 kHz, Gain = 20 dB</td>
<td>−70</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common-mode rejection ratio</td>
<td>−56</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>Oscillator frequency (with PWM duty cycle &lt; 96%) $FS2 = 0, FS1 = 0, FS0 = 0$</td>
<td>376</td>
<td>400</td>
<td>424</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$FS2 = 0, FS1 = 0, FS0 = 1$</td>
<td>470</td>
<td>500</td>
<td>530</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$FS2 = 0, FS1 = 1, FS0 = 0$</td>
<td>564</td>
<td>600</td>
<td>636</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$FS2 = 0, FS1 = 1, FS0 = 1$</td>
<td>940</td>
<td>1000</td>
<td>1060</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$FS2 = 1, FS1 = 0, FS0 = 0$</td>
<td>1128</td>
<td>1200</td>
<td>1278</td>
<td>kHz</td>
</tr>
<tr>
<td>Power-on threshold</td>
<td></td>
<td>4.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Power-off threshold</td>
<td></td>
<td>28</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Thermal trip point</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal hysteresis</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Over-current trip point</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Over-voltage trip point</td>
<td></td>
<td>28</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on-sd}$</td>
<td>Turn-on time from shutdown to waveform</td>
<td>10</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{OFF-sd}$</td>
<td>Turn-off time</td>
<td>5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{on-stby}$</td>
<td>Turn-on time from standby to waveform</td>
<td>6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

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6.7 Typical Characteristics

<table>
<thead>
<tr>
<th>VDD - Supply Voltage (V)</th>
<th>Shutdown Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>10.0</td>
</tr>
<tr>
<td>6</td>
<td>15.0</td>
</tr>
<tr>
<td>8</td>
<td>20.0</td>
</tr>
<tr>
<td>10</td>
<td>25.0</td>
</tr>
<tr>
<td>12</td>
<td>30.0</td>
</tr>
<tr>
<td>14</td>
<td>35.0</td>
</tr>
<tr>
<td>16</td>
<td>40.0</td>
</tr>
<tr>
<td>18</td>
<td>45.0</td>
</tr>
<tr>
<td>20</td>
<td>50.0</td>
</tr>
<tr>
<td>22</td>
<td>55.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VDD - Supply Voltage (V)</th>
<th>Standby Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>12.00</td>
</tr>
<tr>
<td>6</td>
<td>14.00</td>
</tr>
<tr>
<td>8</td>
<td>16.00</td>
</tr>
<tr>
<td>10</td>
<td>18.00</td>
</tr>
<tr>
<td>12</td>
<td>20.00</td>
</tr>
<tr>
<td>14</td>
<td>22.00</td>
</tr>
<tr>
<td>16</td>
<td>24.00</td>
</tr>
<tr>
<td>18</td>
<td>26.00</td>
</tr>
<tr>
<td>20</td>
<td>28.00</td>
</tr>
</tbody>
</table>

[图 1. Shutdown Current vs VDD Voltage][1]  [图 2. Standby Current vs VDD Voltage][2]

[1] DRV2511-Q1 www.tij.co.jp


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7 Detailed Description

7.1 Overview
The DRV2511-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 8 A of peak current.

The design uses an ultra-efficient switching output technology developed by Texas Instruments, but with features added for the automotive industry. The DRV2511-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system.

The DRV2511-Q1 device is automotive qualified.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Analog Input and Configurable Pre-amplifier

The DRV2511-Q1 device features a differential input stage that cancels common-mode noise that appears on the inputs. The DRV2511-Q1 device also features four gain settings that are configurable via external resistors.

表1. Gain Configuration Table

<table>
<thead>
<tr>
<th>GAIN</th>
<th>R1</th>
<th>R2</th>
<th>INPUT IMPEDANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 dB</td>
<td>5.6 kΩ</td>
<td>open</td>
<td>60 kΩ</td>
</tr>
<tr>
<td>26 dB</td>
<td>20 kΩ</td>
<td>100 kΩ</td>
<td>30 kΩ</td>
</tr>
<tr>
<td>32 dB</td>
<td>39 kΩ</td>
<td>100 kΩ</td>
<td>15 kΩ</td>
</tr>
<tr>
<td>36 dB</td>
<td>47 kΩ</td>
<td>75 kΩ</td>
<td>9 kΩ</td>
</tr>
</tbody>
</table>

图3. Gain Configuration

7.3.2 Pulse-Width Modulator (PWM)

The DRV2511-Q1 device features BD modulation scheme with high bandwidth, low noise, low distortion, and excellent stability.

The BD modulation scheme allows for smaller ripple currents through the load. Each output switches from 0 V to the supply voltage. With no input, the OUT+ and OUT- pins are in phase with each other so that there is little or no current in the load. For positive differential inputs, the duty cycle of OUT+ is greater than 50% and the duty cycle of OUT- is lower than 50% for a positive differential output voltage. The opposite is true for negative differential inputs. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces the $I^2R$ losses in the load.
### 7.3.3 Designed for low EMI

The DRV2511-Q1 device design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that causes EMI. Follow the recommended design requirements in the *Design Requirements* section.

### 7.3.4 Device Protection Systems

The DRV2511-Q1 device features a complete set of protection circuits carefully designed to protect the device against permanent failures due to shorts, over-temperature, over-voltage, and under-voltage scenarios. The INTZ pin signals if an error is detected.
### 2. Fault Reporting Table

<table>
<thead>
<tr>
<th>FAULT</th>
<th>TRIGGERING CONDITION</th>
<th>INTZ</th>
<th>ACTION</th>
<th>LATCH?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over-current</td>
<td>Output short or short to PVDD or GND</td>
<td>pulled low</td>
<td>output in high impedance</td>
<td>Latched</td>
</tr>
<tr>
<td>Over-temperature</td>
<td>$T_j &gt; 150 \degree C$</td>
<td>pulled low</td>
<td>output in high impedance</td>
<td>Latched</td>
</tr>
<tr>
<td>Under-voltage</td>
<td>PVDD &lt; 4.5 V</td>
<td>-</td>
<td>output in high impedance</td>
<td>Self-clearing</td>
</tr>
<tr>
<td>Over-voltage</td>
<td>PVDD &gt; 27 V</td>
<td>-</td>
<td>output in high impedance</td>
<td>Self-clearing</td>
</tr>
</tbody>
</table>

When the "Latched" conditions happen, the device must be reset with the EN signal in order to clear the fault. If automatic recovery from these conditions is desired, connect the INTZ pin directly to the EN pin. This allows the INTZ pin function to automatically drive the EN pin low which clears the latched condition.

### 7.4 Device Functional Modes

The DRV2511-Q1 device has multiple power states to optimize power consumption.

#### 7.4.1 Operation in Shutdown Mode

The NRST pin of the DRV2511-Q1 device puts the device in a shutdown mode. When NRST is asserted (logic low), all internal blocks of the device are off to achieve ultra low power.

#### 7.4.2 Operation in Standby Mode

The STDBY pin of the DRV2511-Q1 device puts the device in a standby mode. When STDBY is asserted (logic high), some internal blocks of the device are off to achieve low power while preserving the ability to wake up quickly to achieve low latency waveform playback.

#### 7.4.3 Operation in Active Mode

The DRV2511-Q1 device is in active mode when it has a valid supply, and it is not in either shutdown or standby modes. In this mode the DRV2511-Q1 device is fully on and reproducing at the output the input times the gain.

### 7.5 Programming

#### 7.5.1 Gain

The DRV2511-Q1 device has a configurable gain that is controlled through external resistors. Please see the Analog Input and Configurable Pre-amplifier section for more details.
8 Application and Implementation

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The DRV2511-Q1 device is a high-efficiency driver for inductive loads, such as solenoids and voice-coils. The typical use of the device is on haptic applications where short, strong waveforms are desired to create a haptic event that will be coming from the application processor.

8.2 Typical Applications

8.2.1 Single-Ended Source
To use the DRV2511-Q1 with a single-ended source, apply either a voltage divider to bias INB to 3 V, tie to GND or use a 0.1-μF cap from INB to GND to have the device self bias. Apply the single-ended signal to the INA pin.

8.2.1.1 Design Requirements
For most applications the following component values found in 表 3 below can be used.

![Typical Application Schematic](image-url)
Typical Applications (continued)

### Table 3. Component Requirements Table

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>DESCRIPTION</th>
<th>SPECIFICATION</th>
<th>TYPICAL VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>Supply capacitor</td>
<td>Capacitance</td>
<td>22 µF and 0.1 µF for PVDD &amp; AVDD</td>
</tr>
<tr>
<td>C2/C3</td>
<td>Boost capacitor</td>
<td>Capacitance</td>
<td>0.22 µF</td>
</tr>
<tr>
<td>C4/C5</td>
<td>Output snubber capacitor</td>
<td>Capacitance</td>
<td>470 pF</td>
</tr>
<tr>
<td>C6</td>
<td>Regulator capacitor</td>
<td>Capacitance</td>
<td>1 µF</td>
</tr>
<tr>
<td>C9</td>
<td>Input decoupling capacitor</td>
<td>Capacitance</td>
<td>0.1 µF</td>
</tr>
<tr>
<td>R1/R2</td>
<td>Output snubber resistor</td>
<td>Resistance</td>
<td>3.3 Ω</td>
</tr>
<tr>
<td>R(\text{P(U)})</td>
<td>Pull-up resistor</td>
<td>Resistance</td>
<td>100 kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### 8.2.1.2 Detailed Design Procedure

##### 8.2.1.2.1 Optional Components

Note that in the diagrams, there are a few optional external components. These optional external components may be needed in the application to meet EMI/EMC standards and specifications by filters necessary frequency spectrums.

##### 8.2.1.2.2 Capacitor Selection

A bulk bypass capacitor should be mounted between VBAT and GND. The capacitance needs to be >22 µF with a X5R or better rating on the power pins to GND. Also include two ceramic capacitors in the ranges of 220 pF to 1 µF and 100 nF to 1 µF. The bootstrap capacitors, BSTA and BSTB, should be 220-nF ceramic capacitors of quality X5R or better rated for at least the maximum rating of the pin.

##### 8.2.1.2.3 Solenoid Selection

The DRV2511-Q1 solenoid driver can accommodate a variety of solenoids. Solenoids should have an equivalent resistance of 1.6 Ω or greater. Solenoids with lower resistances are prone to driving high currents. A maximum peak current of 8-A should not be exceeded. The DRV2511-Q1 will go into a shutdown mode to protect itself from overcurrent.

##### 8.2.1.2.4 Output Filter Considerations

The output filter is optional and is mainly for limiting peak currents. A second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See 式 2, 式 3, and 式 4 for example filter design.

\[
H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \quad (1)
\]

\[
L_x = \frac{\sqrt{2} \times R_L}{2 \omega_0} \quad (2)
\]

\[
2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{\omega_0}} \quad (3)
\]

\[
\omega_0 = 2\pi \times f \quad (4)
\]

### 8.2.1.3 Application Curves

These application curves were taken using an HA200 solenoid with a 100-g mass, and the acceleration was measured using the DRV-AAC16-EVM accelerometer. The following scales apply to the graphs:

- Output Differential Voltage scale is shown on the plots at 5-V/div
- Acceleration scale is 5.85-G/div
- Current scale is 2-A/div
8.2.1.4 Differential Input Diagram

To use the DRV2511-Q1 with a differential input source, apply both inputs differentially from a control source (GPIO, DAC, etc...).
图 10. Typical Application Schematic
9 Power Supply Recommendations

The DRV2511-Q1 device operates from 4.5 V - 26 V and this supply should be able to handle high surge currents in order to meet the high current draws for haptics effects. Additionally the DRV2511-Q1 should have 22-µF and 0.1-µF ceramic capacitors near the PVDD & AVDD pins for additional decoupling from trace routing.

10 Layout

10.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The DRV2511-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. It is best practice to use the same/similar layout as shown below in the DRV2511Q1EVM.

10.2 Layout Example

![Driver 2511 Q1 EVM Diagram](image)
11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.4 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.
12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV2511QDAPRQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>DAP</td>
<td>32</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>DRV2511Q</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

![Diagram of reel dimensions and tape dimensions](image)

## TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

## PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV2511QDAPRQ1</td>
<td>HTSSOP</td>
<td>DAP</td>
<td>32</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>8.6</td>
<td>11.5</td>
<td>1.6</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV2511QDAPRQ1</td>
<td>HTSSOP</td>
<td>DAP</td>
<td>32</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, for information regarding recommended board layout. This document is available at www.ti.com (http://www.ti.com).

⚠ Falls within JEDEC MO-153 Variation DCT.

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THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters

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