DRV8872-Q1 オートモーティブ、3.6Aブラシ付きDCモータ・ドライバ、エラー報告機能付き

1 特長

- 車載アプリケーション用にAEC-Q100認定済み:
  - デバイス温度グレード1: 動作時周囲温度範囲 -40℃ 〜 +125℃
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4B
- Hブリッジ・モータ・ドライバ
  - 1台のDCモータ、ステッピングモータの1つの巻線、またはその他の負荷を駆動
- 6.8V〜45Vの広い動作電圧範囲
- 標準値565mΩの直流オン抵抗(ハイサイドとローサイド)
- 3.6Aのピーク駆動電流
- PWM制御インターフェイス
- 電流レギュレーション機能を内蔵
- 低電力スリープ・モード
- エラー状態出力ピン
- 小さなパッケージと占有面積
  - 8ピンHSOP: PowerPAD™
  - 4.9 × 6 mm
- 保護機能を内蔵
  - VM低電圧誤動作防止(UVLO)
  - 過電流保護(OCP)
  - サーマル・シャットダウン(TSD)
  - エラー報告機能(nFAULT)
  - エラーからの自動復旧

2 アプリケーション

- 車載インフォテインメント
- HUDプロジェクタの調整
- 電動シフター・ノブ
- 圧電型ホーン・ドライバ

概略回路図

3 概要

DRV8872-Q1デバイスは、情報エンターテインメント、HUDプロジェクタの調整、電動シフター・ノブ、圧電型ホーン・ドライバ向けのブラシ付きDC (BDC)モータ・ドライバです。2つのロジック入力がHブリッジドライバを制御します。ドライバは4つのnチャネルMOSFETを装備し、最大ピーク電流3.6Aまでのモータを双方向制御します。入力をパルス幅変調(PWM)し電流減衰モードを選択してモータ回転数を制御できます。両方の入力を“L”にすると低消費電力スリープ・モードになります。

DRV8872-Q1デバイスは、内部基準電圧またはISENピンの電圧を基準にできる電流レギュレーション機能を内蔵しており、ISENピンには、外付けの検出抵抗器を通るモータ電流に比例した電圧が印加されます。電流を既知のレベルに制限できるため、システムに必要な電力を大幅に低減でき、特にモータの始動時や失速時に安定した電圧を維持するのに必要なパルク容量も低減できます。

デバイスは、低電圧誤動作防止(UVLO)、過電流保護(OCP)、サーマル・シャットダウン(TSD)などの機能によりエラー状態から完全に保護されています。エラーの場合は、nFAULT出力が“L”になることで通知されます。エラー状態が解消されると、デバイスは自動的に通常動作状態に復帰します。

製品情報

<table>
<thead>
<tr>
<th>型番</th>
<th>パッケージ</th>
<th>本体サイズ(公称)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8872-Q1</td>
<td>HSOP (8)</td>
<td>4.90mm×6.00mm</td>
</tr>
</tbody>
</table>

(1) 提供されているすべてのパッケージについては、巻末の注文情報に参照してください。
目次

1 特長 ........................................................................ 1
2 アプリケーション .................................................... 1
3 概要 ......................................................................... 1
4 改訂履歴 .................................................................. 2
5 Pin Configuration and Functions ............................. 3
6 Specifications ......................................................... 3
   6.1 Absolute Maximum Ratings ............................... 3
   6.2 ESD Ratings ....................................................... 4
   6.3 Recommended Operating Conditions ................. 4
   6.4 Thermal Information ........................................... 4
   6.5 Electrical Characteristics .................................. 5
   6.6 Typical Characteristics ..................................... 6
7 Detailed Description .................................................. 7
   7.1 Overview .......................................................... 7
   7.2 Functional Block Diagram .................................. 7
   7.3 Feature Description ............................................ 8
   7.4 Device Functional Modes ................................. 10
8 Application and Implementation ............................ 11
   8.1 Application Information ..................................... 11
   8.2 Typical Application ........................................... 11
9 Power Supply Recommendations ........................... 14
   9.1 Bulk Capacitance .............................................. 14
10 Layout .................................................................... 15
   10.1 Layout Guidelines ............................................ 15
   10.2 Layout Example ............................................... 15
   10.3 Thermal Considerations .................................... 15
   10.4 Power Dissipation ............................................ 15
11 デバイスおよびドキュメントのサポート .................. 17
   11.1 ドキュメントのサポート ................................ 17
   11.2 ドキュメントの更新通知を受け取る方法 .......... 17
   11.3 コミュニティ・リソース ................................ 17
   11.4 商標 .......................................................... 17
   11.5 静電気放電に関する注意事項 ........................... 17
   11.6 用語集 ....................................................... 17
12 メカニカル、パッケージ、および注文情報 ............. 17

4 改訂履歴
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<table>
<thead>
<tr>
<th>日付</th>
<th>改訂内容</th>
<th>注</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016年11月</td>
<td>*</td>
<td>初版</td>
</tr>
</tbody>
</table>

Copyright © 2016, Texas Instruments Incorporated
5 Pin Configuration and Functions

DDA Package
8-Pin HSOP With Exposed Thermal Pad
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>PWR</td>
<td>Logic ground</td>
</tr>
<tr>
<td>IN1</td>
<td>I</td>
<td>Logic inputs</td>
</tr>
<tr>
<td>IN2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>ISEN</td>
<td>PWR</td>
<td>High-current ground path</td>
</tr>
<tr>
<td>nFAULT</td>
<td>OD</td>
<td>Fault status (open-drain)</td>
</tr>
<tr>
<td>OUT1</td>
<td>O</td>
<td>H-bridge outputs</td>
</tr>
<tr>
<td>OUT2</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>VM</td>
<td>PWR</td>
<td>6.8-V to 45-V power supply</td>
</tr>
<tr>
<td>PAD</td>
<td>—</td>
<td>Thermal pad</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage (VM)</td>
<td>−0.3</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>Logic input voltage (IN1, IN2)</td>
<td>−0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Fault pin (nFAULT)</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Continuous phase node pin voltage (OUT1, OUT2)</td>
<td>−0.7</td>
<td>VM + 0.7</td>
<td>V</td>
</tr>
<tr>
<td>Current sense input pin voltage (ISEN)(^{(2)})</td>
<td>−0.5</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Output current (100% duty cycle)</td>
<td>3.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Transients of ±1 V for less than 25 ns are acceptable.
6.2 ESD Ratings

<table>
<thead>
<tr>
<th>V_{(ESD)}</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per AEC Q100-002&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±500</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>All pins</td>
<td>±750</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Corner pins (1, 4, 5, and 8)</td>
<td>±750</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>Power supply voltage</td>
<td>6.8</td>
<td>45</td>
</tr>
<tr>
<td>V_I</td>
<td>Logic input voltage (IN1, IN2)</td>
<td>0</td>
<td>5.5</td>
</tr>
<tr>
<td>f_{PWM}</td>
<td>Logic input PWM frequency (IN1, IN2)</td>
<td>0</td>
<td>200&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>I_{peak}</td>
<td>Peak output current&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>0</td>
<td>3.6</td>
</tr>
<tr>
<td>T_A</td>
<td>Operating ambient temperature</td>
<td>−40</td>
<td>125</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400 ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.

<sup>(2)</sup> Power dissipation and thermal limits must be observed.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>DRV8872-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA}</td>
<td>Junction-to-ambient thermal resistance</td>
<td>41.7</td>
</tr>
<tr>
<td>R_{JC(top)}</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>53.7</td>
</tr>
<tr>
<td>R_{JB}</td>
<td>Junction-to-board thermal resistance</td>
<td>12.4</td>
</tr>
<tr>
<td>ψ_{JT}</td>
<td>Junction-to-top characterization parameter</td>
<td>3</td>
</tr>
<tr>
<td>ψ_{JB}</td>
<td>Junction-to-board characterization parameter</td>
<td>12.6</td>
</tr>
<tr>
<td>R_{JC(bot)}</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>2.6</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).
### 6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for \( T_A = 25°C \) and \( V_{VM} = 24 \) V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY (VM)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{VM} )</td>
<td>VM operating voltage</td>
<td>6.8</td>
<td>45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{VM} )</td>
<td>VM operating supply current</td>
<td>3</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{VMSLEEP} )</td>
<td>VM sleep current</td>
<td>VM = 12 V</td>
<td>13</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{ON} )</td>
<td>Turnon time (^{(1)})</td>
<td>VM &gt; ( V_{UVLO} ) with IN1 or IN2 high</td>
<td>40</td>
<td>50</td>
<td>( \mu s )</td>
</tr>
<tr>
<td><strong>LOGIC-LEVEL INPUTS (IN1, IN2)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input logic low voltage</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input logic high voltage</td>
<td></td>
<td></td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Input logic hysteresis</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input logic low current</td>
<td>( V_{IN} = 0 ) V</td>
<td>–1</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Input logic high current</td>
<td>( V_{IN} = 3.3 ) V</td>
<td>33</td>
<td>100</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( R_{PD} )</td>
<td>Pulldown resistance</td>
<td>To GND</td>
<td>100</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Propagation delay</td>
<td>INx to OUTx change (see ( \text{図 6} ))</td>
<td>0.7</td>
<td>1</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{sleep} )</td>
<td>Time to sleep</td>
<td>Inputs low to sleep</td>
<td>1</td>
<td>1.5</td>
<td>ms</td>
</tr>
<tr>
<td><strong>MOTOR DRIVER OUTPUTS (OUT1, OUT2)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{DS(ON)} )</td>
<td>High-side FET on resistance</td>
<td>VM = 24 V, ( I = 1 ) A, ( f_{PWM} = 25 ) kHz</td>
<td>307</td>
<td>610</td>
<td>mΩ</td>
</tr>
<tr>
<td>( R_{DS(ON)} )</td>
<td>Low-side FET on resistance</td>
<td>VM = 24 V, ( I = 1 ) A, ( f_{PWM} = 25 ) kHz</td>
<td>258</td>
<td>500</td>
<td>mΩ</td>
</tr>
<tr>
<td>( t_{DEAD} )</td>
<td>Output dead time</td>
<td></td>
<td></td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>( V_d )</td>
<td>Body diode forward voltage</td>
<td></td>
<td></td>
<td>0.8</td>
<td>1</td>
</tr>
<tr>
<td><strong>CURRENT REGULATION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{TRIP} )</td>
<td>ISEN voltage for current chopping</td>
<td></td>
<td></td>
<td>0.32</td>
<td>0.35</td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>PWM off-time</td>
<td></td>
<td></td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>( I_{BLANK} )</td>
<td>PWM blanking time</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td><strong>PROTECTION CIRCUITS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{UVLO} )</td>
<td>VM undervoltage lockout</td>
<td>VM falls until UVLO triggers</td>
<td>6.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VM rises until operation recovers</td>
<td>6.4</td>
<td>6.7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{UV,HYS} )</td>
<td>VM undervoltage hysteresis</td>
<td>Rising to falling threshold</td>
<td>100</td>
<td>180</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{OCP} )</td>
<td>Overcurrent protection trip level</td>
<td></td>
<td></td>
<td>3.7</td>
<td>4.5</td>
</tr>
<tr>
<td>( I_{QCP} )</td>
<td>Overcurrent deglitch time</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>( I_{RETRY} )</td>
<td>Overcurrent retry time</td>
<td></td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown temperature (^{(2)})</td>
<td></td>
<td></td>
<td>155</td>
<td>180</td>
</tr>
<tr>
<td>( T_{HYS} )</td>
<td>Thermal shutdown hysteresis (^{(2)})</td>
<td></td>
<td></td>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>

**nFAULT OPEN DRAIN OUTPUT**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OL} )</td>
<td>Output low voltage</td>
<td>( I_O = 5 ) mA</td>
<td></td>
<td></td>
<td>0.5</td>
</tr>
<tr>
<td>( I_{OH} )</td>
<td>Output high leakage current</td>
<td>( V_O = 3.3 ) V</td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

\(^{(1)}\) \( I_{ON} \) applies when the device initially powers up, and when it exits sleep mode.

\(^{(2)}\) Ensured by design
6.6 Typical Characteristics

![Graph 1: R_{DS(on)} vs Temperature](DD01)

![Graph 2: V_{TRIP} vs Temperature](DD03)

![Graph 3: I_{VMSLEEP} vs VM at 25°C](DD04)
7 Detailed Description

7.1 Overview

The DRV8872-Q1 device is an optimized 8-pin device for driving brushed DC motors with 6.8 to 45 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{\text{ds(on)}}$ of 565 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 200 kHz. The device has an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevent the device from being damaged if a system fault occurs.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Bridge Control

The DRV8872-Q1 output consists of four N-channel MOSFETs that are designed to drive high current. These MOSFETs are controlled by the two logic inputs IN1 and IN2, according to Table 1.

<table>
<thead>
<tr>
<th>IN1</th>
<th>IN2</th>
<th>OUT1</th>
<th>OUT2</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>L</td>
<td>H</td>
<td>Reverse (current OUT2 → OUT1)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>H</td>
<td>L</td>
<td>Forward (current OUT1 → OUT2)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>L</td>
<td>L</td>
<td>Brake; low-side slow decay</td>
</tr>
</tbody>
</table>

The inputs can be set to static voltages for 100% duty-cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of its max RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. The input pins can be powered before VM is applied.

7.3.2 Sleep Mode

When IN1 and IN2 are both low for time $t_{SLEEP}$ (typically 1 ms), the DRV8872-Q1 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (microamps) of current. If the device is powered up while both inputs are low, sleep mode is immediately entered. After IN1 or IN2 are high for at least 5 µs, the device is operational 50 µs ($t_{ON}$) later.

7.3.3 Current Regulation

The DRV8872-Q1 device limits the output current based on the resistance of an external sense resistor on pin ISEN, according to Equation 1.
\[ I_{\text{TRIP}} (A) = \frac{V_{\text{TRIP}} (V)}{R_{\text{ISEN}} (\Omega)} = \frac{0.35 (V)}{R_{\text{ISEN}} (\Omega)} \]  

(1)

For example, if \( R_{\text{ISEN}} = 0.16 \, \Omega \), the DRV8872-Q1 device limits motor current to 2.2 A no matter how much load torque is applied. For guidelines on selecting a sense resistor, see the Sense Resistor section.

When \( I_{\text{TRIP}} \) has been reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for time \( t_{\text{OFF}} \) (typically 25 \( \mu \)s).

After \( t_{\text{OFF}} \) has elapsed, the output is re-enabled according to the two inputs INx. The drive time \( t_{\text{DRIVE}} \) until reaching another \( I_{\text{TRIP}} \) event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

### 7.3.4 Dead Time

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. \( t_{\text{DEAD}} \) is the time in the middle when the output is High-Z. If the output pin is measured during \( t_{\text{DEAD}} \), the voltage will depend on the direction of current. If current is leaving the pin, the voltage is a diode drop below ground. If current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.
7.3.5 Protection Circuits

The DRV8872-Q1 device is fully protected against VM undervoltage, overcurrent, and overtemperature events. When the device is in a protected state, nFAULT is driven low. When the fault condition is removed, nFAULT becomes a high-impedance state.

7.3.5.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when VM rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold $I_{OCP}$ for longer than $t_{OCP}$, all FETs in the H-bridge are disabled for a duration of $t_{RETRY}$. After that, the H-bridge re-enables according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge is disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

<table>
<thead>
<tr>
<th>Fault</th>
<th>Condition</th>
<th>H-Bridge Becomes</th>
<th>nFault Becomes</th>
<th>Recovery</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM undervoltage lockout (UVLO)</td>
<td>VM &lt; $V_{UVLO}$</td>
<td>Disabled</td>
<td>Low</td>
<td>VM &gt; $V_{UVLO}$</td>
</tr>
<tr>
<td>Overcurrent (OCP)</td>
<td>$I_{OUP} &gt; I_{OCP}$</td>
<td>Disabled</td>
<td>Low</td>
<td>$t_{RETRY}$</td>
</tr>
<tr>
<td>Thermal shutdown (TSD)</td>
<td>$T_J &gt; 150^\circ C$</td>
<td>Disabled</td>
<td>Low</td>
<td>$T_J &lt; T_{SD} - T_{HYS}$</td>
</tr>
</tbody>
</table>

7.4 Device Functional Modes

The DRV8872-Q1 device can be used in multiple ways to drive a brushed DC motor.

7.4.1 PWM With Current Regulation

This scheme uses all of the capabilities of the device. The $I_{TRIP}$ current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake and slow decay is typically used during the off-time.

7.4.2 PWM Without Current Regulation

If current regulation is not needed, the ISEN pin should be directly connected to the PCB ground plane. This mode provides the highest possible peak current: up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or over-temperature shutdown (TSD). If that occurs, the device disables and protects itself for about 3 ms ($t_{RETRY}$) and then resumes normal operation.

7.4.3 Static Inputs With Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and $I_{TRIP}$ can be used to control the current, speed, and torque capability of the motor.

7.4.4 VM Control

In some systems, varying VM as a means of changing motor speed is desirable. See the Motor Voltage section for more information.
8 Application and Implementation

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8872-Q1 device is typically used to drive one brushed DC motor.

8.2 Typical Application

![Typical Connections](image)

8.2.1 Design Requirements

表 3 lists the design parameters.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>REFERENCE</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motor voltage</td>
<td>$V_M$</td>
<td>24 V</td>
</tr>
<tr>
<td>Motor RMS current</td>
<td>$I_{RMS}$</td>
<td>0.8 A</td>
</tr>
<tr>
<td>Motor startup current</td>
<td>$I_{START}$</td>
<td>2 A</td>
</tr>
<tr>
<td>Motor current trip point</td>
<td>$I_{TRIP}$</td>
<td>2.2 A</td>
</tr>
<tr>
<td>Sense resistance</td>
<td>$R_{ISEN}$</td>
<td>0.16 $\Omega$</td>
</tr>
<tr>
<td>PWM frequency</td>
<td>$f_{PWM}$</td>
<td>5 kHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage used depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in 式 2.

$$P_D = I^2 \left( R_{DS(on)Source} + R_{DS(on)Sink} \right)$$  (2)
The DRV8872-Q1 device has been measured to be capable of 2-A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency. Typically, switching the inputs at 200 kHz compared to 20 kHz causes 20% more power loss in heat.

### 8.2.2.3 Sense Resistor

For optimal performance, the sense resistor must have the features that follow:

- Surface-mount device
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 1.5 A, and a 0.2-Ω sense resistor is used, the resistor dissipates $1.5^2 \times 0.2 \, \Omega = 0.45 \, W$. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. It is always best to measure the actual sense resistor temperature in a final system.

Because power resistors are larger and more expensive than standard resistors, multiple standard resistors can be used in parallel, between the sense node and ground. This configuration distributes the current and heat dissipation.

### 8.2.3 Application Curves

![Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 12 V](#)

![Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 24 V](#)
图 10. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 45 V

图 11. \(i_{PD}\)

图 12. Current Regulation With \(R_{SENSE} = 0.26\) Ω

图 13. OCP With 24 V and Outputs Shorted Together
9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. More bulk capacitance is generally beneficial but with the disadvantages of increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:
- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate that the current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.
10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

图 15 shows the recommended layout and component placement.

10.2 Layout Example

图 15. Layout Recommendation

10.3 Thermal Considerations

The DRV8872-Q1 device has thermal shutdown (TSD) as described in the Thermal Shutdown (TSD) section. If the die temperature exceeds approximately $175^\circ$C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8872-Q1 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use 2 from the Drive Current section to calculate the estimated average power dissipation of when driving a load.

Note that at startup, the output current is much higher than normal running current; this peak current and its duration must be also be considered.
Power Dissipation (continued)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

---

\[ R_{\text{DS(on)}} \text{ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.} \]

---

The power dissipation of the DRV8872-Q1 is a function of RMS motor current and the FET resistance \( R_{\text{DS(ON)}} \) of each output.

\[ \text{Power} \approx \text{I}_{\text{RMS}}^2 \times (\text{High-side } R_{\text{DS(ON)}} + \text{Low-side } R_{\text{DS(ON)}}) \quad (3) \]

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of \( R_{\text{DS(ON)}} \) is about 0.72 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat is 0.8 A\(^2\) × 0.72 Ω = 0.46 W.

The temperature that the DRV8872-Q1 reaches depends on the thermal resistance to the air and PCB. Soldering the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, is important to dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8872-Q1 had an effective thermal resistance \( R_{\theta JA} \) of 48°C/W, and a \( T_J \) value as shown in 式 4.

\[ T_J = T_A + (P_D \times R_{\theta JA}) = 58°C + (0.46 \text{ W} \times 48°C/W) = 80°C \quad (4) \]

10.4.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the TI application report, PowerPAD™ Thermally Enhanced Package (SLMA002), and the TI application brief, PowerPAD Made Easy™ (SLMA004), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.
11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料
関連資料については、以下を参照してください。
- 『電流再循環モードと電流減衰モード』(SLVA321)
- 『モータ・ドライバの消費電力の計算』(SLVA504)
- 『DRV8872-Q1を使用したエンジン・グリル・シャッター・モータの駆動』(SLVA858)
- 『放熱特性の優れたPowerPAD™パッケージ』(SLMA002)
- 『PowerPAD™の簡単な使用法』(SLMA004)
- 『モータ・ドライバの電流定格について』(SLVA505)

11.2 ドキュメントの更新通知を受け取る方法
ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™オンライン・コミュニティ TIのE2E (Engineer-to-Engineer) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標
PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項
すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。
静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 用語集
SLYZ022 — TI用語集。
この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8872DDARQ1</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>8872Q</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image-url)

**NOTE:** All linear dimensions are in millimeters.

PowerPAD is a trademark of Texas Instruments.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.
重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、アプリケーションや設計に関する各種アドバイス、Webツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI製品を使用する設計の経験を積んだ開発者への提供を意図したもので、(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TIや第三者の知的財産権のライセンスが付与されている訳ではありません。

TIの製品は、TIの販売条件（www.tij.co.jp/ja-ja/legal/termsOfSale.html）、またはti.com やかかる TI製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TIがこれらのリソースを提供することは、適用されるTIの保証または他の保証の拡大や変更を意味するものではありません。

Copyright © 2019, Texas Instruments Incorporated
日本語版 日本テキサス・インスツルメンツ株式会社