SINGLE-ENDED ANALOG-INPUT 16-BIT STEREO ANALOG-TO-DIGITAL CONVERTER

FEATURES

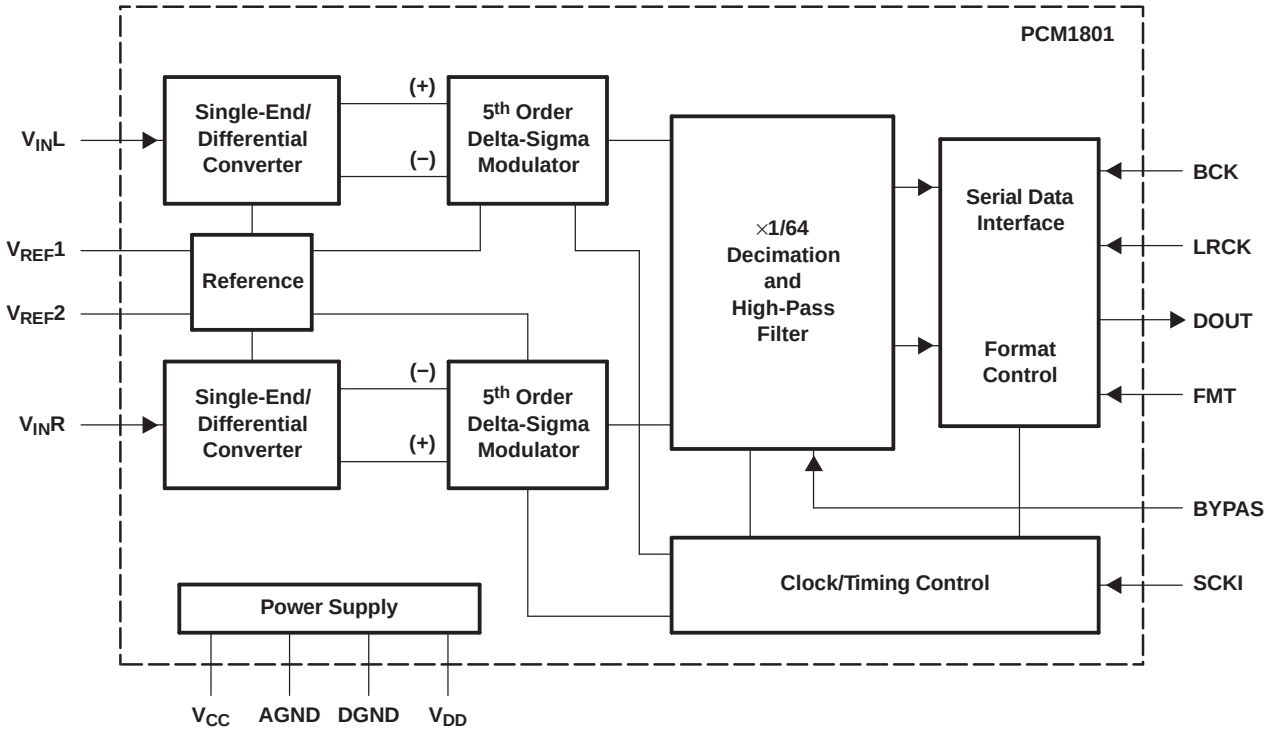
- **Dual 16-Bit Monolithic ΔΣ ADC**
- **Single-Ended Voltage Input**
- **Antialiasing Filter Included**
- **64× Oversampling Decimation Filter:**
  Pass-Band Ripple: ±0.05 dB
  Stop-Band Attenuation: –65 dB
- **Analog Performance:**
  THD+N: –88 dB (typical)
  SNR: 93 dB (typical)
  Dynamic Range: 93 dB (typical)
  Internal High-Pass Filter
- **PCM Audio Interface: Left-Justified, I^2S**
- **Sampling Rate: 4 kHz to 48 kHz**
- **System Clock: 256 f_S, 384 f_S, or 512 f_S**
- **Single 5-V Power Supply**
- **Small SO-14 Package**

APPLICATIONS

- **DVD Recorders**
- **DVD Receivers**
- **AV Amplifier Receivers**
- **Electric Musical Instruments**

DESCRIPTION

The PCM1801 is a low-cost, single-chip stereo analog-to-digital converter (ADC) with single-ended analog voltage inputs. The PCM1801 uses a delta-sigma modulator with 64 times oversampling, a digital decimation filter, and a serial interface that supports slave mode operation and two data formats. The PCM1801 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE TYPE	PACKAGE CODE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA	QUANTITY
PCM1801U	14-pin SOIC	D	PCM1801U	PCM1801U	Rails	56
				PCM1801U/2K	Tape and reel	2000

ABSOLUTE MAXIMUM RATINGS

Supply voltage: V_{DD}, V_{CC}	–0.3 V to 6.5 V
Supply voltage differences: V_{DD}, V_{CC}	±0.1 V
GND voltage differences: AGND, DGND	±0.1 V
Digital input voltage	–0.3 V to (V_{DD} + 0.3 V), < 6.5 V
Analog input voltage	–0.3 V to (V_{CC} + 0.3 V), < 6.5 V
Input current (any pin except supplies)	±10 mA
Power dissipation	300 mW
Operating temperature range	–25°C to 85°C
Storage temperature	–55°C to 125°C
Lead temperature, soldering	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

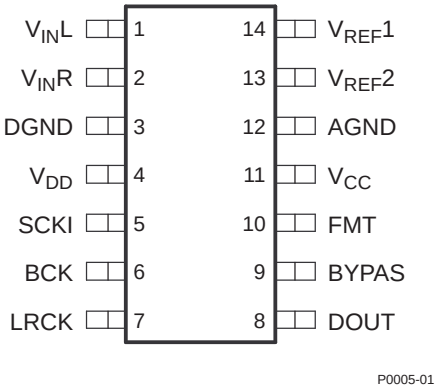
RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		4.5	5	5.5	V
Analog input voltage, full-scale (–0 dB)			2.828		Vp-p
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		24.576	MHz
	Sampling clock	32		48	kHz
Digital output load capacitance			10		pF
Operating free-air temperature, T_A		–25		85	°C

PIN CONFIGURATION

PCM1801
(TOP VIEW)



P0005-01

Table 1. PIN ASSIGNMENTS

NAME	PIN	I/O	DESCRIPTION
AGND	12	–	Analog ground
BCK	6	I	Bit clock input
BYPAS	9	I	HPF bypass control(1) L: HPF enabled H: HPF disabled
DGND	3	–	Digital ground
DOUT	8	O	Audio data output
FMT	10	I	Audio data format(1) L: MSB-first, left-justified H: MSB-first, I^2S
LRCK	7	I	Sampling clock input
SCKI	5	I	System clock input; 256 f_S, 384 f_S, or 512 f_S
V_{CC}	11	–	Analog power supply
V_{DD}	4	–	Digital power supply
$V_{IN}L$	1	I	Analog input, Lch
$V_{IN}R$	2	I	Analog input, Rch
$V_{REF}1$	14	–	Reference 1 decoupling capacitor
$V_{REF}2$	13	–	Reference 2 decoupling capacitor

(1) With 100-kΩ typical pulldown resistor

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, 16-bit data, and SYSCLK = 384 f_S, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM1801U			UNITS
			MIN	TYP	MAX	
RESOLUTION				16		Bits
DIGITAL INPUT/OUTPUT						
V_{IH} (1)	Input logic level		2			VDC
V_{IL} (1)					0.8	
I_{IN} (2)	Input logic current				±10	µA
I_{IN} (3)					100	
V_{OH} (4)	Output logic level	I_{OH} = –1.6 mA	4.5			VDC
V_{OL} (4)		I_{OL} = 3.2 mA			0.5	
f_S	Sampling frequency		4	44.1	48	kHz
	System clock frequency	256 f_S	1.024	11.2896	12.288	MHz
		384 f_S	1.536	16.9344	18.432	
		512 f_S	2.048	22.5792	24.576	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±2.5	% of FSR
	Gain error			±2	±5	% of FSR
	Gain drift			±20		ppm of FSR/°C
	Bipolar zero error	High-pass filter bypassed		±2		% of FSR
	Bipolar zero drift	High-pass filter bypassed		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE (5)						
	THD+N	FS (–0.5 dB)		–88	–80	dB
		–60 dB		–90		
	Dynamic range	A-weighted	90	93		dB
	Signal-to-noise ratio	A-weighted	90	93		dB
	Channel separation		87	90		dB
ANALOG INPUT						
	Input range	FS (V_{IN} = 0 dB)		2.828		Vp-p
	Center voltage			2.1		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time (latency)			17.4/f_S		s
	High-pass frequency response	–3 dB		0.019 f_S		mHz

(1) Pins 5, 6, 7, 9, and 10 (SCKI, BCK, LRCK, BYPAS, and FMT)
(2) Pins 5, 6, 7 (SCKI, BCK, LRCK) Schmitt-trigger input
(3) Pins 9, 10 (BYPAS, FMT) Schmitt-trigger input with 100-kΩ typical pulldown resistor
(4) Pin 8 (DOUT)
(5) f_{IN} = 1 kHz, using the System Two™ audio measurement system by Audio Precision™ in rms mode with 20-kHz LPF and 400-Hz HPF in the performance calculation.

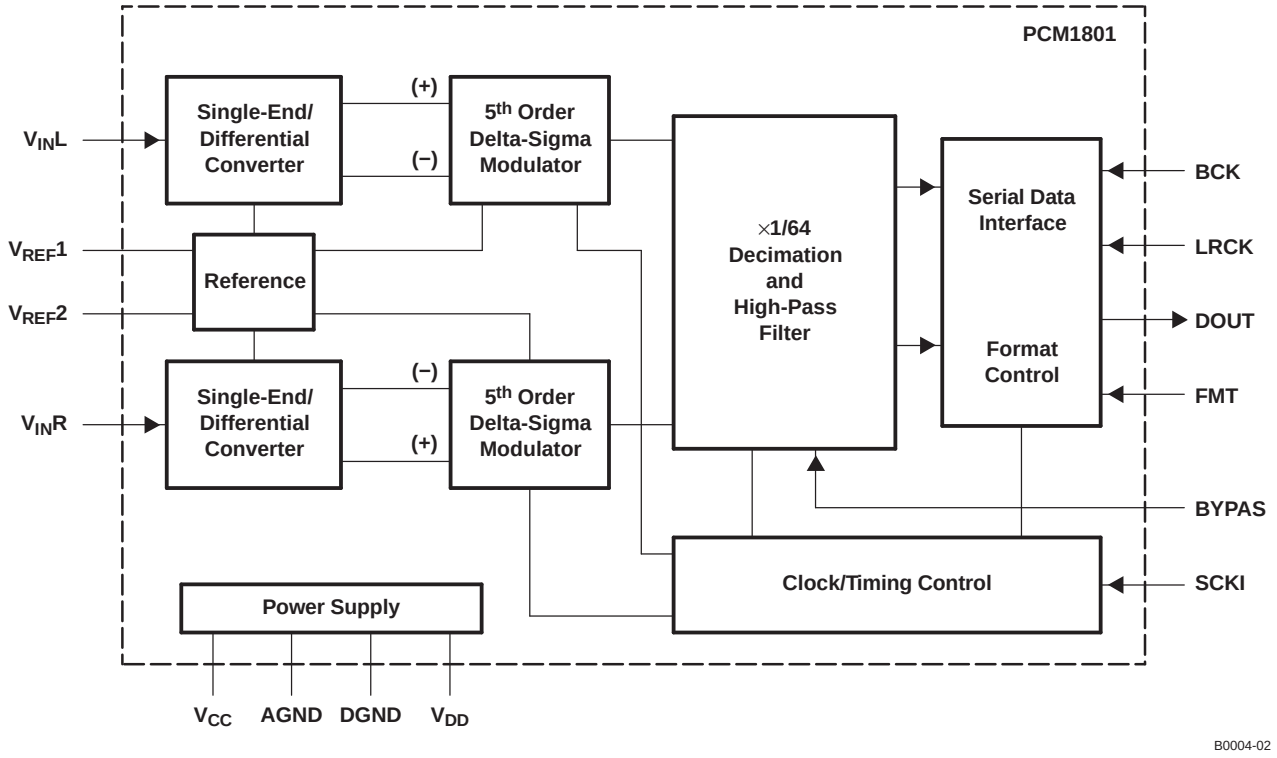
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, 16-bit data, and SYSCLK = 384 f_S, unless otherwise noted.

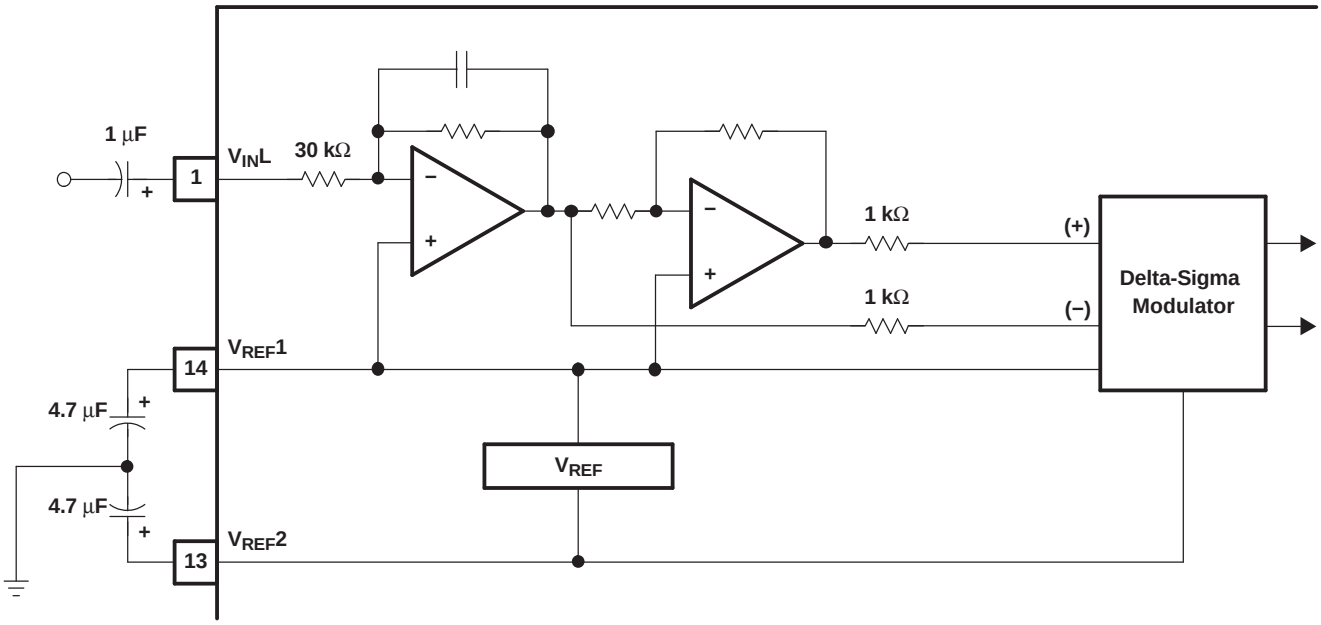
PARAMETER		TEST CONDITIONS	PCM1801U			
			MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			4.5	5	5.5	
	Supply current(6)	V_{CC} = V_{DD} = 5 V		18	24	mA
	Power dissipation	V_{CC} = V_{DD} = 5 V		90	120	mW
TEMPERATURE RANGE						
T_A	Operation		–25		85	°C
T_{stg}	Storage		–55		125	°C
θ_{JA}	Thermal resistance			100		°C/W

(6) No load on DOUT (pin 8)

BLOCK DIAGRAM



ANALOG FRONT-END (Single Channel)



TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

ANALOG DYNAMIC PERFORMANCE

TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE

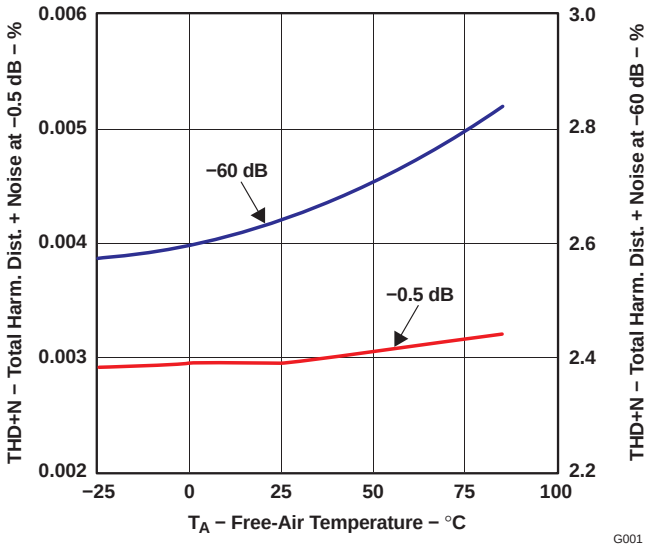


Figure 1.

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO vs TEMPERATURE

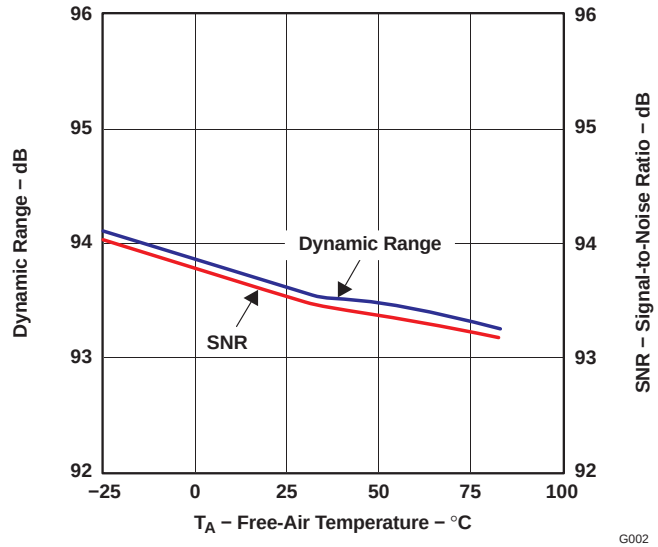


Figure 2.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE

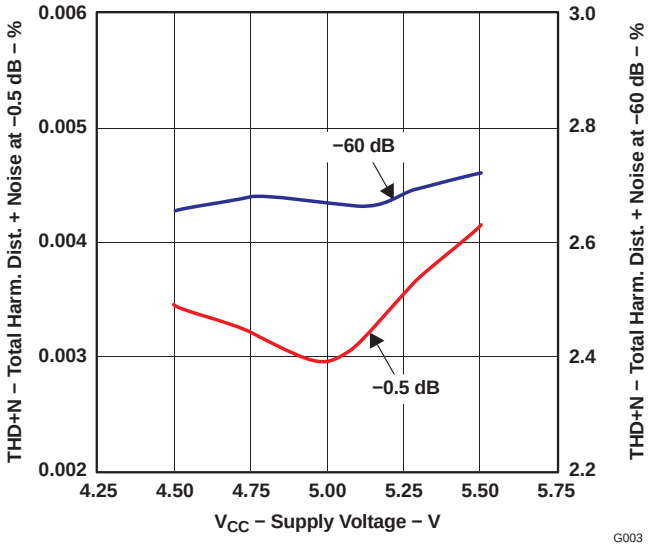


Figure 3.

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs
SUPPLY VOLTAGE

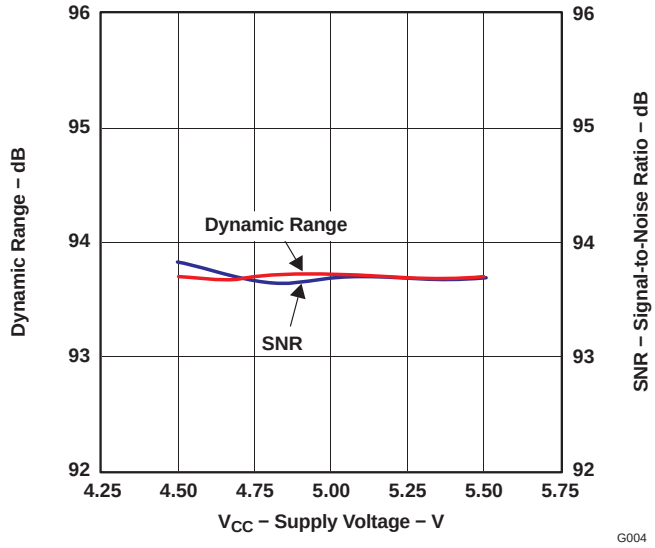


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
SAMPLING RATE

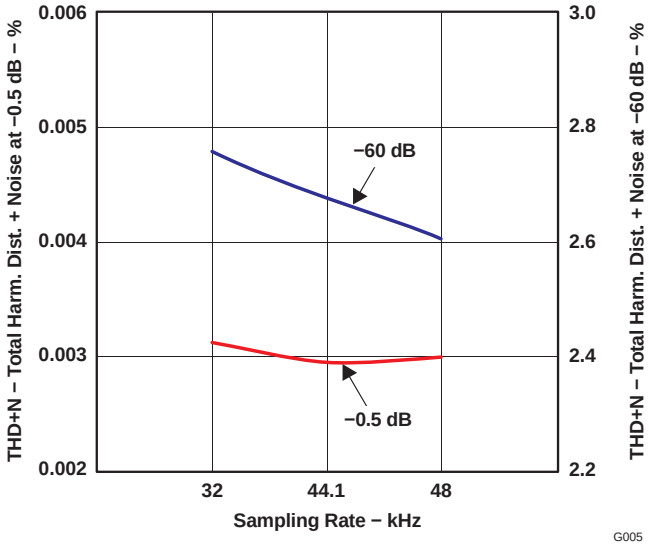


Figure 5.

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs
SAMPLING RATE

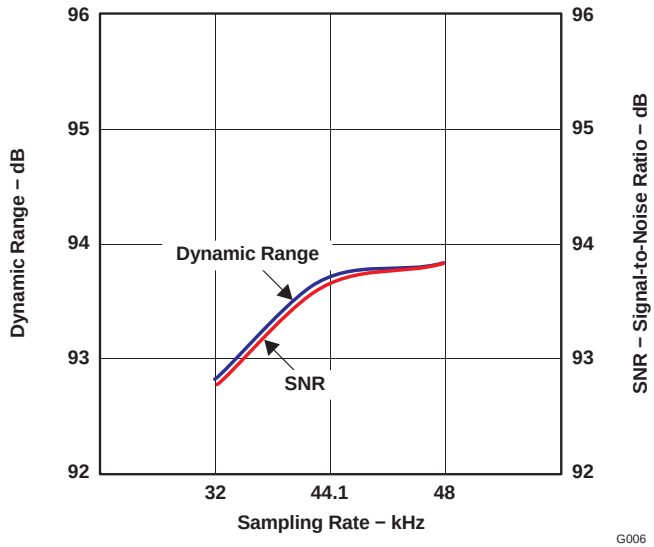


Figure 6.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

SUPPLY CURRENT

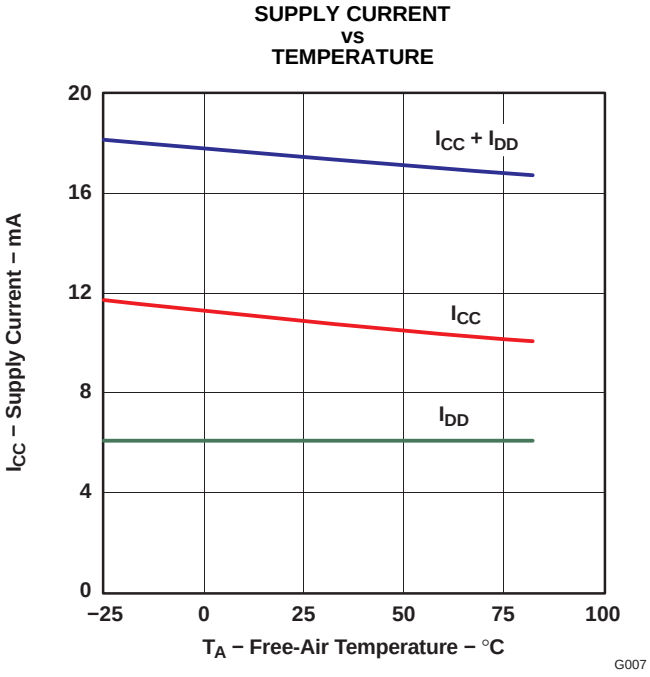


Figure 7.

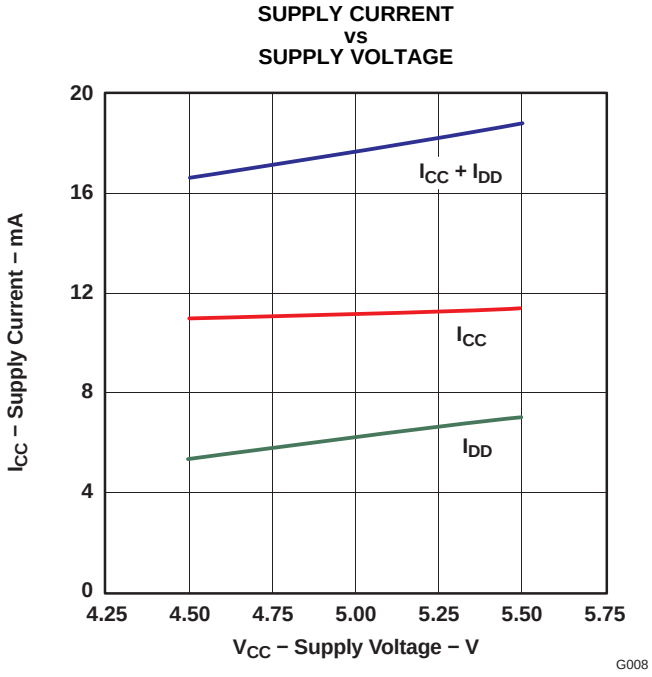


Figure 8.

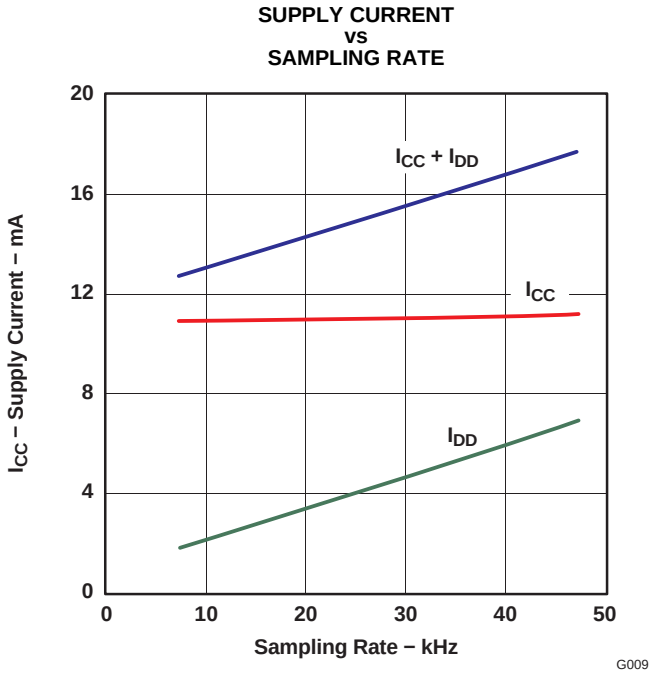


Figure 9.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

OUTPUT SPECTRUM

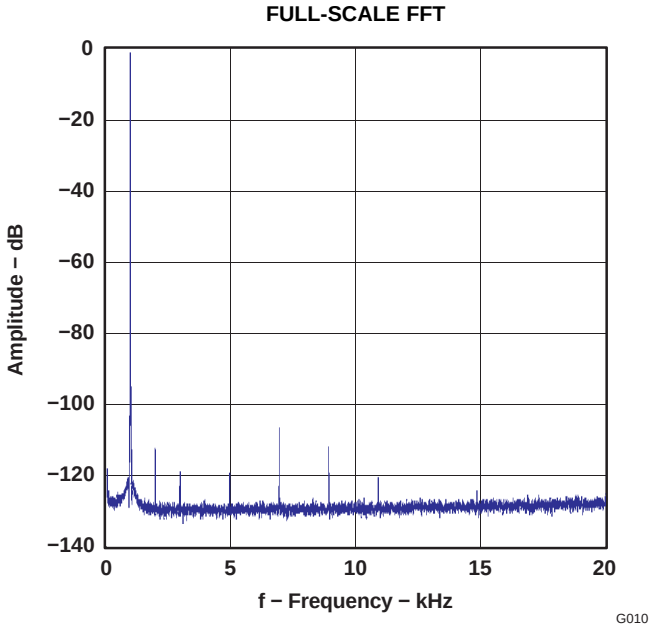


Figure 10.

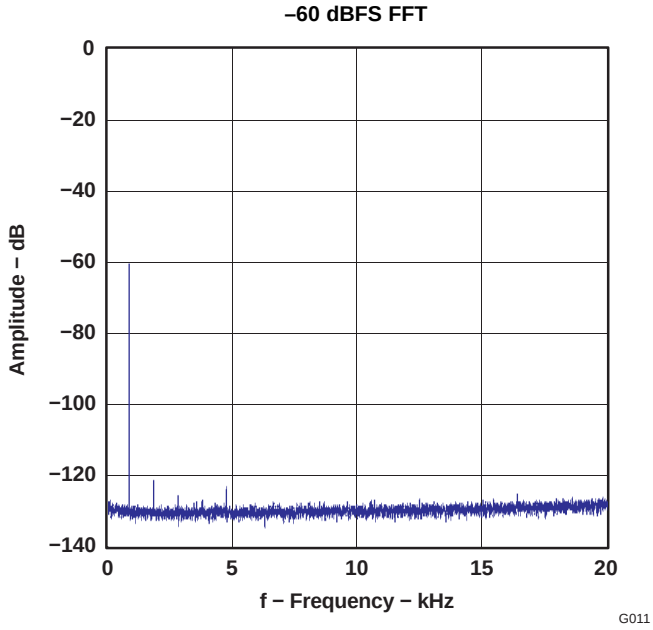


Figure 11.

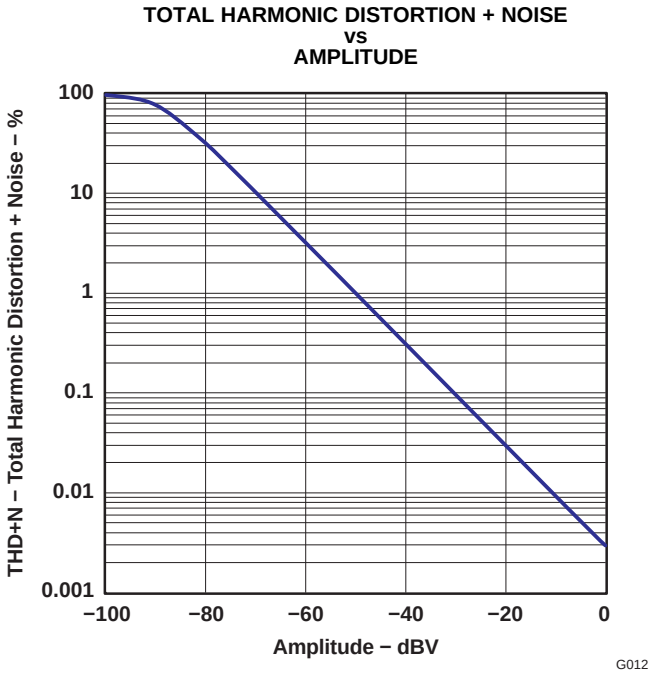


Figure 12.

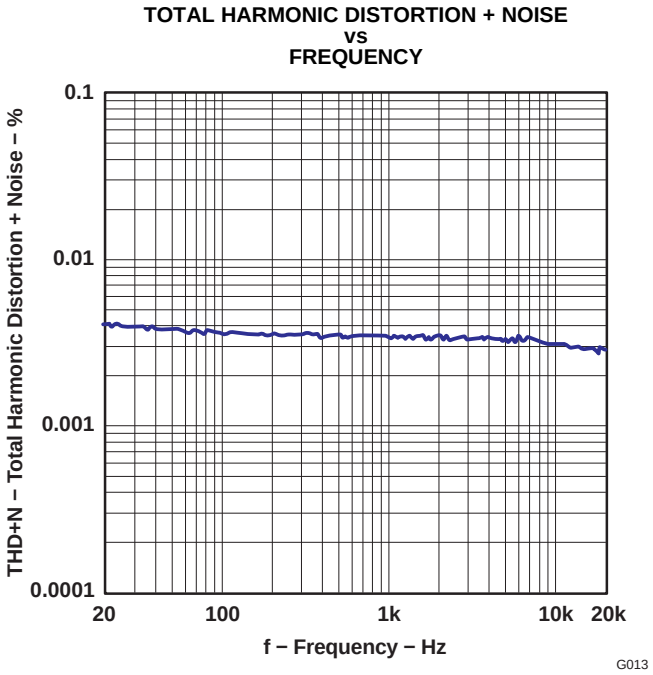


Figure 13.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

DECIMATION FILTER

OVERALL CHARACTERISTICS

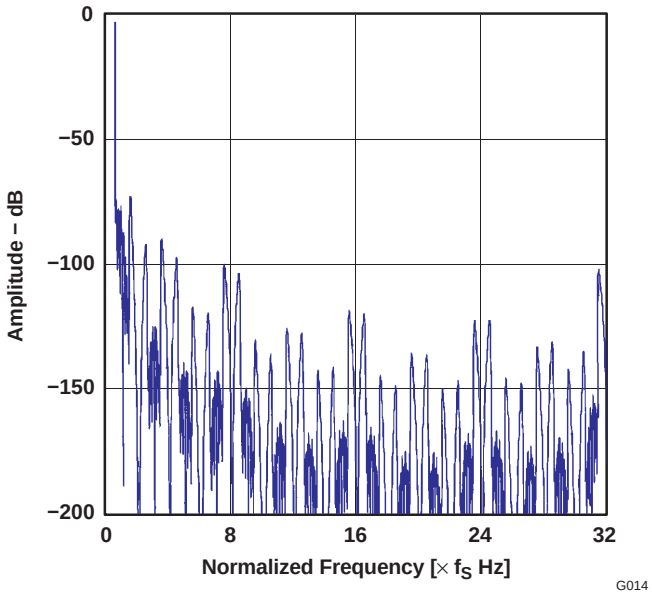


Figure 14.

STOP-BAND ATTENUATION CHARACTERISTICS

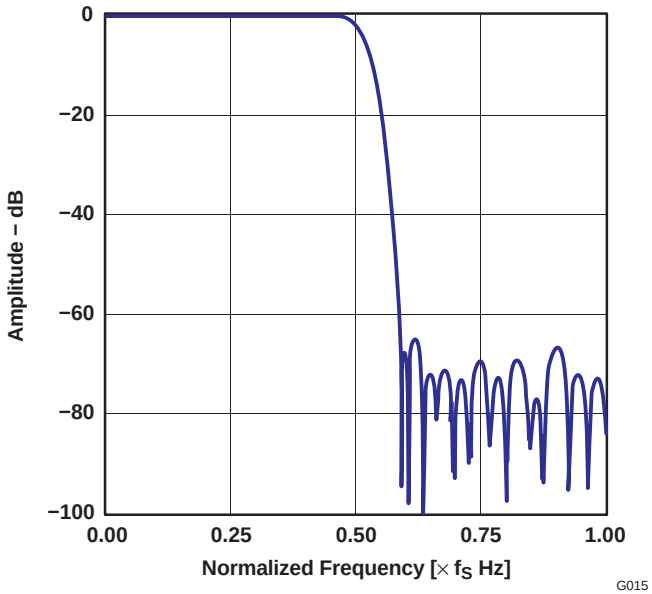


Figure 15.

PASS-BAND RIPPLE CHARACTERISTICS

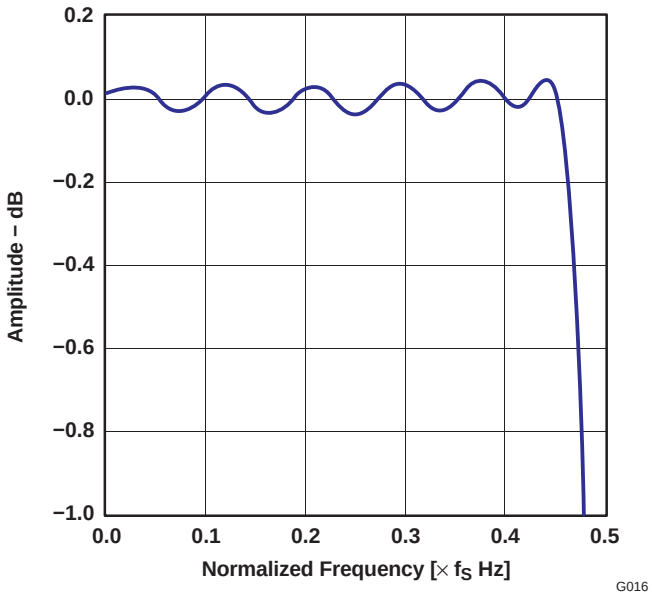


Figure 16.

TRANSITION BAND CHARACTERISTICS

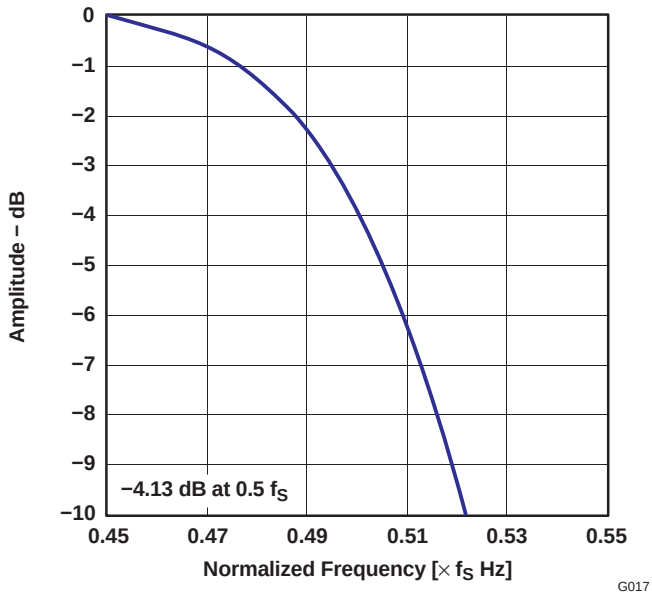


Figure 17.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, f_S = 44.1 kHz, and SYSCLK = 384 f_S, unless otherwise noted

HIGH-PASS FILTER

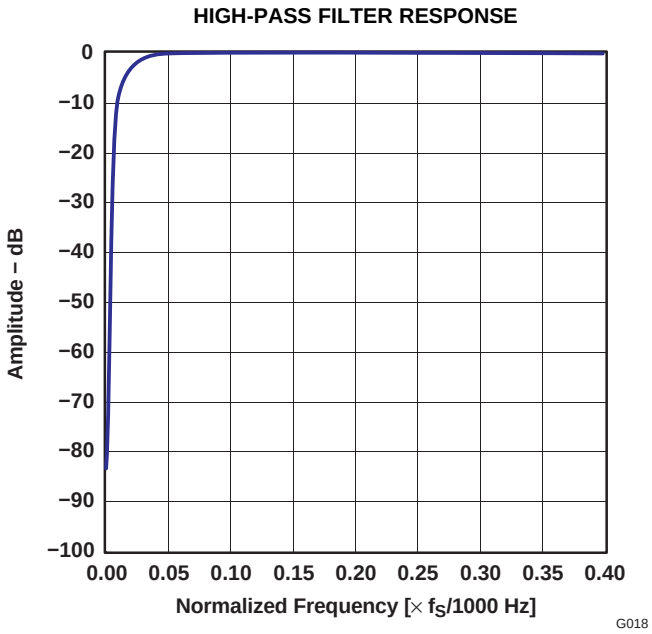


Figure 18.

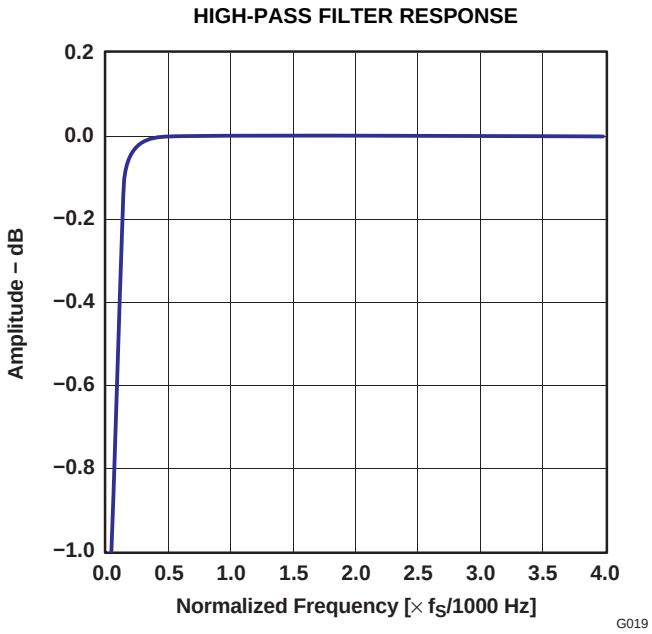


Figure 19.

ANTIALIASING FILTER

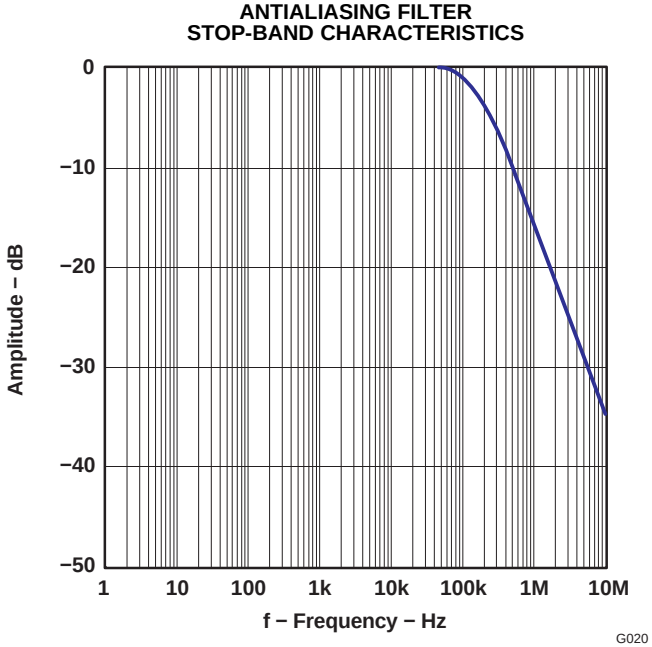


Figure 20.

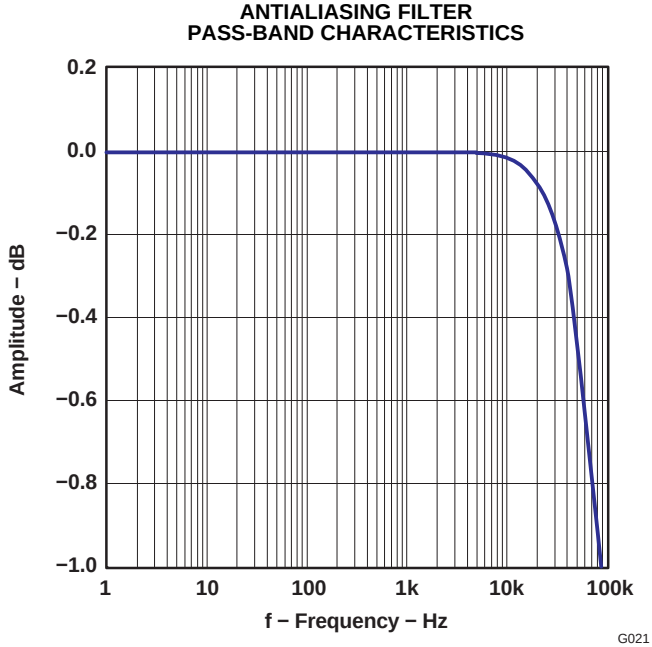


Figure 21.

THEORY OF OPERATION

The PCM1801 consists of a band-gap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high-pass), and a serial interface circuit. The block diagram illustrates the total architecture of the PCM1801, and the analog front-end diagram illustrates the architecture of the single-to-differential converter and the antialiasing filter. Figure 22 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high-precision reference with two external capacitors provides all reference voltages which are required by the converter, and defines the full-scale voltage range of both channels. The internal single-ended to differential voltage converter saves the design, space, and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance.

The input signal is sampled at a 64× oversampling rate, eliminating the need for a sample-and-hold circuit and simplifying antialias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a 1-bit digital-to-analog converter (DAC). The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The 64-f_S, 1-bit stream from the modulator is converted to 1-f_S, 16-bit digital data by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a digital high-pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats.

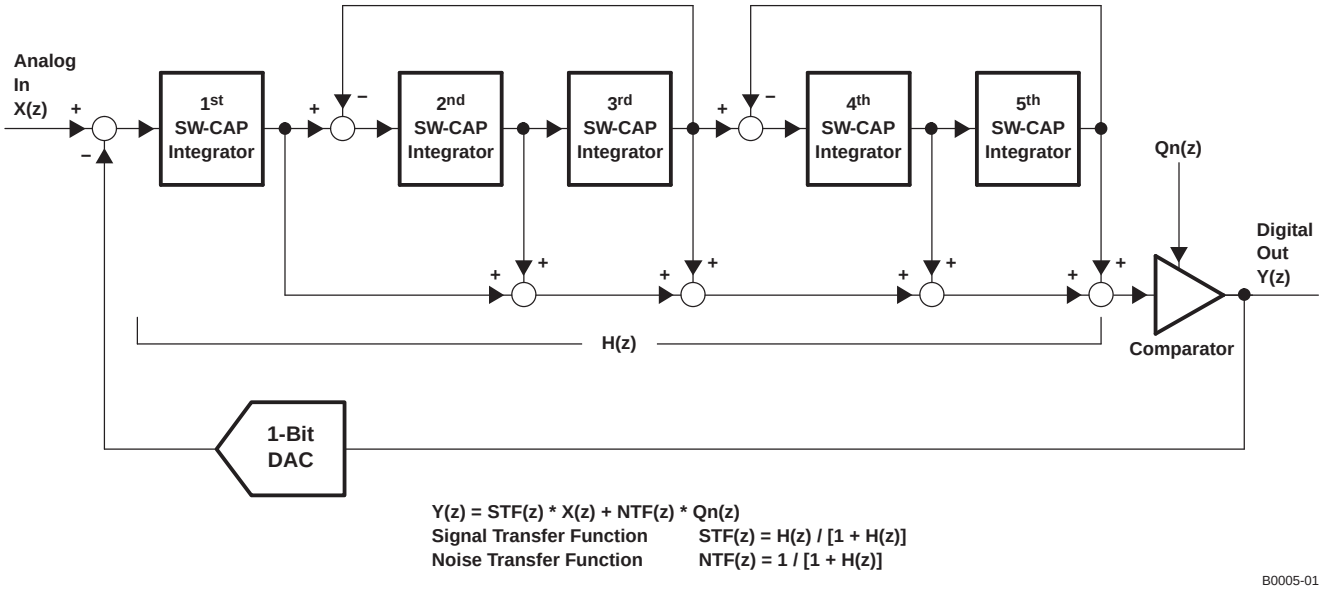


Figure 22. Simplified Diagram of the PCM1801 5th-Order Delta-Sigma Modulator

SYSTEM CLOCK

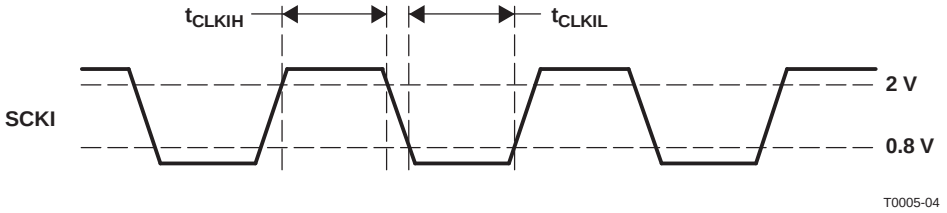
The system clock for the PCM1801 must be either 256 f_S, 384 f_S, or 512 f_S, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 5).

The PCM1801 also has a system clock detection circuit that automatically senses if the system clock is operating at 256 f_S, 384 f_S, or 512 f_S.

When a 384-f_S or 512-f_S system clock is used, the PCM1801 automatically divides the clock down to 256 f_S internally. This 256-f_S clock is used to operate the digital filter and the modulator. Table 2 lists the relationship of typical sampling frequencies and system clock frequencies. Figure 23 illustrates the system clock timing.

Table 2. System Clock Frequencies

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY		
	256 f_S	384 f_S	512 f_S
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

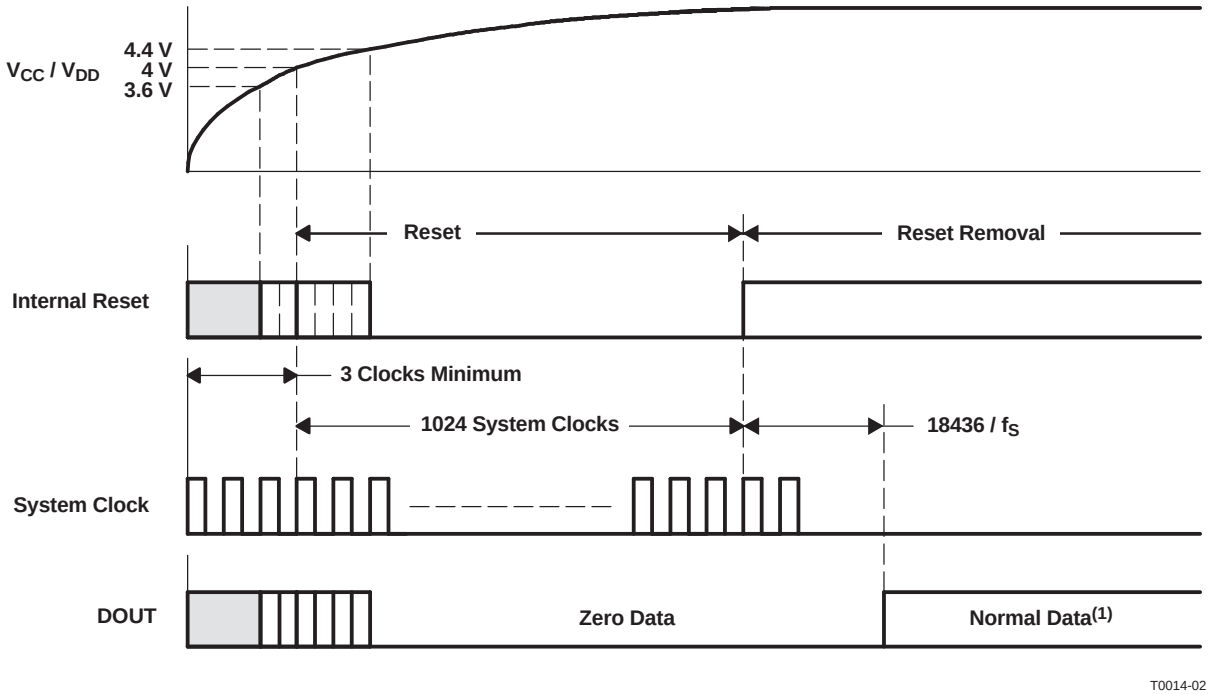


System clock pulse duration, HIGH	$t_{(CLKIH)}$	12 ns (min)
System clock pulse duration, LOW	$t_{(CLKIL)}$	12 ns (min)

Figure 23. System Clock Timing

POWER-ON RESET

The PCM1801 has an internal power-on reset circuit, which initializes (resets) when the supply voltage (V_{CC}/V_{DD}) exceeds 4 V (typical). Because the system clock is used as the clock signal for the reset circuit, the system clock must be supplied as soon as power is applied; more specifically, the device must receive at least three system clock cycles before V_{DD} > 4 V. While V_{CC}/V_{DD} < 4 V (typical) and for 1024 system clock cycles after V_{CC}/V_{DD} > 4 V, the PCM1801 stays in the reset state and the digital output is forced to zero. The digital output is valid 18,436 f_S periods after release from the reset state. Figure 24 illustrates the internal power-on reset timing and the digital output for power-on reset.



(1) The transient response (exponentially attenuated signal from ±0.2% dc of FSR with a 200-ms time constant) appears initially.

Figure 24. Internal Power-On Reset Timing

SERIAL AUDIO DATA INTERFACE

The PCM1801 interfaces the audio system through BCK (pin 6), LRCK (pin 7), and DOUT (pin 8).

The PCM1801 accepts 64-BCK/LRCK, 48-BCK/LRCK (only for a 384-f_S system clock) or 32-BCK/LRCK format for the left-justified format. And the PCM1801 accepts the 64-BCK/LRCK or 48-BCK/LRCK format (only for a 384-f_S system clock) for I^2S format.

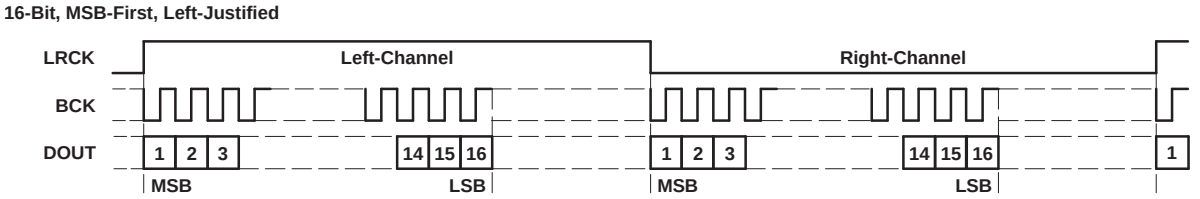
DATA FORMAT

The PCM1801 supports two audio data formats in slave mode, which are selected by the FMT control input (pin 10) as shown in Table 3. Figure 25 illustrates the data format. If the application system cannot ensure an effective system clock prior to power up of the PCM1801, the FMT pin must be held LOW until the power-on reset sequence is completed. In this case, if the I^2S format (FMT = HIGH) is required in the application, FMT can be set HIGH after the power-on reset sequence is completed.

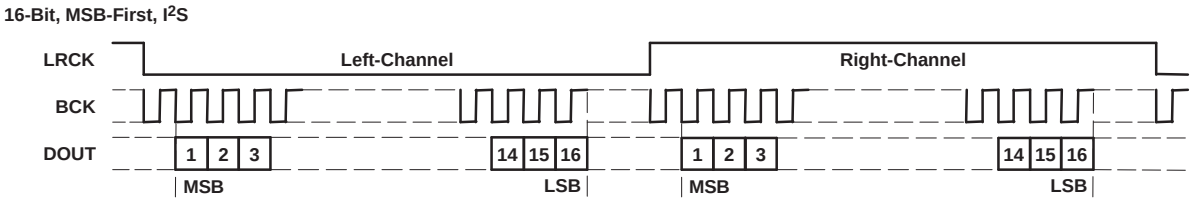
Table 3. Data Format

FMT	DATA FORMAT
0 (L)	16-bit, left-justified
1 (H)	16-bit, I^2S

FMT = L



FMT = H

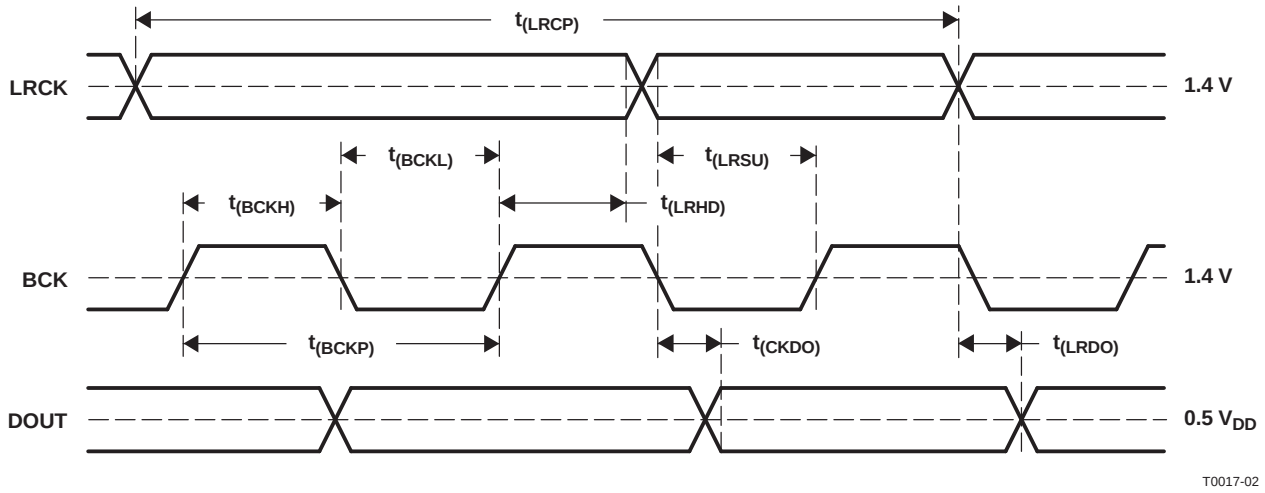


T0016-03

Figure 25. Audio Data Format

INTERFACE TIMING

Figure 26 illustrates the interface timing.



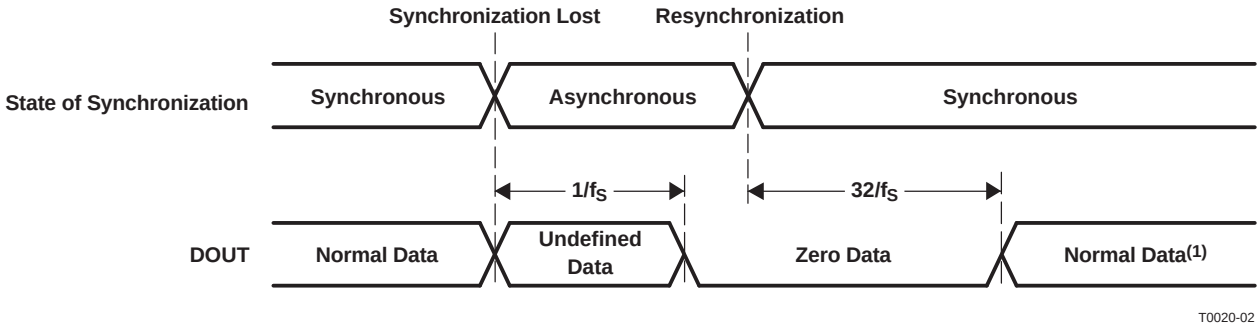
DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK period	$t_{(BCKP)}$	300			ns
BCK pulse duration, HIGH	$t_{(BCKH)}$	120			ns
BCK pulse duration, LOW	$t_{(BCKL)}$	120			ns
LRCK setup time to BCK rising edge	$t_{(LRSU)}$	80			ns
LRCK hold time to BCK rising edge	$t_{(LRHD)}$	40			ns
LRCK period	$t_{(LRCP)}$	20			µs
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$	–20		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$	–20		40	ns
Rising time of all signals	$t_{(RISE)}$			20	ns
Falling time of all signals	$t_{(FALL)}$			20	ns

NOTE: Timing measurement reference level is $(V_{IH} + V_{IL})/2$. Rising and falling time is measured from 10% to 90% of the I/O signal swing. Load capacitance of the DOUT signal is 20 pF.

Figure 26. Audio Data Interface Timing

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

The PCM1801 operates with LRCK synchronized to the system clock (SCKI). The PCM1801 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI. If the relationship between LRCK and SCKI changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and the digital output is forced to BPZ until resynchronization between LRCK and SCKI is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur and the previously described digital output control and discontinuity do not occur. Figure 27 illustrates the ADC digital output for lost synchronization and resynchronization. During undefined data, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity of data on the digital output and may generate some noise in the audio signal.



(1) The transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 27. ADC Digital Output for Loss of Synchronization and Re-Synchronization

HPF Bypass Control

The built-in function for dc component rejection can be bypassed by BYPAS (pin 9) control (see Table 4). In bypass mode, the dc component of the input analog signal, the internal dc offset, etc., are also converted and output in the digital output data.

Table 4. HPF Bypass Control

BYPAS	HIGH-PASS FILTER (HPF) MODE
Low	Normal (dc cut) mode
High	Bypass (through) mode

APPLICATION INFORMATION

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} PINS

The digital and analog power supply lines to the PCM1801 should be bypassed to the corresponding ground pins with both 0.1-µF ceramic and 10-µF tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1801 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply problems, such as latch-up due to power supply sequencing.

AGND, DGND PINS

To maximize the dynamic performance of the PCM1801, the analog and digital grounds are not internally connected. These points should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1801 package to reduce potential noise problems.

V_{IN} PINS

A 1.0-µF tantalum capacitor is recommended as an ac-coupling capacitor, which establishes a 5.3-Hz cutoff frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the V_{IN} pins.

V_{REF} PINS

To ensure low source impedance, 4.7-µF tantalum capacitors are recommended from $V_{REF}1$ to AGND and from $V_{REF}2$ to AGND. These capacitors should be located as close as possible to the $V_{REF}1$ and $V_{REF}2$ pins to reduce dynamic errors on the ADC references.

APPLICATION INFORMATION (continued)

DOUT PIN

The DOUT pin has a large load-drive capability, but locating a buffer near the PCM1801 and minimizing load capacitance is recommended in order to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

FMT PIN

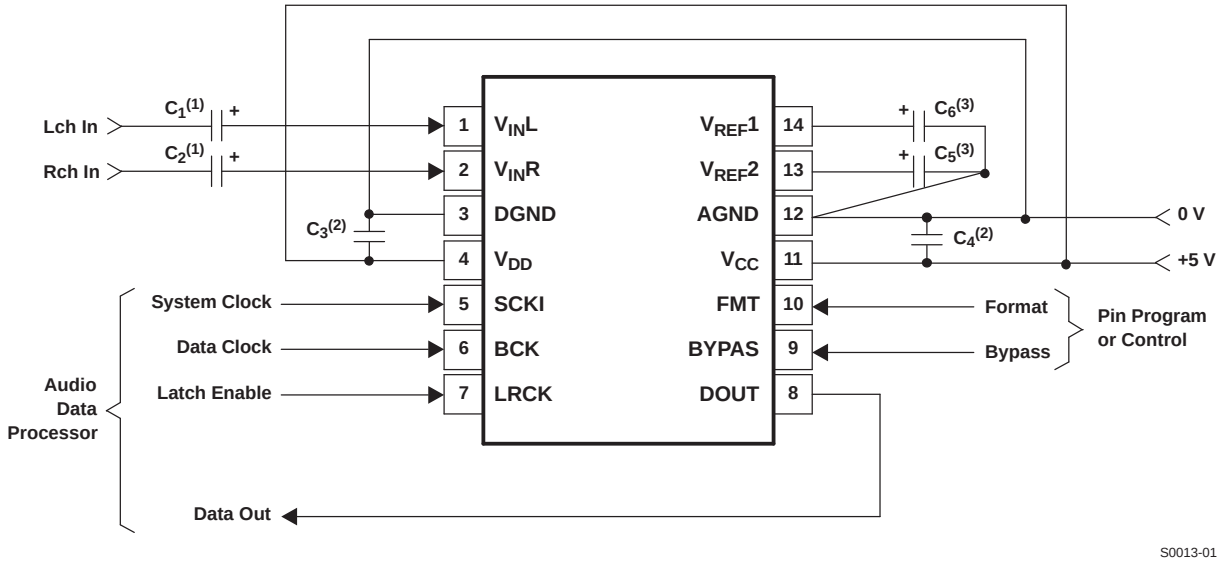
In general, the FMT pin is used for audio data format selection by tying up DGND or V_{DD} in accordance with interface requirements. If the application system cannot ensure an effective system clock prior to power up of the PCM1801 when I^2S format is required, then the FMT pin must be set HIGH after the power-on reset sequence. This input control can be accomplished easily by connecting a C-R delay circuit with a delay time greater than 1 ms to the FMT pin.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance in the PCM1801. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks results in a power dissipation increase of up to three times normal dissipation and may degrade long-term reliability if the maximum power dissipation limit is exceeded.

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 28 is a typical connection diagram illustrating a circuit for which the input HPF cutoff frequency is about 5 Hz.



(1) C1 and C2: A 1-µF capacitor gives a 5.3-Hz (τ = 1 µF * 30 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on setting time of 30 ms at power up.

(2) C3 and C4: Bypass capacitors, 0.1-µF ceramic and 10-µF tantalum or aluminum electrolytic, depending on layout and power supply

(3) C5 and C6: 4.7-µF tantalum or aluminum electrolytic capacitors

Figure 28. Typical Circuit Connection

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1801U	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1801U
PCM1801U/2K	Active	Production	SOIC (D) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1801U
PCM1801U/2KG4	Active	Production	SOIC (D) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See PCM1801U/2K	PCM1801U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

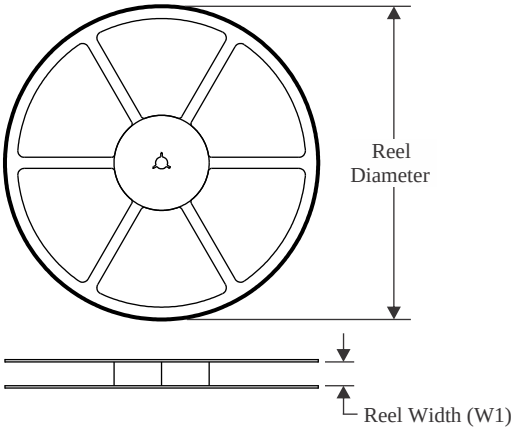
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

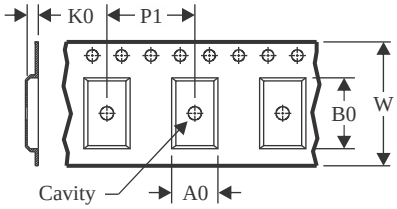
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

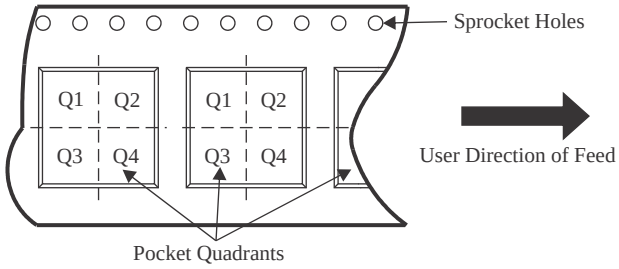


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

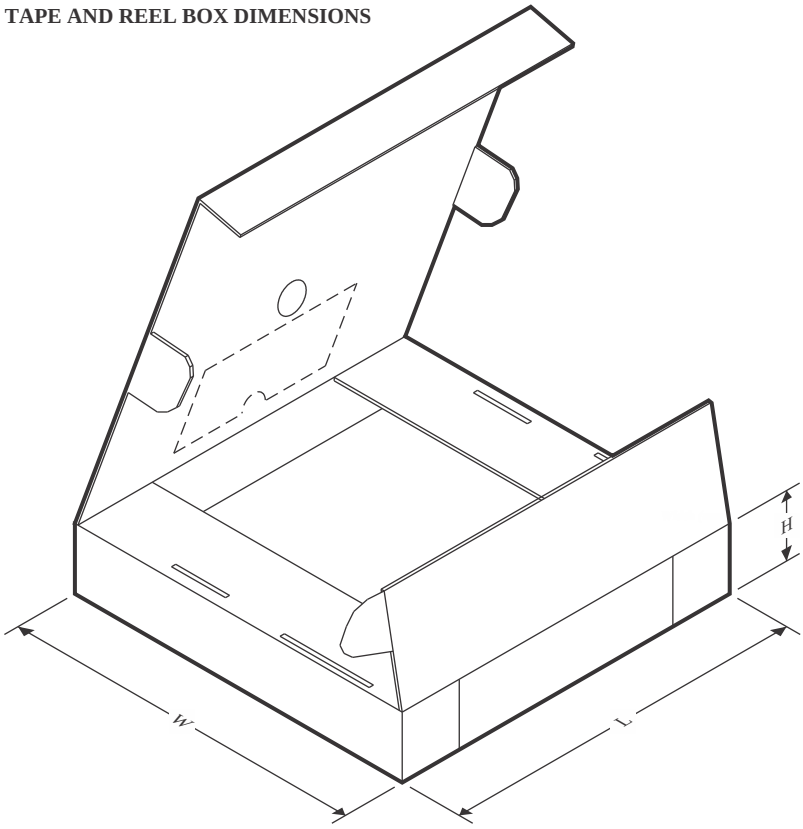
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1801U/2K	SOIC	D	14	2000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

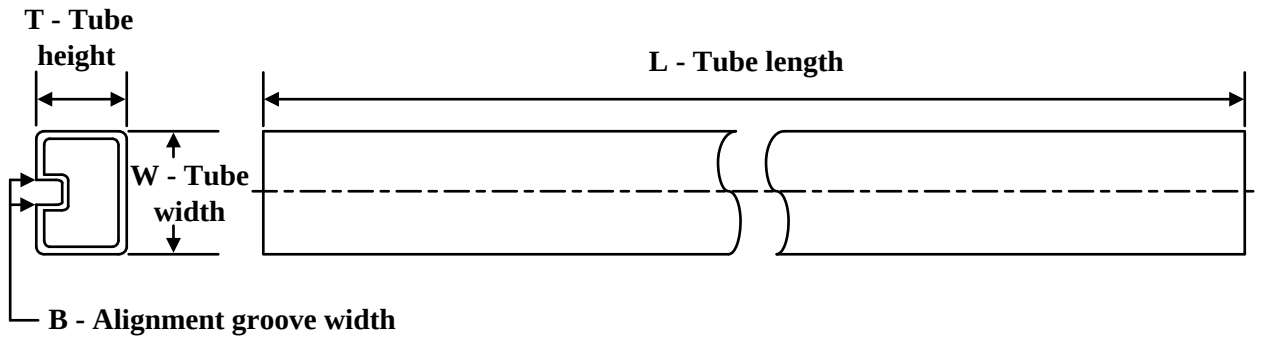
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

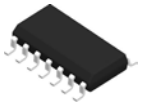
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1801U/2K	SOIC	D	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1801U	D	SOIC	14	50	506.6	8	3940	4.32

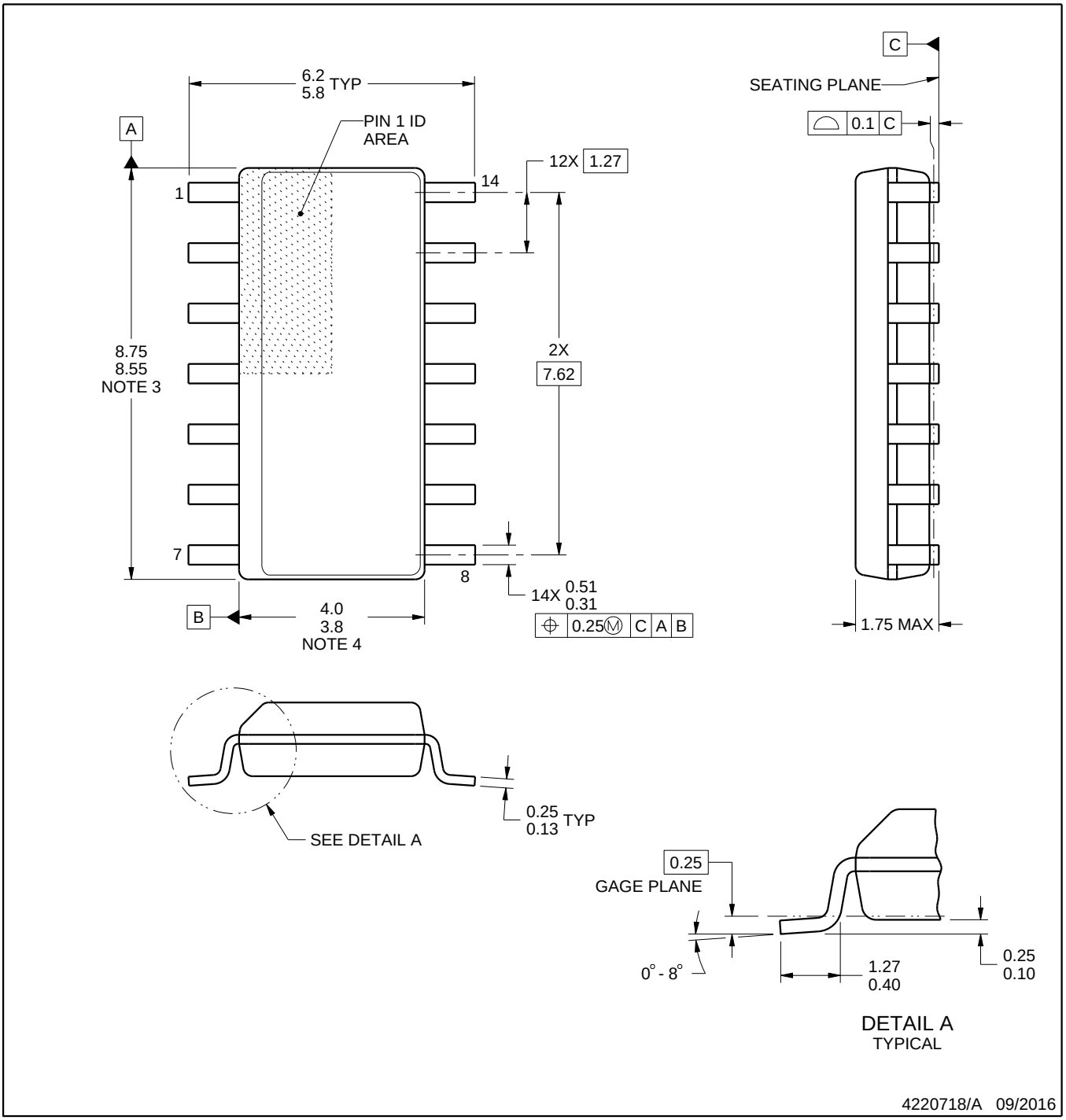


PACKAGE OUTLINE

D0014A

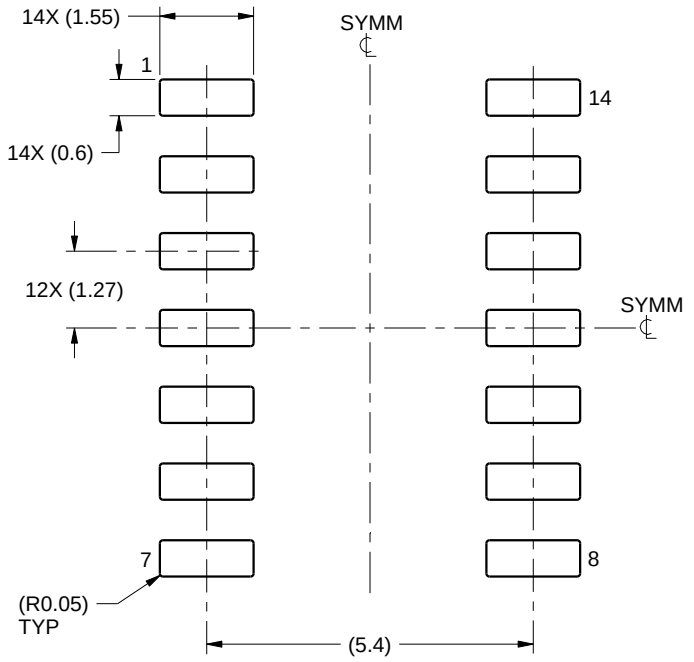
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

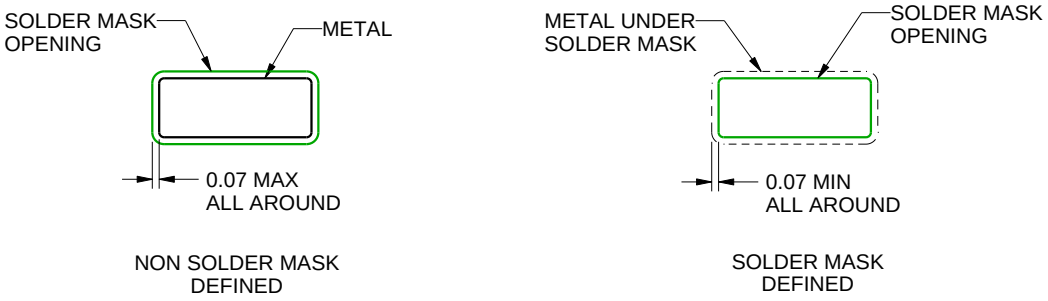


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

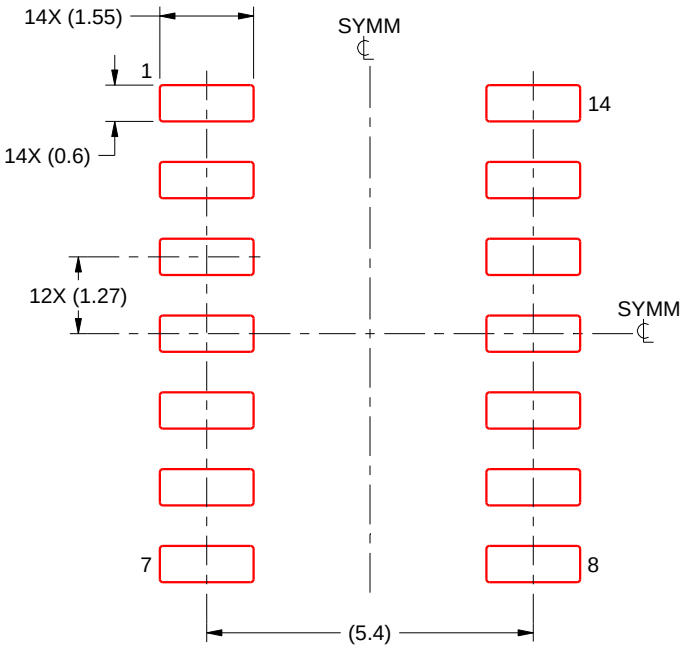
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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