I²C Controlled 4.5A Single Cell USB/Adapter Charger
With Narrow VDC Power Path Management and USB OTG

Check for Samples: bq24190, bq24192, bq24192l, bq24193

FEATURES

• High Efficiency 4.5A Switch Mode Charger
  – 92% Charge Efficiency at 2A, 90% at 4A
  – Accelerate Charge Time by Battery Path Impedance Compensation

• Highest Battery Discharge Efficiency with 12mΩ Battery Discharge MOSFET up to 9A Discharge Current

• Single Input USB-compliant/Adapter Charger
  – USB Host or Charging Port D+/D- Detection Compatible to USB Battery Charger Spec 1.2
  – Input Voltage and Current Limit Supports USB2.0 and USB 3.0
  – Input Current Limit: 100mA, 150mA, 500mA, 900mA, 1.2A, 1.5A, 2A and 3A

• 3.9V–17V Input Operating Voltage Range
  – Support All Kinds of Adapter with Input Voltage DPM Regulation

• USB OTG 5V at 1.3A Synchronous Boost Converter Operation
  – 93% 5V Boost Efficiency at 1A

• Narrow VDC (NVDC) Power Path Management
  – Instant-on Works with No Battery or Deeply Discharged Battery
  – Ideal Diode Operation in Battery Supplement Mode

• 1.5MHz Switching Frequency for Low Profile Inductor

• Autonomous Battery Charging with or without Host Management
  – Battery Charge Enable
  – Battery Charge Preconditioning
  – Charge Termination and Recharge

• High Accuracy (0°C to 125°C)
  – ±0.5% Charge Voltage Regulation
  – ±7% Charge Current Regulation
  – ±7.5% Input Current Regulation
  – ±2% Output Regulation in Boost Mode

• High Integration
  – Power Path Management
  – Synchronous Switching MOSFETs
  – Integrated Current Sensing
  – Bootstrap Diode
  – Internal Loop Compensation

• Safety
  – Battery Temperature Sensing and Charging Safety Timer
  – JEITA Guideline Compliant (bq24193)
  – Thermal Regulation and Thermal Shutdown
  – Input System Over-Voltage Protection
  – MOSFET Over-Current Protection

• Charge Status Outputs for LED or Host Processor

• Low Battery Leakage Current and Support Shipping Mode

• 4mm x 4mm QFN-24 Package

APPLICATIONS

• Tablet PC
• Smart Phone
• Portable Audio Speaker
• Portable Media Players
• Internet Devices

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The bq24190, bq24192, bq24192I, and bq24193 are highly-integrated switch-mode battery charge management and system power path management devices for single cell Li-Ion and Li-polymer battery in a wide range of tablet and other portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I\(^2\)C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port and high power DC adapter. To set the default input current limit, the bq24190 detects the input source following the USB battery charging spec 1.2, and the bq24192, bq24192I, and bq24193 takes the results from detection circuit in the system, such as USB PHY device. The bq24190,192,192I, and 193 are compliant with USB 2.0 and USB 3.0 power specifications with input current and voltage regulation. Meanwhile, the bq24190, bq24192, bq24192I, and bq24193 meets USB On-the-Go operation power rating specification by supplying 5V on the VBUS with a current limit up to 1.3A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode operation prevents overloading the input source.

The devices initiate and complete a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The bq24190, bq24192, bq24192I, and bq24193 provide various safety features for battery charging and system operation, including dual pack negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The bq24193 supports JEITA guideline compliant temperature profile. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable).

The STAT output reports the charging status and any fault conditions. The PG output in the bq24192, bq24192I, and bq24193 indicates if a good power source is present. The INT immediately notifies the host when a fault occurs.

The bq24190, bq24192, bq24192I, and bq24193 are available in a 24-pin, 4x4 mm\(^2\) thin QFN package.

bq2419x Family Table

<table>
<thead>
<tr>
<th></th>
<th>bq24190</th>
<th>bq24192</th>
<th>bq24192I</th>
<th>bq24193</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>I(^2)C Address</strong></td>
<td>6BH</td>
<td>6BH</td>
<td>6BH</td>
<td>6BH</td>
</tr>
<tr>
<td><strong>USB Detection</strong></td>
<td>D+/D−</td>
<td>PSEL</td>
<td>PSEL</td>
<td>PSEL</td>
</tr>
<tr>
<td><strong>Default VINDPM</strong></td>
<td>4.36V</td>
<td>4.36V</td>
<td>4.44V</td>
<td>4.36V</td>
</tr>
<tr>
<td><strong>Default Battery Voltage</strong></td>
<td>4.208V</td>
<td>4.208V</td>
<td>4.112V</td>
<td>4.208V</td>
</tr>
<tr>
<td><strong>Default Charge Current</strong></td>
<td>2.048A</td>
<td>2.048A</td>
<td>1.024A</td>
<td>2.048A</td>
</tr>
<tr>
<td><strong>Default Adapter Current Limit</strong></td>
<td>1.5A</td>
<td>3A</td>
<td>1.5A</td>
<td>3A</td>
</tr>
<tr>
<td><strong>Maximum Pre-charge Current</strong></td>
<td>2.048A</td>
<td>2.048A</td>
<td>640mA</td>
<td>2.048A</td>
</tr>
<tr>
<td><strong>Charging Temperature Profile</strong></td>
<td>Cold/Hot</td>
<td>Cold/Hot</td>
<td>Cold/Hot</td>
<td>JEITA</td>
</tr>
<tr>
<td></td>
<td>2 TS pins</td>
<td>2 TS pins</td>
<td>2 TS pins</td>
<td>1 TS pin</td>
</tr>
<tr>
<td><strong>Status Output</strong></td>
<td>STAT</td>
<td>STAT, PG</td>
<td>STAT, PG</td>
<td>STAT, PG</td>
</tr>
<tr>
<td><strong>STAT During Fault</strong></td>
<td>Blinking @ 1Hz</td>
<td>Blinking @ 1Hz</td>
<td>10k to ground</td>
<td>Blinking @ 1Hz</td>
</tr>
<tr>
<td>PART NUMBER</td>
<td>PART MARKING</td>
<td>PACKAGE</td>
<td>ORDERING NUMBER</td>
<td>QUANTITY</td>
</tr>
<tr>
<td>-------------</td>
<td>--------------</td>
<td>-----------------</td>
<td>-----------------</td>
<td>----------</td>
</tr>
<tr>
<td>bq24190</td>
<td>bq24190</td>
<td>24-pin 4mmx4mm VQFN</td>
<td>bq24190RGER</td>
<td>3000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bq24190RGET</td>
<td>250</td>
</tr>
<tr>
<td>bq24192</td>
<td>bq24192</td>
<td>24-pin 4mmx4mm VQFN</td>
<td>bq24192RGER</td>
<td>3000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bq24192RGET</td>
<td>250</td>
</tr>
<tr>
<td>bq24192I</td>
<td>bq24192I</td>
<td>24-pin 4mmx4mm VQFN</td>
<td>bq24192IRGER</td>
<td>3000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bq24192IRGET</td>
<td>250</td>
</tr>
<tr>
<td>bq24193</td>
<td>bq24193</td>
<td>24-pin 4mmx4mm VQFN</td>
<td>bq24193RGER</td>
<td>3000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bq24193RGET</td>
<td>250</td>
</tr>
</tbody>
</table>
Figure 1. bq24190 with D+/D- Detection and USB On-The-Go (OTG)

Figure 2. bq24192 with PSEL and USB On-The-Go (OTG)
Figure 3. bq24192I with PSEL, USB On-The-Go (OTG), No Thermistor Connections

Figure 4. bq24193 with PSEL, USB On-The-Go (OTG) and Support JEITA Profile
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NAME</strong></td>
<td><strong>NO.</strong></td>
<td><strong>DESCRIPTION</strong></td>
</tr>
<tr>
<td><strong>VBUS</strong></td>
<td>1,24</td>
<td>P Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. (Refer to Application Information Section for details)</td>
</tr>
<tr>
<td><strong>D+</strong></td>
<td>2</td>
<td>I Analog Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.</td>
</tr>
<tr>
<td><strong>D−</strong></td>
<td>3</td>
<td>I Analog Negative line of the USB data line pair. D+/D− based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.</td>
</tr>
<tr>
<td><strong>PG</strong></td>
<td>3</td>
<td>O Digital Open drain active low power good indicator. Connect to the pull up rail via 10kohm resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30mA.</td>
</tr>
<tr>
<td><strong>STAT</strong></td>
<td>4</td>
<td>O Digital Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kohm. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin in bq24190, bq24192, bq24193 blinks at 1Hz, and STAT pin in bq24192I has a 10kΩ resistor to ground.</td>
</tr>
<tr>
<td><strong>SCL</strong></td>
<td>5</td>
<td>I Digital I²C Interface clock. Connect SCL to the logic rail through a 10kΩ resistor.</td>
</tr>
<tr>
<td><strong>SDA</strong></td>
<td>6</td>
<td>I/O Digital I²C Interface data. Connect SDA to the logic rail through a 10kΩ resistor.</td>
</tr>
<tr>
<td><strong>INT</strong></td>
<td>7</td>
<td>O Digital Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256us pulse to host to report charger device status and fault.</td>
</tr>
<tr>
<td><strong>OTG</strong></td>
<td>8</td>
<td>I Digital USB current limit selection pin during buck mode, and active high enable pin during boost mode. In buck mode with USB host (PSEL=High), when OTG = High, IIN limit = 500mA and when OTG = Low, IIN limit = 100mA. The boost mode is activated when the REG01[5:4]=10 and OTG pin is High.</td>
</tr>
<tr>
<td><strong>CE</strong></td>
<td>9</td>
<td>I Digital Active low Charge Enable pin. Battery charging is enabled when REG01[5:4]=01 and CE pin = Low. CE pin must be pulsed high or low.</td>
</tr>
<tr>
<td><strong>ILIM</strong></td>
<td>10</td>
<td>I Analog ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1V. A resistor is connected from ILIM pin to ground to set the maximum limit as ( I_{\text{MAX}} = \frac{(1V)}{R_{\text{ILIM}}} \times 530 ). The actual input current limit is the lower one set by ILIM and by ( \frac{1}{2} ) REG00[2:0]. The minimum input current programmed on ILIM pin is 500mA.</td>
</tr>
</tbody>
</table>
### PIN FUNCTIONS (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS1</td>
<td>I</td>
<td>Temperature qualification voltage input #1. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be shorted together in bq24193.</td>
</tr>
<tr>
<td>TS2</td>
<td>I</td>
<td>Temperature qualification voltage input #2. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS2 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be shorted together in bq24193.</td>
</tr>
<tr>
<td>BAT</td>
<td>P</td>
<td>Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.</td>
</tr>
<tr>
<td>SYS</td>
<td>P</td>
<td>System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. (Refer to Application Information Section for inductor and capacitor selection)</td>
</tr>
<tr>
<td>PGND</td>
<td>P</td>
<td>Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.</td>
</tr>
<tr>
<td>SW</td>
<td>O</td>
<td>Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047µF bootstrap capacitor from SW to BTST.</td>
</tr>
<tr>
<td>BTST</td>
<td>P</td>
<td>PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047µF bootstrap capacitor from SW to BTST.</td>
</tr>
<tr>
<td>REGN</td>
<td>P</td>
<td>PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. For VBUS above 6V, connect 1-µF ceramic capacitor from REGN to analog GND. For VBUS below 6V, connect a 4.7-µF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS1 and TS2 pins.</td>
</tr>
<tr>
<td>PMID</td>
<td>O</td>
<td>Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Given the total input capacitance, connect a 1-µF capacitor on VBUS to PGND, and the rest all on PMID to PGND. (Refer to Application Information Section for details)</td>
</tr>
<tr>
<td>PowerPAD</td>
<td>–</td>
<td>Exposed pad beneath the IC for heat dissipation. Always solder PowerPAD™ to the board, and have vias on the Power Pad plane star-connecting to PGND and ground plane for high-current power converter.</td>
</tr>
</tbody>
</table>

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBUS</td>
</tr>
<tr>
<td>PMID, STAT, PG</td>
</tr>
<tr>
<td>BTST</td>
</tr>
<tr>
<td>SW</td>
</tr>
<tr>
<td>BAT, SYS (converter not switching)</td>
</tr>
<tr>
<td>SDA, SCL, INT, OTG, ILIM, REGN, TS1, TS2, CE, PSEL, D+, D−</td>
</tr>
<tr>
<td>BTST TO SW</td>
</tr>
<tr>
<td>PGND to GND</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUTPUT SINK CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT, STAT, PG</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction temperature</td>
<td>−40°C to 150°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>−65°C to 150°C</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>( V )</td>
<td>3.9</td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>( A )</td>
<td>3</td>
</tr>
<tr>
<td>( I_{SYS} )</td>
<td>( A )</td>
<td>4.5</td>
</tr>
<tr>
<td>( V_{BAT} )</td>
<td>( V )</td>
<td>4.4</td>
</tr>
</tbody>
</table>
**RECOMMENDED OPERATING CONDITIONS (continued)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{\text{BAT}}$</td>
<td>Fast charging current</td>
<td>4.5</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Discharging current with internal MOSFET</td>
<td>6 (continuous)</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>9 (peak)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(up to 1 sec duration)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating free-air temperature range</td>
<td>–40</td>
<td>°C</td>
<td>85</td>
<td></td>
</tr>
</tbody>
</table>

**THERMAL INFORMATION**

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>RGE PACKAGE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>32.2</td>
</tr>
<tr>
<td>$\theta_{JC\text{top}}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>29.8</td>
</tr>
<tr>
<td>$\theta_{JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>9.1</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
<td>0.3</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
<td>9.1</td>
</tr>
<tr>
<td>$\theta_{JC\text{bot}}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>2.2</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

**ELECTRICAL CHARACTERISTICS**

$V_{\text{BUS UVLOZ}} < V_{\text{VBUS}} < V_{\text{ACOV}}$ and $V_{\text{BUS}} > V_{\text{BAT}}$, $T_J = –40^\circ C$ to $125^\circ C$ and $T_J = 25^\circ C$ for typical values unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{\text{BAT}}$</td>
<td>Battery discharge current (BAT, SW, SYS)</td>
<td>$V_{\text{VBUS}} &lt; V_{\text{UVLO}}, V_{\text{BAT}} = 4.2$ V, leakage between BAT and VBUS</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1)</td>
<td>12</td>
<td>20</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Z Mode, or no VBUS, REG07[5] = 0, $–40^\circ C – 85^\circ C$</td>
<td>32</td>
<td>55</td>
<td>µA</td>
</tr>
<tr>
<td>$i_{\text{VBUS}}$</td>
<td>Input supply current (VBUS)</td>
<td>$V_{\text{BUS}} = 5$ V, High-Z mode</td>
<td>15</td>
<td>30</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{BUS}} = 17$ V, High-Z mode</td>
<td>30</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{BUS}} &gt; V_{\text{UVLO}}, V_{\text{BUS}} &gt; V_{\text{BAT}},$ converter not switching</td>
<td>1.5</td>
<td>3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{BUS}} &gt; V_{\text{UVLO}}, V_{\text{BUS}} &gt; V_{\text{BAT}},$ converter switching, $V_{\text{BAT}} = 3.2$ V, $I_{\text{SYS}} = 0$ A</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{BUS}} &gt; V_{\text{UVLO}}, V_{\text{BUS}} &gt; V_{\text{BAT}},$ converter switching, $V_{\text{BAT}} = 3.8$ V, $I_{\text{SYS}} = 0$ A</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$i_{\text{TOTBOOST}}$</td>
<td>Battery Discharge Current in boost mode</td>
<td>$VBAT=4.2$ V, Boost mode, $I_{\text{VBUS}} = 0$ A, converter switching</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{\text{BUS OP}}$</td>
<td>VBUS operating range</td>
<td>3.9</td>
<td>17</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{BUS UVLOZ}}$</td>
<td>VBUS for active PC, no battery</td>
<td>$V_{\text{VBUS}}$ rising</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{SLEEP}}$</td>
<td>Sleep mode falling threshold</td>
<td>$V_{\text{VBUS}}$ falling, $V_{\text{BUS}}&lt;\text{VBAT}$</td>
<td>35</td>
<td>80</td>
<td>120</td>
</tr>
<tr>
<td>$V_{\text{SLEEPZ}}$</td>
<td>Sleep mode rising threshold</td>
<td>$V_{\text{VBUS}}$ rising, $V_{\text{BUS}}&lt;\text{VBAT}$</td>
<td>170</td>
<td>250</td>
<td>300</td>
</tr>
<tr>
<td>$V_{\text{ACOV}}$</td>
<td>VBUS over-voltage rising threshold</td>
<td>$V_{\text{VBUS}}$ rising</td>
<td>17.4</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{ACOV HYST}}$</td>
<td>VBUS Over-Voltage Falling Hysteresis</td>
<td>$V_{\text{VBUS}}$ falling</td>
<td>700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{BAT UVLOZ}}$</td>
<td>Battery for active PC, no VBUS</td>
<td>$V_{\text{BAT}}$ rising</td>
<td>2.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{BAT DPL}}$</td>
<td>Battery depletion threshold</td>
<td>$V_{\text{BAT}}$ falling</td>
<td>2.4</td>
<td>2.6</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{BAT DPL HY}}$</td>
<td>Battery depletion rising hysteresis</td>
<td>$V_{\text{BAT}}$ rising</td>
<td>170</td>
<td>230</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{VBUS MIN}}$</td>
<td>Bad adapter detection threshold</td>
<td>$V_{\text{VBUS}}$ falling</td>
<td>3.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{BADSRC}}$</td>
<td>Bad adapter detection current source</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{BADSRC}}$</td>
<td>Bad source detection duration</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

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### ELECTRICAL CHARACTERISTICS (continued)

\( V_{\text{VBUS UVLOZ}} < V_{\text{VBUS}} < V_{\text{ACOV}} \) and \( V_{\text{VBUS}} > V_{\text{SLEEP}} \), \( T_J = -40^\circ \text{C} \) to 125\(^\circ \text{C} \) and \( T_J = 25^\circ \text{C} \) for typical values unless otherwise noted.

#### POWER PATH MANAGEMENT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{SYS_RANGE}} )</td>
<td>System regulation voltage ( I_{\text{sys}} = 0 , \text{A}, Q4 \text{off}, V_{\text{BAT}} \text{up to 4.2,V, REG01[3:1]}=101, V_{\text{SYS_MIN}} = 3.5 , \text{V} )</td>
<td>3.5</td>
<td>4.35</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{SYS_MIN}} )</td>
<td>System voltage output ( \text{REG01[3:1]}=101, V_{\text{SYS_MIN}} = 3.5 , \text{V} )</td>
<td>3.55</td>
<td>3.65</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{ON_RBFET}} )</td>
<td>Internal top reverse blocking MOSFET on-resistance measured between VBUS and PMID</td>
<td>23</td>
<td>38</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{ON_HSFET}} )</td>
<td>Internal top switching MOSFET on-resistance between PMID and SW</td>
<td>27</td>
<td>35</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{ON_LSFET}} )</td>
<td>Internal bottom switching MOSFET on-resistance between SW and PGND</td>
<td>27</td>
<td>45</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{FWD}} )</td>
<td>BATFET forward voltage in supplement mode</td>
<td>BAT discharge current 10mA</td>
<td>30</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{SYS_BAT}} )</td>
<td>SYS/BAT Comparator ( V_{\text{SYS}} \text{falling} )</td>
<td>3.4</td>
<td>3.55</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{BAT_GD_HYST}} )</td>
<td>Battery good comparator falling threshold ( V_{\text{BAT}} \text{falling} )</td>
<td>3.4</td>
<td>3.55</td>
<td>3.7</td>
<td>V</td>
</tr>
</tbody>
</table>

#### BATTERY CHARGER

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{BAT_REG_ACC}} )</td>
<td>Charge voltage regulation accuracy ( V_{\text{BAT}} = 4.112,\text{V} \text{and 4.208,V} )</td>
<td>–0.5%</td>
<td>0.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{CHG_REG_ACC}} )</td>
<td>Fast charge current regulation accuracy ( V_{\text{BAT}} = 3.8,\text{V}, I_{\text{CHG}} = 1792,\text{mA}, T_J = 25^\circ \text{C} )</td>
<td>–4%</td>
<td>4%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{CHG_20pct}} )</td>
<td>Charge current with 20% option on ( V_{\text{BAT}} = 3.1,\text{V}, I_{\text{CHG}} = 104,\text{mA}, \text{REG02}=03 )</td>
<td>75</td>
<td>100</td>
<td>125</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{\text{BAT_LOW_V_HYST}} )</td>
<td>Battery LOWV rising threshold Precharge to fast charge, ( \text{REG04[1]} = 1 )</td>
<td>2.8</td>
<td>3.0</td>
<td>3.1</td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{PRECHG_ACC}} )</td>
<td>Precharge current regulation accuracy ( V_{\text{BAT}} = 2.6,\text{V}, I_{\text{CHG}} = 256,\text{mA} )</td>
<td>–20%</td>
<td>20%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{TERM_ACC}} )</td>
<td>Termination current accuracy ( I_{\text{TERM}} = 256,\text{mA}, I_{\text{CHG}} = 960,\text{mA} )</td>
<td>–20%</td>
<td>20%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{SHORT}} )</td>
<td>Battery Short Voltage</td>
<td>V_{\text{BAT}} falling</td>
<td>1.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{SHORT_HYST}} )</td>
<td>Battery Short Voltage hysteresis</td>
<td>V_{\text{BAT}} rising</td>
<td>200</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SHORT}} )</td>
<td>Battery short current</td>
<td>V_{\text{BAT}} &lt; 2.2,\text{V}</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{RECHG}} )</td>
<td>Recharge threshold below V_{\text{BAT_REG}}</td>
<td>V_{\text{BAT}} falling, ( \text{REG04[0]} = 0 )</td>
<td>100</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{RECHG}} )</td>
<td>Recharge deglitch time</td>
<td>V_{\text{BAT}} falling, ( \text{REG04[0]}=0 )</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{ON_BATFET}} )</td>
<td>SYS-BAT MOSFET on-resistance ( T_J = 25^\circ \text{C} )</td>
<td>12</td>
<td>15</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( T_{\text{J}} )</td>
<td>( T_J = -40^\circ \text{C} \text{-- 125^\circ C} )</td>
<td>12</td>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### INPUT VOLTAGE/CURRENT REGULATION

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{INDPM_REG_ACC}} )</td>
<td>Input voltage regulation accuracy</td>
<td></td>
<td>–2%</td>
<td>2%</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{USB_DPM}} )</td>
<td>USB Input current regulation limit, VBUS = 5V, current pulled from SW</td>
<td>USB100</td>
<td>85</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{ADPT_DPM}} )</td>
<td>Input current regulation accuracy</td>
<td>Input current limit 1.5A</td>
<td>1.4</td>
<td>1.5</td>
<td>1.6</td>
</tr>
<tr>
<td>( I_{\text{IN_START}} )</td>
<td>Input current limit during system start up</td>
<td>( V_{\text{SYS}} &lt; 2.2,\text{V} )</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( K_{\text{LIM}} )</td>
<td>( I_{\text{LIM}} = K_{\text{LIM}} R_{\text{LIM}} )</td>
<td>LINDPM = 1.5A</td>
<td>440</td>
<td>485</td>
<td>530</td>
</tr>
</tbody>
</table>

#### D+/D- DETECTION

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{D_SRC}} )</td>
<td>D+ voltage source</td>
<td></td>
<td>0.5</td>
<td>0.6</td>
<td>0.7</td>
</tr>
<tr>
<td>( I_{\text{D_SRC}} )</td>
<td>D+ connection check current source</td>
<td></td>
<td>7</td>
<td>14</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{\text{D_SINK}} )</td>
<td>D– current sink</td>
<td></td>
<td>50</td>
<td>100</td>
<td>150</td>
</tr>
<tr>
<td>( I_{\text{D_LKG}} )</td>
<td>Leakage current into D+/D–</td>
<td>D–, switch open</td>
<td>–1</td>
<td>1</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{\text{D_LOW}} )</td>
<td>D+ Low comparator threshold</td>
<td>D+, switch open</td>
<td>–1</td>
<td>1</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( V_{\text{D_LOW_WAKE}} )</td>
<td>D– Low comparator threshold</td>
<td></td>
<td>0.7</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>( R_{\text{D_DWN}} )</td>
<td>D– Pulldown for connection check</td>
<td></td>
<td>250</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{\text{SDP_DEFAULT}} )</td>
<td>Charging timer with 100mA USB host in default mode</td>
<td></td>
<td>14.25</td>
<td>24.8</td>
<td>k( \Omega )</td>
</tr>
</tbody>
</table>

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**ELECTRICAL CHARACTERISTICS (continued)**

\[ V_{BUS, ULOZ} < V_{BUS} < V_{ACOV} \text{ and } V_{BUS} > V_{BAT} + V_{SLEEP}, T_J = -40^\circ C \text{ to } 125^\circ C \text{ and } T_J = 25^\circ C \text{ for typical values unless otherwise noted.} \]

<table>
<thead>
<tr>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BAT OVER-VOLTAGE PROTECTION</strong></td>
<td>Battery over-voltage threshold</td>
<td>[ V_{BAT} ] rising, as percentage of [ V_{BAT, REG} ]</td>
<td>104%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Battery over-voltage hysteresis</td>
<td>[ V_{BAT} ] falling, as percentage of [ V_{BAT, REG} ]</td>
<td>2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Battery over-voltage deglitch time to disable charge</td>
<td></td>
<td>1</td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td><strong>THERMAL REGULATION AND THERMAL SHUTDOWN</strong></td>
<td>Junction temperature regulation accuracy</td>
<td>[ REG0[1:0] = 11 ]</td>
<td>115</td>
<td>120</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown rising temperature</td>
<td>Temperature increasing</td>
<td>160</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown hysteresis</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown rising deglitch time</td>
<td>Temperature increasing delay</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown falling deglitch time</td>
<td>Temperature decreasing delay</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>COLD/HOT THERMISTER COMPARATOR (bq24190, bq24192, bq24192I)</strong></td>
<td>Cold temperature threshold, TS pin voltage rising threshold</td>
<td>Charger suspends charge. As Percentage to [ V_{REGN} ]</td>
<td>73%</td>
<td>73.5%</td>
<td>74%</td>
</tr>
<tr>
<td></td>
<td>Cold temperature hysteresis, TS pin voltage falling threshold</td>
<td>As Percentage to [ V_{REGN} ]</td>
<td>0.2%</td>
<td>0.4%</td>
<td>0.6%</td>
</tr>
<tr>
<td></td>
<td>Hot temperature TS pin voltage falling threshold</td>
<td>As Percentage to [ V_{REGN} ]</td>
<td>46.6%</td>
<td>47.2%</td>
<td>48.8%</td>
</tr>
<tr>
<td></td>
<td>Cut-off temperature TS pin voltage falling threshold</td>
<td>As Percentage to [ V_{REGN} ]</td>
<td>44.2%</td>
<td>44.7%</td>
<td>45.2%</td>
</tr>
<tr>
<td></td>
<td>Deglitch time for temperature out of range detection [ V_{TS} &gt; V_{LTF}, \text{ or } V_{TS} &lt; V_{TCO}, \text{ or } V_{TS} &lt; V_{HTF} ]</td>
<td></td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>JEITA THERMISTER COMPARATOR (bq24193)</strong></td>
<td>T1 (0°C) threshold, Charge suspended below this temperature</td>
<td>[ V_{TS} ] rising, As Percentage to [ V_{REGN} ]</td>
<td>70.2%</td>
<td>70.8%</td>
<td>71.4%</td>
</tr>
<tr>
<td></td>
<td>T1 hysteresis [ V_{TS} ] falling</td>
<td>Hysteresis, [ V_{TS} ] falling</td>
<td>0.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T2 (10°C) threshold, Charge back to [ I_{CHG}/2 ] and 4.2V below this temperature</td>
<td>[ V_{TS} ] rising, as percentage of [ V_{REGN} ]</td>
<td>68.0%</td>
<td>68.6%</td>
<td>69.2%</td>
</tr>
<tr>
<td></td>
<td>T2 hysteresis [ V_{TS} ] falling</td>
<td>Hysteresis, [ V_{TS} ] falling</td>
<td>0.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T3 (45°C) threshold, Charge back to [ I_{CHG} ] and 4.05V above this temperature</td>
<td>[ V_{TS} ] falling, as percentage of [ V_{REGN} ]</td>
<td>55.5%</td>
<td>56.1%</td>
<td>56.7%</td>
</tr>
<tr>
<td></td>
<td>T3 hysteresis [ V_{TS} ] rising</td>
<td>Hysteresis, [ V_{TS} ] rising</td>
<td>0.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T5 (60°C) threshold, charge suspended above this temperature</td>
<td>[ V_{TS} ] falling, as percentage of [ V_{REGN} ]</td>
<td>47.6%</td>
<td>48.1%</td>
<td>48.6%</td>
</tr>
<tr>
<td></td>
<td>T5 hysteresis [ V_{TS} ] rising</td>
<td>Hysteresis, [ V_{TS} ] rising</td>
<td>1.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CHARGE OVER-CURRENT COMPARATOR</strong></td>
<td>HSFET over-Current threshold</td>
<td>[ I_{HSFET} ]</td>
<td>5.3</td>
<td>7</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>System over load threshold</td>
<td>[ I_{BATFET} ]</td>
<td>9</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td><strong>CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)</strong></td>
<td>LSFET charge under-current falling threshold</td>
<td>From sync mode to non-sync mode</td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>PWM OPERATION</strong></td>
<td>PWM Switching frequency, and digital clock</td>
<td>[ F_{SW} ]</td>
<td>1300</td>
<td>1500</td>
<td>1700</td>
</tr>
<tr>
<td></td>
<td>Maximum PWM duty cycle</td>
<td>[ D_{MAX} ]</td>
<td>97%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bootstrap refresh comparator threshold [ V_{BTST, REFRESH} ]</td>
<td></td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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ELECTRICAL CHARACTERISTICS (continued)

$V_{\text{VBUSUVLOZ}} < V_{\text{VBUS}} < V_{\text{ACOV}}$ and $V_{\text{VBUS}} > V_{\text{BAT}} + V_{\text{SLEEP}}$, $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values unless other noted.

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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{OTG, REG}}$</td>
<td>OTG output voltage</td>
<td>$I(\text{VBUS}) = 0$</td>
<td>5.00</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OTG, ACC}}$</td>
<td>OTG output voltage accuracy</td>
<td>$I(\text{VBUS}) = 0$</td>
<td>-2%</td>
<td>2%</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{OTG}}$</td>
<td>OTG mode output current</td>
<td>REG0[0] = 0</td>
<td>0.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{OTG}}$</td>
<td>OTG over-voltage threshold</td>
<td>REG0[0] = 1</td>
<td>1.3</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OTG, OVP}}$</td>
<td>OTG under current threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OTG, ILIM}}$</td>
<td>LSFET cycle-by-cycle current limit</td>
<td></td>
<td>3.2</td>
<td>4.6</td>
<td>A</td>
</tr>
<tr>
<td>$V_{\text{OTG, HZCP}}$</td>
<td>HSFET under current falling threshold</td>
<td>REG0[0] = 1</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{RBFET, OCP}}$</td>
<td>RBFET over-current threshold</td>
<td>REG0[0] = 1</td>
<td>1.4</td>
<td>1.8</td>
<td>2.7</td>
</tr>
<tr>
<td>$V_{\text{REGN}}$</td>
<td>REGN LDO output voltage</td>
<td>$V_{\text{VBUS}} = 10\text{V}$, $I_{\text{REGN}} = 40\text{mA}$</td>
<td>5.6</td>
<td>6</td>
<td>6.4</td>
</tr>
<tr>
<td>$I_{\text{REGN}}$</td>
<td>REGN LDO current limit</td>
<td>$V_{\text{VBUS}} = 10\text{V}$, $V_{\text{REGN}} = 3.8\text{V}$</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IH}}$</td>
<td>Input high threshold level</td>
<td>VPULL-UP = 1.8V, SDA and SCL</td>
<td>1.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IL}}$</td>
<td>Input low threshold level</td>
<td>VPULL-UP = 1.8V, SDA and SCL</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OL}}$</td>
<td>Output low saturation voltage</td>
<td>Sink current = 5 mA</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{BIAS}}$</td>
<td>High-level leakage current</td>
<td>Pull up rail 1.8V</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{SCL}}$</td>
<td>SCL clock frequency</td>
<td>REGN LDO enabled</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{HZ}}$</td>
<td>Digital crude clock</td>
<td>REGN LDO disabled</td>
<td>15</td>
<td>35</td>
<td>50</td>
</tr>
<tr>
<td>$f_{\text{DIG}}$</td>
<td>Digital clock</td>
<td>REGN LDO enabled</td>
<td>1300</td>
<td>1500</td>
<td>1700</td>
</tr>
<tr>
<td>$t_{\text{WDT}}$</td>
<td>REG0[5:4]=11</td>
<td>REGN LDO enabled</td>
<td>136</td>
<td>160</td>
<td>sec</td>
</tr>
</tbody>
</table>

TYPICAL CHARACTERISTICS

Table 1. Tables of Figures

<table>
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<tr>
<th>FIGURE NO.</th>
<th>FIGURE</th>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Figure 5</td>
<td>Figure 5</td>
</tr>
<tr>
<td>6</td>
<td>Figure 6</td>
<td>Figure 6</td>
</tr>
<tr>
<td>7</td>
<td>Figure 7</td>
<td>Figure 7</td>
</tr>
<tr>
<td>8</td>
<td>Figure 8</td>
<td>Figure 8</td>
</tr>
<tr>
<td>9</td>
<td>Figure 9</td>
<td>Figure 9</td>
</tr>
<tr>
<td>10</td>
<td>Figure 10</td>
<td>Figure 10</td>
</tr>
<tr>
<td>11</td>
<td>Figure 11</td>
<td>Figure 11</td>
</tr>
<tr>
<td>12</td>
<td>Figure 12</td>
<td>Figure 12</td>
</tr>
<tr>
<td>13</td>
<td>Figure 13</td>
<td>Figure 13</td>
</tr>
<tr>
<td>14</td>
<td>Figure 14</td>
<td>Figure 14</td>
</tr>
<tr>
<td>15</td>
<td>Figure 15</td>
<td>Figure 15</td>
</tr>
<tr>
<td>16</td>
<td>Figure 16</td>
<td>Figure 16</td>
</tr>
<tr>
<td>17</td>
<td>Figure 17</td>
<td>Figure 17</td>
</tr>
<tr>
<td>18</td>
<td>Figure 18</td>
<td>Figure 18</td>
</tr>
<tr>
<td>19</td>
<td>Figure 19</td>
<td>Figure 19</td>
</tr>
</tbody>
</table>
**TYPICAL CHARACTERISTICS (continued)**

Table 1. Tables of Figures (continued)

<table>
<thead>
<tr>
<th>Figure No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIGURE 20</td>
<td>Load Transient during Supplement Mode (VBUS 9V, IIN 1.5A, VBAT 3.8V)</td>
</tr>
<tr>
<td>FIGURE 21</td>
<td>PWM Switching Waveform (VBUS 12V, VBAT 3.8V, ICHG 3A)</td>
</tr>
<tr>
<td>FIGURE 22</td>
<td>PFM Switching Waveform (VBUS 9V, No Battery, ISYS 10 mA, Charge Disable)</td>
</tr>
<tr>
<td>FIGURE 23</td>
<td>Boost Mode Switching Waveform (VBAT 3.8V, ILOAD 1A)</td>
</tr>
<tr>
<td>FIGURE 24</td>
<td>Boost Mode Load Transient (VBAT 3.8V)</td>
</tr>
</tbody>
</table>

**FIGURE 5.** CHARGING EFFICIENCY vs CHARGING CURRENT

**FIGURE 6.** SYSTEM LIGHT LOAD EFFICIENCY vs SYSTEM LOAD CURRENT

**FIGURE 7.** BOOST MODE EFFICIENCY vs VBUS LOAD CURRENT

**FIGURE 8.** SYS VOLTAGE REGULATION vs SYSTEM LOAD
Figure 9. BOOST MODE VBUS VOLTAGE REGULATION vs VBUS LOAD CURRENT

Figure 10. SYS VOLTAGE vs TEMPERATURE

Figure 11. BAT VOLTAGE vs TEMPERATURE

Figure 12. INPUT CURRENT LIMIT vs TEMPERATURE

Figure 13. CHARGE CURRENT vs TEMPERATURE

Figure 14. bq24190 Power Up from USB100mA (VBAT 3.2V)
Figure 15. bq24192 Power Up with Charge Disabled (VBAT 3.2V)

Figure 16. bq24193 Power Up with Charge Enabled

Figure 17. Charge Enable (VBUS 5V)

Figure 18. Charge Disable (VBUS 12V)

Figure 19. Input Current DPM Response without Battery (VBUS 5V, IIN 3A, Charge Disable)

Figure 20. Load Transient during Supplement Mode (VBUS 9V, IIN 1.5A, VBAT 3.8V)
PWM Switching Waveform
(VBUS 12V, VBAT 3.8V, ICHG 3A)

Figure 21.

PFM Switching Waveform
(VBUS 9V, No Battery, ISYS 10 mA, Charge Disable)

Figure 22.

Boost Mode Switching Waveform
(VBAT 3.8V, ILOAD 1A)

Figure 23.

Boost Mode Load Transient (VBAT 3.8V)

Figure 24.
I²C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are read only.

### Input Source Control Register REG00 (bq24190, bq24192, bq24193 default 00110000, or 30; bq24192l default 00111000, or 38)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EN_HIZ</td>
</tr>
<tr>
<td>6</td>
<td>VINDPM[3]</td>
</tr>
<tr>
<td>5</td>
<td>VINDPM[2]</td>
</tr>
<tr>
<td>4</td>
<td>VINDPM[1]</td>
</tr>
<tr>
<td>3</td>
<td>VINDPM[0]</td>
</tr>
</tbody>
</table>

### Input Voltage Limit (Actual input current limit is the lower of I²C and ILIM)

- **Bit 2**: IINLIM[2] 000 – 100mA, 001 – 150mA, 010 – 500mA, 011 – 900mA, 100 – 1.2A, 101 – 1.5A, 110 – 2A, 111 – 3A Default SDP: 100mA (000)(OTG pin=0) or 500mA (010)(OTG pin=1) Default DCP/CDP: bq24190/bq24192I/bq24193: 1.5A (101), bq24192/bq24193: 3A (111)
- **Bit 1**: IINLIM[1] 110 – 2A, 111 – 3A
- **Bit 0**: IINLIM[0] 1.5A (101), bq24190/bq24192I: 1.5A (101), bq24192/bq24193: 3A (111)

### Power-On Configuration Register REG01 (default 00011011, or 1B)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Register Reset</td>
</tr>
<tr>
<td>6</td>
<td>I²C Watchdog</td>
</tr>
<tr>
<td>5</td>
<td>CHG_CONFIG[1]</td>
</tr>
<tr>
<td>4</td>
<td>CHG_CONFIG[0]</td>
</tr>
<tr>
<td>3</td>
<td>SYS_MIN[2]</td>
</tr>
<tr>
<td>2</td>
<td>SYS_MIN[1]</td>
</tr>
<tr>
<td>1</td>
<td>SYS_MIN[0]</td>
</tr>
<tr>
<td>0</td>
<td>BOOST_LIM</td>
</tr>
</tbody>
</table>

### Charger Configuration

- **Bit 5**: CHG_CONFIG[1] 00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG Default: Charge Battery (01)
- **Bit 4**: CHG_CONFIG[0] 10/11 – OTG

### Minimum System Voltage Limit

- **Bit 3**: SYS_MIN[2] 0.4V Offset: 3.0V, Range 3.0V-3.7V
- **Bit 2**: SYS_MIN[1] 0.2V Default: 3.5V (101)
- **Bit 1**: SYS_MIN[0] 0.1V

### Boost Mode Current Limit

- **Bit 0**: BOOST_LIM 0 – 500mA, 1 – 1.3A Default: 1.3A (1)

### Charge Current Control Register REG02 (bq24190, bq24192, bq24193 default 01100000, or 60; bq24192l default 00100000, or 20)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ICHG[5] 2048mA Offset: 512mA</td>
</tr>
<tr>
<td>6</td>
<td>ICHG[4] 1024mA Range: 512-4544mA</td>
</tr>
<tr>
<td>5</td>
<td>ICHG[3] 512mA Default: bq24190, bq24192, bq24193: 2048mA (011000), bq24192l: 1024mA (001000)</td>
</tr>
<tr>
<td>4</td>
<td>ICHG[2] 256mA</td>
</tr>
<tr>
<td>3</td>
<td>ICHG[1] 128mA</td>
</tr>
<tr>
<td>2</td>
<td>ICHG[0] 64mA</td>
</tr>
<tr>
<td>1</td>
<td>Reserved 0 - Reserved</td>
</tr>
<tr>
<td>0</td>
<td>FORCE_20PCT 0 – ICHG as REG02[7:2] programmed 1 – ICHG as 20% of REG02[7:2] programmed Default: ICHG as REG02[7:2] programmed (0)</td>
</tr>
</tbody>
</table>
Pre-Charge/Termination Current Control Register REG 03 (default 00010001, or 11)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>IPRECHG[3]</td>
<td>1024mA</td>
</tr>
<tr>
<td>Bit 6</td>
<td>IPRECHG[2]</td>
<td>512mA</td>
</tr>
<tr>
<td>Bit 5</td>
<td>IPRECHG[1]</td>
<td>256mA</td>
</tr>
<tr>
<td>Bit 4</td>
<td>IPRECHG[0]</td>
<td>128mA</td>
</tr>
<tr>
<td>Bit 3</td>
<td>ITERM[3]</td>
<td>1024mA</td>
</tr>
<tr>
<td>Bit 2</td>
<td>ITERM[2]</td>
<td>512mA</td>
</tr>
<tr>
<td>Bit 1</td>
<td>ITERM[1]</td>
<td>256mA</td>
</tr>
<tr>
<td>Bit 0</td>
<td>ITERM[0]</td>
<td>128mA</td>
</tr>
</tbody>
</table>

Termination Current Limit

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>IPRECHG[3]</td>
<td>1024mA</td>
</tr>
<tr>
<td>Bit 6</td>
<td>IPRECHG[2]</td>
<td>512mA</td>
</tr>
<tr>
<td>Bit 5</td>
<td>IPRECHG[1]</td>
<td>256mA</td>
</tr>
<tr>
<td>Bit 4</td>
<td>IPRECHG[0]</td>
<td>128mA</td>
</tr>
<tr>
<td>Bit 3</td>
<td>ITERM[3]</td>
<td>1024mA</td>
</tr>
<tr>
<td>Bit 2</td>
<td>ITERM[2]</td>
<td>512mA</td>
</tr>
<tr>
<td>Bit 1</td>
<td>ITERM[1]</td>
<td>256mA</td>
</tr>
<tr>
<td>Bit 0</td>
<td>ITERM[0]</td>
<td>128mA</td>
</tr>
</tbody>
</table>

Charge Voltage Control Register REG04 (bq24190, bq241192, bq241193 default: 10110010, or B2; bq24192I default 10011010, or 9A)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>VREG[5]</td>
<td>512mV</td>
</tr>
<tr>
<td>Bit 6</td>
<td>VREG[4]</td>
<td>256mV</td>
</tr>
<tr>
<td>Bit 5</td>
<td>VREG[3]</td>
<td>128mV</td>
</tr>
<tr>
<td>Bit 4</td>
<td>VREG[2]</td>
<td>64mV</td>
</tr>
<tr>
<td>Bit 3</td>
<td>VREG[1]</td>
<td>32mV</td>
</tr>
<tr>
<td>Bit 2</td>
<td>VREG[0]</td>
<td>16mV</td>
</tr>
</tbody>
</table>

Battery Precharge to Fast Charge Threshold

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 1</td>
<td>BATLOWV</td>
<td>0 – 2.8V, 1 – 3.0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: 3.0V (1)</td>
</tr>
</tbody>
</table>

Battery Recharge Threshold (below battery regulation voltage)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 0</td>
<td>VRECHG</td>
<td>0 – 100mV, 1 – 300mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: 100mV (0)</td>
</tr>
</tbody>
</table>

Charge Termination/Timer Control Register REG05 (default 10011010, or 9A)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>EN_TERM</td>
<td>0 – Disable, 1 – Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: Enable termination (1)</td>
</tr>
</tbody>
</table>

Termination Indicator Threshold

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 6</td>
<td>TERM_STAT</td>
<td>0 – Match ITERM, 1 – STAT pin high before actual termination when charge current below 800 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default Match ITERM (0)</td>
</tr>
</tbody>
</table>

I2C Watchdog Timer Setting

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 5</td>
<td>WATCHDOG[1]</td>
<td>00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s</td>
</tr>
<tr>
<td>Bit 4</td>
<td>WATCHDOG[0]</td>
<td>00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: 40s (01)</td>
</tr>
</tbody>
</table>

Charging Safety Timer Enable

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 3</td>
<td>EN_TIMER</td>
<td>0 – Disable, 1 – Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: Enable (1)</td>
</tr>
</tbody>
</table>

Fast Charge Timer Setting

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 2</td>
<td>CHG_TIMER[1]</td>
<td>00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs</td>
</tr>
<tr>
<td>Bit 1</td>
<td>CHG_TIMER[0]</td>
<td>00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: 8hours (01)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(See Charging Safety Timer for details)</td>
</tr>
</tbody>
</table>

JEITA Low Temperature Current Setting

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 0</td>
<td>JEITA_ISET</td>
<td>0 – 50%, 1 – 20%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Percentage w.r.t ICHG REG02[7:2]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default: 50% (0)</td>
</tr>
</tbody>
</table>
### IR Compensation / Thermal Regulation Control Register REG06 (default 00000011, or 03)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>BAT_COMP[2]</td>
<td>40mΩ</td>
</tr>
<tr>
<td>Bit 6</td>
<td>BAT_COMP[1]</td>
<td>20mΩ</td>
</tr>
<tr>
<td>Bit 5</td>
<td>BAT_COMP[0]</td>
<td>10mΩ</td>
</tr>
</tbody>
</table>

**IR Compensation Voltage Clamp (above regulation voltage)**

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 4</td>
<td>VCLAMP[2]</td>
<td>64mV</td>
</tr>
<tr>
<td>Bit 3</td>
<td>VCLAMP[1]</td>
<td>32mV</td>
</tr>
<tr>
<td>Bit 2</td>
<td>VCLAMP[0]</td>
<td>16mV</td>
</tr>
</tbody>
</table>

**Thermal Regulation Threshold**

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 1</td>
<td>TREG[1]</td>
<td>00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C</td>
</tr>
<tr>
<td>Bit 0</td>
<td>TREG[0]</td>
<td></td>
</tr>
</tbody>
</table>

### Misc Operation Control Register REG07 (default 01001011, or 4B)

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>DPDM_EN</td>
<td>0 – Not in D+/D– detection; 1 – Force D+/D– detection</td>
</tr>
</tbody>
</table>

**Safety Timer Setting during Input DPM and Thermal Regulation**

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 6</td>
<td>TMR2X_EN</td>
<td>0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation</td>
</tr>
</tbody>
</table>

**Force BATFET Off**

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 5</td>
<td>BATFET_Disable</td>
<td>0 – Allow Q4 turn on, 1 – Turn off Q4</td>
</tr>
<tr>
<td>Bit 4</td>
<td>JEITA_VSET (45°C-60°C)</td>
<td>0 – 4.05V, 1 – 4.2V</td>
</tr>
<tr>
<td>Bit 3</td>
<td>Reserved</td>
<td>1 - Reserved</td>
</tr>
<tr>
<td>Bit 2</td>
<td>Reserved</td>
<td>0 - Reserved</td>
</tr>
<tr>
<td>Bit 1</td>
<td>INT_MASK[1]</td>
<td>0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT</td>
</tr>
<tr>
<td>Bit 0</td>
<td>INT_MASK[0]</td>
<td>0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT</td>
</tr>
</tbody>
</table>

### System Status Register REG08

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>VBUS_STAT[1]</td>
</tr>
<tr>
<td>Bit 6</td>
<td>VBUS_STAT[0]</td>
</tr>
<tr>
<td>Bit 5</td>
<td>CHRG_STAT[1]</td>
</tr>
<tr>
<td>Bit 4</td>
<td>CHRG_STAT[0]</td>
</tr>
<tr>
<td>Bit 3</td>
<td>DPM_STAT</td>
</tr>
<tr>
<td>Bit 2</td>
<td>PG_STAT</td>
</tr>
<tr>
<td>Bit 1</td>
<td>THERM_STAT</td>
</tr>
<tr>
<td>Bit 0</td>
<td>VSYS_STAT</td>
</tr>
</tbody>
</table>
Fault Register REG09

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>WATCHDOG_FAULT</td>
</tr>
<tr>
<td>Bit 6</td>
<td>BOOST_FAULT</td>
</tr>
<tr>
<td>Bit 5</td>
<td>CHRG_FAULT[1]</td>
</tr>
<tr>
<td>Bit 4</td>
<td>CHRG_FAULT[0]</td>
</tr>
<tr>
<td>Bit 3</td>
<td>BAT_FAULT</td>
</tr>
<tr>
<td>Bit 2</td>
<td>NTC_FAULT[2]</td>
</tr>
<tr>
<td>Bit 1</td>
<td>NTC_FAULT[1]</td>
</tr>
<tr>
<td>Bit 0</td>
<td>NTC_FAULT[0]</td>
</tr>
</tbody>
</table>

Vendor / Part / Revision Status Register REG0A

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>Reserved</td>
</tr>
<tr>
<td>Bit 6</td>
<td>Reserved</td>
</tr>
<tr>
<td>Device Configuration</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>PN[1]</td>
</tr>
<tr>
<td>Bit 3</td>
<td>PN[0]</td>
</tr>
<tr>
<td>Bit 2</td>
<td>TSPROFILE</td>
</tr>
<tr>
<td>Bit 1</td>
<td>DEV_REG[0]</td>
</tr>
<tr>
<td>Bit 0</td>
<td>DEV_REG[1]</td>
</tr>
</tbody>
</table>

**DETAILED DESCRIPTION**

The bq24190, bq24192, bq24192I, bq24193 is an I²C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFT, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

**Device Power Up**

**Power-On-Reset (POR)**

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I²C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

**Power Up from Battery without DC Source**

If only battery is present and the voltage is above depletion threshold (V_BAT,DEPL), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low RDSON in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

**BATFET Turn Off**

The BATFET can be forced off by the host through I²C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery.

When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.
Shipping Mode

When end equipment is assembled, the system is connected to battery through BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage.

In order to keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4]=00) and disable BATFET (REG07[5]=1) at the same time.

Once the BATFET is disabled, the BATFET can be turned on by plugging in adapter.

Power Up from DC Source

When the DC source plugs in, the bq24190, bq24192, bq24192I, bq24193 checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS1/TS2 external resistors. The pull-up rail of STAT and PG can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.
1. VBUS above UVLOZ
2. VBUS above battery + V_{SLEEP} in buck mode or VBUS below battery + V_{SLEEP} in boost mode
3. After typical 220ms delay (100ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than 50µA from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

Input Source Qualification

After REGN LDO powers up, the bq24190, bq24192, bq24192I, bq24193 checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.
1. VBUS voltage below 18V (not in ACOV)
2. VBUS voltage above 3.8V when pulling 30mA (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high and the PG pin (bq24192, bq24192I, bq24193) goes low. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 1.5A.

After the PG is LOW or REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The bq24190 follows battery charging specification 1.2 (bc1.2) to detect input source through USB D+/D– lines. The bq24192, bq24192I, bq24193 sets input current limit through PSEL and OTG pins.

After the input current limit detection is done, the host can write to REG00[2:0] to change the input current limit.

D+/D– Detection Sets Input Current Limit in bq24190

The bq24190 contains a D+/D– based input source detection to program the input current limit. The D+/D– detection has two steps: data contact detect (DCD) followed by primary detection.
DCD (Data Contact Detection) uses a current source to detect when the D+/D- pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and REG08[2]=1 (power good)
- Turn on D+ I\textsubscript{DP\_SRC} and the D- pull-down resistor R\textsubscript{DM\_DWN} for 40ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec.
- Turn off I\textsubscript{DP\_SRC} and disconnect R\textsubscript{DM\_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V\textsubscript{DP\_SRC} on D+ and I\textsubscript{DM\_SINK} on D- for 40ms
- If PD is attached to a USB host (SDP), the D- is low. If PD is attached to a charging port (CDP or DCP), the D- is high
- Turn off V\textsubscript{DP\_SRC} and I\textsubscript{DM\_SINK}

Table 2 shows the input current limit setting after D+/D- detection.

### Table 2. bq24190 USB D+/D- Detection

<table>
<thead>
<tr>
<th>D+/D- DETECTION</th>
<th>OTG</th>
<th>INPUT CURRENT LIMIT</th>
<th>REG08[7:6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 sec timer expired in DCD</td>
<td>—</td>
<td>100 mA</td>
<td>00</td>
</tr>
<tr>
<td>(D+/D- floating)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB Host</td>
<td>LOW</td>
<td>100 mA</td>
<td>01</td>
</tr>
<tr>
<td>USB Host</td>
<td>HIGH</td>
<td>500 mA</td>
<td>01</td>
</tr>
<tr>
<td>Charging Port</td>
<td>—</td>
<td>1.5 A</td>
<td>10</td>
</tr>
</tbody>
</table>

### Table 3. bq24192, bq24192I, bq24193 Input Current Limit Detection

<table>
<thead>
<tr>
<th>PSEL</th>
<th>OTG</th>
<th>INPUT CURRENT LIMIT</th>
<th>REG08[7:6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>100 mA</td>
<td>01</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>500 mA</td>
<td>01</td>
</tr>
</tbody>
</table>

**PSEL/OTG Pins Set Input Current Limit in bq24192, bq24192I, bq24193**

The bq24192, bq24192I, bq24193 has PSEL instead of D+/D-. It directly takes the USB PHY device output to decide whether the input is USB host or charging port.
### HIZ State with 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100mA USB host, and the battery is above bat-good threshold (\(V_{\text{BATGD}}\)), the device follows battery charging spec and enters high impedance state (HIZ). In HIZ state, the device is in the lowest quiescent state with REGN LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be less than 30 µA. The system is supplied by the battery.

Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7]=0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.

In default mode, the charger IC will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

### Force Input Current Limit Detection

The host can force the charger device to run input current limit detection by setting REG07[7]=1. After the detection is complete, REG07[7] will return to 0 by itself.

### Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The bq24190, bq24192, bq24192I, bq24193 provides soft-start when ramp up the system rail. When the system rail is below 2.2V, the input current limit is forced to 100mA. After the system rises above 2.2V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

As a battery charger, the bq24190, bq24192, bq24192I, bq24193 deploys a 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal sawtooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

### Boost Mode Operation from Battery

The bq24190, bq24192, bq24192I, bq24193 supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500mA output requirement. The maximum output current is 1.3A. The boost operation can be enabled if the following conditions are valid:

1. BAT above BATLOWV threshold (\(V_{\text{BATLOWV}}\) set by REG04[1])
2. VBUS less than BAT+V\(_{\text{SLEEP}}\) (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4]=10)
4. After 220ms delay from boost mode enable

In boost mode, the bq24190, bq24192, bq24192I, bq24193 employs a 1.5MHz step-up switching regulator. Similar to buck operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

During boost mode, the status register REG08[7:6] is set to 11, the VBUS output is 5V and the output current can reach up to 500mA or 1.3A, selected via I2C (REG01[0]).
Any fault during boost operation, including VBUS over-voltage or over-current, sets the fault register REG09[6] to 1 and an INT is asserted.

**Power Path Management**

The bq24190, bq24192, bq24192I, bq24193 accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

**Narrow VDC Architecture**

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the $V_{DS}$ of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

![Figure 26. V(SYS) vs V(BAT)](image)

**Dynamic Power Management**

To meet maximum current limit in USB spec and avoid over loading the adapter, the bq24190, bq24192, bq24192I, bq24193 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

Figure 27 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current and 3.4V minimum system voltage setting.
Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET $V_{DS}$ stays at 30mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce $R_{DSON}$ until the BATFET is in full conduction. At this point onwards, the BATFET $V_{DS}$ linearly increases with discharge current. Figure 28 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

Battery Charging Management

The bq24190, bq24192, bq24192l, bq24193 charges 1-cell Li-Ion battery with up to 4.5A charge current for high capacity tablet battery. The 12mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.
Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the bq24190, bq24192, bq24192I, bq24193 can complete a charging cycle without host involvement. The device default charging parameters are listed in Table 4.

### Table 4. Charging Parameter Default Setting

<table>
<thead>
<tr>
<th>DEFAULT MODE</th>
<th>bq24190, bq24192</th>
<th>bq24192I</th>
<th>bq24193</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charging Voltage</td>
<td>4.208 V</td>
<td>4.112 V</td>
<td>4.208 V</td>
</tr>
<tr>
<td>Charging Current</td>
<td>2.036 A</td>
<td>1.012 A</td>
<td>2.036 A</td>
</tr>
<tr>
<td>Pre-charge Current</td>
<td>256 mA</td>
<td>256 mA</td>
<td>256 mA</td>
</tr>
<tr>
<td>Termination Current</td>
<td>256 mA</td>
<td>256 mA</td>
<td>256 mA</td>
</tr>
<tr>
<td>Temperature Profile</td>
<td>Hot/Cold</td>
<td>Hot/Cold</td>
<td>JEITA</td>
</tr>
<tr>
<td>Safety Timer</td>
<td>8 hours (1)</td>
<td>8 hours (1)</td>
<td>8 hours (1)</td>
</tr>
</tbody>
</table>

(1) See section Charging Safety Timer for more information.

A new charge cycle starts when the following conditions are valid:
- Converter starts
- Battery charging is enabled by I^2C register bit (REG01[5:4]) = 01 and CE is low
- No thermistor fault on TS1 and TS2
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the bq24190, bq24192, bq24192I, bq24193 automatically starts another charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

### Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

### Table 5. Charging Current Setting

<table>
<thead>
<tr>
<th>VBAT</th>
<th>CHARGING CURRENT</th>
<th>REG DEFAULT SETTING</th>
<th>REG08[5:4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;2V</td>
<td>100mA</td>
<td>–</td>
<td>01</td>
</tr>
<tr>
<td>2V-3V</td>
<td>REG03[7:4]</td>
<td>256mA</td>
<td>01</td>
</tr>
<tr>
<td>&gt;3V</td>
<td>REG02[7:2]</td>
<td>2048mA (bq24190/192/193) 1024mA (bq24192I)</td>
<td>10</td>
</tr>
</tbody>
</table>
If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

\[
V_{\text{BATREG.actual}} = V_{\text{BATREG.I2C}} + \text{lower of } (I_{\text{CHRG.ACTUAL}} \times R_{\text{COMP}}) \text{ and } V_{\text{CLAMP}}
\]  

\[ (1) \]

**Battery Path Impedance IR Compensation**

To speed up the charging cycle, we would like to stay in constant current mode as long as possible. In real system, the parasitic resistance, including routing, connector, MOSFETs and sense resistor in the battery pack, may force the charger device to move from constant current loop to constant voltage loop too early, extending the charge time.

The bq24190, bq24192, bq24192I, bq24193 allows the user to compensate for the parasitic resistance by increasing the voltage regulation set point according to the actual charge current and the resistance. For safe operation, the user should set the maximum allowed regulation voltage to REG06[4:2], and the minimum trace parasitic resistance (REG06[7:5]).

**Thermistor Qualification**

The high capacity battery usually has two or more single cells in parallel. The bq24190, bq24192, bq24192I provides two TS pins to monitor the thermistor (NTC) in each cell independently. The bq24193 applies JEITA profile with TS1/TS2 shorted.

**Cold/Hot Temperature Window (bq24190, bq24192, bq24192I)**

The bq24190, bq24192, bq24192I continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the \( V_{\text{LTF}} \) to \( V_{\text{HTF}} \) thresholds. During the charge cycle the battery temperature must be within the \( V_{\text{LTF}} \) to \( V_{\text{TCO}} \) thresholds, else the device suspends charging and waits until the battery temperature is within the \( V_{\text{LTF}} \) to \( V_{\text{HTF}} \) range.
When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

**Figure 30. TS Resistor Network**

Assuming a 103AT NTC thermistor is used on the battery pack Figure 31, the value RT1 and RT2 can be determined by using the following equation:

\[
RT2 = \frac{V_{\text{VREF}} \times R_{\text{TH,COLD}} \times R_{\text{TH,HOT}} \times \left( \frac{1}{V_{\text{LTH}}} - \frac{1}{V_{\text{TCO}}} \right)}{R_{\text{TH,HOT}} \times \left( \frac{V_{\text{VREF}}}{V_{\text{TCO}}} - 1 \right) - R_{\text{TH,COLD}} \times \left( \frac{V_{\text{VREF}}}{V_{\text{LTF}}} - 1 \right)}
\]

\[
RT1 = \frac{V_{\text{VREF}}}{V_{\text{LTF}}} - 1 \cdot \frac{1}{\frac{1}{RT2} + \frac{1}{R_{\text{TH,COLD}}}}
\]

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

- \(R_{\text{TH,COLD}} = 27.28 \, \text{kΩ}\)
- \(R_{\text{TH,HOT}} = 4.911 \, \text{kΩ}\)
- \(RT1 = 5.52 \, \text{kΩ}\)
- \(RT2 = 31.23 \, \text{kΩ}\)
**JEITA Guideline Compliance (bq24193)**

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the $V_{T1}$ to $V_{T5}$ thresholds. If TS voltage exceeds the T1–T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1–T2), JEITA recommends the charge current to be reduced to at least half of the charge current or lower. At warm temperature (T3–T5), JEITA recommends charge voltage less than 4.1V.

The bq24193 provides flexibility voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3–T5) can be 4.2V or 4.05V (REG07 bit[4]). The current setting at cool temperature (T1–T2) can be further reduced to 20% of fast charge current (REG05 bit[0]).

The resistor bias network has been updated as below.

$$
RT2 = \frac{V_{\text{VREF}} \times R_{\text{TH COLD}} \times R_{\text{TH HOT}} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{R_{\text{TH HOT}} \times \left( \frac{V_{\text{VREF}}}{VT5} - 1 \right) - R_{\text{TH COLD}} \times \left( \frac{V_{\text{VREF}}}{VT1} - 1 \right)}
$$

$$
RT1 = \frac{V_{\text{VREF}}}{VT1} - 1
\frac{1}{1} + \frac{1}{RT2 + R_{\text{TH COLD}}}
$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery,

- $R_{\text{TH T1}} = 27.28 \, \text{k}\Omega$
- $R_{\text{TH T5}} = 3.02 \, \text{k}\Omega$
- $RT1 = 2.27 \, \text{k}\Omega$
- $RT2 = 6.86 \, \text{k}\Omega$

**Charging Termination**

The bq24190, bq24192, bq24192I, bq24193 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG09[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].
Termination when REG02[0] = 1
When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through CE pin or REG01[5:4].

Termination when REG05[6] = 1
Usually the STAT bit indicates charging complete when the charging current falls below termination threshold. Write REG05[6]=1 to enable an early “charge done” indication on STAT pin. The STAT pin goes high when the charge current reduces below 800mA. The charging cycle is still on-going until the current falls below the termination threshold.

Charging Safety Timer
The bq24190, bq24192, bq24192I, bq24193 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

In default mode, the device keeps charging the battery with 5-hour fast charging safety timer regardless of REG05[2:1] default value. At the end of the 5 hours, the EN_HIZ (REG00[7]) is set to signal the buck converter stops and the system load is supplied by the battery. The EN_HIZ bit can be cleared to restart the buck converter.

In host mode, the device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the REG05[2:1] bits (default = 8 hours). At the end of safety timer, the EN_HIZ (REG00[7]) is cleared to signal the buck converter continues to operation to supply system load.

The safety timer is 1 hour when the battery is below BATLOWV threshold. The user can program fast charge safety timer through I2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C (REG05[3]).

The following actions restart the safety timer:
• At the beginning of a new charging cycle
• Toggle the CE pin HIGH to LOW to HIGH (charge enable)
• Write REG01[5:4] from 00 to 01 (charge enable)
• Write REG05[3] from 0 to 1 (safety timer enable)
• Write REG01[7] to 1 (software reset)

During input voltage/current regulation or thermal regulation, the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

USB Timer when Charging from USB100mA Source
The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

Host Mode and Default Mode
The bq24190, bq24192, bq24192I, bq24193 is a host controlled device, but it can operate in default mode without host management. In default mode, bq24190, bq24192, bq24192I, bq24193 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings.

Any write command to bq24190, bq24192, bq24192I, bq24193 transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4]=11.
Plug in USB100mA Source with Good Battery

When the input source is detected as 100mA USB host, and the battery voltage is above batgood threshold ($V_{BATGD}$), the charger device enters HIZ state to meet the battery charging spec requirement.

If the charger device is in host mode, it will stay in HIZ state even after the USB100mA source is removed, and the adapter plugs in. During the HIZ state, REG00[7] is set HIGH and the system load is supplied from battery. It is recommended that the processor host always checks if the charger IC is in HIZ state when it wakes up. The host can write REG00[7] to 0 to exit HIZ state.

If the charger is in default mode, when the DC source is removed, the charger device will get out of HIZ state automatically. When the input source plugs in again, the charger IC runs detection on the input source and update the input current limit.

USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

Status Outputs ($\overline{PG}$, STAT, and INT)

Power Good Indicator ($\overline{PG}$)

In bq24192, bq24192I, bq24193, $\overline{PG}$ goes LOW to indicate a good input source when:
1. VBUS above UVLO
2. VBUS above battery (not in sleep)
3. VBUS below ACOV threshold
4. VBUS above 3.8V when 30mA current is applied (not a poor source)

Charging Status Indicator (STAT)

The bq24190, bq24192, bq24192I, bq24193 indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.
Table 6. STAT Pin State

<table>
<thead>
<tr>
<th>CHARGING STATE</th>
<th>STAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charging in progress (including recharge)</td>
<td>LOW</td>
</tr>
<tr>
<td>Charging complete</td>
<td>HIGH</td>
</tr>
<tr>
<td>Sleep mode, charge disable</td>
<td>HIGH</td>
</tr>
<tr>
<td>Charge suspend (Input over-voltage, TS fault, timer fault, input or system over-voltage)</td>
<td>blinking at 1Hz (bq24190, bq24192, bq24193) or 10kΩ pull down (bq24192I)</td>
</tr>
</tbody>
</table>

When a fault occurs, instead of blinking, the STAT pin in bq24192I has a 10kΩ pull-down resistor to ground. When the pull-up resistor is 30kΩ, the STAT voltage during fault is 1/4 of the pull-up rail.

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256us INT pulse.

- USB/adapter source identified (through PSEL or DPDM detection, with OTG pin)
- Good input source detected
  - not in sleep
  - not in ACOV
  - current limit above 30mA
- Input removed or ACOV
- Charge Complete
- Any FAULT event in REG09

When a fault occurs, the charger device sends out INT and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last INT and the 2nd reads the current fault register status.

Protections

Input Current Limit on ILIM

For safe operation, the bq24190, bq24192, bq24192I, bq24193 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

\[ I_{\text{INMAX}} = \frac{1V}{R_{\text{ILIM}}} \times 530 \]

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 353Ω resistor to ground for 1.5A, the input current limit is 1.5A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1V. If ILIM voltage exceeds 1V, the device enters input current regulation (Refer to Dynamic Power Path Management section).

The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following Equation 5:

\[ I_{\text{IN}} = \frac{V_{\text{ILIM}}}{1V} \times I_{\text{INMAX}} \]

For example, if ILIM pin sets 2A, and the ILIM voltage is 0.6V, the actual input current 1.2A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1V. If ILIM pin is short, the input current limit is set by the register.
Thermal Regulation and Thermal Shutdown

The bq24190, bq24192, bq24192I, bq24193 monitors the internal junction temperature $T_J$ to avoid overheating the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

Voltage and Current Monitoring in Buck Mode

The bq24190, bq24192, bq24192I, bq24193 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is 18V. If VBUS voltage exceeds 18V, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

System Over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

Voltage and Current Monitoring in Boost Mode

The bq24190, bq24192, bq24192I, bq24193 closely monitors the VBUS voltage, as well as HSFET and LSFET current to ensure safe boost mode operation.

VBUS Over-Voltage Protection

The boost mode regulated output is 5V. When an adapter plugs in during boost mode, the VBUS voltage will rise above regulation target. Once the VBUS voltage exceeds 5.3V, the bq24190, bq24192, bq24192I, bq24193 stops switching and the device exits boost mode. The fault register REG09[6] is set high to indicate fault in boost operation. An INT is asserted to the host.

Battery Protection

Battery Over-Current Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[5] goes high and an INT is asserted to the host.

Charging During Battery Short Protection

If the battery voltage falls below 2V, the charge current is reduced to 100mA for battery safety.

System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the BATFET is latched off. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.
Serial Interface

The bq24190, bq24192, bq24192I, bq24193 uses I\(^2\)C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I\(^2\)C is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I\(^2\)C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

![Figure 33. Bit Transfer on the I\(^2\)C Bus](image-url)

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

![Figure 34. START and STOP conditions](image-url)
Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

![Figure 35. Data Transfer on the I²C Bus](image)

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

![Figure 36. Complete Data Transfer](image)

Single Read and Write

![Figure 37. Single Write](image)

![Figure 38. Single Read](image)
If the register address is not defined, the charger IC send back NACK and go back to the idle state.

**Multi-Read and Multi-Write**

The charger device supports multi-read and multi-write on REG00 through REG08.

---

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.
APPLICATION INFORMATION

Inductor Selection
The bq24190, bq24192, bq24192I, bq24193 has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

\[ I_{SAT} \geq I_{CHG} + \left(\frac{1}{2}\right) I_{RIPPLE} \]  

(6)

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle (D = V_{BAT}/V_{BUS}), switching frequency (fs) and inductance (L):

\[ I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_s \times L} \]  

(7)

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Typical inductor value is 2.2\mu H.

Input Capacitor
Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

\[ I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \]  

(8)

For best performance, VBUS should be decouple to PGND with 1\mu F capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 15V input voltage.

Output Capacitor
Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

\[ I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \]  

(9)

The output capacitor voltage ripple can be calculated as follows:

\[ \Delta V_O = \frac{V_{OUT}}{8LC/s^2} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \]  

(10)

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15kHz and 25kHz. With 2.2\mu H inductor, the typical output capacitor value is 20\mu F. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.
PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 41) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, refer to SCBA017 and SLUA271.

Figure 41. High Frequency Current Path
## PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ24190RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24190</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ24190RGET</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24190</td>
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<td>BQ24192RGER</td>
<td>ACTIVE</td>
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<td>RGE</td>
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<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ 24192I</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ24192RGET</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ 24192I</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ24192RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
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<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24192</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ24192RGET</td>
<td>ACTIVE</td>
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<td>RGE</td>
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</tr>
<tr>
<td>BQ24193RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
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<td>BQ24193</td>
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</tr>
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<td>BQ24193RGET</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24193</td>
<td>Samples</td>
</tr>
<tr>
<td>HPA01186RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24190</td>
<td>Samples</td>
</tr>
<tr>
<td>HPA02150RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24190</td>
<td>Samples</td>
</tr>
<tr>
<td>HPA02163RGER</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BQ24193</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

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### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**: Quardrant 1
- **Q2**: Quadrant 2
- **Q3**: Quadrant 3
- **Q4**: Quadrant 4

---

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
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<td>24</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24190RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24192RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24192RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24192RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24192RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24193RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>BQ24193RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>4.25</td>
<td>4.25</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ24190RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24190RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24192IRGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24192IRGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24192RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24192RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24193RGER</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>BQ24193RGET</td>
<td>VQFN</td>
<td>RGE</td>
<td>24</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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