1 Features

- 4-Channel Protected Low-Side Driver
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes
  - Parallel Interface
- DW Package: 1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)
- PWP Package: 2-A (Single Channel On) / 1-A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- 8.2-V to 60-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package

2 Applications

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

3 Description

The DRV8803 provides a 4-channel low side driver with overcurrent protection. It has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

In the SOIC (DW) package, the DRV8803 can supply up to 1.5-A (one channel on) or 800-mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, it can supply up to 2-A (one channel on) or 1-A (four channels on) continuous output current per channel, at 25°C with proper PCB heatsinking.

The device is controlled through a simple parallel interface.

Internal shutdown functions are provided for over current protection, short circuit protection, undervoltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8803 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8803</td>
<td>SOIC (20)</td>
<td>12.80 mm × 7.50 mm</td>
</tr>
<tr>
<td></td>
<td>HTSSOP (16)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

8.2V to 60V

Controller

5, EN / IN
RESET
nFAULT

Fault Protection
Clamp Diodes

DRV8803
Quad Low-Side Driver

M

1 A
1 A
1 A
1 A

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2012) to Revision C

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section</td>
<td>1</td>
</tr>
<tr>
<td>Changed Continuous output current, single channel on, $T_A = 25^\circ C$, HTSSOP package MAX value from 1.5 A to 2 A</td>
<td>4</td>
</tr>
<tr>
<td>Changed Continuous output current, four channels on, $T_A = 25^\circ C$, HTSSOP package MAX value from 0.8 A to 1 A</td>
<td>4</td>
</tr>
</tbody>
</table>

Submit Documentation Feedback

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Product Folder Links: DRV8803
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN LOCATIONS</th>
<th>I/O</th>
<th>DESCRIPTION</th>
<th>EXTERNAL COMPONENTS OR CONNECTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER AND GROUND</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>5, 6, 7, 14, 15, 16</td>
<td></td>
<td>Device ground</td>
<td>All pins must be connected to GND.</td>
</tr>
<tr>
<td>VM</td>
<td>1</td>
<td></td>
<td>Device power supply</td>
<td>Connect to motor supply (8.2 V - 60 V).</td>
</tr>
<tr>
<td><strong>CONTROL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nENBL</td>
<td>10</td>
<td>I</td>
<td>Enable input</td>
<td>Active low enables outputs – internal pulldown</td>
</tr>
<tr>
<td>RESET</td>
<td>11</td>
<td>I</td>
<td>Reset input</td>
<td>Active high resets internal logic and OCP – internal pulldown</td>
</tr>
<tr>
<td>IN1</td>
<td>18</td>
<td>I</td>
<td>Channel 1 input</td>
<td>IN1 = 1 drives OUT1 low – internal pulldown</td>
</tr>
<tr>
<td>IN2</td>
<td>17</td>
<td>I</td>
<td>Channel 2 input</td>
<td>IN2 = 1 drives OUT2 low – internal pulldown</td>
</tr>
<tr>
<td>IN3</td>
<td>13</td>
<td>I</td>
<td>Channel 3 input</td>
<td>IN3 = 1 drives OUT3 low – internal pulldown</td>
</tr>
<tr>
<td>IN4</td>
<td>12</td>
<td>I</td>
<td>Channel 4 input</td>
<td>IN4 = 1 drives OUT4 low – internal pulldown</td>
</tr>
<tr>
<td><strong>STATUS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nFAULT</td>
<td>20</td>
<td>OD</td>
<td>Fault</td>
<td>Logic low when in fault condition (overtemperature, overcurrent)</td>
</tr>
<tr>
<td><strong>OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT1</td>
<td>3</td>
<td>O</td>
<td>Output 1</td>
<td>Connect to load 1</td>
</tr>
<tr>
<td>OUT2</td>
<td>4</td>
<td>O</td>
<td>Output 2</td>
<td>Connect to load 2</td>
</tr>
<tr>
<td>OUT3</td>
<td>8</td>
<td>O</td>
<td>Output 3</td>
<td>Connect to load 3</td>
</tr>
<tr>
<td>OUT4</td>
<td>9</td>
<td>O</td>
<td>Output 4</td>
<td>Connect to load 4</td>
</tr>
<tr>
<td>VCLAMP</td>
<td>2</td>
<td>—</td>
<td>Output clamp voltage</td>
<td>Connect to VM supply, or zener diode to VM supply</td>
</tr>
</tbody>
</table>

(1) Directions: I = input, O = output, OD = open-drain output
6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>–0.3</td>
<td>65</td>
</tr>
<tr>
<td>VOUTx</td>
<td>–0.3</td>
<td>65</td>
</tr>
<tr>
<td>VCLAMP</td>
<td>–0.3</td>
<td>65</td>
</tr>
<tr>
<td>nFAULT</td>
<td>20</td>
<td>mA</td>
</tr>
</tbody>
</table>

Peak clamp diode current
DC or RMS clamp diode current
Digital input pin voltage
Digital output pin voltage

\[\text{PMO} \leq \text{V(out)} \leq \text{VCM}, \text{t} < 1 \mu\text{s}\]

Continuous total power dissipation

Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>ELECTROSTATIC DISCHARGE</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (^{(1)})</td>
<td>±3000 V</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (^{(2)})</td>
<td>±1000 V</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>8.2</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>VCLAMP</td>
<td>0</td>
<td>60</td>
<td>V</td>
</tr>
</tbody>
</table>

\[\text{PMO} \leq \text{V(out)} \leq \text{VCM}, \text{t} < 1 \mu\text{s}\]

<table>
<thead>
<tr>
<th>OUTPUT</th>
<th>CONTINUOUS OUTPUT CURRENT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5 A</td>
<td>Single channel on</td>
<td></td>
</tr>
<tr>
<td>0.8 A</td>
<td>Four channels on</td>
<td></td>
</tr>
<tr>
<td>2 A</td>
<td>Single channel on</td>
<td></td>
</tr>
<tr>
<td>1 A</td>
<td>Four channels on</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) VCLAMP is used only to supply the clamp diodes. It is not a power supply input.

\(^{(2)}\) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (^{(1)})</th>
<th>DRV8803</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DW (SOIC)</td>
<td>PWP (HTSSOP)</td>
</tr>
<tr>
<td></td>
<td>20 PINS</td>
<td>16 PINS</td>
</tr>
<tr>
<td>(R_{\text{JA}}) Junction-to-ambient thermal resistance</td>
<td>67.7</td>
<td>39.6</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}}) Junction-to-case (top) thermal resistance</td>
<td>32.9</td>
<td>24.6</td>
</tr>
<tr>
<td>(R_{\text{JB}}) Junction-to-board thermal resistance</td>
<td>35.4</td>
<td>20.3</td>
</tr>
<tr>
<td>(\psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td>8.2</td>
<td>0.7</td>
</tr>
<tr>
<td>(\psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td>34.9</td>
<td>20.1</td>
</tr>
<tr>
<td>(R_{\text{JC(bot)}}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>2.3</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
## 6.5 Electrical Characteristics

\( T_A = 25^\circ C \), over recommended operating conditions (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLIES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{VM} )</td>
<td>VM operating supply current</td>
<td>( V_M = 24 ) ( V )</td>
<td>1.6</td>
<td>2.1</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{UVLO} )</td>
<td>VM undervoltage lockout voltage</td>
<td>( V_M ) rising</td>
<td>8.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input low voltage</td>
<td></td>
<td>0.6</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input high voltage</td>
<td></td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Input hysteresis</td>
<td></td>
<td>0.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input low current</td>
<td>( VIN = 0 )</td>
<td>–20</td>
<td>20</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Input high current</td>
<td>( VIN = 3.3 ) ( V )</td>
<td>100</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( R_{PD} )</td>
<td>Pulldown resistance</td>
<td></td>
<td></td>
<td>100</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td><strong>nFAULT OUTPUT (OPEN-DRAIN OUTPUT)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output low voltage</td>
<td>( I_O = 5 ) mA</td>
<td></td>
<td>0.5</td>
<td>( V )</td>
</tr>
<tr>
<td>( I_{OH} )</td>
<td>Output high leakage current</td>
<td>( V_O = 3.3 ) ( V )</td>
<td></td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>LOW-SIDE FETS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{DS(ON)} )</td>
<td>FET on resistance</td>
<td>( V_M = 24 ) ( V ), ( I_O = 700 ) mA, ( T_J = 25^\circ C )</td>
<td>0.5</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( V_M = 24 ) ( V ), ( I_O = 700 ) mA, ( T_J = 85^\circ C )</td>
<td>0.75</td>
<td>0.8</td>
<td>( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Off-state leakage current</td>
<td></td>
<td>–50</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>HIGH-SIDE DIODES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_F )</td>
<td>Diode forward voltage</td>
<td>( V_M = 24 ) ( V ), ( I_O = 700 ) mA, ( T_J = 25^\circ C )</td>
<td></td>
<td>1.2</td>
<td>( V )</td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Off-state leakage current</td>
<td>( V_M = 24 ) ( V ), ( T_J = 25^\circ C )</td>
<td></td>
<td>–50</td>
<td>50</td>
</tr>
<tr>
<td><strong>OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_R )</td>
<td>Rise time</td>
<td>( V_M = 24 ) ( V ), ( I_O = 700 ) mA, Resistive load</td>
<td>50</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>( I_F )</td>
<td>Fall time</td>
<td>( V_M = 24 ) ( V ), ( I_O = 700 ) mA, Resistive load</td>
<td>50</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td><strong>PROTECTION CIRCUITS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OCP} )</td>
<td>Overcurrent protection trip level</td>
<td></td>
<td>2.3</td>
<td>3.8</td>
<td>A</td>
</tr>
<tr>
<td>( I_{OCP} )</td>
<td>Overcurrent protection deglitch time</td>
<td></td>
<td></td>
<td>3.5</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{RETRY} )</td>
<td>Overcurrent protection retry time</td>
<td></td>
<td></td>
<td>1.2</td>
<td>ms</td>
</tr>
<tr>
<td>( I_{TSD} )</td>
<td>Thermal shutdown temperature</td>
<td></td>
<td></td>
<td>150</td>
<td>160</td>
</tr>
</tbody>
</table>

(1) Not production tested.
6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( t_{OE(ENABLE)} ) Enable time, nENBL to output low</td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>2</td>
<td>( t_{PD(L-H)} ) Propagation delay time, INx to OUTx, low to high</td>
<td>800</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>( t_{PD(H-L)} ) Propagation delay time, INx to OUTx, high to low</td>
<td>800</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>( t_{RESET} ) RESET pulse width</td>
<td>20</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Not production tested.

![Timing Requirements Diagram](image)

Figure 1. DRV8803 Timing Requirements
6.7 Typical Characteristics

Figure 2. Supply Current Over Temperature

Figure 3. Supply Current Over $V_M$

Figure 4. $R_{DS(on)}$ Over Temperature

Figure 5. $R_{DS(on)}$ Over $V_M$
7 Detailed Description

7.1 Overview
The DRV8803 device is an integrated 4-channel low side driver solution for any low side switch application. The integrated overcurrent protection limits the motor current to a fixed maximum. Four logic inputs control the low-side driver outputs which consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500 mΩ. A single power input VM serves as device power and is internally regulated to power the internal low side gate drive. Motor speed can be controlled with pulse-width modulation at frequencies from 0 kHz to 100 kHz. The device outputs can be disabled by bringing nENBL pin high. The thermal shutdown protection enables the device to automatically shut down if the die temperature exceeds a TTSD limit. UVLO protection will disable all circuitry in the device if $V_M$ drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram

7.3 Feature Description
7.3.1 Output Drivers
The DRV8803 device contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. VCLAMP can also be connected to a Zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.
Feature Description (continued)

7.3.2 Protection Circuits

The DRV8803 device is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the \( t_{OCP} \) deglitch time (approximately 3.5 \( \mu \)s), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the \( t_{RETRY} \) retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and reapplied.

7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Parallel Interface Operation

The DRV8803 device is controlled with a simple parallel interface. Logically, the interface is shown in Figure 6.

![Figure 6. Parallel Interface Operation](image)

7.4.2 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic. All inputs are ignored while RESET is active. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power up.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The DRV8803 device can be used to drive one unipolar stepper motor.

8.2 Typical Application

Figure 7. Typical Application Schematic

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>REFERENCE</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VM</td>
<td>24 V</td>
</tr>
<tr>
<td>Motor Winding Resistance</td>
<td>RL</td>
<td>7.4 Ω/phase</td>
</tr>
<tr>
<td>Motor Full Step Angle</td>
<td>θstep</td>
<td>1.8°/step</td>
</tr>
<tr>
<td>Motor Rated Current</td>
<td>IRATED</td>
<td>0.75 A</td>
</tr>
<tr>
<td>PWM frequency</td>
<td>fPWM</td>
<td>31.25 kHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage
The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

8.2.2.2 Drive Current
The current path is starts from the supply VM, moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

\[ P = I^2 \times R_{DS(on)} \]
The DRV8803 device has been measured to be capable of 1.5-A Single Channel or 800-mA Four Channels with the DW package and 2-A Single Channel or 1-A Four Channels with the PWP package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

8.2.3 Application Curves

- Figure 8. Current Ramp With a 16-Ω, 1-mH RL Load and \( V_M = 8.2 \) V
- Figure 9. Current Ramp With a 16-Ω, 1-mH RL Load and \( V_M = 30 \) V
- Figure 10. OCP With \( V_M = 8.2 \) V and OUT1 Shorted to \( V_M \)
- Figure 11. OCP Separated by \( I_{RETRY} \) With \( V_M = 8.2 \)-V and OUT1 Shorted to \( V_M \)
9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:
- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.
10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

![Diagram of DRV8803 layout](image)

Figure 13. Recommended Layout

10.3 Thermal Consideration

10.3.1 Thermal Protection

The DRV8803 device has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.2 Power Dissipation

Power dissipation in the DRV8803 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 2:

$$ P = R_{DS(on)} \times (I_{OL})^2 $$

where

- $P$ is the power dissipation of one FET
Thermal Consideration (continued)

- $R_{\text{DS(on)}}$ is the resistance of each FET
- $I_{\text{OUT}}$ is equal to the average current drawn by the load. \hspace{1cm} (2)

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and their duration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{\text{DS(on)}}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.3 Heatsinking

The DRV8803DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8803PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI Application Report, PowerPAD Thermally Enhanced Package (SLMA002), and TI Application Brief, PowerPAD Made Easy (SLMA004), available at www.ti.com.
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

• PowerPAD Thermally Enhanced Package, SLMA002.
• PowerPAD Made Easy, SLMA004.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8803DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>DRV8803DW</td>
<td></td>
</tr>
<tr>
<td>DRV8803DWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>DRV8803DW</td>
<td></td>
</tr>
<tr>
<td>DRV8803PWP</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>DRV8803</td>
<td></td>
</tr>
<tr>
<td>DRV8803PWPR</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>DRV8803</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSCOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

## REEL DIMENSIONS

![Reel Dimensions Diagram]

## TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram]

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
<tr>
<td>DRV8803DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.3</td>
<td>2.7</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
<tr>
<td>DRV8803PWPR</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8803DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
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<td>45.0</td>
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<tr>
<td>DRV8803PWPR</td>
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<td>PWP</td>
<td>16</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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