CDCLVD110A Programmable Low-Voltage 1:10 LVDS Clock Driver

1 Features

- Low-Output Skew <30 ps (Typical) for Clock-Distribution Applications
- Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs
- V_{CC} Range: 2.5 V ±5%
- Typical Signaling Rate Capability of Up to 1.1 GHz
- Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, $\overline{CLK0}$ or CLK1, $\overline{CLK1}$ Inputs
- Full Rail-to-Rail Common-Mode Input Range
- Receiver Input Threshold: ±100 mV
- Available in 32-Pin LQFP and VQFN Package
- Fail-Safe I/O-Pins for V_{DD} = 0 V (Power Down)

2 Applications

- General-Purpose Industrial, Communication and Consumer Applications

3 Description

The CDCLVD110A clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0 to Q9) with minimum skew for clock distribution. The CDCLVD110A is specifically designed to drive 50-Ω transmission lines.

When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled or disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when EN = 0, the outputs are not programmable and all outputs are enabled.

The CDCLVD110A has an improved start-up circuit that minimizes enabling time in AC- and DC-coupled systems.

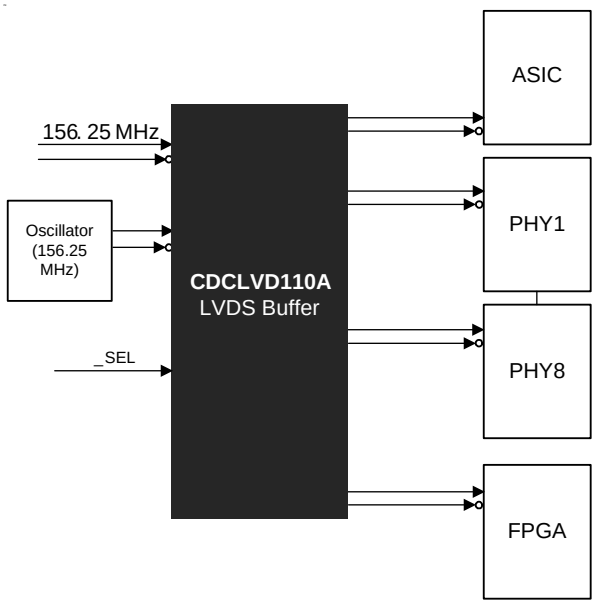
The CDCLVD110A is characterized for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVD110A	LQFN (32)	7.00 mm × 7.00 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example



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4 Revision History

Changes from Revision C (October 2008) to Revision D **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 4
- Added *Thermal Considerations* section ... 18

Changes from Revision B (October 2008) to Revision C **Page**

- Added PowerPAD information to the Pinout Package ... 3
- Added PowerPAD information to the PIN FUNCTIONS table ... 3

Changes from Revision A (January 2008) to Revision B **Page**

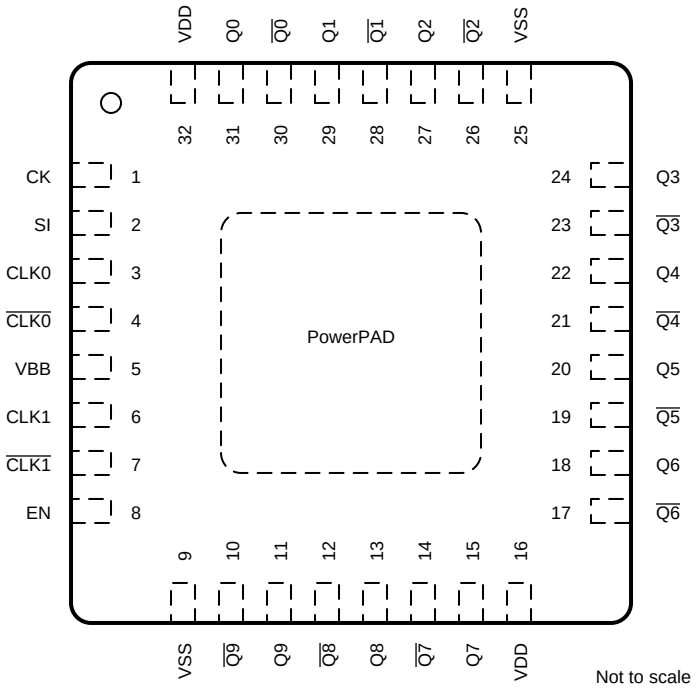
- Changed Feature From: Available in 32-Pin LQFP Package To: Available in 32-Pin LQFP and QFN Package ... 1
- Added Applications ... 1

Changes from Original (February 2007) to Revision A **Page**

- Changed Pinout Package title From: TQFP PACKAGE and QFN PACKAGE To: LQFP PACKAGE and QFN PACKAGE. 1

5 Pin Configuration and Functions

VF or RHB Package
32-Pin LQFP or VQFN
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CK	1	I	Control register input clock, features a 120-kΩ pullup resistor
CLK0	3	I	True differential input, LVDS
$\overline{\text{CLK0}}$	4	I	Complementary differential input, LVDS
CLK1	6	I	True differential input, LVDS
$\overline{\text{CLK1}}$	7	I	Complementary differential input, LVDS
EN	8	I	Control enable (for programmability), features a 120-kΩ pulldown resistor, input
PowerPAD™	—	I/O	The PowerPAD of the VQFN package is thermally connected to the die to improve the heat transfer out of the package. This pad is connected to GND.
Q[9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	O	Clock outputs, these outputs provide low-skew copies of CLKIN
$\overline{\text{Q[9:0]}}$	10, 12, 14, 17, 19, 21,23, 26, 28, 30	O	Complementary clock outputs, these outputs provide low-skew copies of CLKIN
SI	2	I	Control register serial input/CLK Select, features a 120-kΩ pulldown resistor
V_{BB}	5	O	Reference voltage output
V_{DD}	16, 32	—	Supply voltage
V_{SS}	9, 25	—	Device ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.3	2.8	V
Input voltage, V_I	–0.2	V_{DD} + 0.2	V
VI output voltage, V_O	–0.2	V_{DD} + 0.2	V
Driver short-circuit current, I_{OSD} (Qn, $\overline{Qn}$)	Continuous		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) HBM 1.5-kΩ, 100-pF
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.375	2.5	2.625	V
V_{IC}	Receiver common-mode input voltage	0.5 × $\lvert V_{ID}\rvert$		V_{DD} – 0.5 × $\lvert V_{ID}\rvert$	V
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		CDCLVD110A		UNIT
		VF (LQFN)	RHB (VQFN)	
		32 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.1	45.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	37.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	17.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.7	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω	250	450	600	mV
ΔV_{OD}	V_{OD} magnitude change				50	mV
V_{OS}	Offset voltage	–40°C to 85°C	0.95	1.2	1.45	V
ΔV_{OS}	V_{OS} magnitude change				350	mV
I_{OS}	Output short-circuit current	V_O = 0 V			–20	mA
		$\|V_{OD}\|$ = 0 V			20	
V_{BB}	Reference output voltage	V_{DD} = 2.5 V, I_{BB} = –100 µA	1.15	1.25	1.35	V
C_O	Output capacitance	V_O = V_{DD} or GND		3		pF
RECEIVER						
V_{IDH}	Input threshold high				100	mV
V_{IDL}	Input threshold low		–100			mV
$\|V_{ID}\|$	Input differential voltage		200			mV
I_{IH}	Input current, CLK0/$\overline{CLK0}$	V_I = V_{DD}	–5		5	µA
I_{IL}	Input current, CLK1/$\overline{CLK1}$	V_I = 0 V	–5		5	µA
C_I	Input capacitance	V_I = V_{DD} or GND		3		pF
SUPPLY CURRENT						
I_{DD}	Supply current, full loaded and no load	All outputs enabled and loaded, R_L = 100 Ω, f = 100 MHz		100	110	mA
		All outputs enabled and loaded, R_L = 100 Ω, f = 800 MHz		150	160	
		Outputs enabled, no output load, f = 0 Hz			35	
I_{DDZ}	Supply current, 3-state	All outputs 3-state by control logic, f = 0 Hz			35	mA

6.6 Switching Characteristics: LVDS

over recommended operating free-air temperature range and V_{DD} = 2.5 V ±5% (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay low-to-high	CLK0, $\overline{CLK0}$ CLK1, $\overline{CLK1}$	Qn, $\overline{Qn}$		2	3	ns
t_{PHL}	Propagation delay high-to-low	CLK0, $\overline{CLK0}$ CLK1, $\overline{CLK1}$	Qn, $\overline{Qn}$		2	3	ns
t_{duty}	Duty cycle	CLK0, $\overline{CLK0}$ CLK1, $\overline{CLK1}$	Qn, $\overline{Qn}$	45%		55%	
$t_{sk(o)}$	Output skew		Any Qn, $\overline{Qn}$		30		ps
$t_{sk(p)}$	Pulse skew		Any Qn, $\overline{Qn}$			50	ps
$t_{sk(pp)}$	Part-to-part skew		Any Qn, $\overline{Qn}$			600	ps
t_r	Output rise time, 20% to 80%, R_L = 100 Ω, C_L = 5 pF		Any Qn, $\overline{Qn}$			350	ps
t_f	Output fall time, 20% to 80%, R_L = 100 Ω, C_L = 5 pF		Any Qn, $\overline{Qn}$			350	ps
f_{clk}	Max input frequency	CLK0, $\overline{CLK0}$ CLK1, $\overline{CLK1}$	Any Qn, $\overline{Qn}$	900	1100		MHz

6.7 Jitter Characteristics

characterized with CDCLVD110 performance EVM, V_{DD} = 3.3 V, outputs not under test are terminated to 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVDS}$	Additive phase jitter from input to LVDS output Q3 and $\overline{Q3}$	12 kHz to 5 MHz, f_{out} = 30.72 MHz		281		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		111		

6.8 Control Register Characteristics

over recommended operating free-air temperature range, V_{DD} = 2.5 V ±5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum frequency of shift register		100	150		MHz
t_{su}	Set-up time, clock to SI				2	ns
t_h	Hold time, clock to SI				1.5	ns
$t_{removal}$	Removal time, enable to clock				1.5	ns
$t_{startup}$	Start-up time after disable through SI				1	µs
t_w	Clock pulse width, minimum		3			ns
V_{IH}	Logic input high	V_{DD} = 2.5 V	2			V
V_{IL}	Logic input low	V_{DD} = 2.5 V			0.8	V
I_{IH}	Input current, CK pin	$V_I = V_{DD}$	–5		5	µA
	Input current, SI and EN pins	$V_I = V_{DD}$	10		–30	
I_{IL}	Input current, CK pin	V_I = GND	–10		30	µA
	Input current, SI and EN pins	V_I = GND	–5		5	

6.9 Typical Characteristics

Input clock RMS jitter is 55.4 fs from 12 kHz to 20 MHz, additive RMS jitter is 70.4 fs, T_A = 25°C, and V_{DD} = 2.5 V (unless otherwise noted).

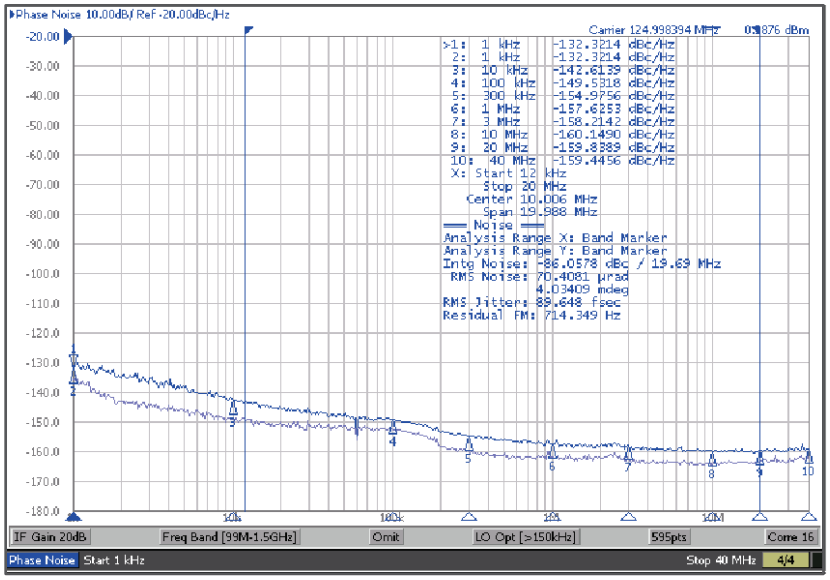
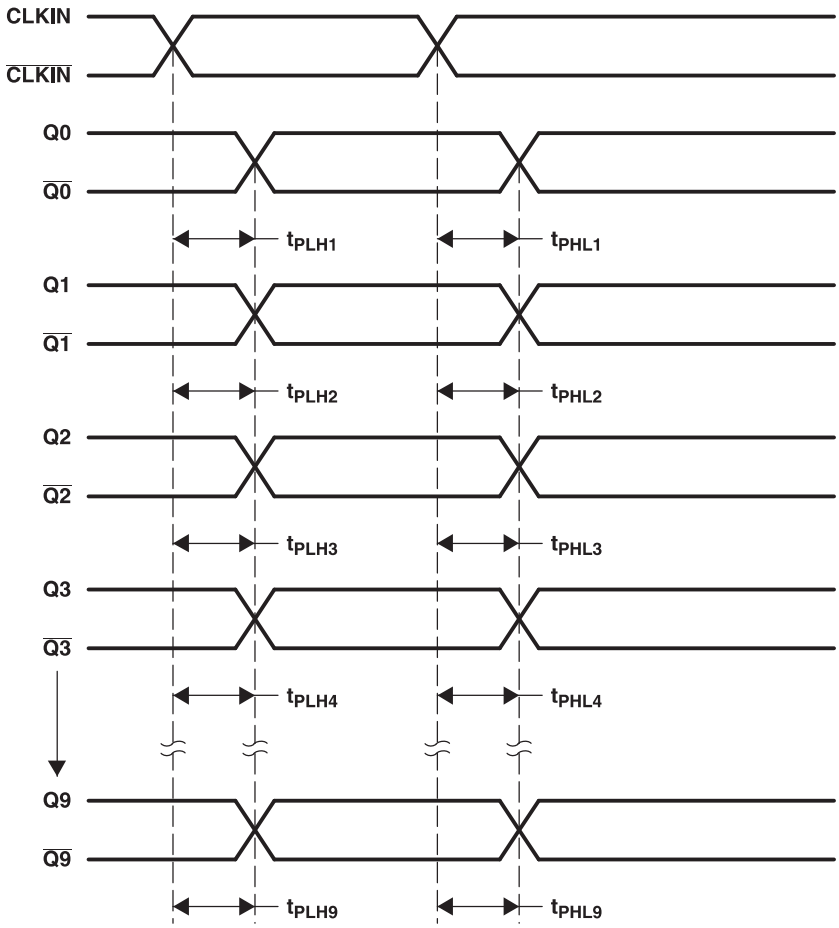


Figure 1. 125-MHz Input and Output Phase Noise Plot

7 Parameter Measurement Information



A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
   – The difference between the fastest and the slowest t_{PLHn} (n = 1, 2,...10)
   – The difference between the fastest and the slowest t_{PHLn} (n = 1, 2,...10)

B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
   – The difference between the fastest and the slowest t_{PLHn} (n = 1, 2,...10) across multiple devices
   – The difference between the fastest and the slowest t_{PHLn} (n = 1, 2,...10) across multiple devices

C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low (t_{PHL}) and the low-to-high (t_{PLH}) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = | t_{PHL} – t_{PLH} |$. Pulse skew is sometimes referred to as pulse-width distortion or duty-cycle skew.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

Parameter Measurement Information (continued)

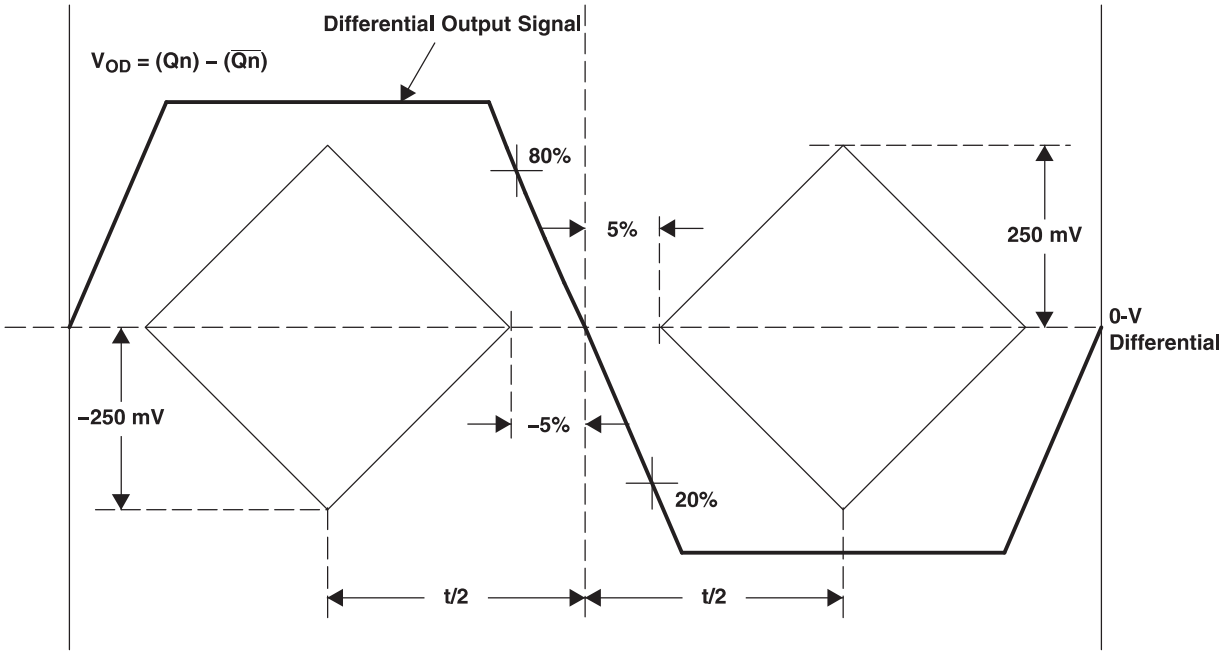


Figure 3. Test Criteria for f_{clk}, Duty Cycle, t_r, t_f, V_{OD}

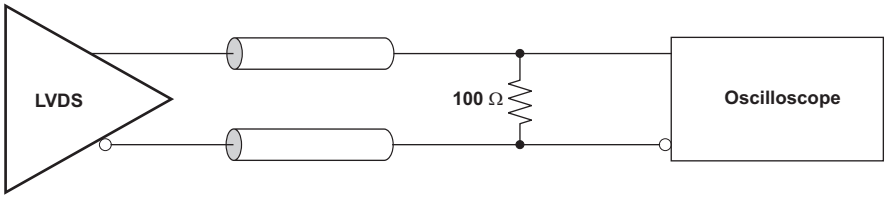


Figure 4. LVDS Output DC Configuration During Device Test

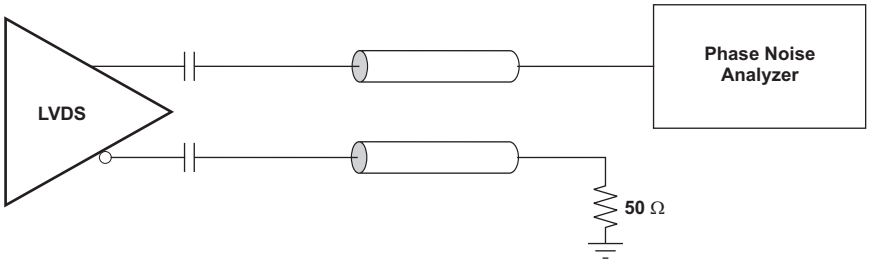


Figure 5. LVDS Output AC Configuration During Device Test

Parameter Measurement Information (continued)

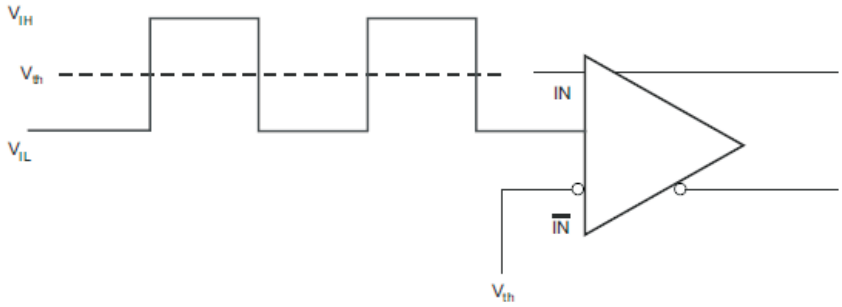


Figure 6. DC-Coupled LVCMOS Input During Device Test

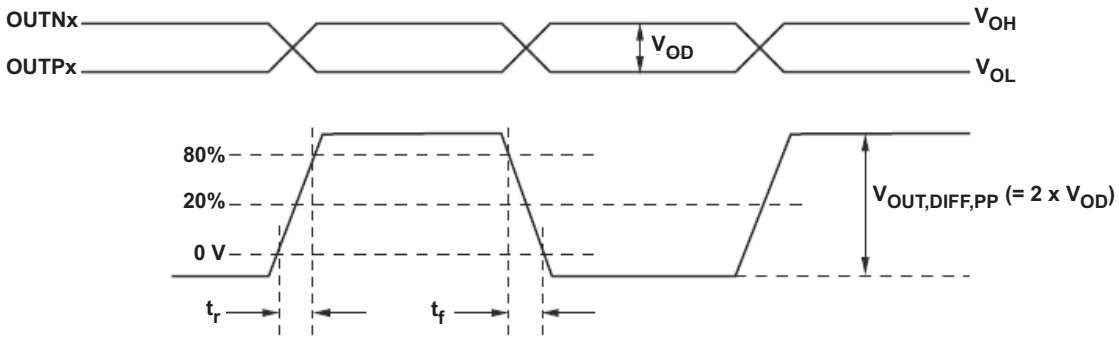


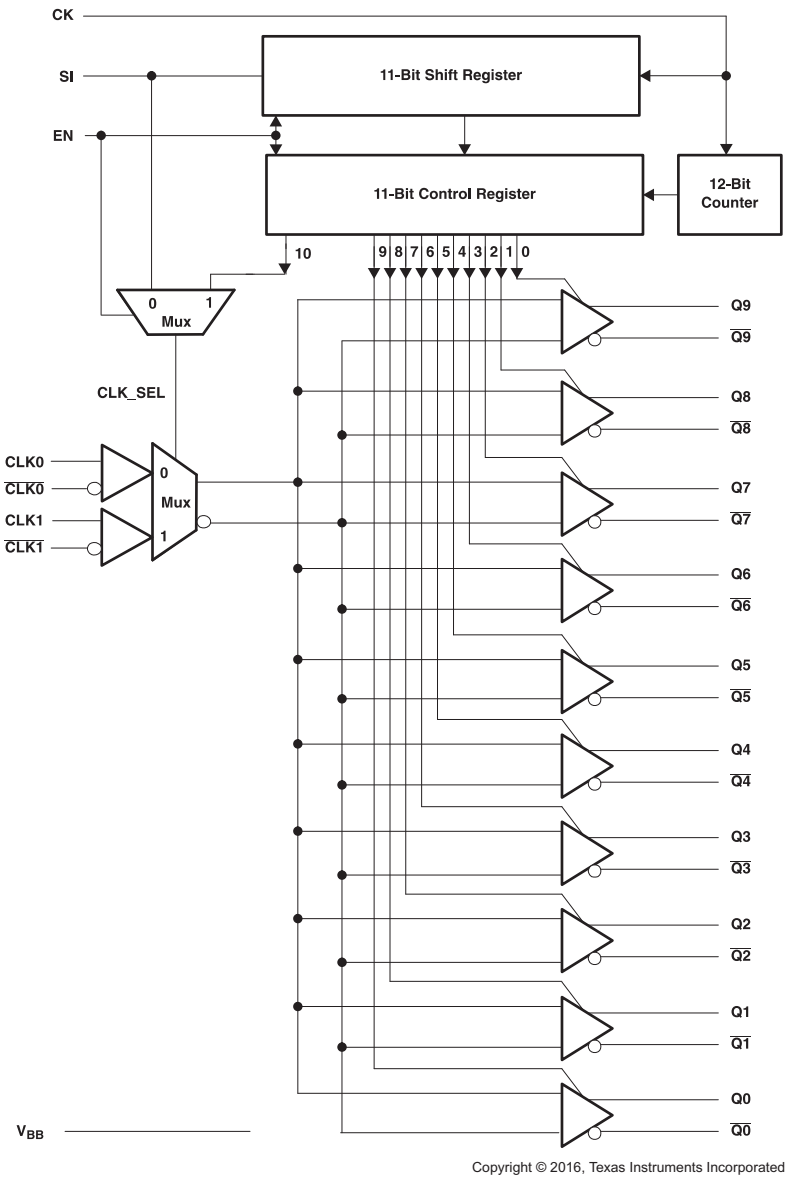
Figure 7. Output Voltage and Rise/Fall Time

8 Detailed Description

8.1 Overview

The CDCLVD110A LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity. The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the CDCLVD110A, AC-coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

8.2 Functional Block Diagram



8.3 Feature Description

The two inputs of the CDCLVD110A are internally muxed together and can be selected trough the control pin. Unused inputs and outputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the CDCLVD110A to provide greater system flexibility.

8.4 Device Functional Modes

Table 1 lists the functional modes of the device.

Table 1. Truth Table For Control Logic

CK	EN	SI	CLK0	$\overline{\text{CLK0}}$	CLK1	$\overline{\text{CLK1}}$	Q(0-9)	$\overline{\text{Q(0-9)}}$
L	L	L	L	H	X	X	L	H
L	L	L	H	L	X	X	H	L
L	L	L	Open	Open	X	X	L	H
L	L	H	X	X	L	H	L	H
L	L	H	X	X	H	L	H	L
L	L	H	X	X	Open	Open	L	H
All outputs enabled		X = Don't care						

8.4.1 Fail-Safe Information

For V_{DD} = 0 V (power-down mode), the CDCLVD110A has fail-safe input and output pins. In power-on mode, fail-safe biasing at input pins can be accomplished with a 10-kΩ pullup resistor from CLK0 or CLK1 to VDD and a 10-kΩ pulldown resistor from $\overline{\text{CLK0}}$ or $\overline{\text{CLK1}}$ to GND.

8.4.2 LVDS Receiver Input Termination

The LVDS receiver inputs require 100-Ω termination resistors placed as close as possible across the input pins.

8.4.3 Input Termination

The CDCLVD110A inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS drivers can be connected to CDCLVD110A inputs with AC- and DC-coupling as shown in Figure 8 and Figure 9 (respectively).

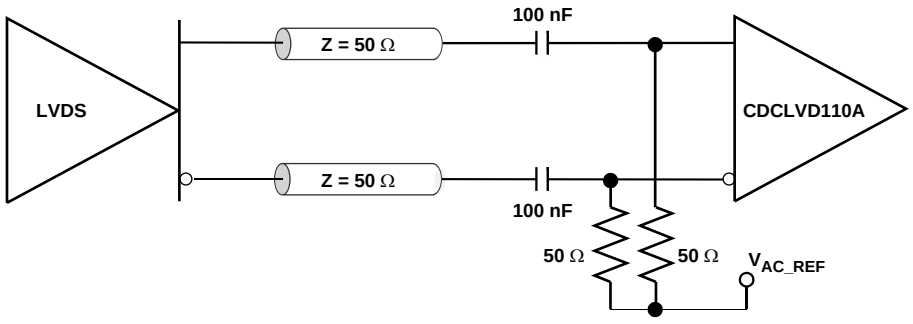


Figure 8. LVDS Clock Driver Connected to CDCLVD110A Input (AC-Coupled)

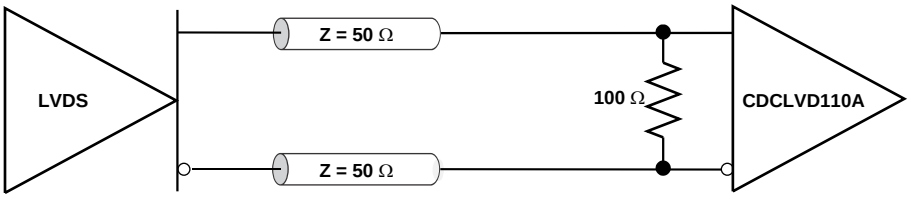


Figure 9. LVDS Clock Driver Connected to CDCLVD110A Input (DC-Coupled)

Figure 10 shows how to connect LVPECL inputs to the CDCLVD110A. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

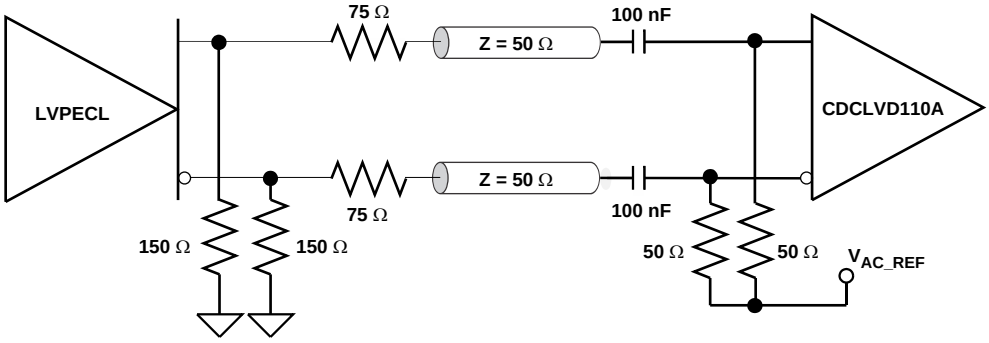


Figure 10. LVPECL Clock Driver Connected to CDCLVD110A Input

Figure 11 illustrates how to couple a 2.5-V LVCMOS clock input to the CDCLVD110A directly. The series resistance, R_S, must be placed close to the LVCMOS driver if required. 3.3-V LVCMOS clock input swing must be limited to $V_{IH} \leq V_{CC}$.

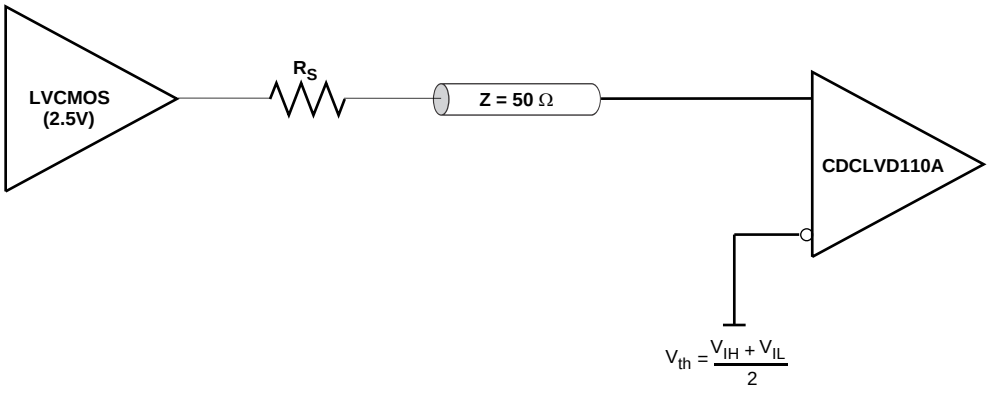


Figure 11. 2.5-V LVCMOS Clock Driver Connected to CDCLVD110A Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

8.4.4 LVDS Output Termination

Unused outputs can be left open without connecting any trace to the output pins.

The CDCLVD110A can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in Figure 12 and Figure 13 (respectively).

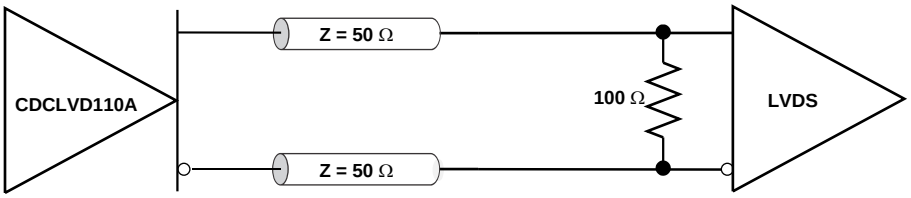


Figure 12. Output DC Termination

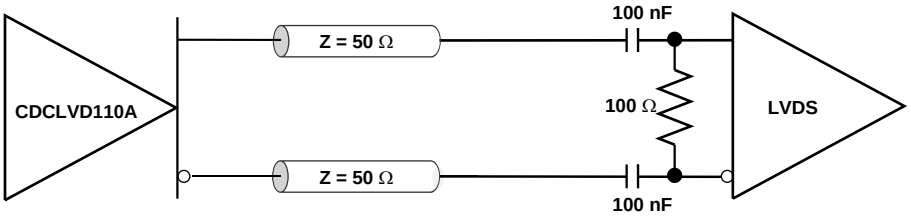


Figure 13. Output AC Termination (With the Receiver Internally Biased)

8.4.5 Control Inputs Termination

No external termination is required. The CK control input has an internal 120-kΩ pullup resistor, while the SI– and EN–control inputs each have an internal 120-kΩ pulldown resistor. If the control pins are left open per the default, all outputs are enabled, CLK0 or $\overline{\text{CLK0}}$ is selected, and the control register is disabled.

8.5 Programming

8.5.1 Specification of Control Register

The CDCLVD110A has an 11-bit, serial-in shift register and an 11-bit control register. The control Register enables or disables each output clock, and selects either CLK0 or CLK1 as the input clock. The CDCLVD110A has two modes of operation: *Programmable Mode (EN = 1)* and *Standard Mode (EN = 0)*.

8.5.1.1 Programmable Mode (EN = 1)

The shift register uses a serial input (SI) and a clock input (CK). Once the shift register is loaded with 11 clock pulses, the 12th clock pulse loads the control register. The first bit (bit 0) on SI enables the Q9-$\overline{\text{Q9}}$ output pair, and the 10th bit (bit 9) enables the Q0-$\overline{\text{Q0}}$ pair. The 11th bit (bit 10) on SI selects either CLK0 or CLK1 as the input clock; a bit value of 0 selects CLK0, whereas a bit value of 1 selects CLK1. To restart the control register configuration, a reset of the state machine must be done with a clock pulse on CK (shift register clock input) and EN set to low. The control register can be configured only once after each reset.

8.5.1.2 Standard Mode (EN = 0)

In this mode, the CDCLVD110A is not programmable and all the clock outputs are enabled. The clock input (CLK0 or CLK1) is selected with the SI pin, as is shown in the table entitled control register.

8.6 Register Maps

Table 2. State-Machine Inputs

EN	SI	CK	OUTPUT
L	L	X	All outputs enabled, CLK0 selected, control register disabled, default state
L	H	X	All outputs enabled, CLK1 selected, control register disabled
H	L	↑	First stage stores L, other stage stores data of previous stage
H	H		First stage stores H, other stage stores data of previous stage
L	X		Reset of state machine, shift and control registers

Table 3. Control Registers

BIT 10	BITS [0-9]	Q_N[0-9]
L	H	CLK0
H	H	CLK1
X	L	Outputs disabled

8.6.1 Register Descriptions

Table 4. Serial Input (SI) Sequence

BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLK_SEL	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCLVD110A device is a low-additive jitter, LVDS fan-out buffer that can generate ten copies of two selectable inputs. The CDCLVD110A can accept reference clock frequencies up to 1100 MHz. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

9.2 Typical Application

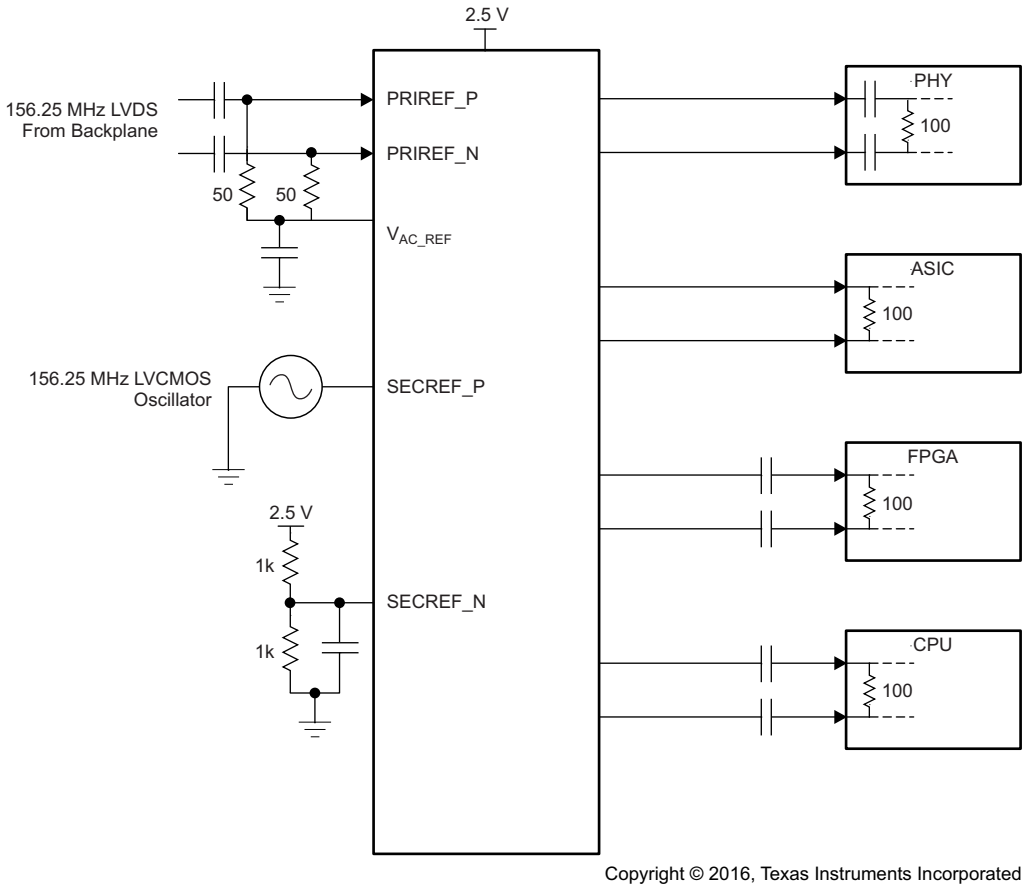


Figure 14. Fan-Out Buffer for Line Card Application

Typical Application (continued)

9.2.1 Design Requirements

The CDCLVD110A shown in Figure 14 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC-coupling with an LVDS driver such as the CDCLVD110A. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the CDCLVD110A. Again, no additional components are required.
- The FPGA requires external AC-coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC-coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.

9.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

Unused outputs can be left floating.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043).

9.2.3 Application Curves

The CDCLVD110A low-additive noise is shown in this line card application. The low-noise 156.25-MHz source with 40-fs RMS jitter drives the CDCLVD12xx, resulting in 64-fs RMS when integrated from 12 kHz to 20 MHz. The resultant additive jitter is a low 50-fs RMS for this configuration.

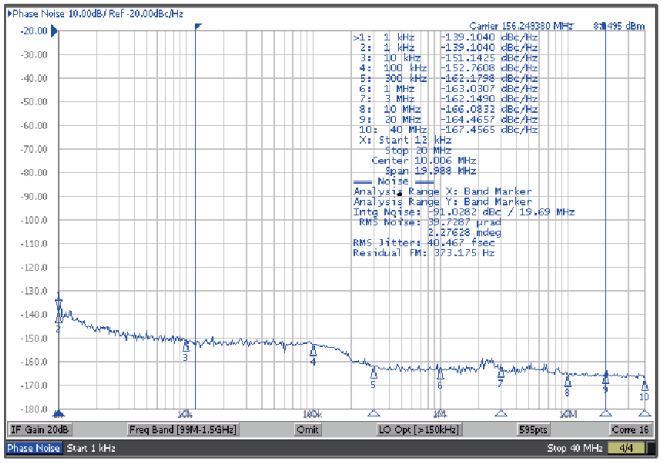


Figure 15. CDCLVD110A Reference Phase Noise, 40-fs RMS (12 kHz to 20 MHz)

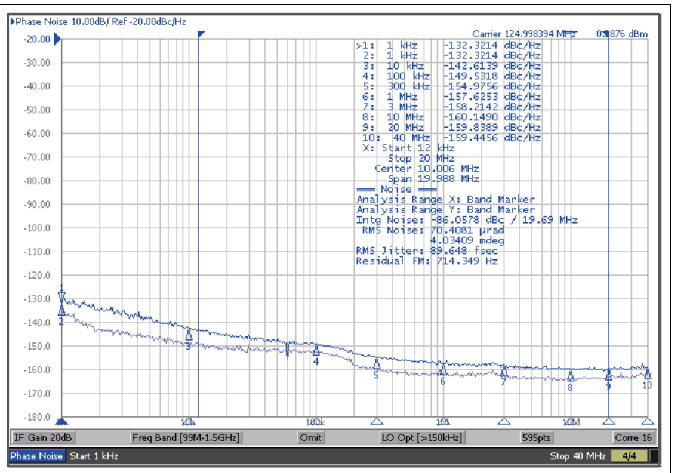


Figure 16. CDCLVD110A Output Phase Noise, 64-fs RMS (12 kHz to 20 MHz)

10 Power Supply Recommendations

10.1 Power Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter and phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power supply terminals and laid out with short loops to minimize inductance. TI recommends to add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply terminals in the package. TI recommends, but does not require, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low dc resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 17 illustrates this recommended power supply decoupling method.

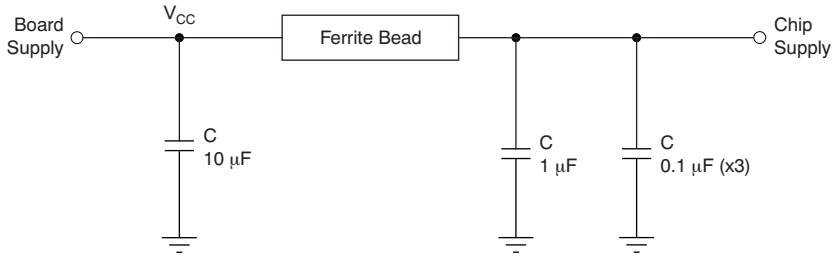


Figure 17. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

Power consumption of the CDCLVP111 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature must be limited to a maximum of 110°C. That is, as an estimate, ambient temperature (T_A) plus device power consumption times $R_{\theta JA}$ must not exceed 110°C.

The device package has an exposed pad that provides the primary heat removal path to the printed-circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 18 shows a recommended land and via pattern.

11.2 Layout Example

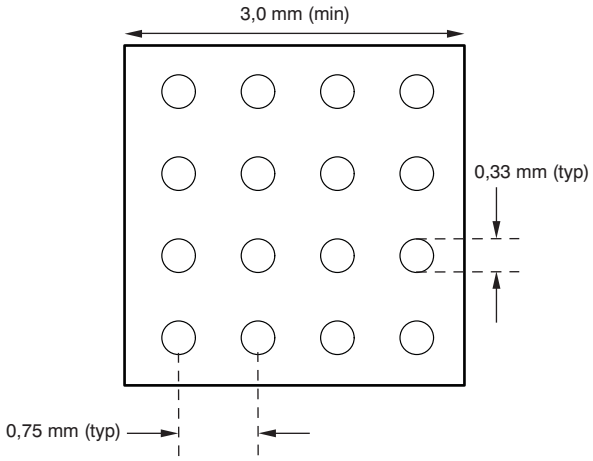


Figure 18. Recommended PCB Layout

11.3 Thermal Considerations

The CDCLVD110A supports high temperatures on the printed-circuit board (PCB) measured at the thermal pad. The system designer must ensure that the maximum junction temperature is not exceeded. Ψ_{JB} can allow the system designer to measure the board temperature with a fine gauge thermocouple and back calculate the junction temperature using Equation 1. Note that Ψ_{JB} is close to $R_{\theta JB}$ as 75% to 95% of a device's heat is dissipated by the PCB.

$$T_J = T_{PCB} + (\Psi_{JB} \times \text{Power}) \quad (1)$$

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

T_{PCB} = 85°C

Ψ_{JB} = 17.9°C/W

$\text{Power}_{\text{inclTerm}} = I_{max} \times V_{max}$ = 160 mA × 3.6 V = 576 mW (maximum power consumption including termination resistors)

$\text{Power}_{\text{exclTerm}}$ = 550.8 mW (maximum power consumption excluding termination resistors, see *Power Consumption of LVPECL and LVDS* for further details)

$\Delta T_J = \Psi_{JB} \times \text{Power}_{\text{exclTerm}}$ = 9.86°C/W × 550.8 mW = 9.86°C

$T_J = \Delta T_J + T_{Chassis}$ = 17.9°C + 85°C = 95.86°C (maximum junction temperature of 125°C is not violated)

Further information can be found at *Semiconductor and IC Package Thermal Metrics* (SPRA953) and *Using Thermal Calculation Tools for Analog Components* (SLUA566).

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Interfacing Between LVPECL, LVDS, and CML* (SCAA056)
- *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043)
- *Power Consumption of LVPECL and LVDS* (SLYT127)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using Thermal Calculation Tools for Analog Components* (SLUA566)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCLVD110ARHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVD110A
CDCLVD110ARHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVD110A
CDCLVD110AVF	Active	Production	LQFP (VF) | 32	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKLVD110A
CDCLVD110AVFR	Active	Production	LQFP (VF) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKLVD110A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

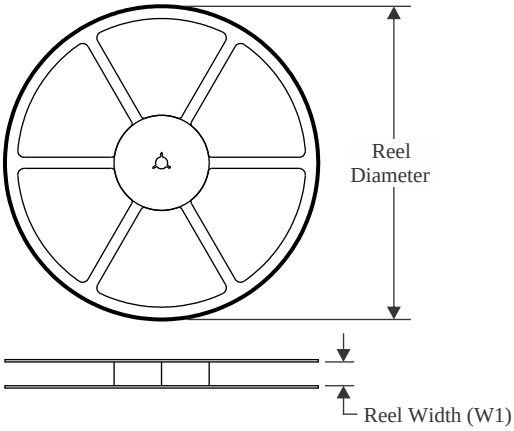
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

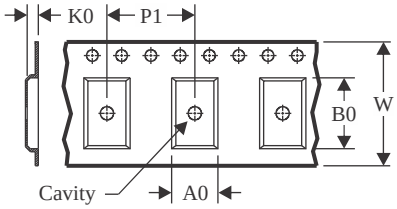
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

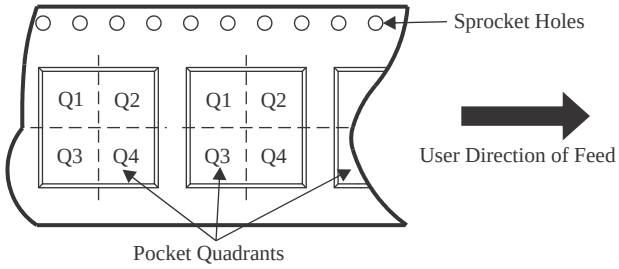


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

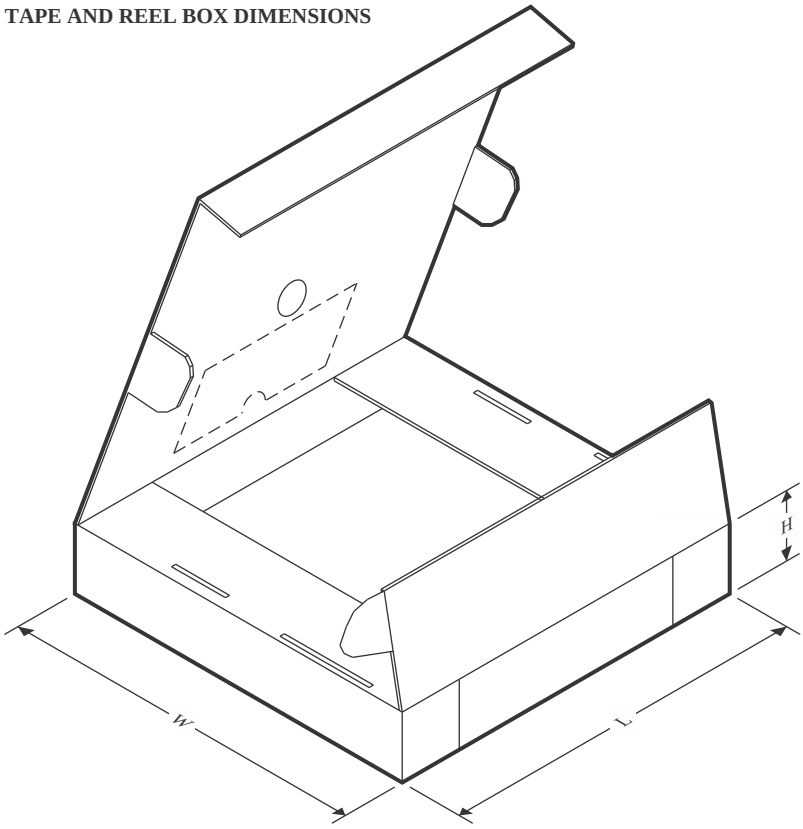
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD110ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCLVD110AVFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD110ARHBR	VQFN	RHB	32	3000	350.0	350.0	43.0
CDCLVD110AVFR	LQFP	VF	32	1000	367.0	367.0	38.0

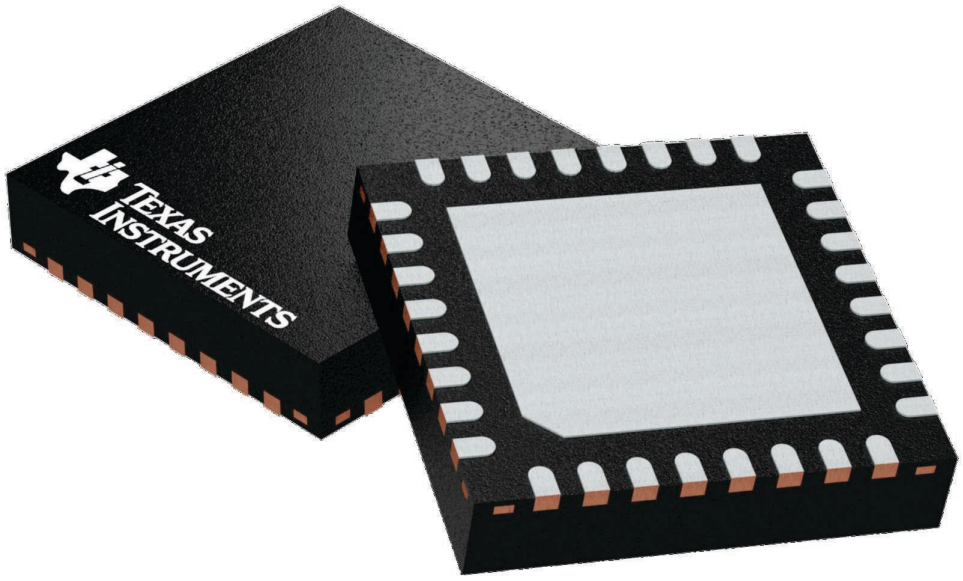
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

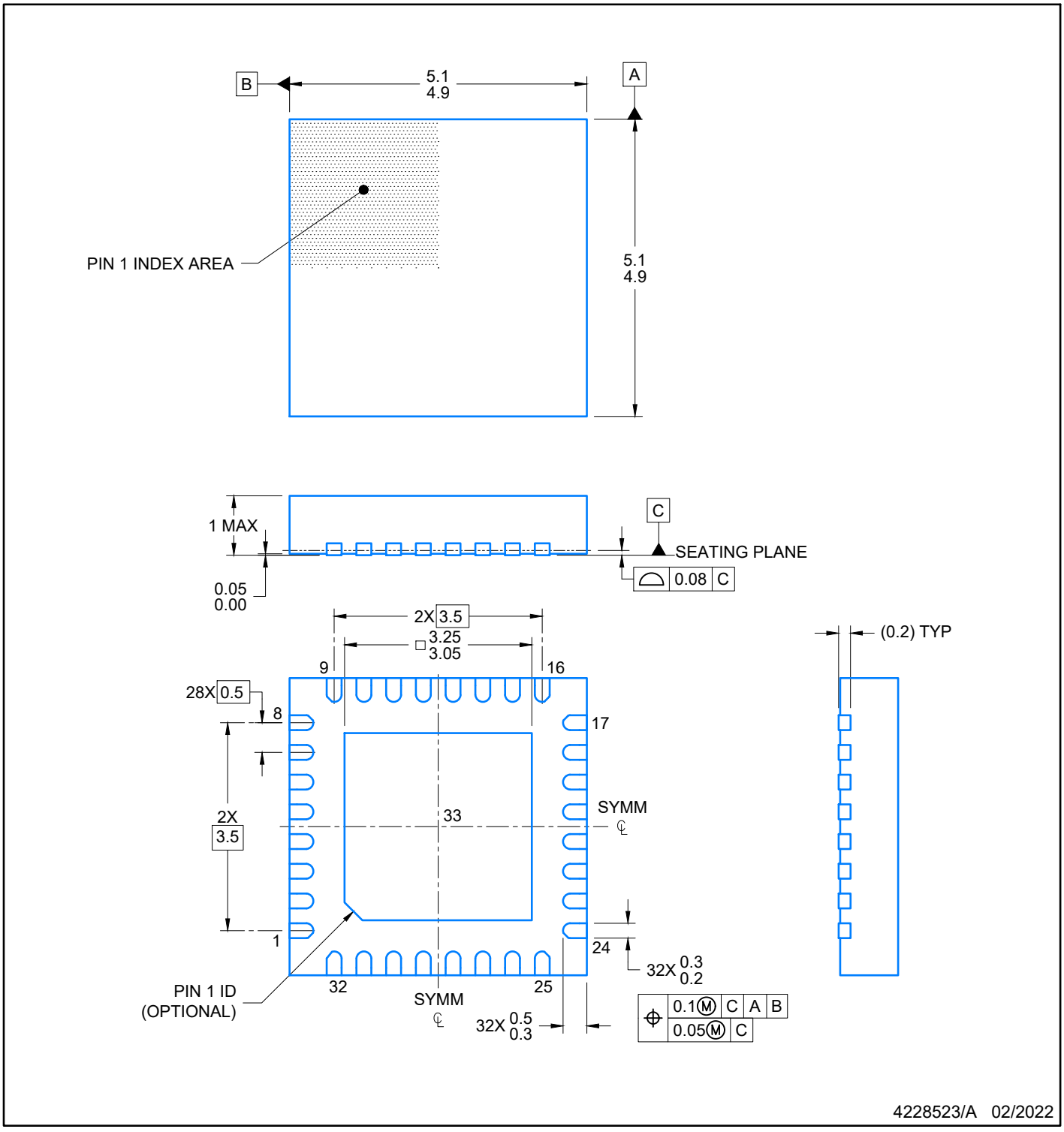
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



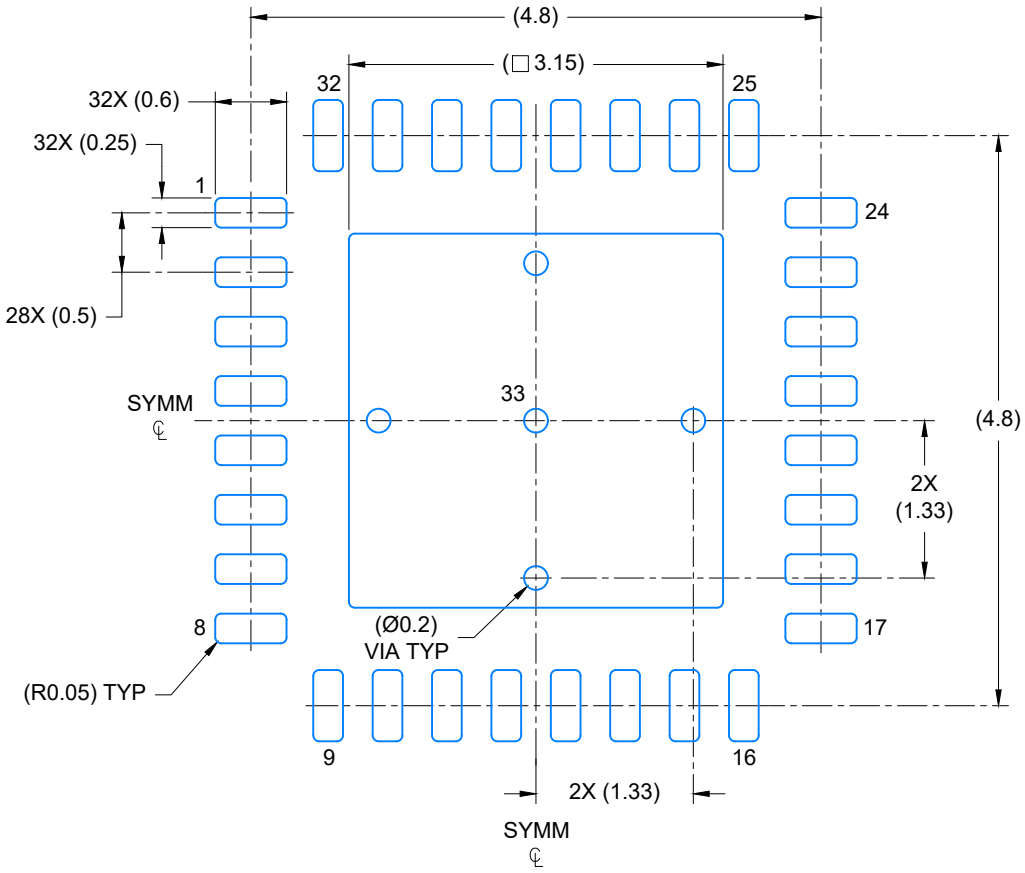
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

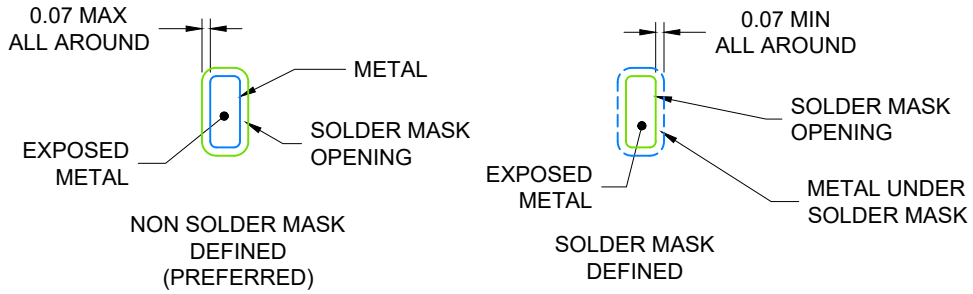


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

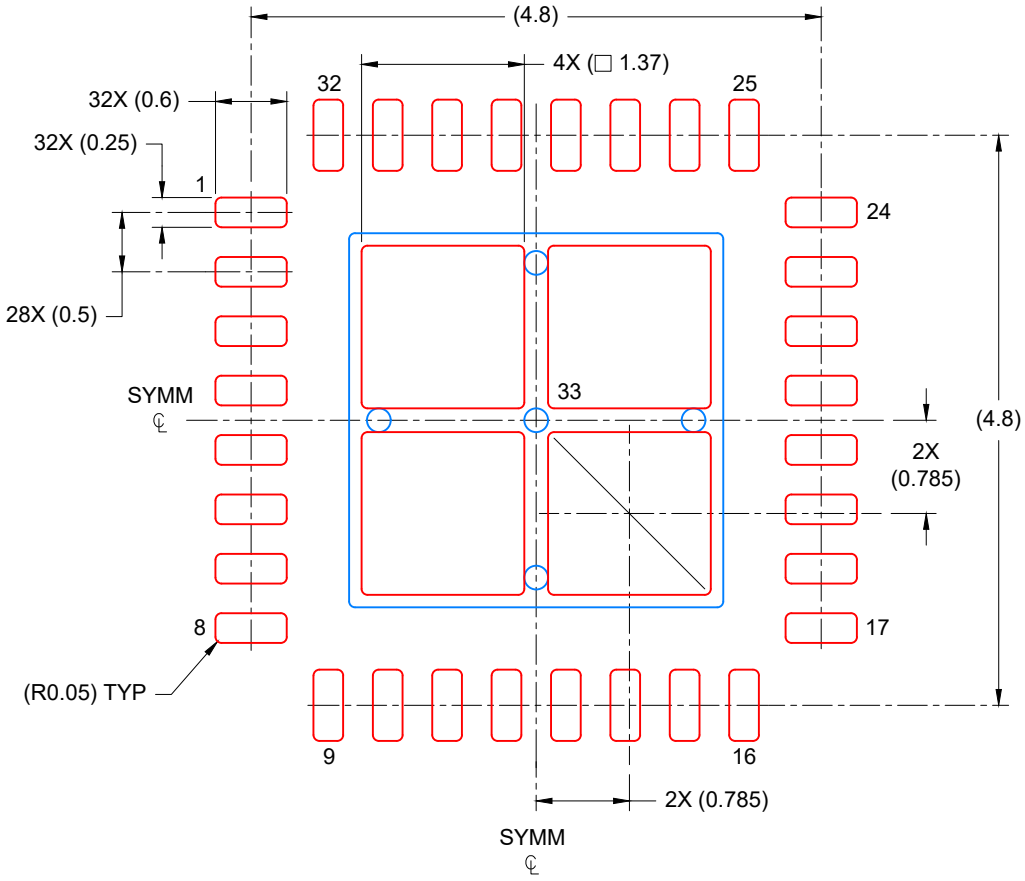


SOLDER MASK DETAILS

4228523/A 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4228523/A 02/2022

NOTES: (continued)

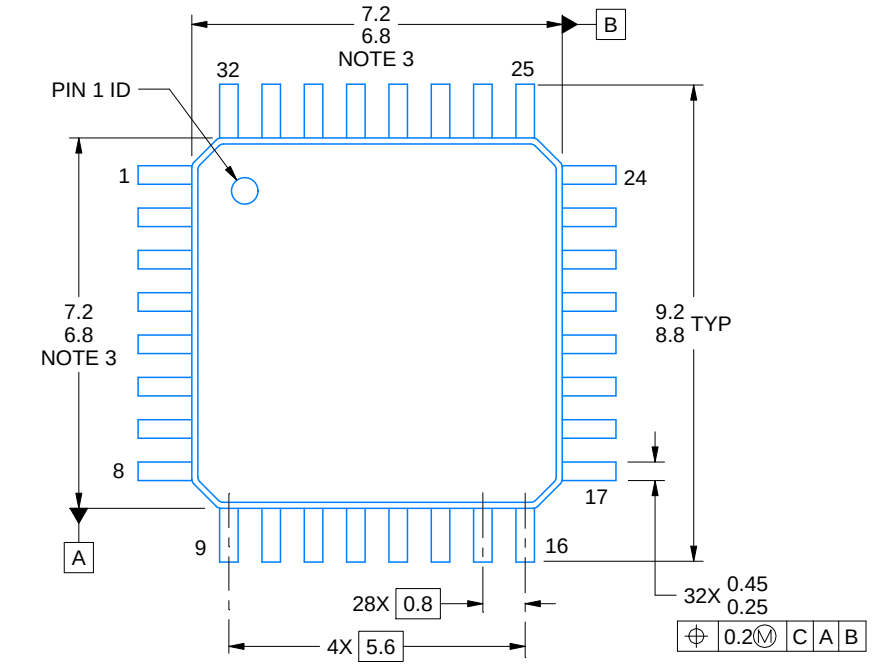
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

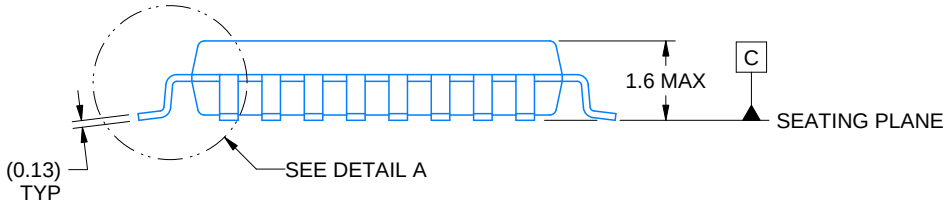
PACKAGE OUTLINE

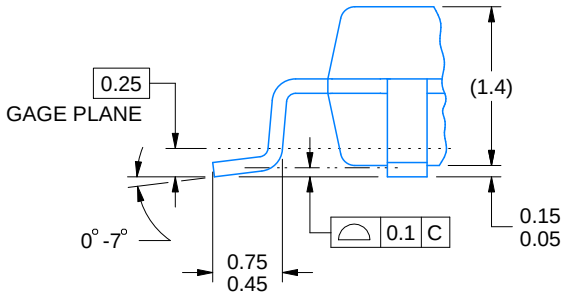
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK







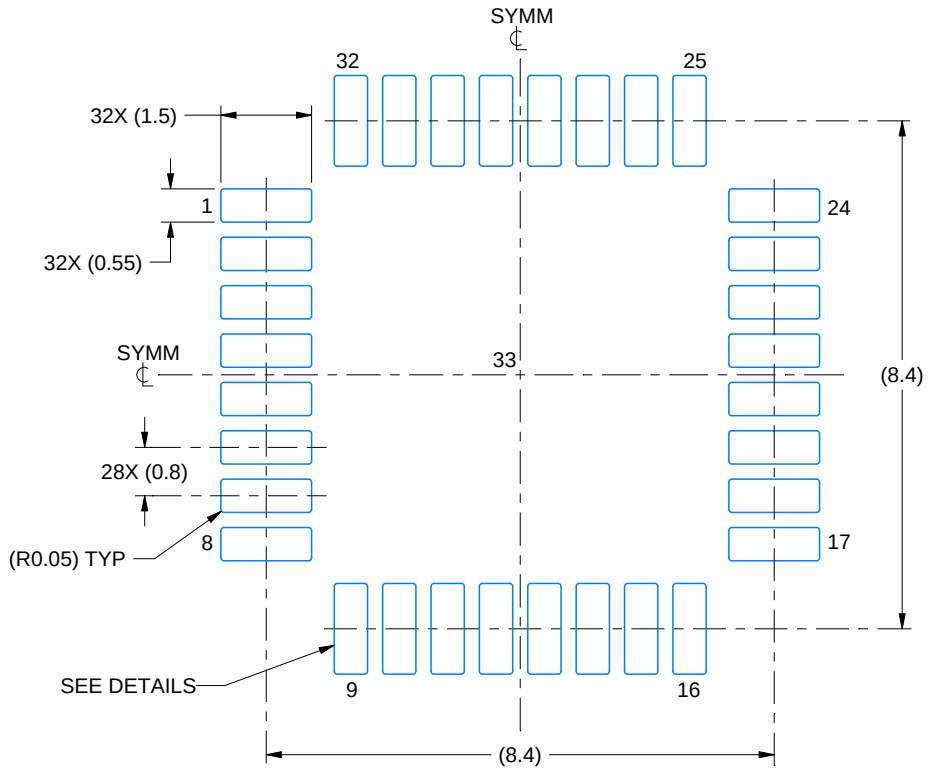
DETAIL A
TYPICAL

4219769/A 04/2019

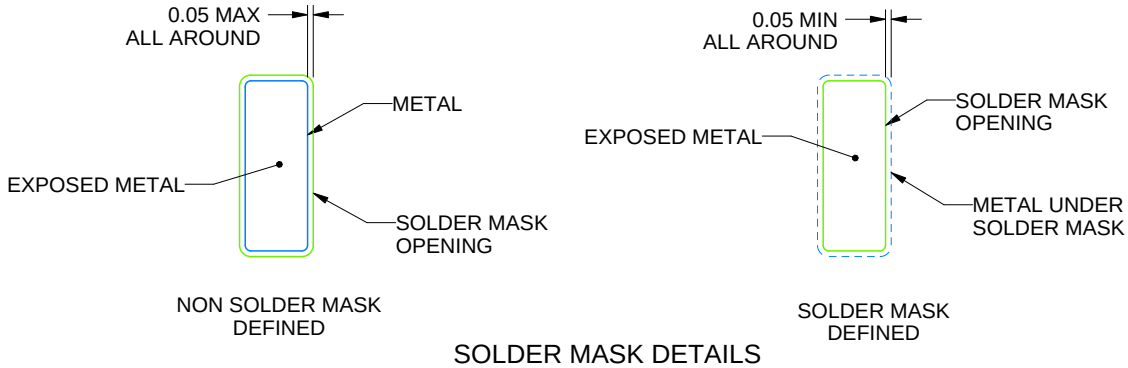
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

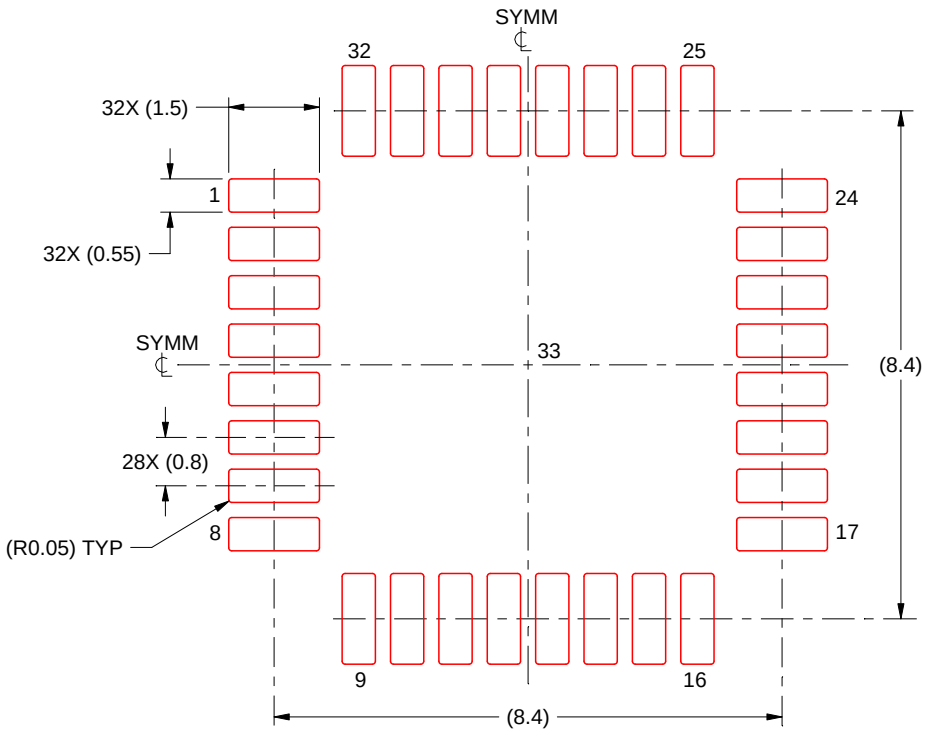


SOLDER MASK DETAILS

4219769/A 04/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4219769/A 04/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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