TEXAS INSTRUMENTS
INA818
JAJSH88A – APRIL 2019 – REVISED JUNE 2019

# INA818 35µV オフセット、8nV/√Hz ノイズ、低消費電力、高精度計装アンプ

## 1 特長

- 低いオフセット電圧： 10µV (標準値)、35µV (最大値)
- ゲイン・ドリフト係数： 5ppm/°C (G = 1)、35ppm/°C (G > 1) (最大値)
- ノイズ: 8nV/√Hz
- 帯域幅: 2MHz (G = 1)、270kHz (G = 100)
- 1nF の容量性負荷で安定
- ±60V まで入力を保護
- 同相除去比： 110dB、G = 10 (最小値)
- 電源電圧除去比：100dB、G = 1 (最小値)
- 消費電流： 385µA (最大値)
- 電源電圧範囲
  - シングル電源: 4.5V～36V
  - デュアル電源: ±2.25V～±18V
- 規定温度範囲: -40°C～+125°C
- パッケージ：8 ピン SOIC

## 2 アプリケーション

- 産業用モニタ
- 流量トランスミッタ
- バッテリ・テスト機器
- マルチパラメータ患者モニタ
- アナログ入力モジュール
- 半導体試験機器
- ポータブル計測装置

## 3 概要

INA818 は、単一電源またはデュアル電源の非常に幅広い電圧範囲で動作する、低消費電力の高精度計装アンプです。1 個の外付け抵抗で、1～10000 の任意のゲインを設定できます。このデバイスは、入力オフセット電圧、オフセット電圧ドリフト、入力バイアス電流、入力電圧ノイズ、入力電流ノイズを極めて低く抑えるスーパーβ入力トランジスタを使用することで、高い精度を実現します。追加回路により、±60V までの過電圧から入力を保護します。

INA818 は、高い同相除去比を実現するよう最適化されています。G = 1 での同相除去比は、全入力同相範囲を通じて 90dB を上回ります。このデバイスは、4.5V 単一電源および最高±18V のデュアル電源による低電圧動作用に設計されています。

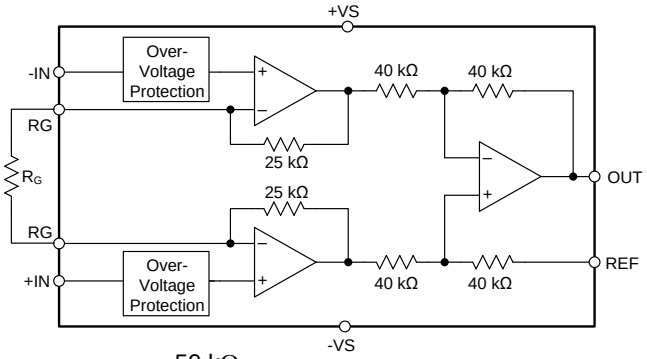
INA818 は 8 ピン SOIC パッケージで供給され、-40℃～+125℃の温度範囲で動作が規定されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| INA818 | SOIC (8) | 4.90mm×3.91mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

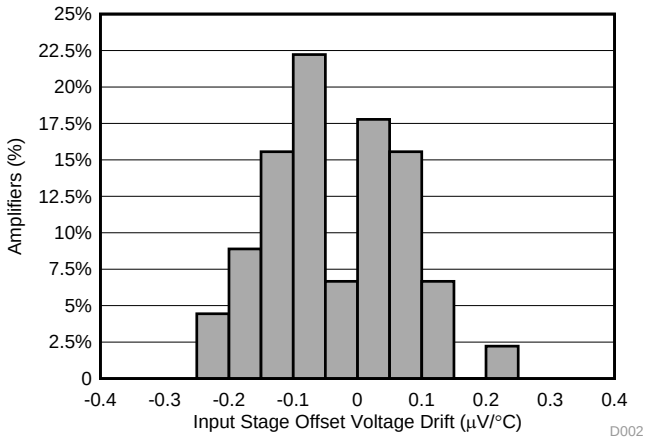
**INA818 の簡略化された内部回路図**




$$G = 1 + \frac{50\ k\Omega}{R_G}$$

$$V_O = G(V_{+IN} - V_{-IN}) + V_{REF}$$

**入力段のオフセット電圧ドリフトの代表的な分布**




D002

# 目次



## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**2019年4月発行のものから更新** **Page**

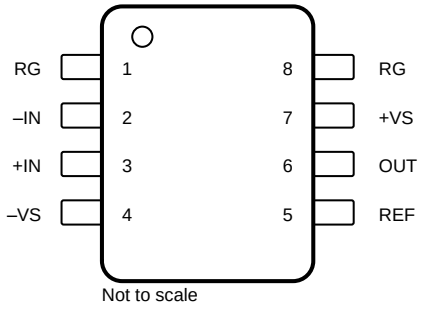
- ドキュメントのステータスを「事前情報」から「量産データ」に 変更 ... 1

# 5 Device Comparison Table

| DEVICE | DESCRIPTION | GAIN EQUATION | RG PINS AT PIN |
|---|---|---|---|
| INA818 | 35-µV Offset, 0.4 µV/°C $V_{OS}$ Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier | G = 1 + 50 kΩ / RG | 1, 8 |
| INA819 | 35-µV Offset, 0.4 µV/°C $V_{OS}$ Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier | G = 1 + 50 kΩ / RG | 2, 3 |
| INA821 | 35-µV Offset, 0.4 µV/°C $V_{OS}$ Drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier | G = 1 + 49.4 kΩ / RG | 2, 3 |
| INA828 | 50-µV Offset, 0.5 µV/°C $V_{OS}$ Drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier | G = 1 + 50 kΩ / RG | 1, 8 |
| INA333 | 25-µV $V_{OS}$, 0.1 µV/°C $V_{OS}$ Drift, 1.8-V to 5-V, RRO, 50-µA $I_Q$, Chopper-Stabilized INA | G = 1 + 100 kΩ / RG | 1, 8 |
| PGA280 | 20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V | Digital programmable | N/A |
| INA159 | G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion | G = 0.2 V/V | N/A |
| PGA112 | Precision Programmable Gain Op Amp With SPI | Digital programmable | N/A |

# 6 Pin Configuration and Functions

**D Package**
**8-Pin SOIC**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN | 2 | I | Negative (inverting) input |
| +IN | 3 | I | Positive (noninverting) input |
| OUT | 6 | O | Output |
| REF | 5 | I | Reference input. This pin must be driven by a low-impedance source. |
| RG | 1, 8 | — | Gain setting pin. Place a gain resistor between pin 1 and pin 8. |
| –VS | 4 | — | Negative supply |
| +VS | 7 | — | Positive supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage dual supply, $V_S$ = (V+) – (V–) | | ±20 | V |
| Supply voltage single supply, $V_S$ = (V+) – (V–) | | 40, (single supply) | V |
| Signal input pins | –60 | 60 | V |
| VREF pin | –20 | 20 | V |
| Signal output pins maximum voltage | ($-V_S$) - 0.5 | ($+V_S$) + 0.5 | V |
| Signal output pins maximum current | -50 | 50 | mA |
| Output short-circuit(2) | Continuous | | |
| Operating Temperature, $T_A$ | –50 | 150 | °C |
| Junction Temperature, $T_J$ | | 175 | |
| Storage Temperature, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to $V_S$ / 2.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage $V_S$ | Single-supply | 4.5 | 36 | V |
| | Dual-supply | ±2.25 | ±18 | |
| Specified temperature | Specified temperature | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | INA818 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 119.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 66.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 61.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 61.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{OSI}$ | Input stage offset voltage(1)(2) | | | 10 | 35 | µV |
| | | $T_A$ = –40°C to 125°C(3) | | | 75 | µV |
| | | drift vs temperature, $T_A$ = –40°C to 125°C | | | 0.4 | µV/°C |
| $V_{OSO}$ | Output stage offset voltage(1)(2) | | | 50 | 300 | µV |
| | | $T_A$ = –40°C to 125°C(3) | | | 800 | µV |
| | | drift vs temperature, $T_A$ = –40°C to 125°C | | | 5 | µV/°C |
| PSRR | Power-supply rejection ratio | G = 1, RTI | 110 | 120 | | dB |
| | | G = 10, RTI | 114 | 130 | | |
| | | G = 100, RTI | 130 | 135 | | |
| | | G = 1000, RTI | 136 | 140 | | |
| $z_{id}$ | Differential impedance | | | 100 \|\| 1 | | GΩ \|\| pF |
| $z_{ic}$ | Common-mode impedance | | | 100 \|\| 4 | | GΩ \|\| pF |
| | RFI filter, –3-dB frequency | | | 32 | | MHz |
| $V_{CM}$ | Operating input range(4) | | (V–) + 2 | | (V+) – 2 | V |
| | | $V_S$ = ±2.25 V to ±18 V, $T_A$ = –40°C to 125°C | See 図 51 to 図 54 | | | |
| | Input overvoltage range | $T_A$ = –40°C to 125°C(3) | | | ±60 | V |
| CMRR | Common-mode rejection ratio | At DC to 60 Hz, RTI, $V_{CM}$ = (V–) + 2 V to (V+) – 2 V, G = 1 | 90 | 105 | | dB |
| | | At DC to 60 Hz, RTI, $V_{CM}$ = (V–) + 2 V to (V+) – 2 V, G = 10 | 110 | 125 | | |
| | | At DC to 60 Hz, RTI, $V_{CM}$ = (V–) + 2 V to (V+) – 2 V, G = 100 | 130 | 145 | | |
| | | At DC to 60 Hz, RTI, $V_{CM}$ = (V–) + 2 V to (V+) – 2 V, G = 1000 | 140 | 150 | | |
| **BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = $V_S$ / 2 | | 0.15 | 0.5 | nA |
| | | $T_A$ = –40°C to 125°C | | | 2 | |
| $I_{OS}$ | Input offset current | $V_{CM}$ = $V_S$ / 2 | | 0.15 | 0.5 | nA |
| | | $T_A$ = –40°C to 125°C | | | 2 | |
| **NOISE VOLTAGE** | | | | | | |
| $e_{NI}$ | Input stage voltage noise(5) | f = 1 kHz, G = 100, $R_S$ = 0 Ω | | 8 | | nV/√Hz |
| | | $f_B$ = 0.1 Hz to 10 Hz, G = 100, $R_S$ = 0 Ω | | 0.19 | | $µV_{PP}$ |
| $e_{NO}$ | Output stage voltage noise(5) | f = 1 kHz, $R_S$ = 0 Ω | | 80 | | nV/√Hz |
| | | $f_B$ = 0.1 Hz to 10 Hz, $R_S$ = 0 Ω | | 2.6 | | $µV_{PP}$ |
| $I_n$ | Noise current | f = 1 kHz | | 130 | | fA/√Hz |
| | | $f_B$ = 0.1 Hz to 10 Hz, G = 100 | | 4.7 | | $pA_{PP}$ |
| **GAIN** | | | | | | |
| | Gain equation | | | 1 + (50 kΩ / $R_G$) | | V/V |
| G | Gain | | 1 | | 1000 | V/V |
| GE | Gain error | G = 1, $V_O$ = ±10 V | | ±0.005% | ±0.025% | |
| | | G = 10, $V_O$ = ±10 V | | ±0.025% | ±0.15% | |
| | | G = 100, $V_O$ = ±10 V | | ±0.025% | ±0.15% | |
| | | G = 1000, $V_O$ = ±10 V | | ±0.05% | | |
| | Gain error drift(6) | G = 1, $T_A$ = –40°C to 125°C, $V_O$ = ±10 V | | | ±5 | ppm/°C |
| | | G > 1, $T_A$ = –40°C to 125°C, $V_O$ = ±10 V | | | ±35 | |

(1) Total offset, referred-to-input (RTI): $V_{OS}$ = ($V_{OSI}$) + ($V_{OSO}$ / G).
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Specified by characterization.
(4) Input voltage range of the INA818 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves 図 51 through 図 54 for more information.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$
(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, $R_G$.

## Electrical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Gain nonlinearity | G = 1 to 10, $V_O$ = –10 V to 10 V, $R_L$ = 10 kΩ | | 1 | 10 | ppm |
| | | G = 100, $V_O$ = –10 V to 10 V, $R_L$ = 10 kΩ | | | 15 | |
| | | G = 1000, $V_O$ = –10 V to 10 V, $R_L$ = 10 kΩ | | 10 | | |
| | | G = 1 to 100, $V_O$ = –10 V to 10 V, $R_L$ = 2 kΩ | | 30 | | |
| **OUTPUT** | | | | | | |
| | Voltage swing | | (V–) + 0.15 | | (V+) – 0.15 | V |
| | Load capacitance stability | | | 1000 | | pF |
| $Z_O$ | Closed-loop output impedance | f = 10 kHz | | 5.0 | | Ω |
| $I_{SC}$ | Short-circuit current | Continuous to $V_S$ / 2 | | ±20 | | mA |
| **FREQUENCY RESPONSE** | | | | | | |
| BW | Bandwidth, –3 dB | G = 1 | | 2.0 | | MHz |
| | | G = 10 | | 890 | | kHz |
| | | G = 100 | | 270 | | |
| | | G = 1000 | | 30 | | |
| SR | Slew rate | G = 1, $V_O$ = ±10 V | | 0.9 | | V/µs |
| $t_S$ | Settling time | 0.01%, G = 1 to 100, $V_{STEP}$ = 10 V | | 12 | | µs |
| | | 0.01%, G = 1000, $V_{STEP}$ = 10 V | | 40 | | |
| | | 0.001%, G = 1 to 100, $V_{STEP}$ = 10 V | | 16 | | |
| | | 0.001%, G = 1000, $V_{STEP}$ = 10 V | | 60 | | |
| **REFERENCE INPUT** | | | | | | |
| $R_{IN}$ | Input impedance | | | 40 | | kΩ |
| | Voltage range | | (V–) | | (V+) | V |
| | Gain to output | | | 1 | | V/V |
| | Reference gain error | | | 0.01% | | |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current | $V_{IN}$ = 0 V | | 350 | 385 | µA |
| | | $V_{IN}$ = 0 V, $T_A$ = –40°C to 125°C | | | 520 | |

## 7.6 Typical Characteristics: Table of Graphs

**表 1. Table of Graphs**

| DESCRIPTION | FIGURE |
|---|---|
| Typical Distribution of Input Stage Offset Voltage | 図 1 |
| Typical Distribution of Input Stage Offset Voltage Drift | 図 2 |
| Typical Distribution of Output Stage Offset Voltage | 図 3 |
| Typical Distribution of Output Stage Offset Voltage Drift | 図 4 |
| Input Stage Offset Voltage vs Temperature | 図 5 |
| Output Stage Offset Voltage vs Temperature | 図 6 |
| Typical Distribution of Input Bias Current $T_A$ = 25°C | 図 7 |
| Typical Distribution of Input Bias Current $T_A$ = 90°C | 図 8 |
| Typical Distribution of Input Offset Current | 図 9 |
| Input Bias Current vs Temperature | 図 10 |
| Input Offset Current vs Temperature | 図 11 |
| Typical CMRR Distribution G = 1 | 図 12 |
| Typical CMRR Distribution G = 10 | 図 13 |
| CMRR vs Temperature G = 1 | 図 14 |
| CMRR vs Temperature G = 10 | 図 15 |
| Input Current vs Input Overvoltage | 図 16 |
| CMRR vs Frequency (RTI) | 図 17 |
| CMRR vs Frequency (RTI, 1-kΩ source imbalance) | 図 18 |
| Positive PSRR vs Frequency (RTI) | 図 19 |
| Negative PSRR vs Frequency (RTI) | 図 20 |
| Gain vs Frequency | 図 21 |
| Voltage Noise Spectral Density vs Frequency (RTI) | 図 22 |
| Current Noise Spectral Density vs Frequency (RTI) | 図 23 |
| 0.1-Hz to 10-Hz RTI Voltage Noise G = 1 | 図 24 |
| 0.1-Hz to 10-Hz RTI Voltage Noise G = 1000 | 図 25 |
| 0.1-Hz to 10-Hz RTI Current Noise | 図 26 |
| Typical Distribution of Gain Error G = 1 | 図 28 |
| Typical Distribution of Gain Error G = 10 | 図 29 |
| Input Bias Current vs Common-Mode Voltage | 図 27 |
| Gain Error vs Temperature G = 1 | 図 30 |
| Gain Error vs Temperature G = 10 | 図 31 |
| .Supply Current vs Temperature | 図 32 |
| Gain Nonlinearity G = 1 | 図 33 |
| Gain Nonlinearity G = 10 | 図 34 |
| Offset Voltage vs Negative Common-Mode Voltage | 図 35 |
| Offset Voltage vs Positive Common-Mode Voltage | 図 36 |
| Positive Output Voltage Swing vs Output Current | 図 37 |
| Negative Output Voltage Swing vs Output Current | 図 38 |
| Short Circuit Current vs Temperature | 図 39 |
| Large-Signal Frequency Response | 図 40 |
| THD+N vs Frequency | 図 41 |
| Overshoot vs Capacitive Loads | 図 42 |
| Small-Signal Response G = 1 | 図 43 |
| Small-Signal Response G = 10 | 図 44 |
| Small-Signal Response G = 100 | 図 45 |
| Small-Signal Response G = 1000 | 図 46 |

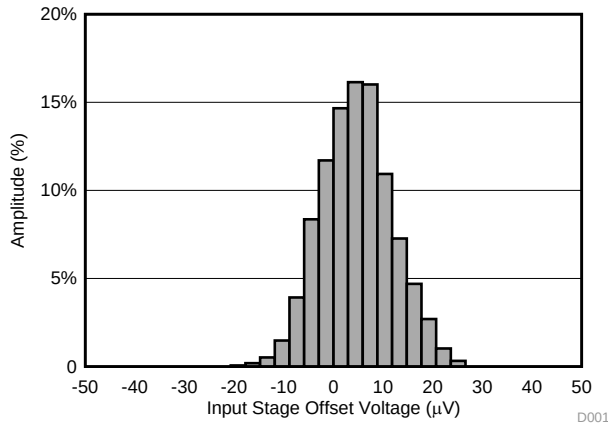
## Typical Characteristics: Table of Graphs (continued)

**表 1. Table of Graphs (continued)**

| DESCRIPTION | FIGURE |
|---|---|
| Large Signal Step Response | 図 47 |
| Closed-Loop Output Impedance | 図 48 |
| Differential-Mode EMI Rejection Ratio | 図 49 |
| Common-Mode EMI Rejection Ratio | 図 50 |
| Input Common-Mode Voltage vs Output Voltage G = 1, $V_S$ = 5 V | 図 51 |
| Input Common-Mode Voltage vs Output Voltage G = 100, $V_S$ = 5 V | 図 52 |
| Input Common-Mode Voltage vs Output Voltage $V_S$ =±5 V | 図 53 |
| Input Common-Mode Voltage vs Output Voltage $V_S$ =±15 V | 図 54 |

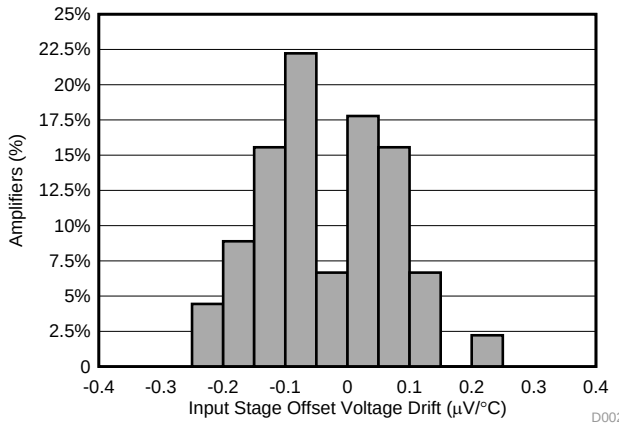
## 7.7 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)



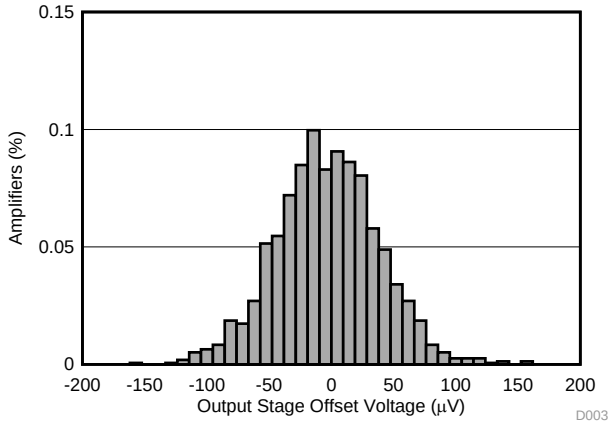

N = 1555 Mean = 4.71 µV Std. Dev. = 7.12 µV

**図 1. Typical Distribution of Input Stage Offset Voltage**



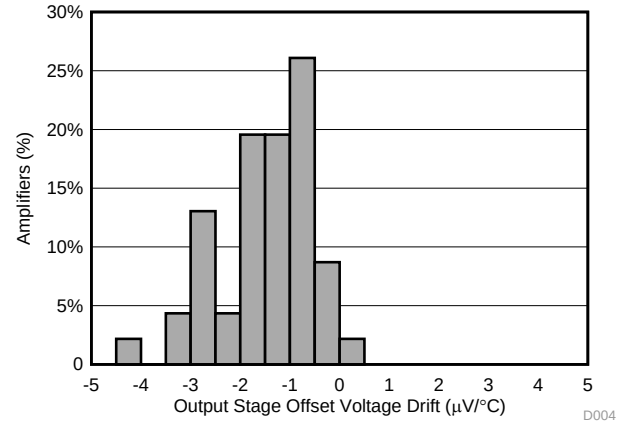

N = 45 Mean = 0.0357 µV/°C Std. Dev. = 0.099 µV/°C

**図 2. Typical Distribution of Input Stage Offset Voltage Drift**



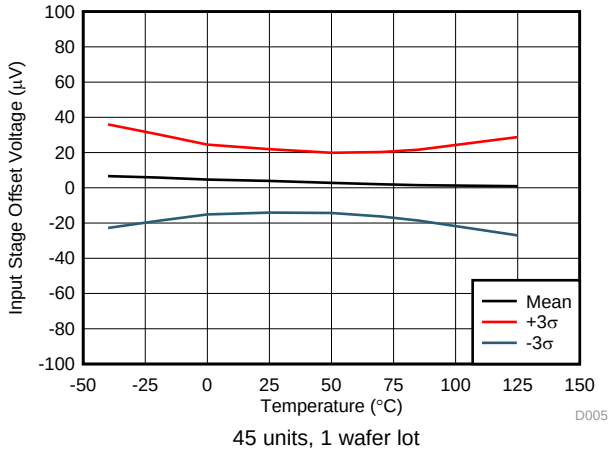

N = 1555 Mean = –3.18 µV Std. Dev. = 41.26 µV

**図 3. Typical Distribution of Output Stage Offset Voltage**



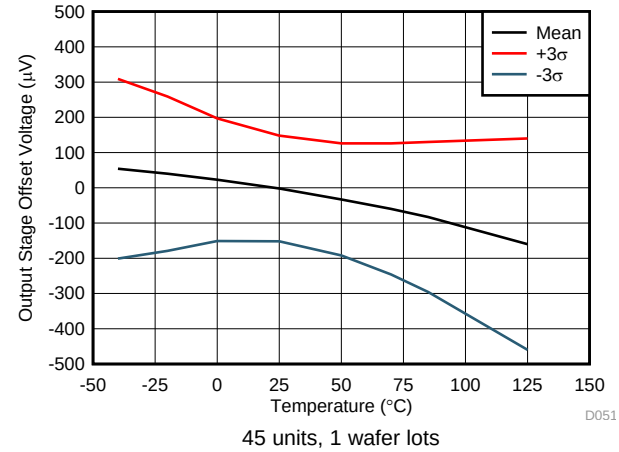

N = 45 Mean = –1.49 µV/°C Std. Dev. = 0.89 µV/°C

**図 4. Typical Distribution of Output Stage Offset Voltage Drift**




45 units, 1 wafer lot

**図 5. Input Stage Offset Voltage vs Temperature**

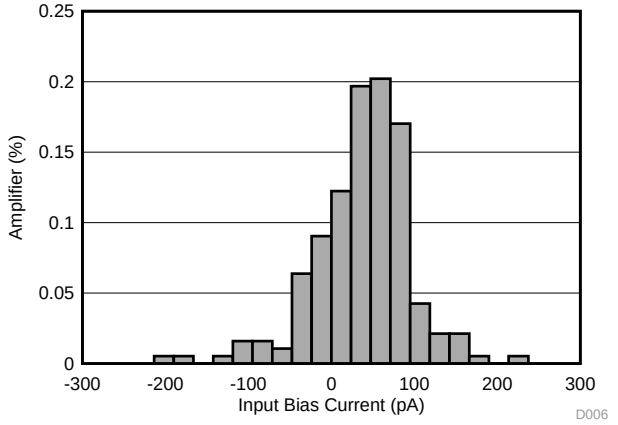



45 units, 1 wafer lots

**図 6. Output Stage Offset Voltage vs Temperature**

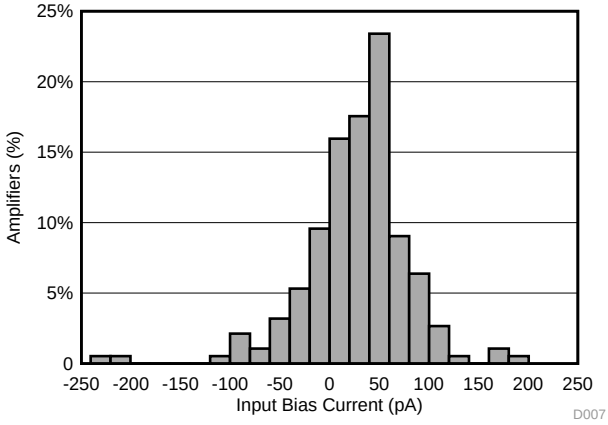
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)



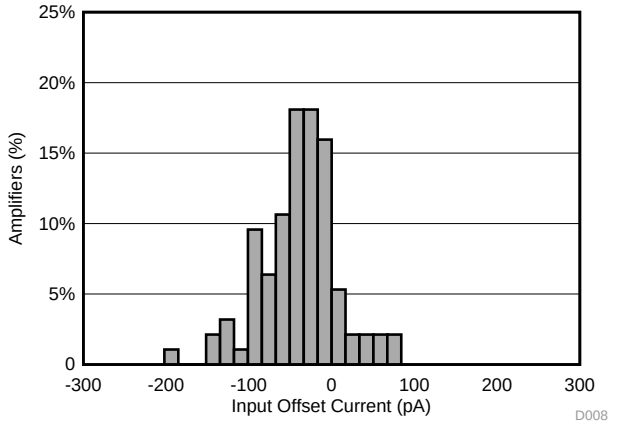

N = 94 Mean = 37.13 pA Std. Dev. = 57.65 pA
$T_A$ = 25°C

**図 7. Typical Distribution of Input Bias Current**



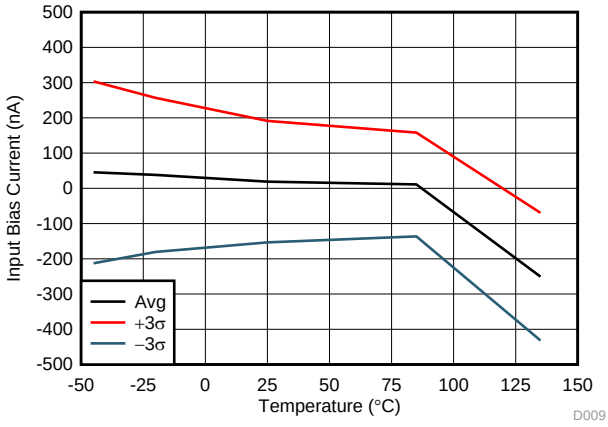

N = 94 Mean = –27.65 pA Std. Dev. = 52.58 pA
$T_A$ = 90°C

**図 8. Typical Distribution of Input Bias Current**



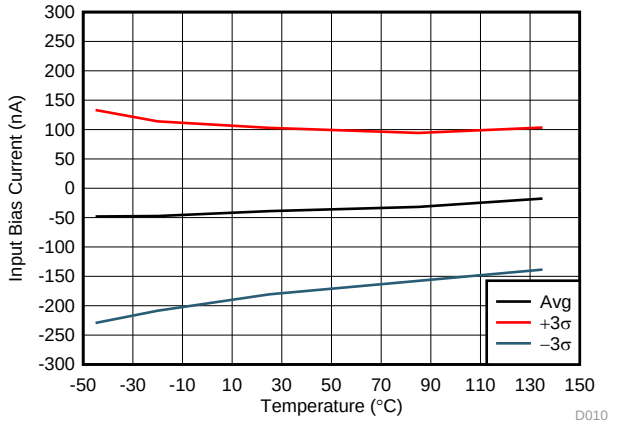

N = 94 Mean = –38.82 pA Std. Dev. = 47.24 pA

**図 9. Typical Distribution of Input Offset Current**



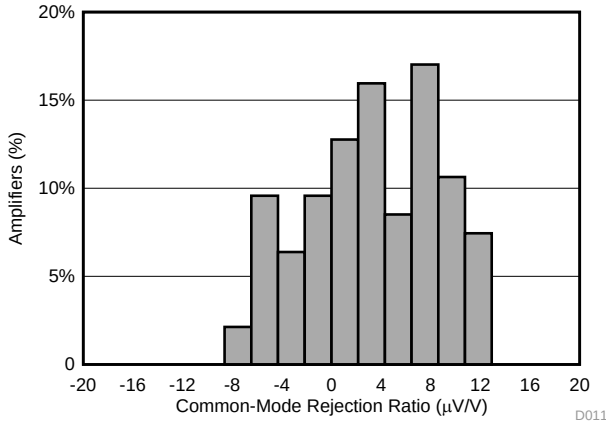

N = 94 G = 1

**図 10. Input Bias Current vs Temperature**




N = 94 G = 1

**図 11. Input Offset Current vs Temperature**

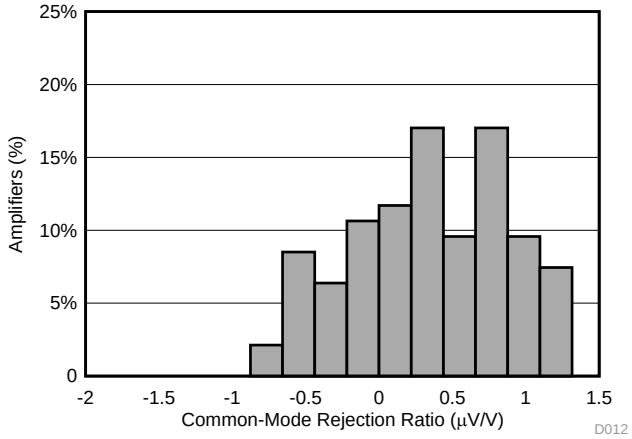



N = 94 Mean = 3.23 µV/V Std. Dev. = 5.38 µV/V
G = 1

**図 12. Typical CMRR Distribution**

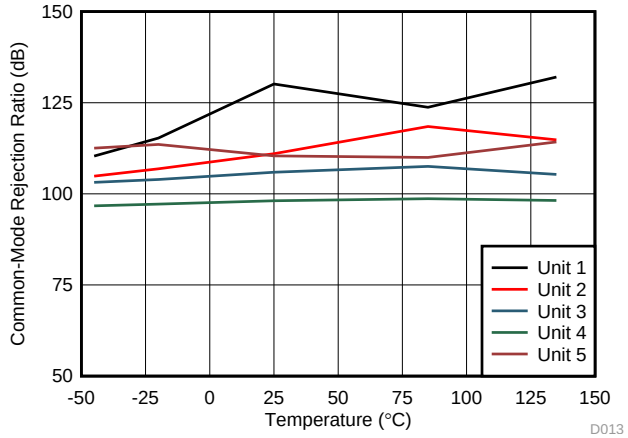
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)



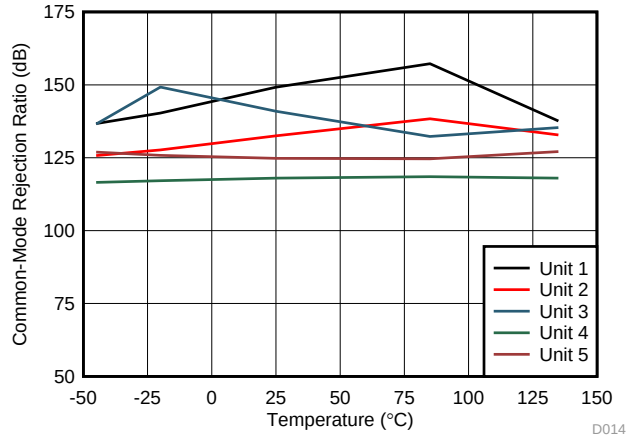

N = 94 Mean = 0.34 µV/V Std. Dev. = 0.54 µV/V
G = 10

**図 13. Typical CMRR Distribution**



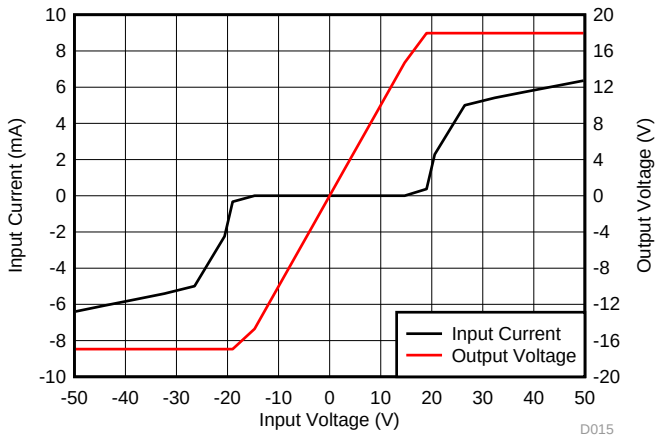

5 typical units G = 1

**図 14. CMRR vs Temperature**




5 typical units G = 10

**図 15. CMRR vs Temperature**




$V_S$ = 36 V

**図 16. Input Current vs Input Overvoltage**

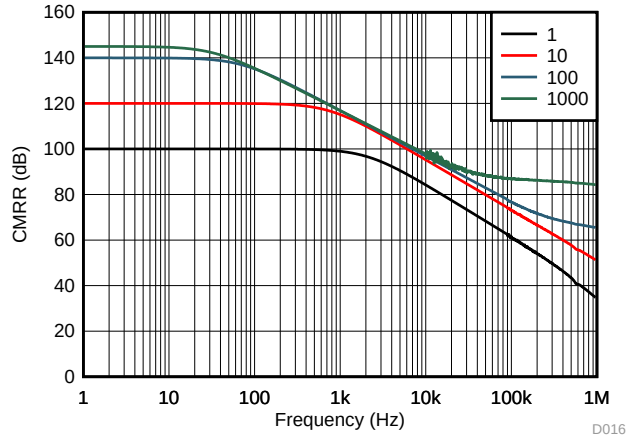
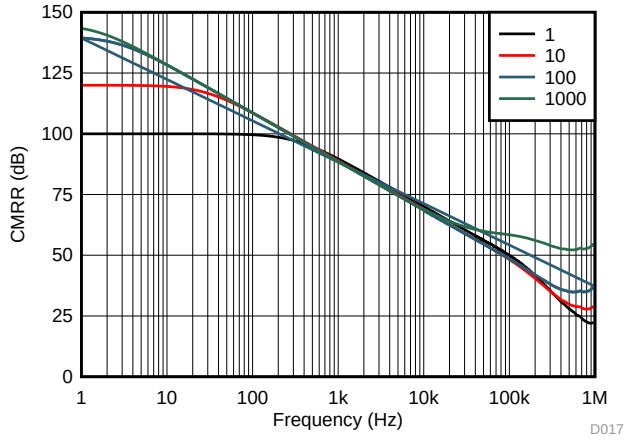



**図 17. CMRR vs Frequency (RTI)**




1-kΩ source imbalance

**図 18. CMRR vs Frequency (RTI)**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

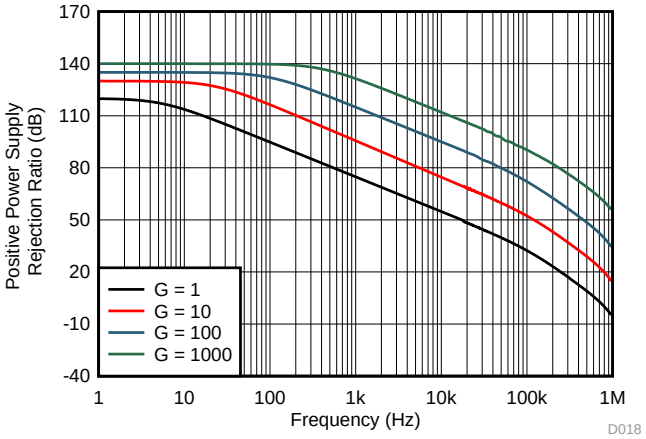



図 19. Positive PSRR vs Frequency (RTI)

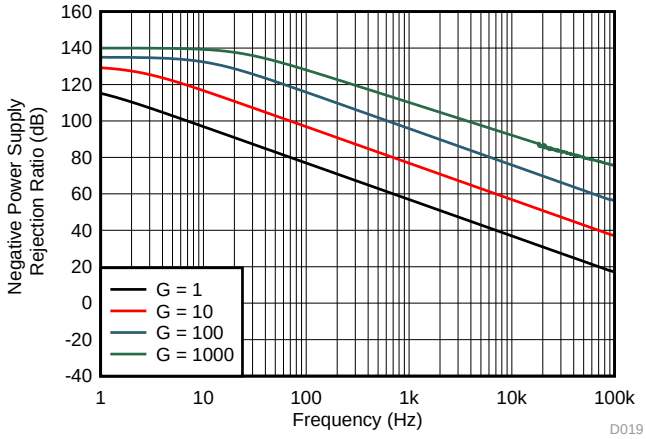



図 20. Negative PSRR vs Frequency (RTI)

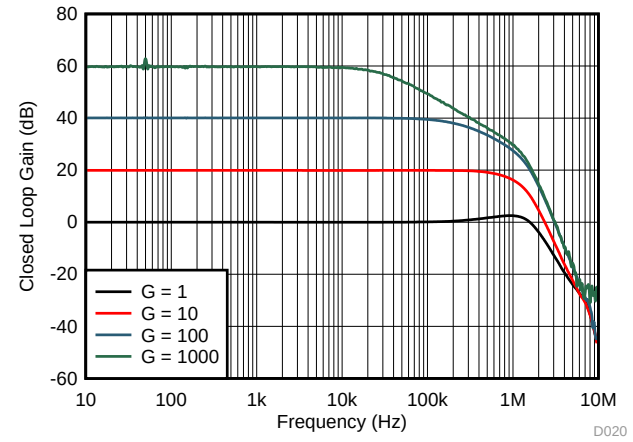



図 21. Gain vs Frequency

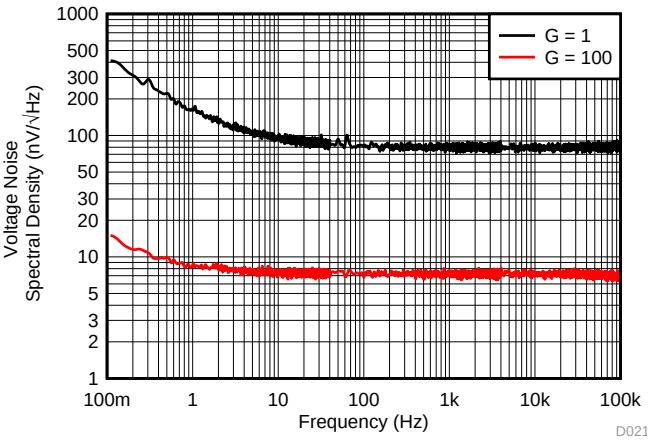



図 22. Voltage Noise Spectral Density vs Frequency (RTI)

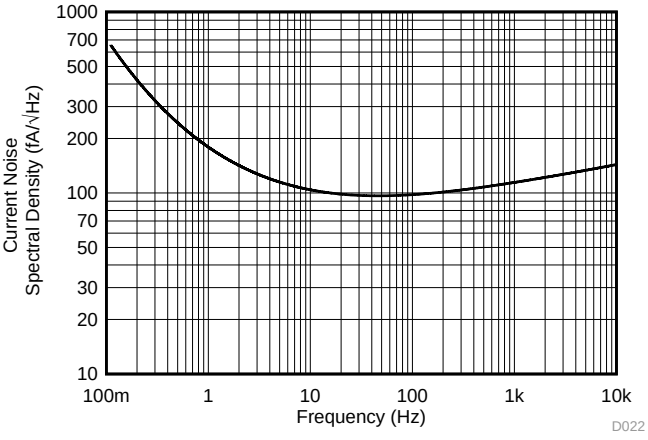
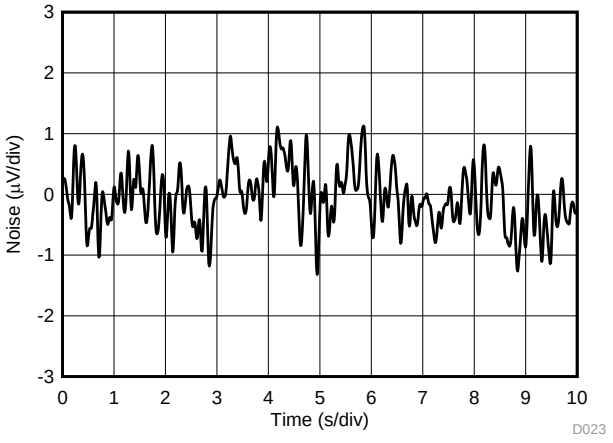



図 23. Current Noise Spectral Density vs Frequency (RTI)

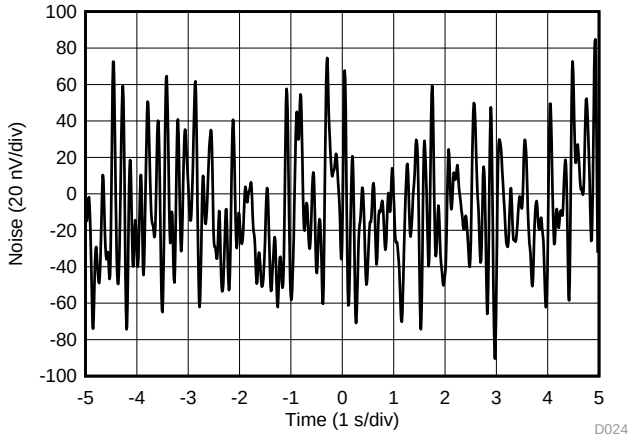



G = 1

図 24. 0.1-Hz to 10-Hz RTI Voltage Noise

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)




G = 1000

**図 25. 0.1-Hz to 10-Hz RTI Voltage Noise**

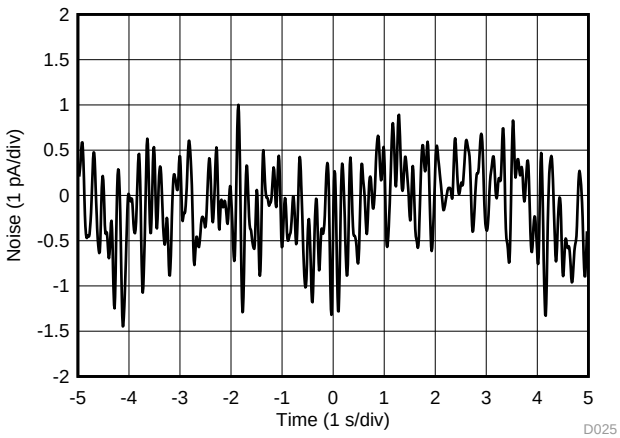
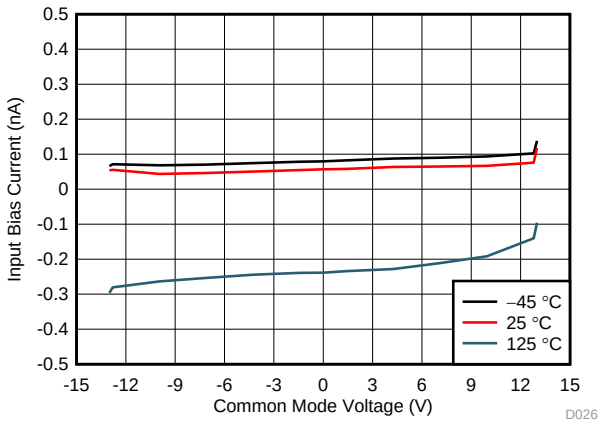
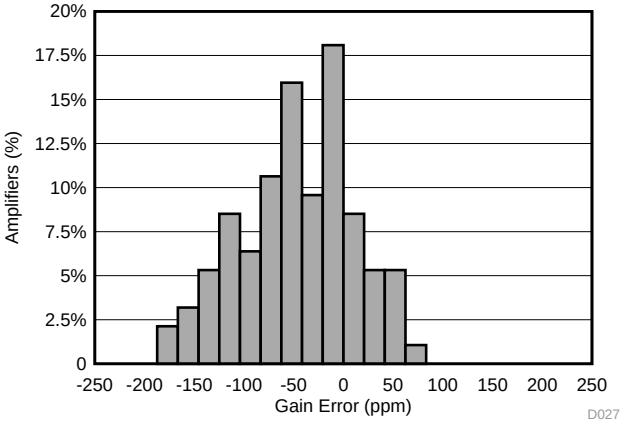



**図 26. 0.1-Hz to 10-Hz RTI Current Noise**



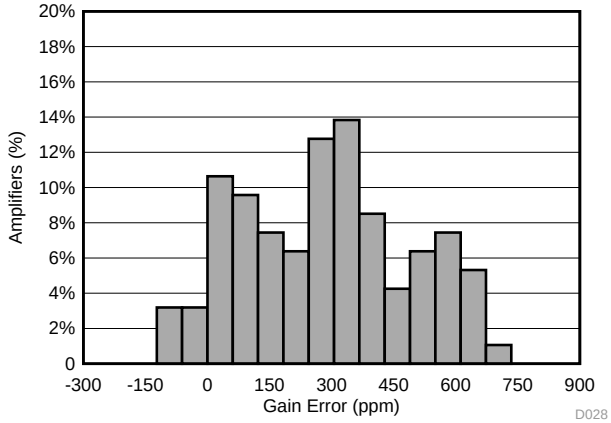

$V_S$ = ±15 V

**図 27. Input Bias Current vs Common-Mode Voltage**



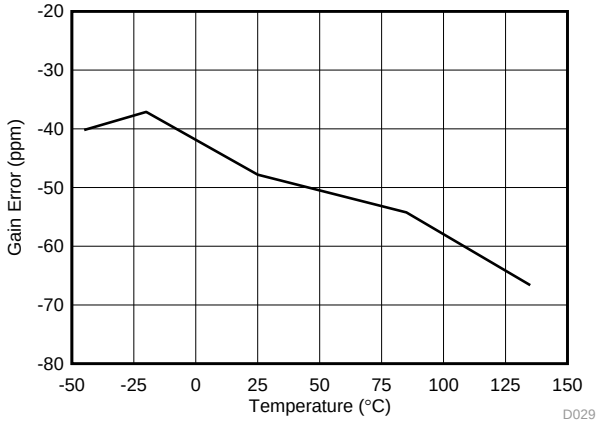

N = 94 Mean = –48 ppm Std. Dev. = 58 ppm
G = 1

**図 28. Typical Distribution of Gain Error G = 1**




N = 94 Mean = 286 ppm Std. Dev. = 204 ppm
G = 10

**図 29. Typical Distribution of Gain Error G = 10**




G = 1

**図 30. Gain Error vs Temperature**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

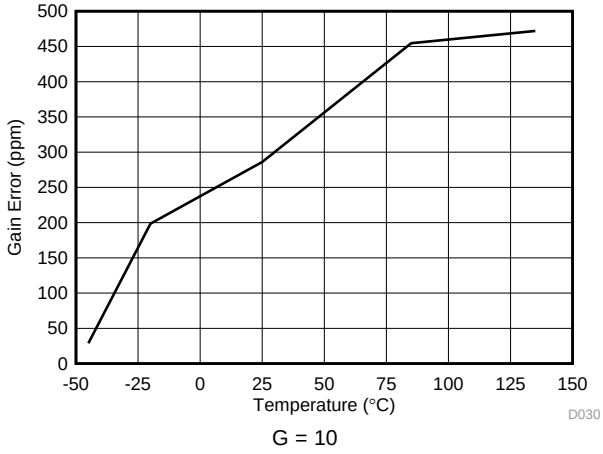



図 31. Gain Error vs Temperature

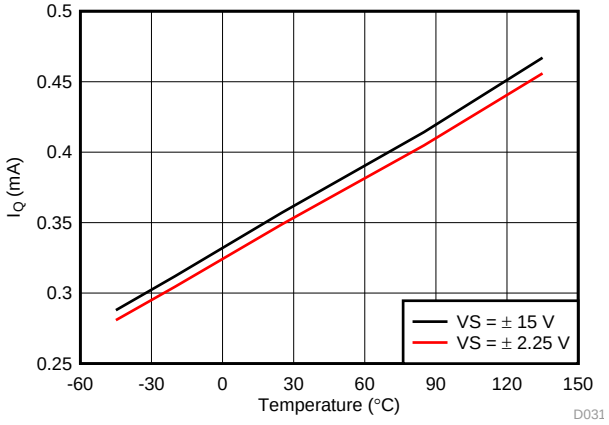



図 32. Supply Current vs Temperature

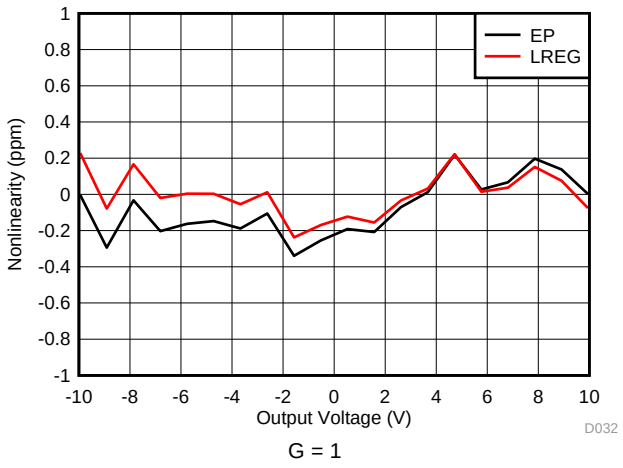



図 33. Gain Nonlinearity

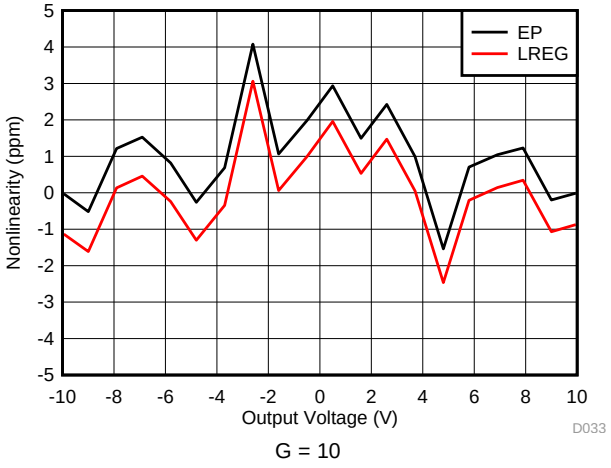



図 34. Gain Nonlinearity

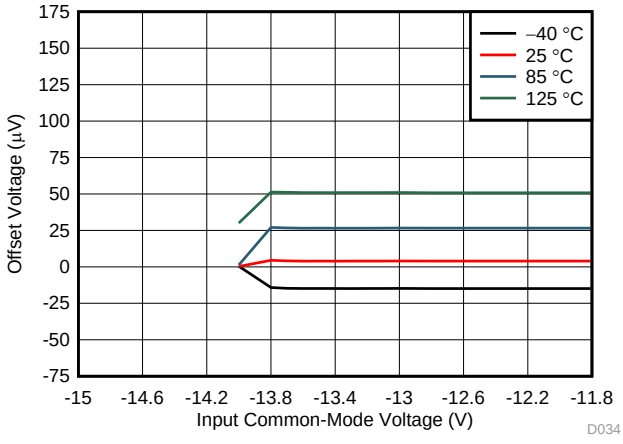



図 35. Offset Voltage vs Negative Common-Mode Voltage

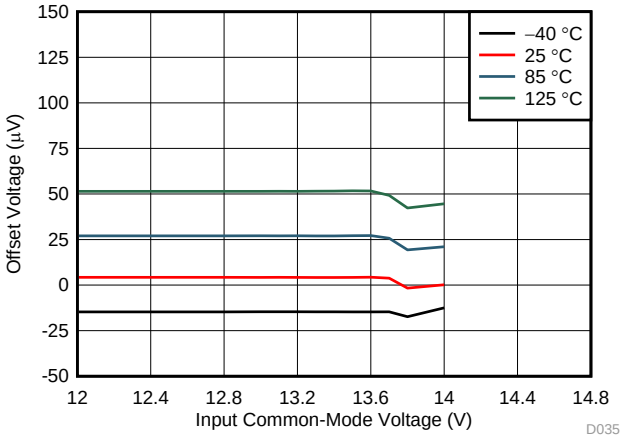



図 36. Offset Voltage vs Positive Common-Mode Voltage

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

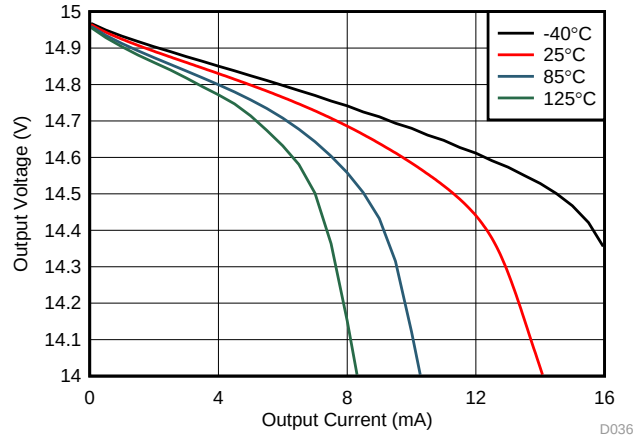



図 37. Positive Output Voltage Swing vs Output Current

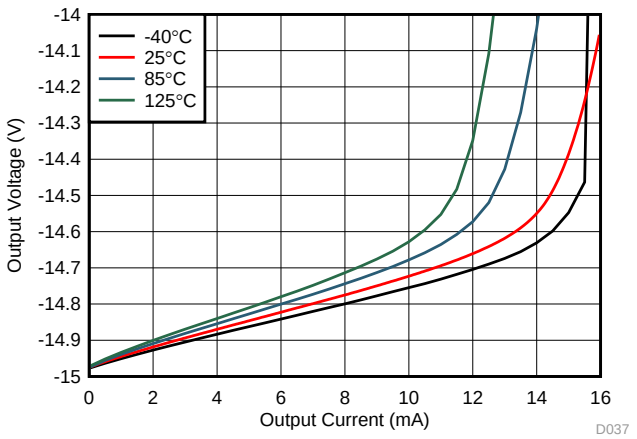



図 38. Negative Output Voltage Swing vs Output Current

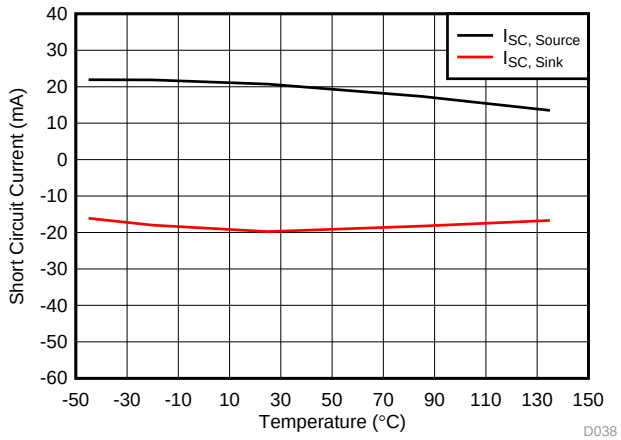



図 39. Short Circuit Current vs Temperature

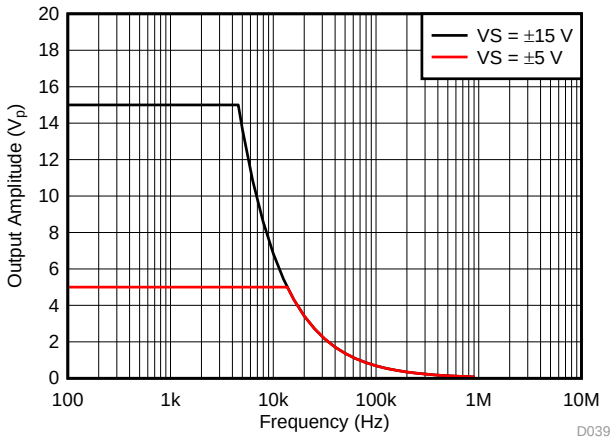
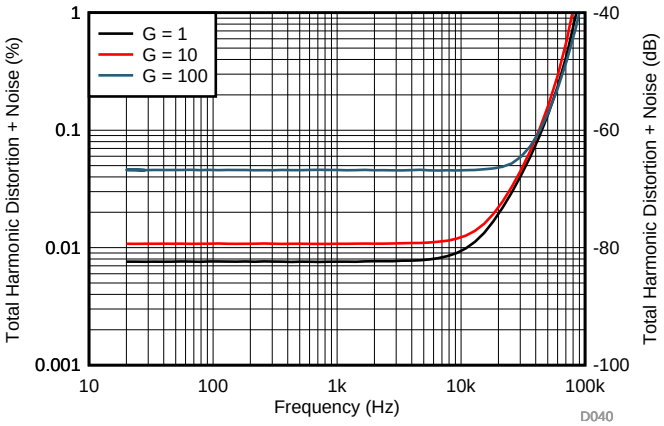



図 40. Large-Signal Frequency Response




500-kHz measurement bandwidth

1-$V_{RMS}$ output voltage 100-kΩ load

図 41. THD+N vs Frequency

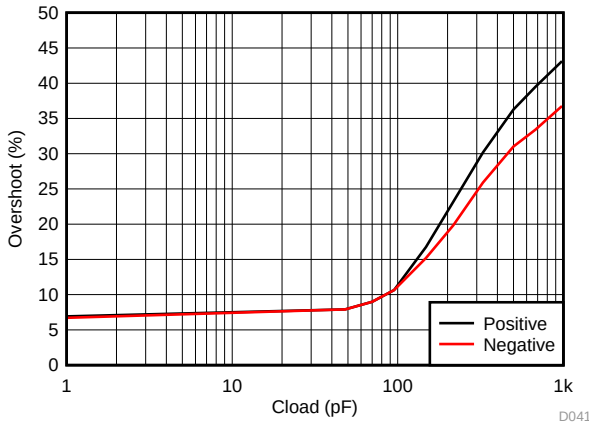
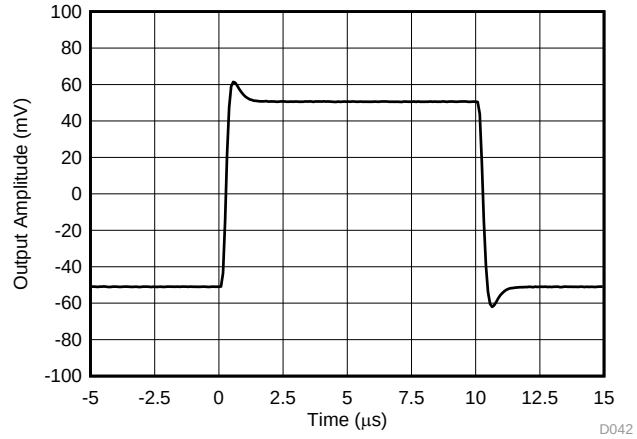



図 42. Overshoot vs Capacitive Loads

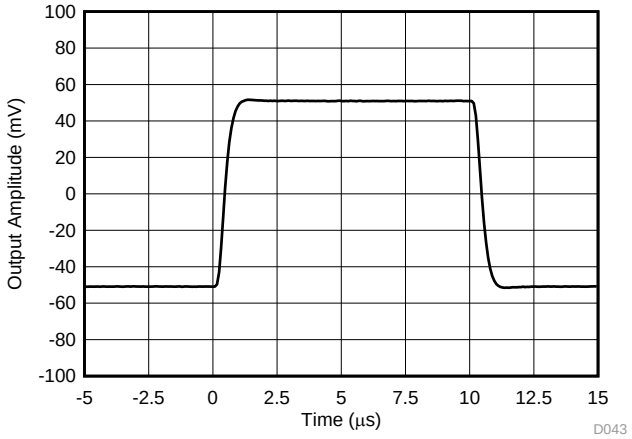
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)



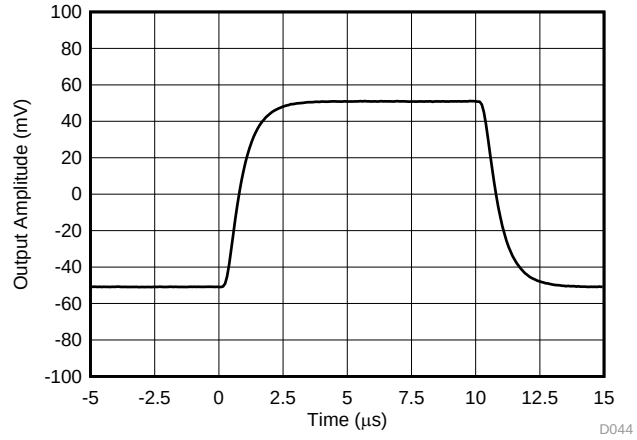

G = 1 $R_L$ = 10 kΩ $C_L$ = 100 pF

**図 43. Small-Signal Response**



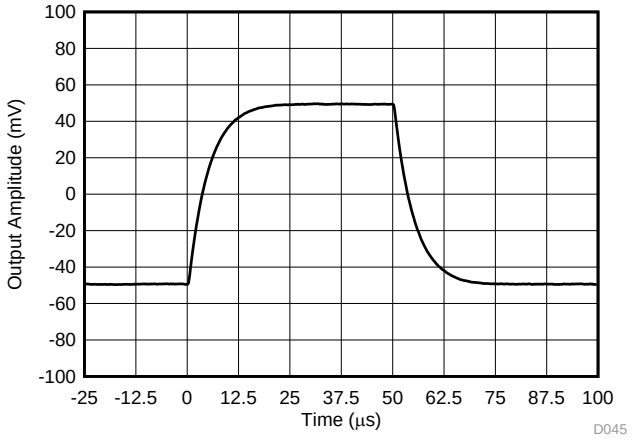

G = 10 $R_L$ = 10 kΩ $C_L$ = 100 pF

**図 44. Small-Signal Response**




G = 100 $R_L$ = 10 kΩ $C_L$ = 100 pF

**図 45. Small-Signal Response**




G = 1000 $R_L$ = 10 kΩ $C_L$ = 100 pF

**図 46. Small-Signal Response**

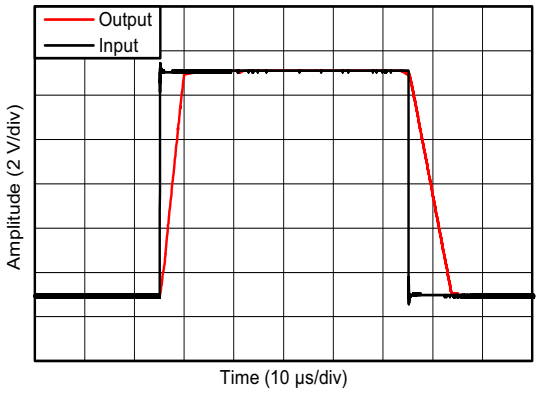



**図 47. Large Signal Step Response**

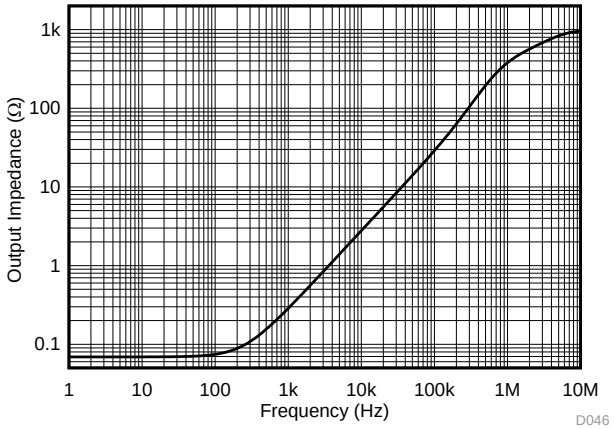



**図 48. Closed-Loop Output Impedance**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, $V_{REF}$ = 0 V, and G = 1 (unless otherwise noted)

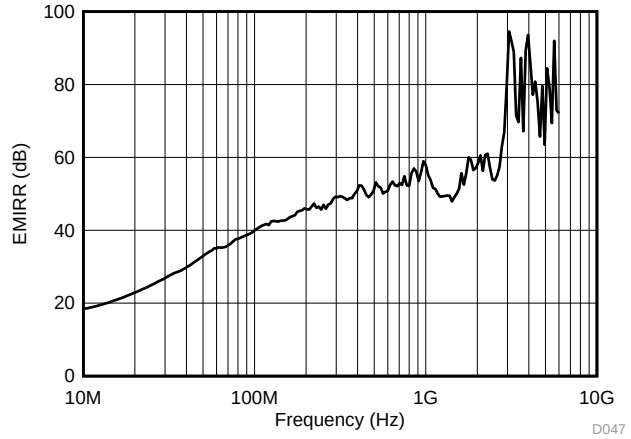



図 49. Differential-Mode EMI Rejection Ratio

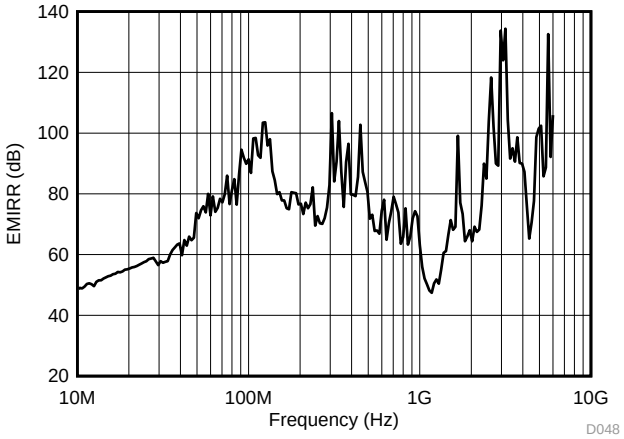
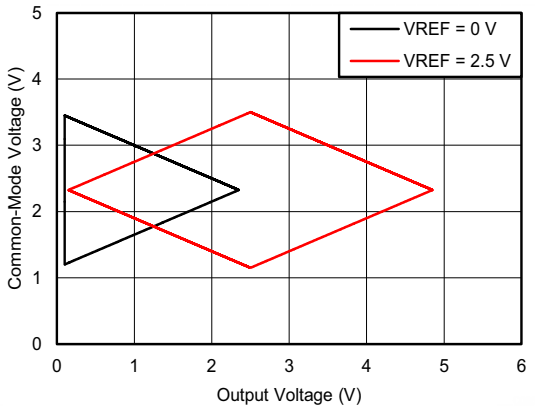
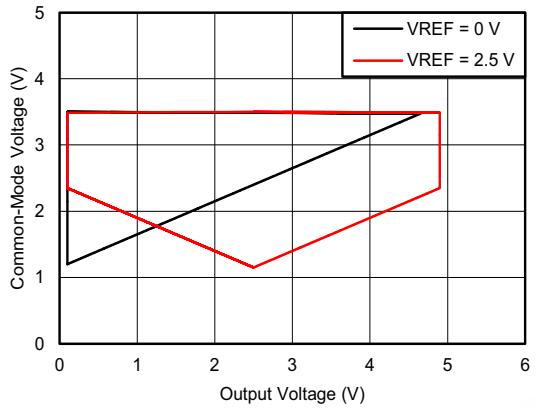



図 50. Common-Mode EMI Rejection Ratio



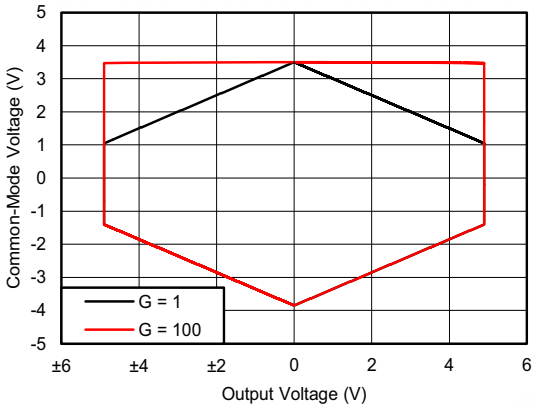

$V_S$ = 5 V G = 1

図 51. Input Common-Mode Voltage vs Output Voltage



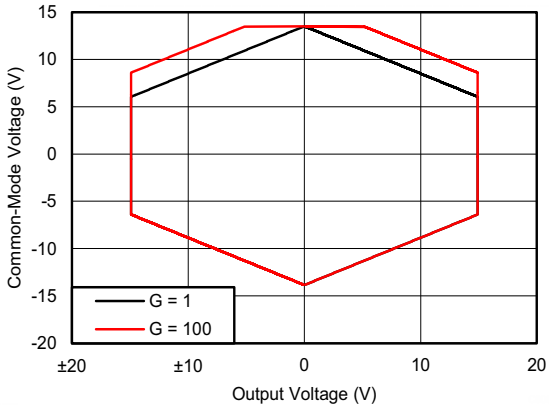

$V_S$ = 5 V G = 100

図 52. Input Common-Mode Voltage vs Output Voltage




$V_S$ = ±5 V $V_{REF}$ = 0 V

図 53. Input Common-Mode Voltage vs Output Voltage




$V_S$ = ±15 V $V_{REF}$ = 0 V

図 54. Input Common-Mode Voltage vs Output Voltage

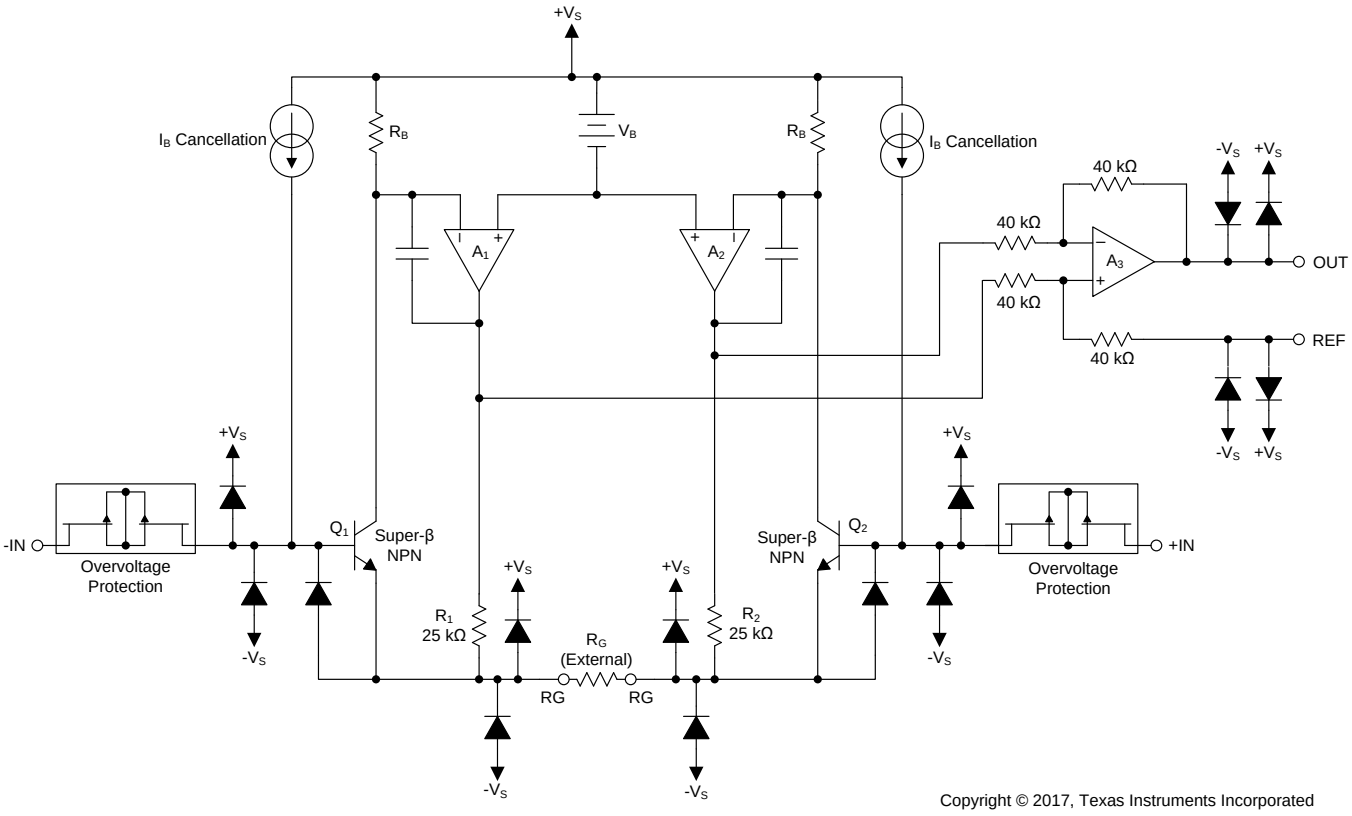
# 8 Detailed Description

## 8.1 Overview

The INA818 is a monolithic, precision instrumentation amplifier incorporating a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by transistors $Q_1$ and $Q_2$ and is forced across resistor $R_G$, which causes a signal current to flow through resistors $R_G$, $R_1$, and $R_2$. The output difference amplifier, $A_3$, removes the common-mode component of the input signal and refers the output signal to the REF pin. The $V_{BE}$ and voltage drop across $R_1$ and $R_2$ produce output voltages on $A_1$ and $A_2$ that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

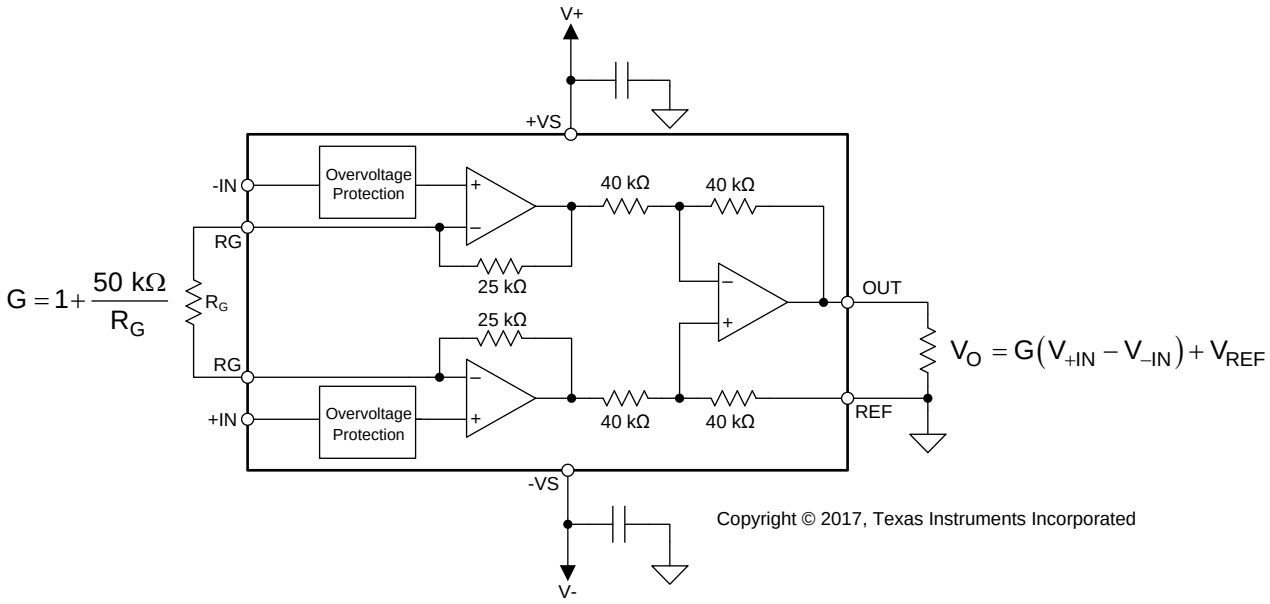
## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Setting the Gain

図 55 shows that the gain of the INA818 is set by a single external resistor ($R_G$) connected between the RG pins (pins 1 and 8).




$$G = 1 + \frac{50\ k\Omega}{R_G}$$

$$V_O = G\left(V_{+IN} - V_{-IN}\right) + V_{REF}$$

**図 55. Simplified Diagram of the INA818 With Gain and Output Equations**

The value of $R_G$ is selected according to 式 1:

$$G = 1 + \frac{50\ k\Omega}{R_G} \quad (1)$$

表 2 lists several commonly-used gains and resistor values. The 50-kΩ term in 式 1 comes from the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA818. As shown in 図 55 and explained in more details in the *Layout* section, make sure to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground that are placed as close to the device as possible.

**表 2. Commonly-Used Gains and Resistor Values**

| DESIRED GAIN | $R_G$ (Ω) | NEAREST 1% $R_G$ (Ω) |
|---|---|---|
| 1 | NC | NC |
| 2 | 50 k | 49.9 k |
| 5 | 12.5 k | 12.4 k |
| 10 | 5.556 k | 5.49 k |
| 20 | 2.632 k | 2.61 k |
| 50 | 1.02 k | 1.02 k |
| 100 | 505.1 | 511 |
| 200 | 251.3 | 249 |
| 500 | 100.2 | 100 |
| 1000 | 50.05 | 49.9 |

#### 8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor ($R_G$ ) also affects gain. The contribution of $R_G$ to gain accuracy and drift is determined from 式 1.

The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA818 uses G = 1 without $R_G$ connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier ($A_3$). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of $A_1$ and $A_2$, relative to the drift of the external gain resistor ($R_G$.) The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at $R_G$ connections. Careful matching of any parasitics on the $R_G$ pins maintains optimal CMRR over frequency.

### 8.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA818 to reject EMI. The offset resulting from an input EMI signal is calculated using 式 2:

$$\Delta V_{OS} = \left( \frac{V_{RF\_PEAK}^2}{100\ mV_P} \right) \cdot 10^{-\left( \frac{EMIRR\ (dB)}{20} \right)} \quad (2)$$

where

- $V_{RF\_PEAK}$ is the peak amplitude of the input EMI signal.

図 56 and 図 57 show the INA818 EMIRR graphs for differential and common-mode EMI rejection across this frequency range. 表 3 lists the EMIRR values for the INA818 at frequencies commonly encountered in real-world applications. Applications listed in 表 3 are centered on or operated near the frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system. Incorporating known good practices, such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing may also be required.

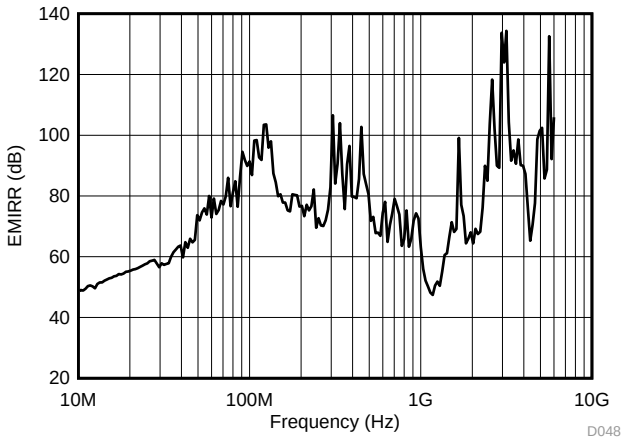



図 56. Common-Mode EMIRR Testing

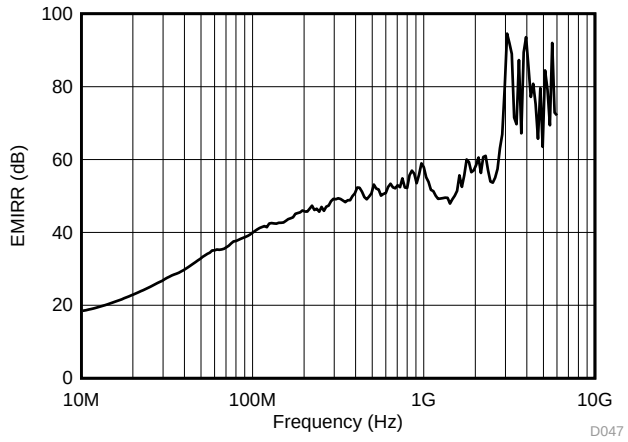


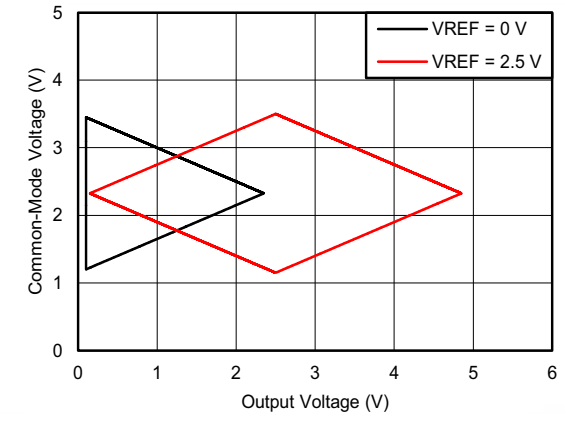

図 57. Differential Mode EMIRR Testing

**表 3. INA818 EMIRR for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | DIFFERENTIAL EMIRR | COMMON-MODE EMIRR |
|---|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications | 52 dB | 80 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 55 dB | 71 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 58 dB | 73 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 59 dB | 95 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 78 dB | 96 dB |
| 5 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 70 dB | 100 dB |

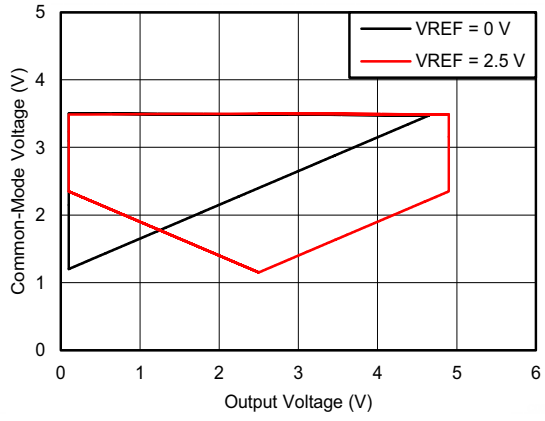
### 8.3.3 Input Common-Mode Range

The linear input voltage range of the INA818 input circuitry extends within 1.5 V (typical) of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 図 58, 図 53, and 図 54. The common-mode range for other operating conditions is best calculated using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers*.



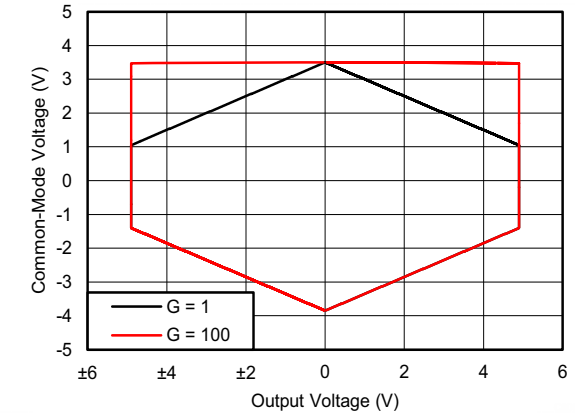

$V_S$ = 5 V G = 1

**図 58. Input Common-Mode Voltage vs Output Voltage**



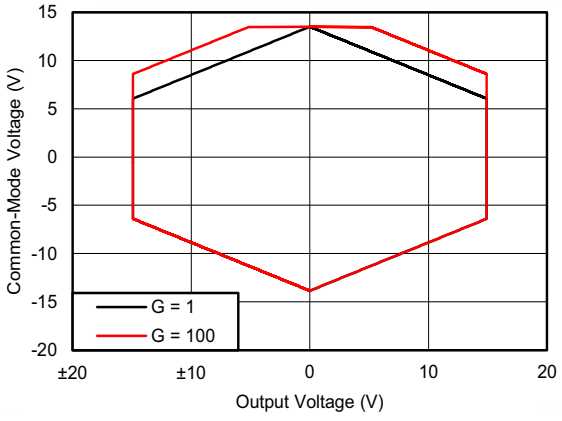

$V_S$ = 5 V G = 100

**図 59. Input Common-Mode Voltage vs Output Voltage**




$V_S$ = ±5 V $V_{REF}$ = 0 V

**図 60. Input Common-Mode Voltage vs Output Voltage**




$V_S$ = ±15 V $V_{REF}$ = 0 V

**図 61. Input Common-Mode Voltage vs Output Voltage**

### 8.3.4 Input Protection

The inputs of the INA818 device are individually protected for voltages up to ±60 V. For example, a condition of –60 V on one input and +60 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

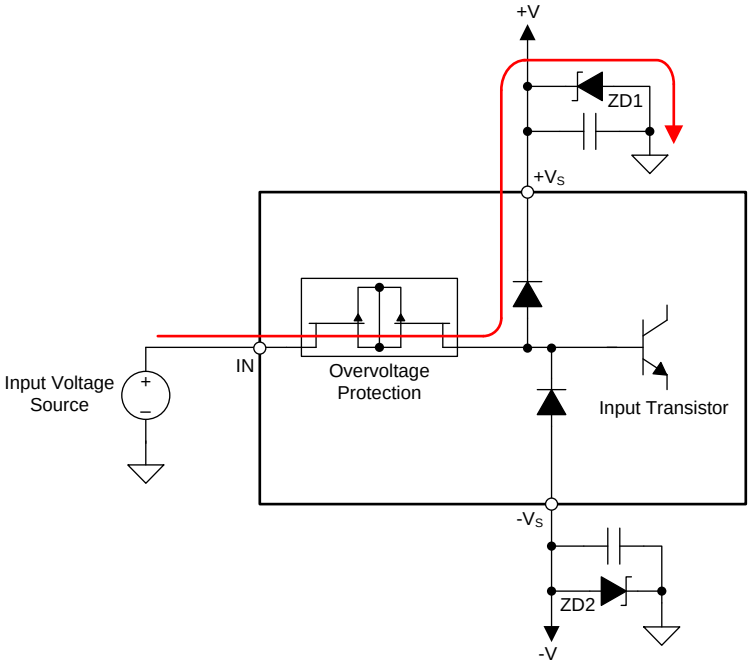



**図 62. Input Current Path During an Overvoltage Condition**

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see 図 62. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in 図 62) must be placed on the power supplies to provide a current pathway to ground. 図 63 shows the input current for input voltages from –50 V to +50 V when the INA818 is powered by ±15-V supplies.

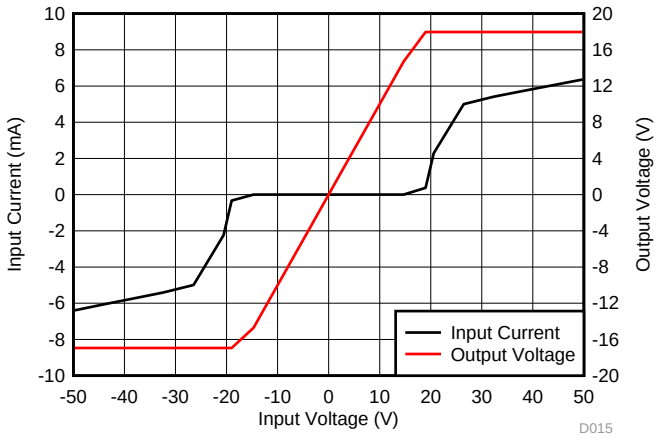



**図 63. Input Current vs Input Overvoltage**

### 8.3.5 Operating Voltage

The INA818 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

> **注意**
>
> Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in *Typical Characteristics* .

### 8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimize these errors by choosing high-precision components, such as the INA818, that have improved specifications in critical areas that impact the precision of the overall system. 図 64 shows an example application.

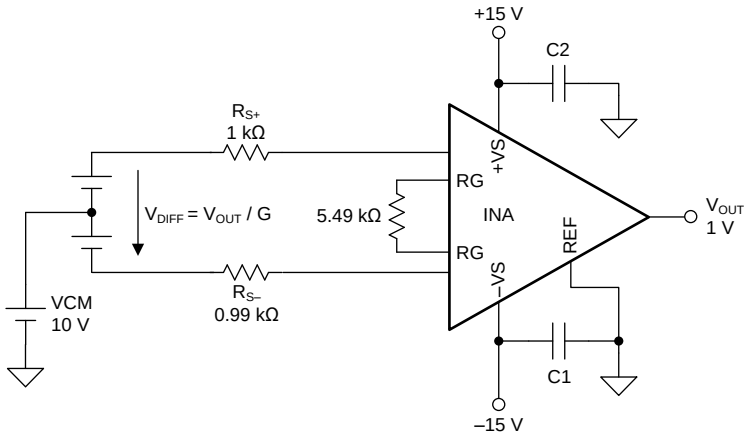



**図 64. Example Application With G = 10 V/V and 1-V Output Voltage**

Resistor-adjustable devices (such as the INA818) show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA818 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). 表 5 summarizes the major error sources in common INA applications and compares the three cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor) and G = 100 (511-Ω external resistor). All calculations are assuming an output voltage of $V_{OUT}$ = 1 V. Thus, the input signal $V_{DIFF}$ (given by $V_{DIFF}$= $V_{OUT}$ / G) exhibits smaller and smaller amplitudes with increasing gain G. $V_{DIFF}$ = 1 mV at G = 1000 in this example. All calculations refer the error to the input for easy comparison and system evaluation. As 表 5 shows, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain, while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. The gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors are the key factors limiting overall system performance.

## 表 4. System Specifications for Error Calculation

| QUANTITY | VALUE | UNIT |
|---|---|---|
| $V_{OUT}$ | 1 | V |
| VCM | 10 | V |
| VS | 1 | V |
| $R_{S+}$ | 1000 | Ω |
| $R_{S–}$ | 999 | Ω |
| RG tolerance | 0.01 | % |
| RG drift | 10 | ppm/°C |
| Temperature range upper limit | 105 | °C |

## 表 5. Error Calculation

| ERROR SOURCE | ERROR CALCULATION | INA818 VALUES | | | | |
|---|---|---|---|---|---|---|
| | | SPECIFICATION | UNIT | G = 1 ERROR (ppm) | G = 100 ERROR (ppm) | G = 1000 ERROR (ppm) |
| **ABSOLUTE ACCURACY AT 25°C** | | | | | | |
| Input offset voltage | $V_{OSI}$ / $V_{DIFF}$ | 35 | µV | 35 | 350 | 3500 |
| Output offset voltage | $V_{OSO}$ / (G × $V_{DIFF}$) | 300 | µV | 300 | 300 | 300 |
| Input offset current | $I_{OS}$ × maximum ($R_{S+}$, $R_{S–}$) / $V_{DIFF}$ | 0.5 | nA | 1 | 5 | 50 |
| CMRR (min) | $V_{CM}$ / ($10^{CMRR/20}$ × $V_{DIFF}$) | 90 (G = 1), 110 (G = 10), 130 (G = 100) | dB | 316 | 316 | 316 |
| PSRR (min) | ($V_{CC}$ -$V_S$)/ ($10^{PSRR/20}$ × $V_{DIFF}$) | 110 (G = 1), 114 (G = 10), 130 (G = 100) | dB | 3 | 20 | 32 |
| Gain error from INA (max) | GE(%) × $10^4$ | 0.02 (G = 1), 0.15 (G = 10, 100) | % | 200 | 1500 | 1500 |
| Gain error from external resistor RG (max) | GE(%) × $10^4$ | 0.01 | % | 100 | 100 | 100 |
| Total absolute accuracy error (ppm) at 25°C, worst case | sum of all errors | — | — | 955 | 2591 | 5798 |
| Total absolute accuracy error (ppm) at 25°C, average | rms sum of all errors | — | — | 491 | 1604 | 3835 |
| **DRIFT TO 105°C** | | | | | | |
| Gain drift from INA (max) | GTC × ($T_A$ – 25) | 5 (G = 1), 35 (G = 10, 100) | ppm/°C | 400 | 2800 | 2800 |
| Gain drift from external resistor RG (max) | GTC × ($T_A$ – 25) | 10 | ppm/°C | 800 | 800 | 800 |
| Input offset voltage drift (max) | ($V_{OSI\_TC}$ / $V_{DIFF}$) × ($T_A$ – 25) | 0.4 | µV/°C | 32 | 320 | 3200 |
| Output offset voltage drift | [$V_{OSO\_TC}$ / ( G × $V_{DIFF}$)] × ($T_A$ – 25) | 5 | µV/°C | 400 | 400 | 400 |
| Offset current drift | $I_{OS\_TC}$ × maximum ($R_{S+}$, $R_{S–}$) × ($T_A$ – 25) / $V_{DIFF}$ | 20 | pA/°C | 2 | 16 | 160 |
| Total drift error to 105°C (ppm), worst case | sum of all errors | — | — | 1634 | 4336 | 7360 |
| Total drift error to 105°C (ppm), typical | rms sum of all errors | — | — | 980 | 2957 | 4348 |
| **RESOLUTION** | | | | | | |
| Gain nonlinearity | | 10 (G = 1, 10), 15 (G = 100) | ppm of FS | 10 | 10 | 15 |
| Voltage noise (at 1 kHz) | $\sqrt{BW} \times \sqrt{\left(e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2\right) \times \frac{6}{V_{DIFF}}}$ | $e_{NI}$ = 8, $e_{NO}$ = 90 | $\mu V_{PP}$ | 1204 | 1070 | 3941 |
| Current noise (at 1kHz) | $I_N$ × maximum ($R_{S+}$, $R_{S–}$) × $\sqrt{BW}$ / $V_{DIFF}$ | 0.13 | pA/$\sqrt{Hz}$ | 0.3 | 2 | 11 |
| Total resolution error (ppm), worst case | sum of all errors | — | — | 1214 | 1080 | 3956 |
| Total resolution error (ppm), typical | rms sum of all errors | — | — | 1204 | 1070 | 3941 |
| **TOTAL ERROR** | | | | | | |
| Total error (ppm), worst case | sum of all errors | — | — | 3802 | 8007 | 17113 |
| Total error (ppm), typical | rms sum of all errors | — | — | 1628 | 3530 | 7010 |

## 8.4 Device Functional Modes

The INA818 has a single functional mode and operates when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA818 is 36 V (±18 V.)

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Reference Pin

The output voltage of the INA818 is developed with respect to the voltage on the reference pin, REF. In dual-supply operation, REF (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA818 drives a single-supply ADC.

The voltage source applied to the reference pin must have a low output impedance. As shown in 図 65, any resistance at the reference pin (shown as $R_{REF}$ in 図 65) is in series with an internal 40-kΩ resistor.

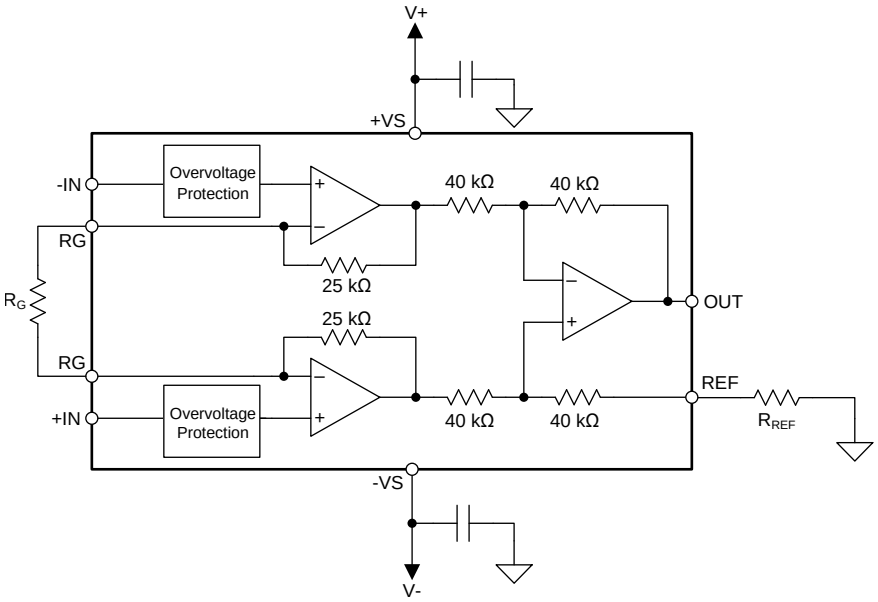



**図 65. Parasitic Resistance Shown at the Reference Pin**

## Application Information (continued)

The parasitic resistance at the reference pin ($R_{REF}$) creates an imbalance in the four resistors of the internal difference amplifier, which degrades the common-mode rejection ratio (CMRR). 図 66 shows the degradation in CMRR of the INA818 as a result of increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin ($R_{REF}$) below 5 Ω.

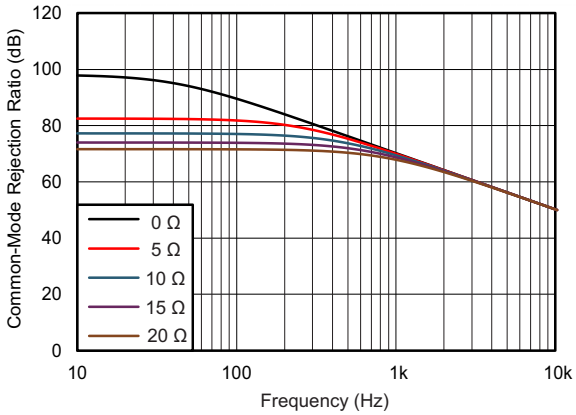



**図 66. The Effect of Increasing Resistance at the Reference Pin**

Voltage-reference devices are a suitable option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as 図 67 shows, in order to avoid CMRR degradation.

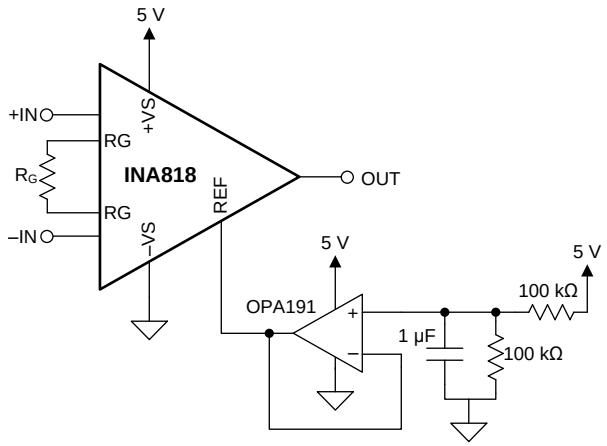



**図 67. Using an Op Amp to Buffer Reference Voltages**

## Application Information (continued)

### 9.1.2 Input Bias Current Return Path

The input impedance of the INA818 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for input bias current. 図 68 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA818, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can connect to one input (as shown in the thermocouple example in 図 68). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

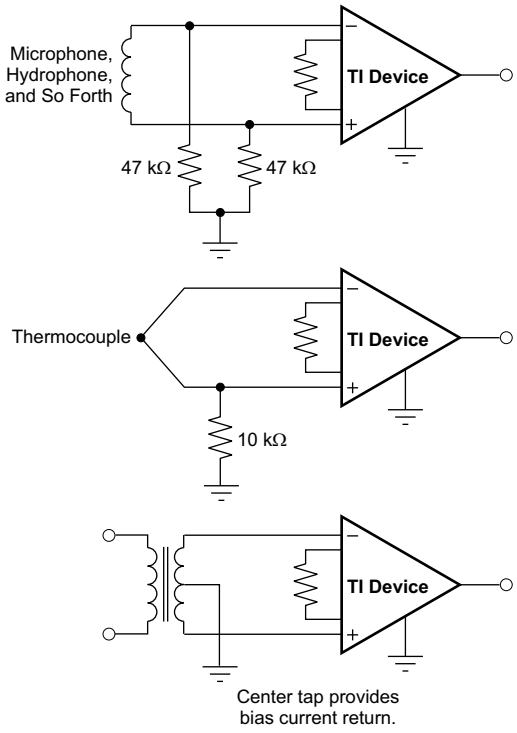





**図 68. Providing an Input Common-Mode Current Path**

## 9.2 Typical Applications

### 9.2.1 Three-Pin Programmable Logic Controller (PLC)

図 69 shows a three-pin programmable-logic controller (PLC) design for the INA818. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

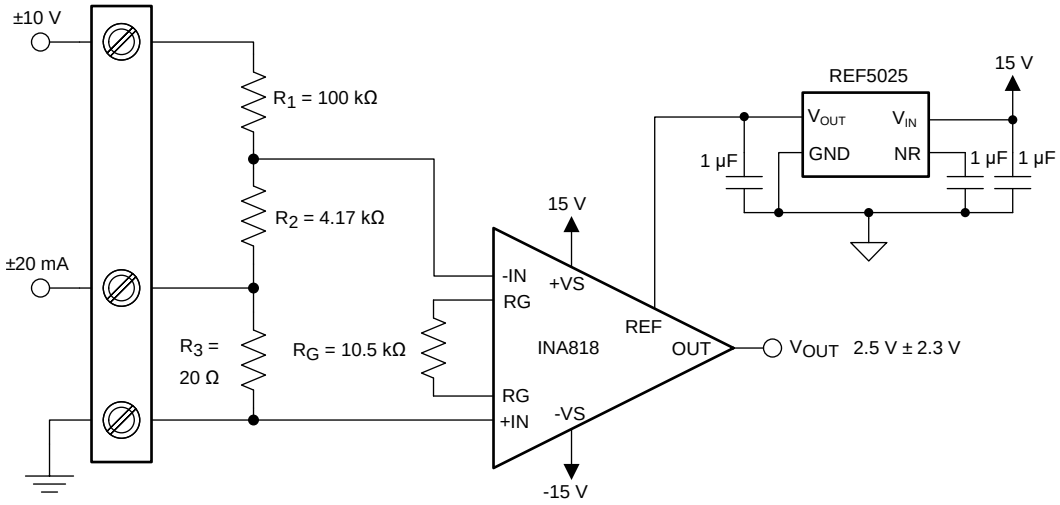





**図 69. PLC Input (±10 V, 4 mA to 20 mA)**

#### 9.2.1.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

#### 9.2.1.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 図 69: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, 式 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (3)$$

where

- G represents the gain of the instrumentation amplifier
- $V_D$ represents the differential voltage at the INA818 inputs
- $V_{REF}$ is the voltage at the INA818 REF pin
- $I_{IN}$ is the input current

式 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (4)$$

where

- $V_{IN}$ is the input voltage

## Typical Applications (continued)

$R_1$ sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for $R_1$ because increasing the $R_1$ value also increases noise. The value of $R_3$ must be extremely small compared to $R_1$ and $R_2$. 20 Ω for $R_3$ is selected because that resistance value is much smaller than $R_1$ and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Use 式 5 to calculate $R_2$ given $V_D$ = ±400 mV, $V_{IN}$ = ±10 V, and $R_1$ = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \tag{5}$$

The value obtained from 式 5 is not a standard 0.1% value, so 4.17 kΩ is selected. $R_1$ and $R_2$ also use 0.1% tolerance resistors to minimize error.

Use 式 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \tag{6}$$

式 7 calculates the gain-setting resistor value using the INA818 gain equation, 式 1.

$$R_G = \frac{50\ k\Omega}{G - 1} = \frac{50\ k\Omega}{5.75 - 1} = 10.5\ k\Omega \tag{7}$$

10.5 kΩ is a standard 0.1% resistor value that can be used in this design.

### 9.2.1.3 Application Curves

図 70 and 図 71 show typical characteristic curves for the circuit in 図 69.

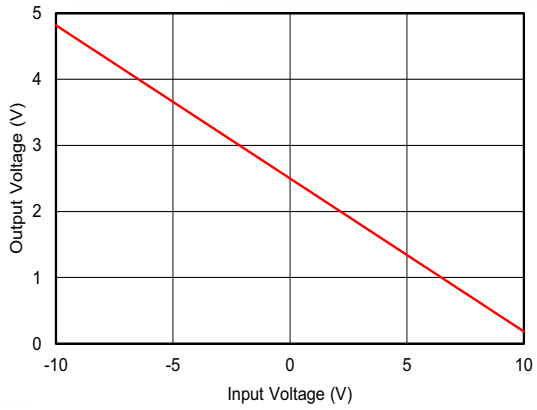



**図 70. PLC Output Voltage vs Input Voltage**

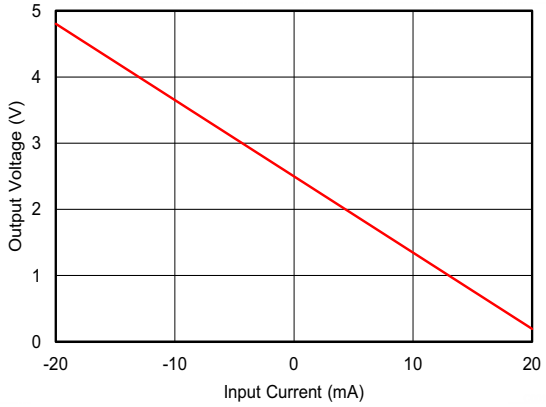



**図 71. PLC Output Voltage vs Input Current**

## Typical Applications (continued)

### 9.2.2 Resistance Temperature Detector Interface

図 72 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 V to 5 V. The linearization technique employed is described in the *Analog linearization of resistance temperature detectors* analog application journal. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

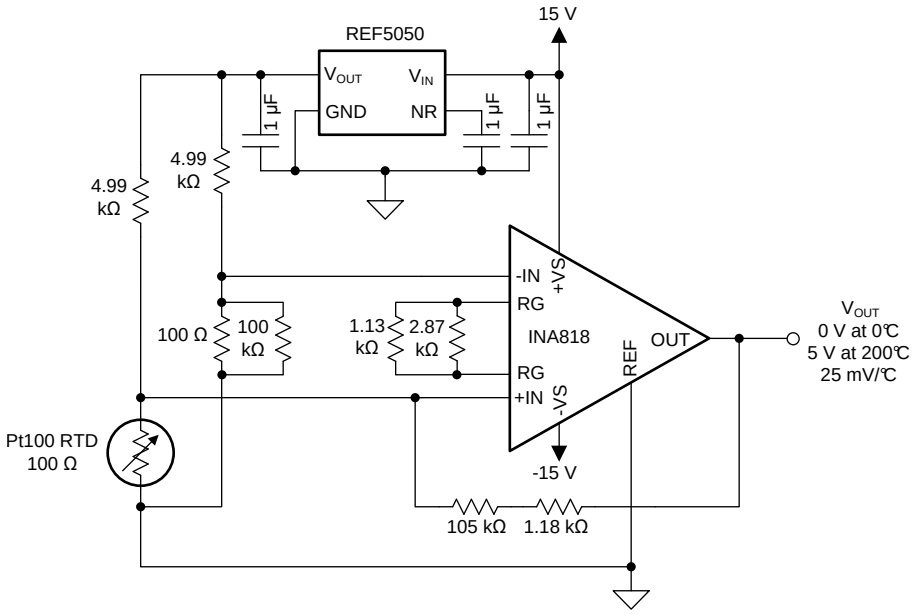





**図 72. A 3-Wire Interface for RTDs With Analog Linearization**

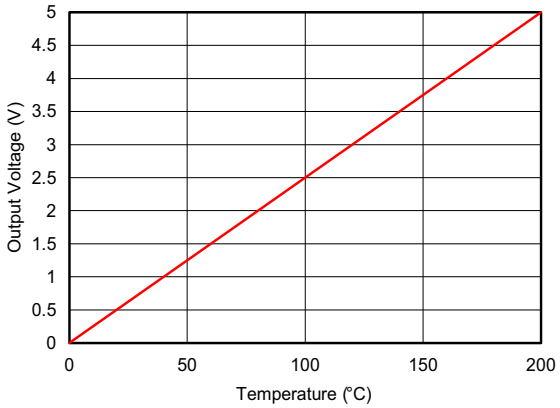



**図 73. Transfer Function of a 3-Wire RTD Interface**

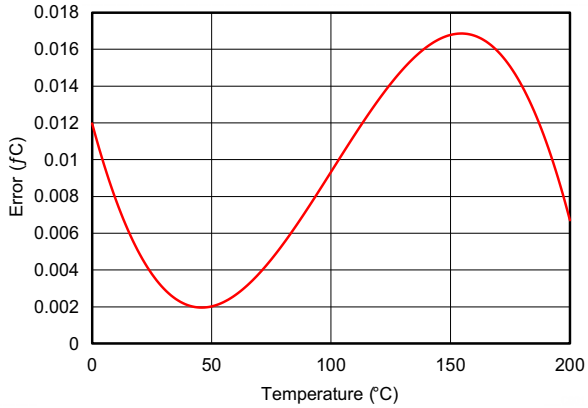



**図 74. Temperature Error Over the Full Temperature Range**

# 10 Power Supply Recommendations

The nominal performance of the INA818 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device can also be operated using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in the *Typical Characteristics* section.

# 11 Layout

## 11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of $R_G$, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 75, keeping $R_G$ close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

## 11.2 Layout Example

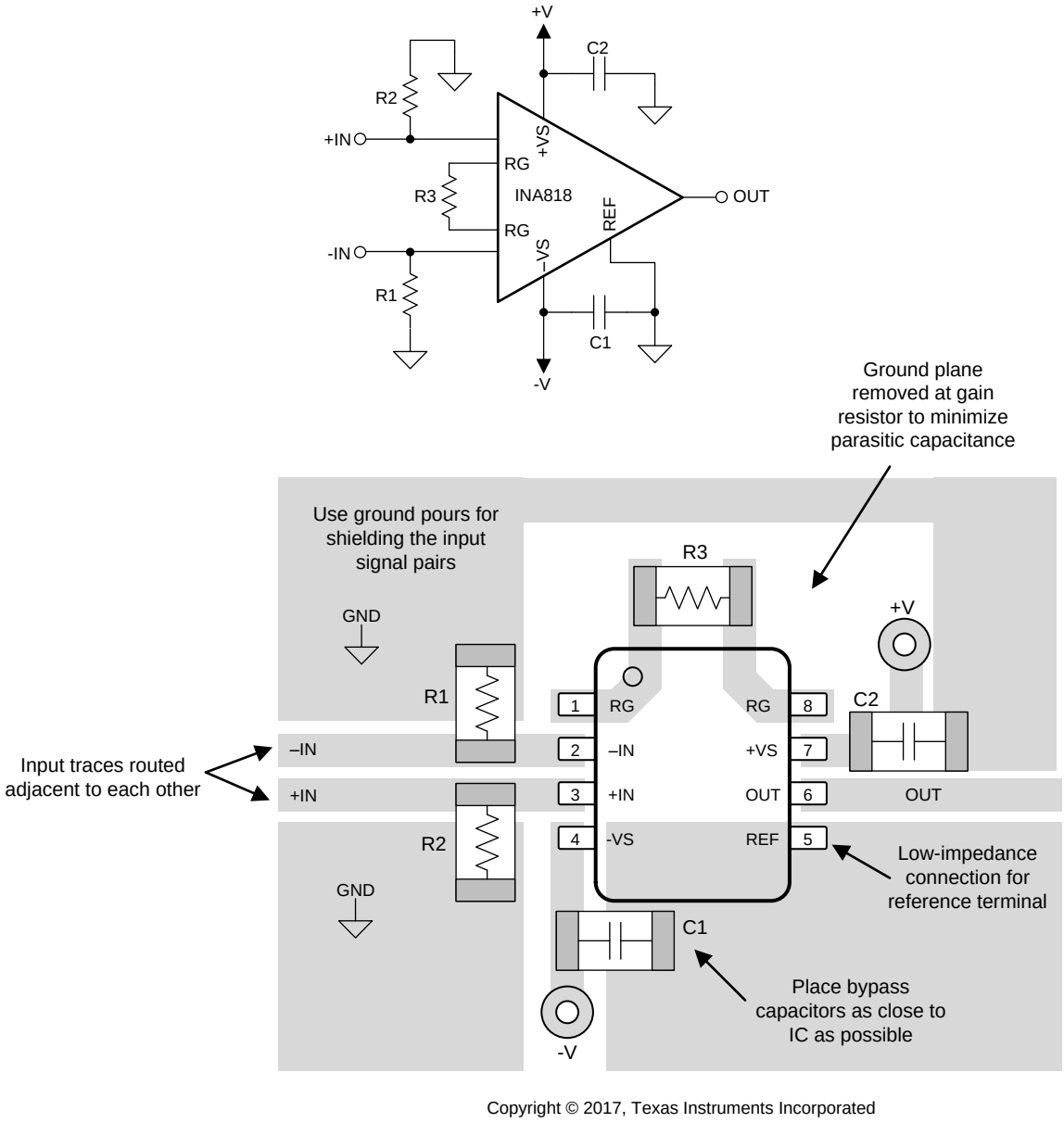





**図 75. Example Schematic and Associated PCB Layout**

# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントのサポート

### 12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『*Universal Instrumentation Amplifier EVM*』ユーザー・ガイド (英語)
- テキサス・インスツルメンツ、『*Comprehensive Error Calculation for Instrumentation Amplifiers*』アプリケーション・ノート (英語)

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 商標

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
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## 12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| INA818ID | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |
| INA818ID.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |
| INA818IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |
| INA818IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |
| INA818IDRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |
| INA818IDRG4.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | INA818 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

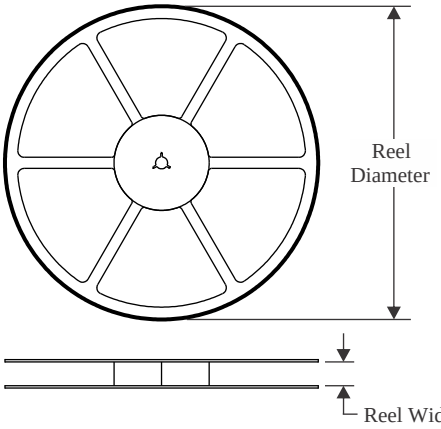
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

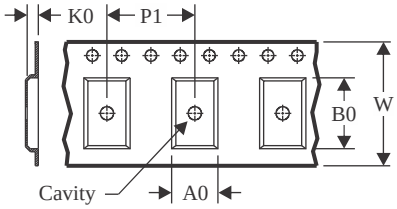
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

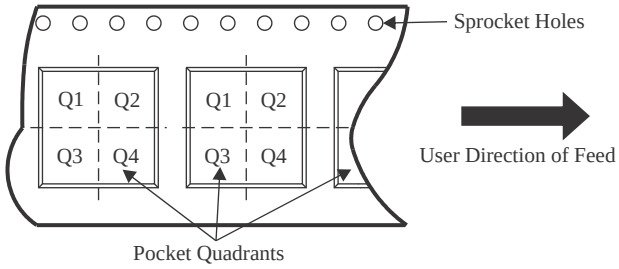



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

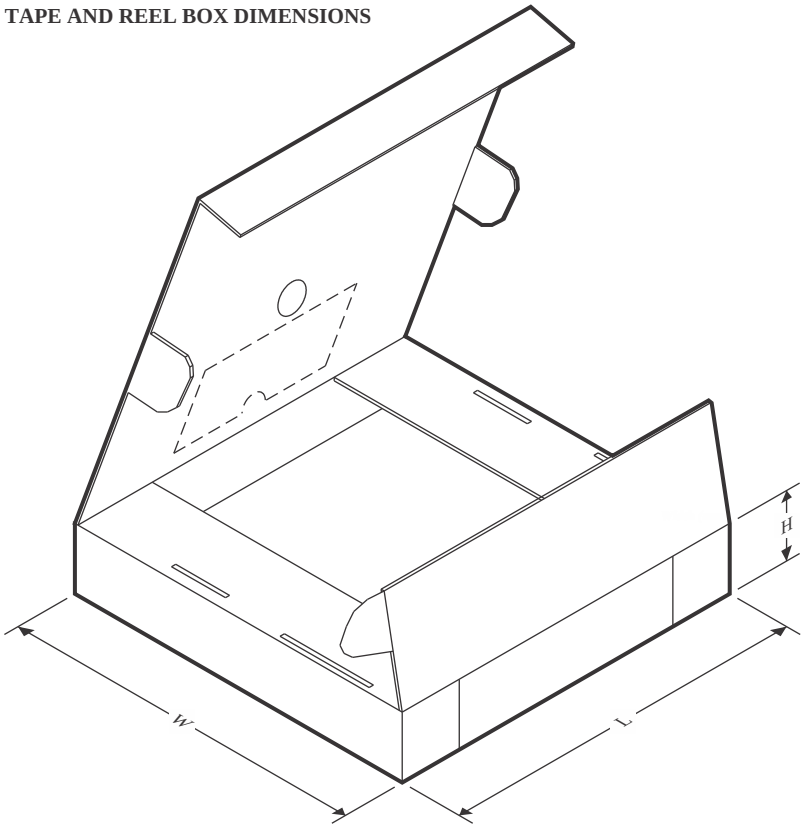
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA818IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA818IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

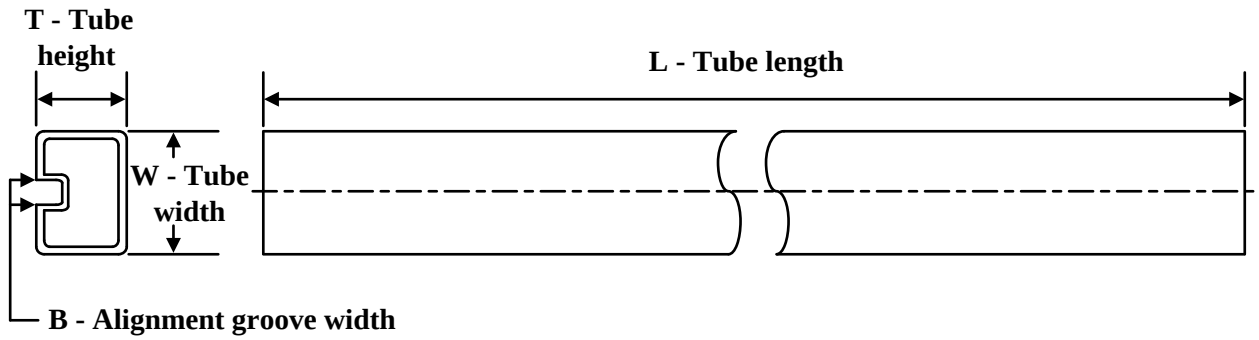
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

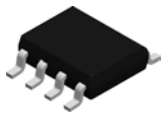
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA818IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA818IDRG4 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| INA818ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| INA818ID.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

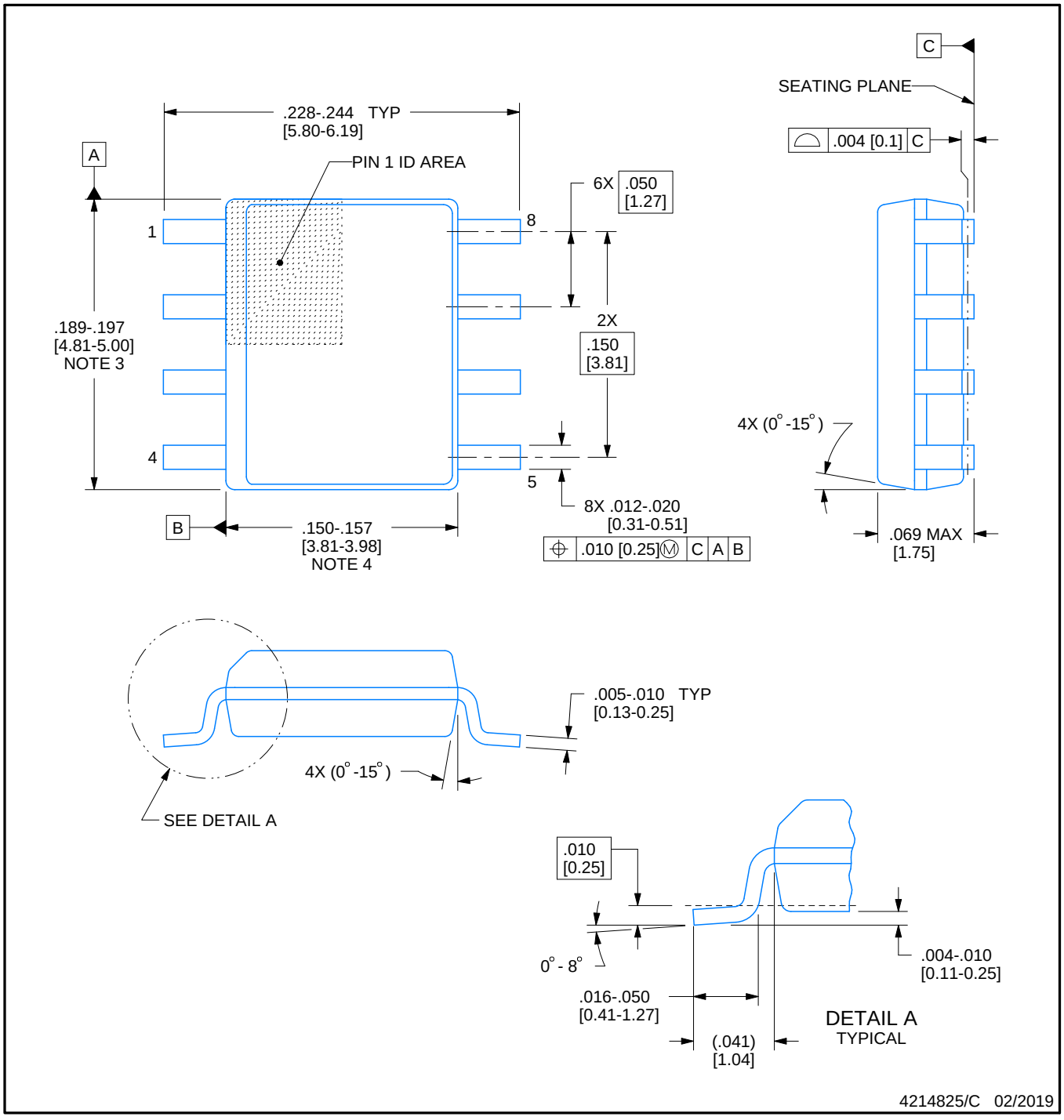


# PACKAGE OUTLINE

## D0008A

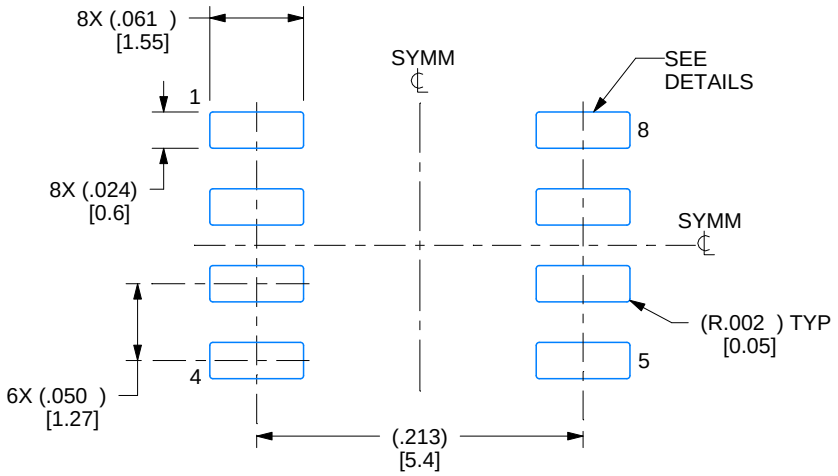
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

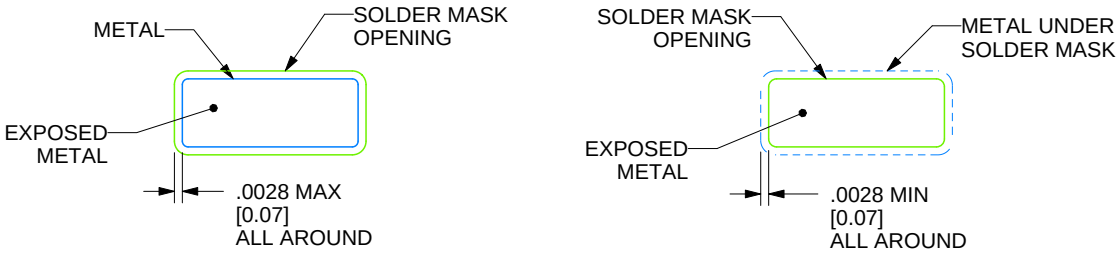



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

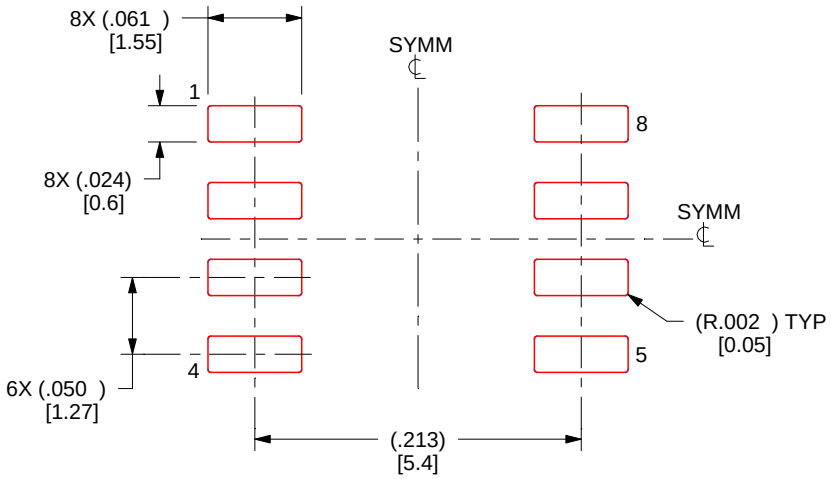
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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