OPA2626 高速、高精度、低歪みの 16 ビット / 18 ビット A/D コンバータ (ADC) ドライバ

1 特長

- 非常に優れた動的性能
  - 低歪み:100kHz において HD2 で –122dBc、HD3 で –140dBc
  - ゲイン帯域幅 (G = 100):120MHz
  - スルーレート:115 V/µs
  - 4V ステップでの 16 ビット・セトリング:280ns
  - 低い電圧ノイズ: 10 kHz で 2.5nV/√Hz
  - 低い出力インピーダンス:1MHz において 1Ω
- 非常に優れた DC 精度
  - オフセット電圧:±100µV (最大値)
  - オフセット電圧ドリフト:±3µV/ºC (最大値)
  - 低い静止電流:2mA (標準値)
- 負レールを含む入力同相範囲
- レール・ツー・レール出力
- 広い温度範囲 : –40℃～+125℃で完全に動作を規定

2 アプリケーション

- 高精度 SAR ADC ドライバ
- 高精度の基準電圧バッファ
- プログラマブル・ロジック・コントローラ
- 試験および計測機器
- 科学計測機器
- 高スループットのデータ・アクイジション・システム
- 高密度の多重化されたデータ・アクイジション・システム

3 概要

OPA2626 オペアンプは、全高調波歪み (THD) とノイズが少ない 16 ビットおよび 18 ビット高精度逐次比較型 (SAR) アナログ / デジタル・コンバータ (ADC) ドライバです。このオペアンプは、真の 16 ビット実効ビット数 (ENOB) を実現できる 280ns の 16 ビット・セトリング時間で仕様が完全に規定されています。わずか 100µV のオフセット電圧という高い DC 精度、120MHz の広いゲイン帯域幅積、わずか 2.5nV/√Hz の優れた広帯域ノイズ特性を備えたこのデバイスは、ADS88xx SAR ADC ファミリなどの高スループット高分解能 SAR ADC を駆動するために最適化されています。

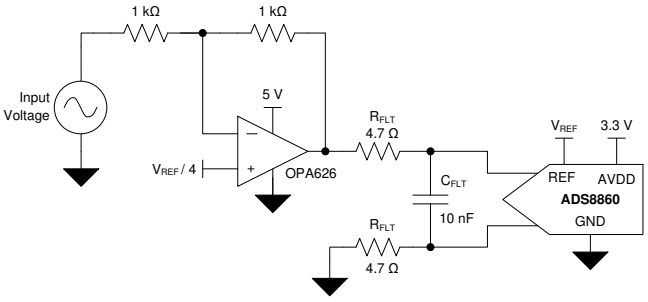
OPA2626 は小型の 8 ピン VSSOP パッケージで供給され、–40℃～+125℃で動作が規定されています。

製品情報(1)

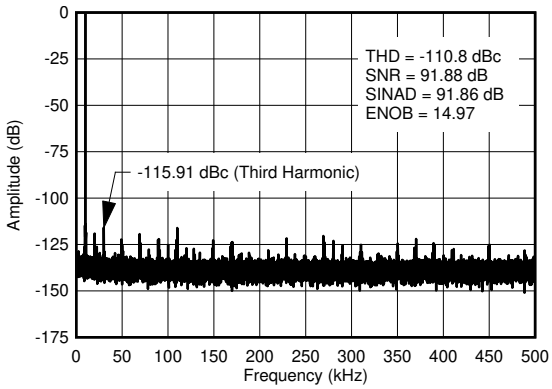
型番	パッケージ	本体サイズ(公称)
OPA2626	VSSOP (8)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

SAR ADCドライバ



高忠実度のトポロジによる動的性能の改善 (f_{IN} = 10kHz、1MSPS FFT)



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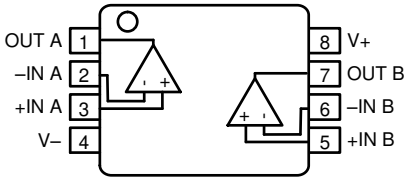
4 改訂履歴

2016年7月発行のものから更新 **Page**

- ドキュメントから OPA626 (5 ピンの SOT DBV パッケージ) を 削除 ... 1
- 追加 18-bit SAR ADC to amplifier description in *Overview* section ... 21
- 追加 18-bit level to device description in *Application Information* section ... 23
- 追加 *(pins 3 and 4)* to input terminals in *Design Requirements* section of first typical application for clarity ... 24
- 変更 description of slew and settle time in *Design Requirements* section of second typical application for clarity ... 26

5 Pin Configuration and Functions

OPA2626 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2626

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	5	I	Noninverting input for channel B
–IN B	6	I	Inverting input for channel B
OUT A	1	O	Output terminal for channel A
OUT B	7	O	Output terminal for channel B
V+	8	—	Positive supply voltage
V–	4	—	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S	(V+) – (V–)		6	V
Input voltage(2)	+IN	(V–) – 0.3	(V+) + 0.3	V
	–IN	(V–) – 0.3	(V+) + 0.3	
Output voltage	OUT	(V–)	(V+)	V
Sink current	+IN		10	mA
	–IN		10	
	OUT		150	
Source current	+IN		10	mA
	–IN		10	
	OUT		150	
Temperature	Operating junction	–40	150	°C
	Operating free-air, T_A	–55	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply input voltage, (V+) – (V–)		2.7		5.5	V
V_I	Input voltage	+IN	(V–)		(V+) – 1.15	V
		–IN	(V–)		(V+) – 1.15	
V_O	Output voltage		(V–)		(V+)	V
I_O	Output current		–120		120	mA
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA2626 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics: High-Supply

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			80		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			120		MHz
SR	Slew rate	V_O = 1-V step, G = 1			45		V/µs
		V_O = 4-V step, G = 2			115		
t_{settle}	Settling time	V_O = 4-V step, G = 2	Settling time to 0.1% (10-bit accuracy)		80		ns
			to 0.005% (14-bit accuracy)		110		
			to 0.00153% (16-bit accuracy)		280		
	Overshoot	V_O = 4-V step, G = 2			2.5%		
	Undershoot	V_O = 4-V step, G = 2			3%		
HD2	Second-order harmonic distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		144		dBc
			f = 100 kHz		122		
			f = 1 MHz		80		
HD3	Third-order harmonic distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		155		dBc
			f = 100 kHz		140		
			f = 1 MHz		80		
	Second-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			90		dBc
	Third-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			100		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz, peak-to-peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz, rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 1 kHz			3.2		$nV/\sqrt{Hz}$
		f = 10 kHz			2.5		
I_n	Input current noise density	f = 1 kHz			6.6		$pA/\sqrt{Hz}$
		f = 10 kHz			3.5		
t_{OR}	Overload recovery time	G = 5			50		ns
Z_o	Open-loop output impedance	f = 1 MHz			1		Ω
	Crosstalk	At DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							

Electrical Characteristics: High-Supply (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3	µV/°C
					0.6	±4	
PSRR	Power-supply rejection ratio	2.7 V ≤ (V+) ≤ 5 V		100			dB
			T_A = –40°C to 125°C	90	120		
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
						6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
						350	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			0.6		nA/°C
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	106	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	110	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 1.2		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.5		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{sc}	Short-circuit current				130		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			2	2.2	mA
			T_A = –40°C to 125°C			3.1	

6.6 Electrical Characteristics: Low-Supply

at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			76		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			110		MHz
SR	Slew rate	V_O = 1-V step, G = 2			45		V/µs
t_{settle}	Settling time	V_O = 1-V step, G = 2	to 0.1%		80		ns
			to 0.01%		170		
			to 0.000763% (17-bit accuracy)		250		
	Overshoot	V_O = 1-V step, G = 2			6%		
	Undershoot	V_O = 1-V step, G = 2			5%		
HD2	Second-order harmonic distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		136		dBc
			f = 100 kHz		118		
			f = 1 MHz		80		
HD3	Third-order harmonic distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		143		dBc
			f = 10 kHz		143		
			f = 100 kHz		130		
			f = 100 kHz		125		
			f = 1 MHz		85		
			f = 1 MHz		74		
	Second-order intermodulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			95		dBc
	Third-order intermodulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1V, V_O = 1 V_{PP}, f = 1 MHz, 200-kHz tone spacing			104		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz, peak-to-peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz, rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 10 kHz			2.5		nV/√Hz
I_n	Input current noise density	f = 10 kHz			3.5		pA/√Hz
t_{OR}	Overload recovery time	G = 5			35		ns
Z_o	Open-loop output impedance	f = 1 MHz			1.3		Ω
	Crosstalk	At DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3.1	µV/°C
					0.6	±4	
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
						6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
						200	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			80		pA/°C
OPEN-LOOP GAIN							

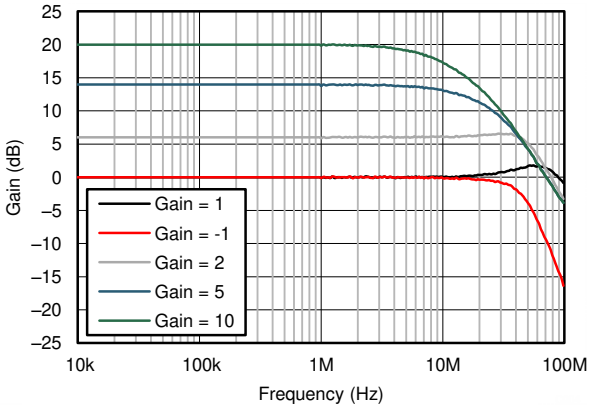
Electrical Characteristics: Low-Supply (continued)

at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	100	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	104	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 0.8		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.2		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{SC}	Short-circuit current				80		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			2	2.1	mA
			T_A = –40°C to 125°C			2.8	

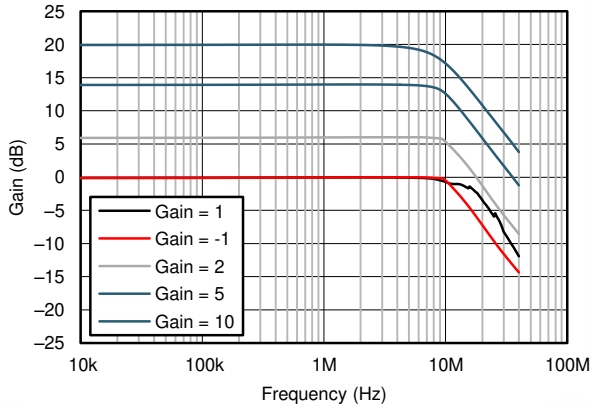
6.7 Typical Characteristics

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



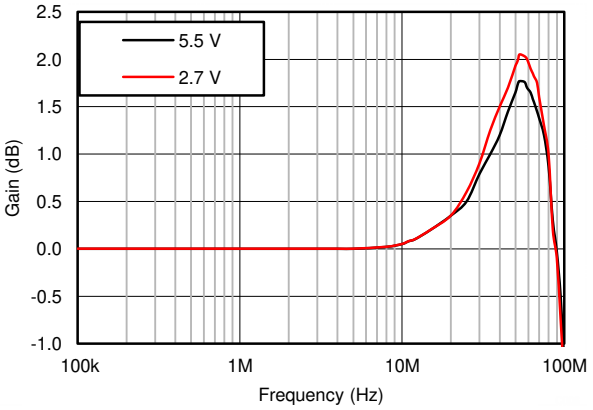
V_O = 10 mV_{PP}

図 1. Small-Signal Frequency Response for Various Gains



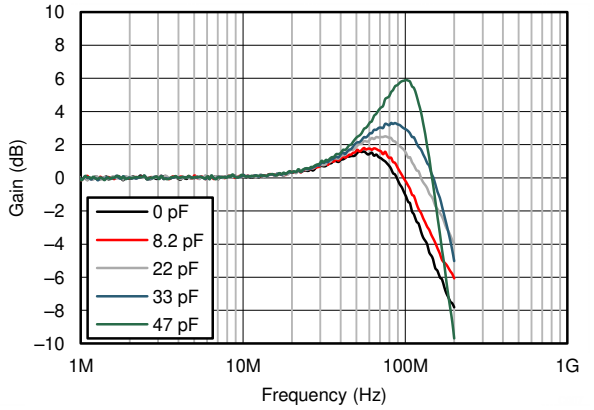
V_O = 2 V_{PP}

図 2. Large-Signal Frequency Response for Various Gains



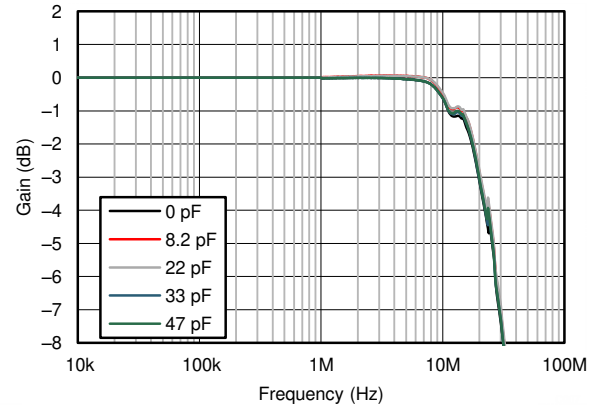
V_O = 10 mV_{PP}, G = 1

図 3. Small-Signal Frequency Response for Various Power Supply Voltages



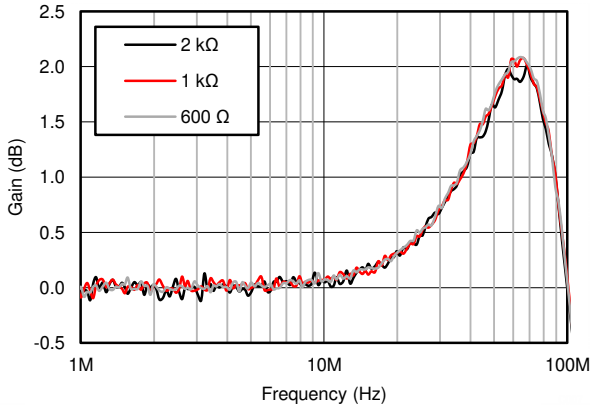
V_O = 10 mV_{PP} , G = 1

図 4. Small-Signal Frequency Response for Various Capacitive Loads



V_O = 2 V_{PP}, G = 1

図 5. Large-Signal Frequency Response for Various Capacitive Loads



V_O = 10 mV_{PP} , G = 1

図 6. Small-Signal Frequency Response for Various Resistive Loads

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

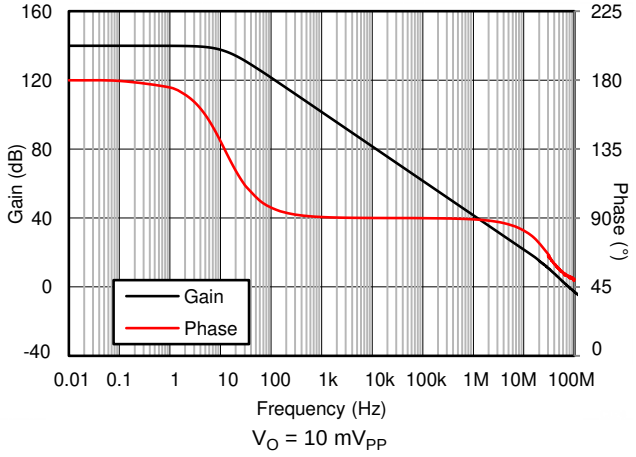


図 7. Open-Loop Gain and Phase vs Frequency

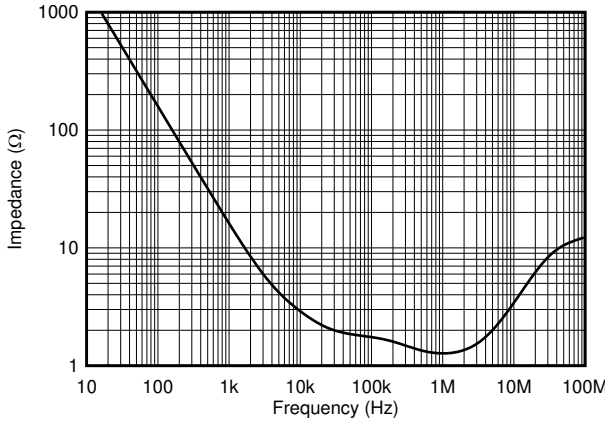


図 8. Open-Loop Output Impedance vs Frequency

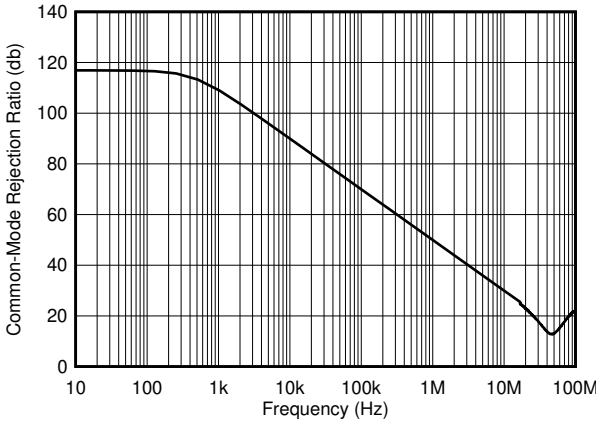


図 9. Common-Mode Rejection Ratio vs Frequency

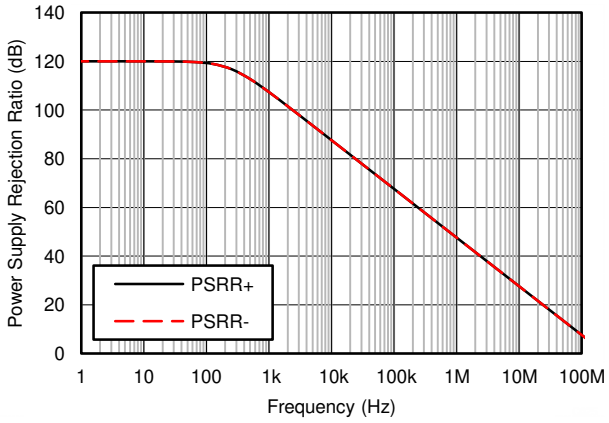


図 10. Power-Supply Rejection Ratio vs Frequency

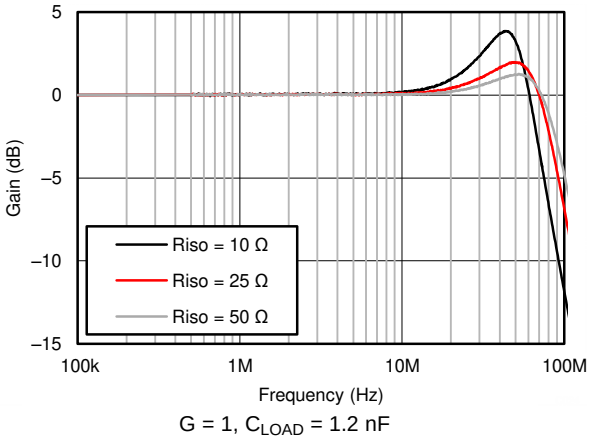


図 11. Series Resistance for Capacitive Load Stability

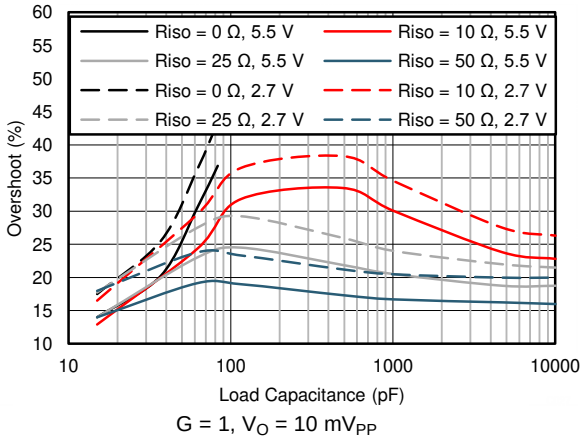
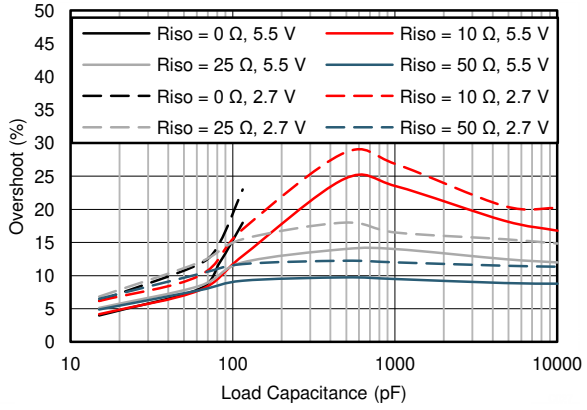


図 12. Overshoot vs Capacitive Load, G = 1

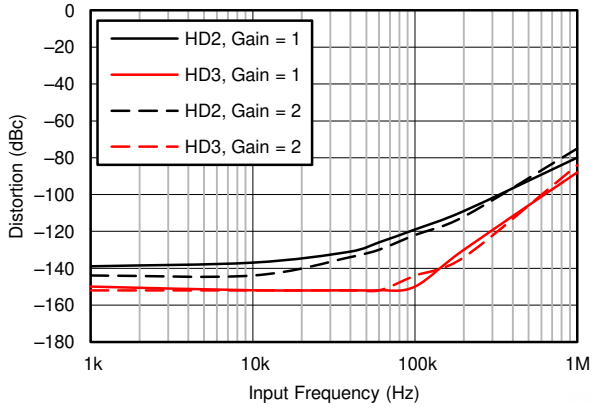
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



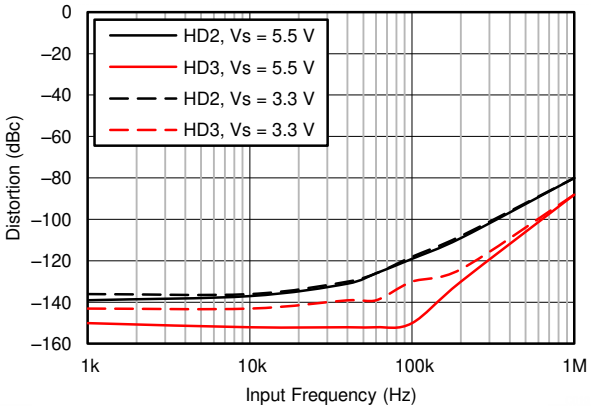
G = –1, V_O = 10 mV_{PP}

図 13. Overshoot vs Capacitive Load, G = –1



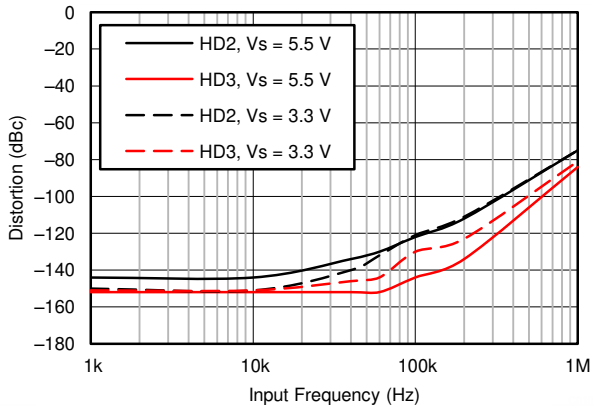
V_S = 5.5 V, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

図 14. Distortion vs Frequency for Various Gains



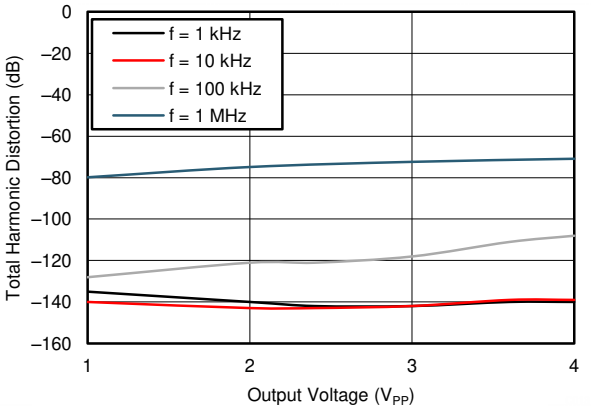
G = 1, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

図 15. Distortion vs Frequency for Various Power Supplies



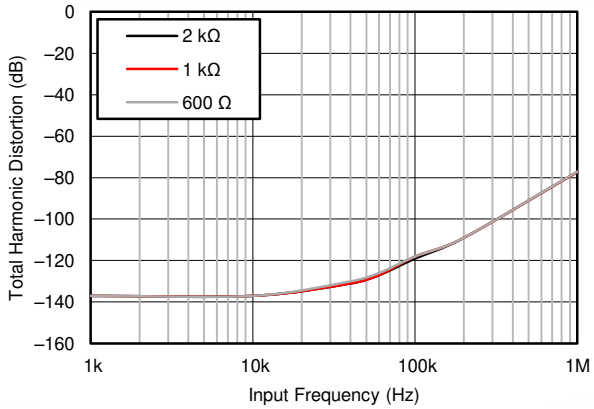
G = 2, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

図 16. Distortion vs Frequency for Various Power Supplies



G = 1, R_{LOAD} = 600 Ω

図 17. Total Harmonic Distortion vs Output Voltage for Various Frequencies



G = 1, V_O = 2 V_{PP} , R_{LOAD} = 600 Ω

図 18. Total Harmonic Distortion vs Frequency for Various Loads

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

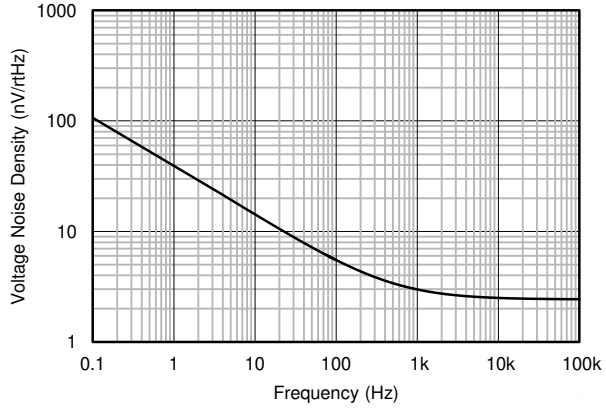


図 19. Voltage Noise Density vs Frequency

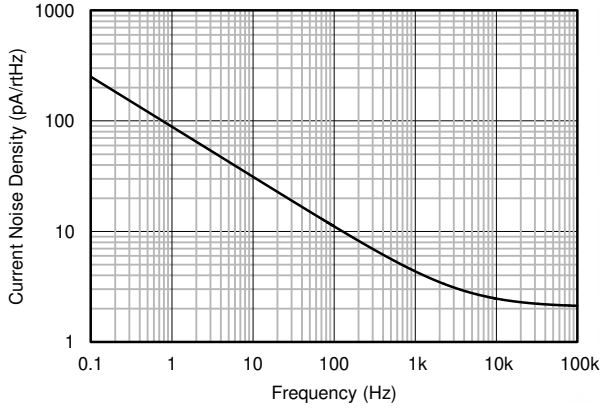


図 20. Current Noise Density vs Frequency

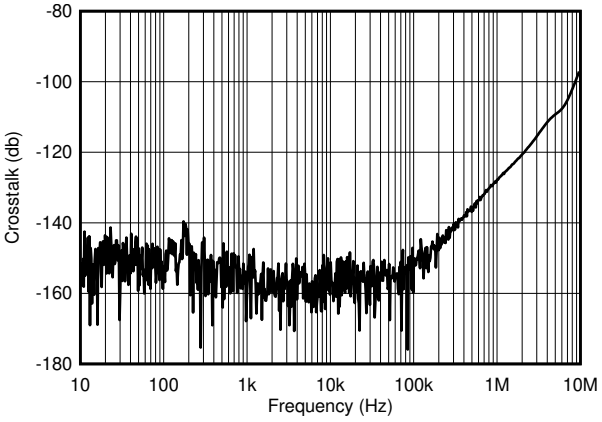


図 21. Crosstalk vs Frequency

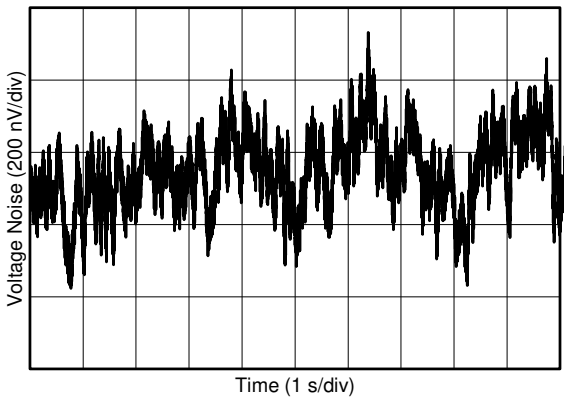


図 22. 0.1-Hz to 10-Hz Voltage Noise

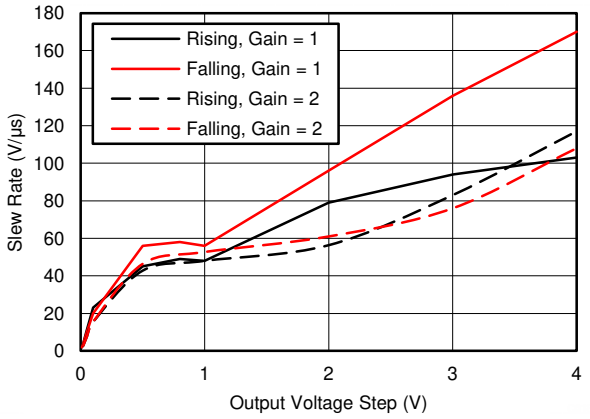


図 23. Slew Rate vs Output Step Size

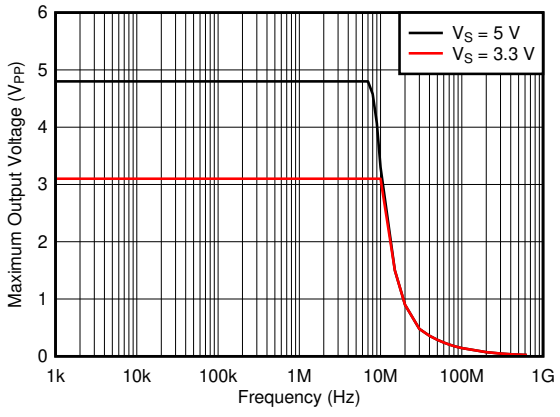
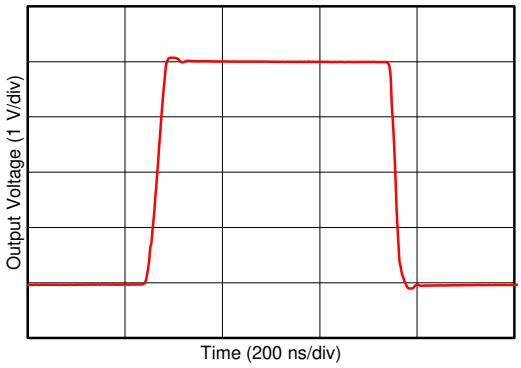


図 24. Maximum Output Voltage vs Frequency

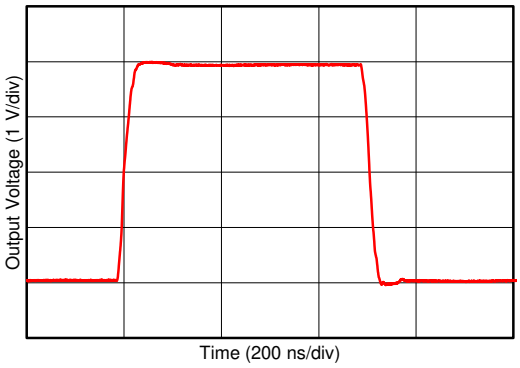
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



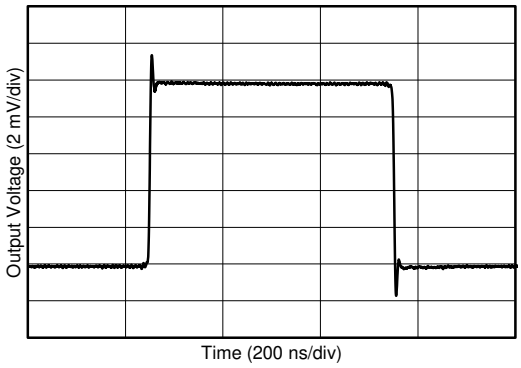
G = 1, V_O = 4-V step

図 25. Large-Signal Pulse Response



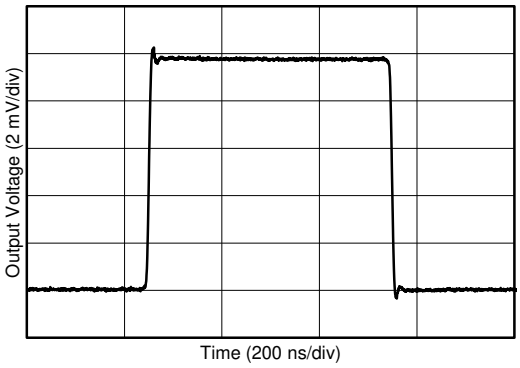
G = –1, V_O = 4-V step

図 26. Large-Signal Pulse Response



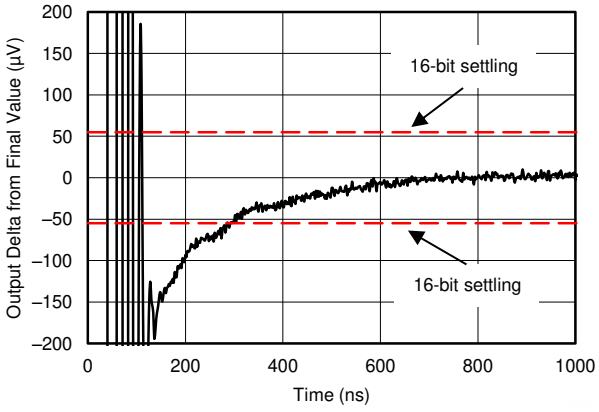
G = 1, V_O = 10-mV step

図 27. Small-Signal Pulse Response



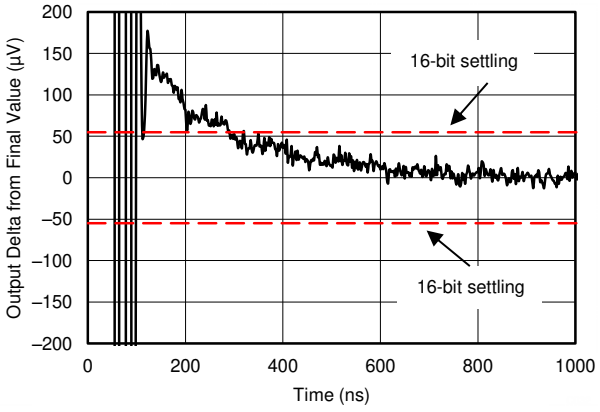
G = –1, V_O = 10-mV step

図 28. Small-Signal Pulse Response



V_O = 3.6-V step at t = 0 s

図 29. 16-Bit Negative Settling Time

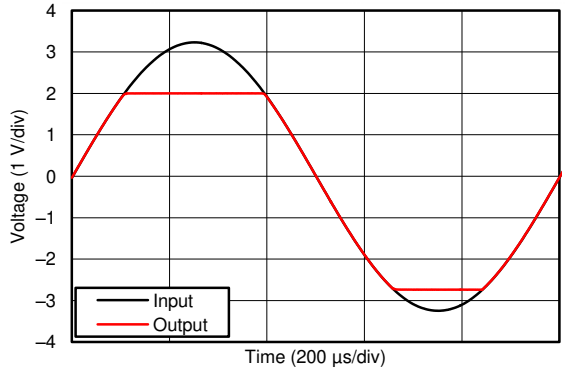


V_O = 3.6-V step at t = 0 s

図 30. 16-Bit Positive Settling Time

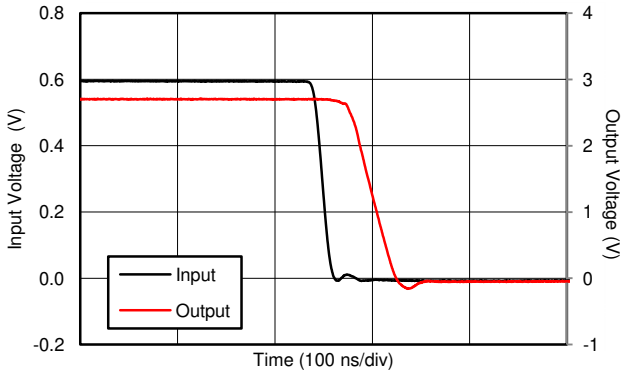
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



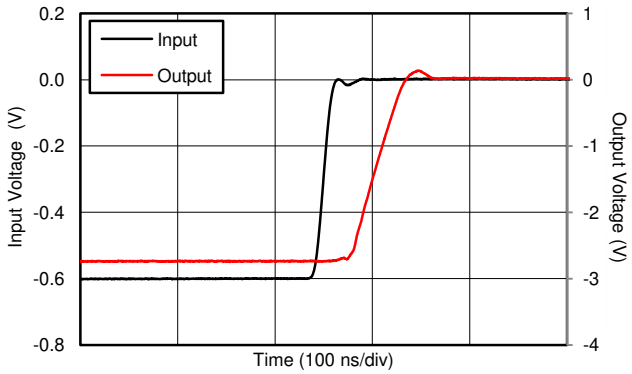
V_S = ±2.75 V, G = 1

図 31. No Phase Reversal



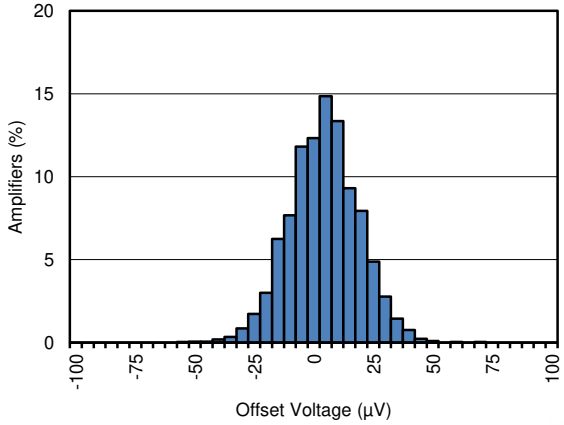
V_S = ±2.75 V, G = 5

図 32. Positive Overload Recovery



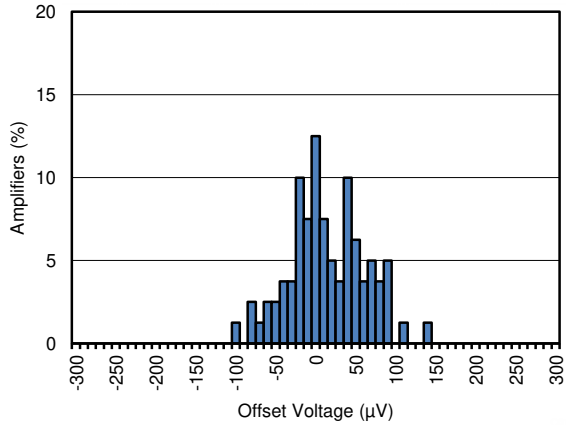
V_S = ±2.75 V, G = 5

図 33. Negative Overload Recovery



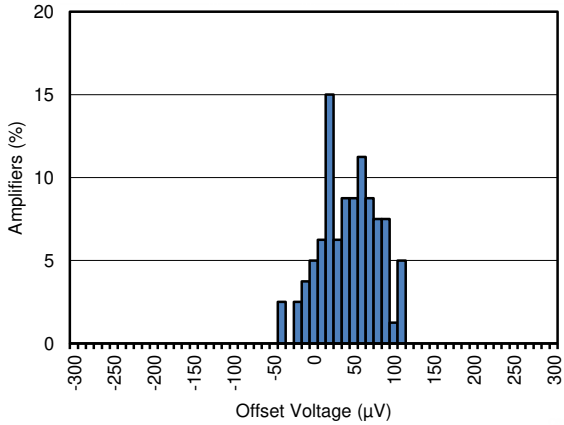
Distribution taken from 3139 amplifiers, T_A = 25°C

図 34. Input Offset Voltage Distribution



Distribution taken from 80 amplifiers, T_A = 125°C

図 35. Input Offset Voltage Distribution

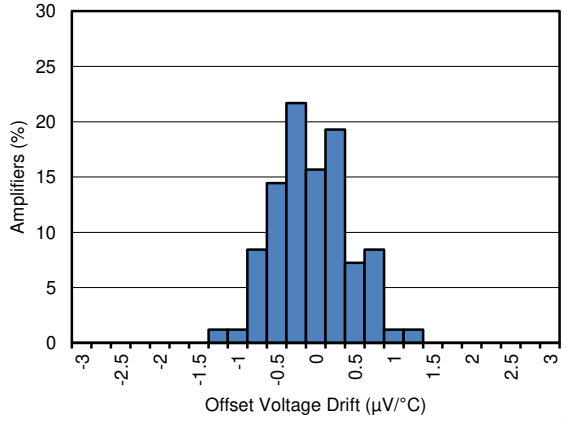


Distribution taken from 80 amplifiers, T_A = –40°C

図 36. Input Offset Voltage Distribution

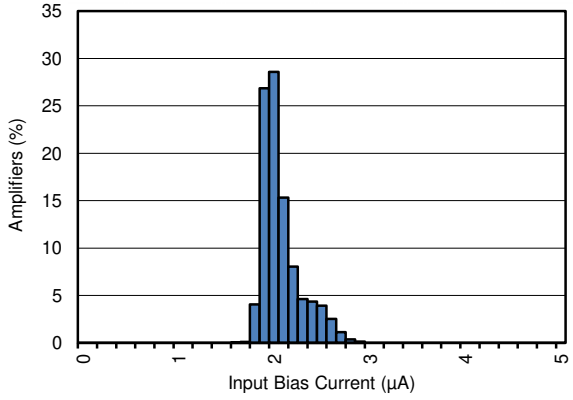
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



Distribution taken from 75 amplifiers, T_A = –40°C to +125°C

図 37. Input Offset Voltage Drift Distribution



Distribution taken from 3139 amplifiers

図 38. Input Bias Current Distribution

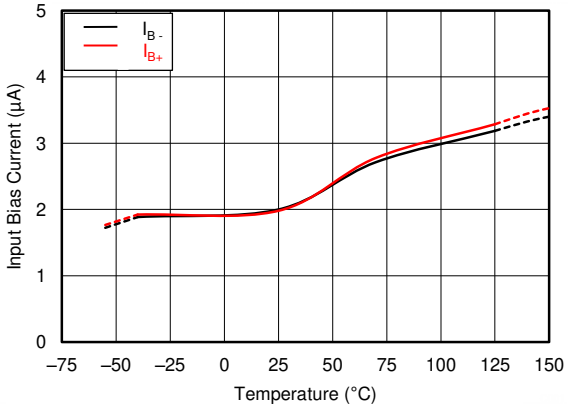
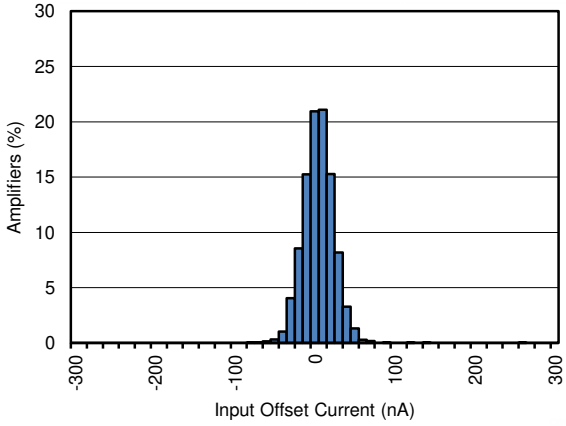


図 39. Input Bias Current vs Temperature



Distribution taken from 3139 amplifiers

図 40. Input Offset Current Distribution

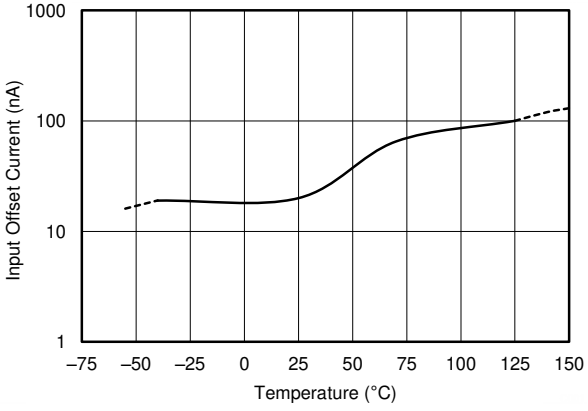


図 41. Input Offset Current vs Temperature

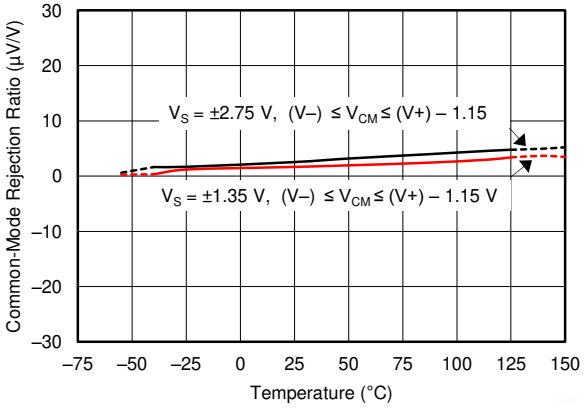
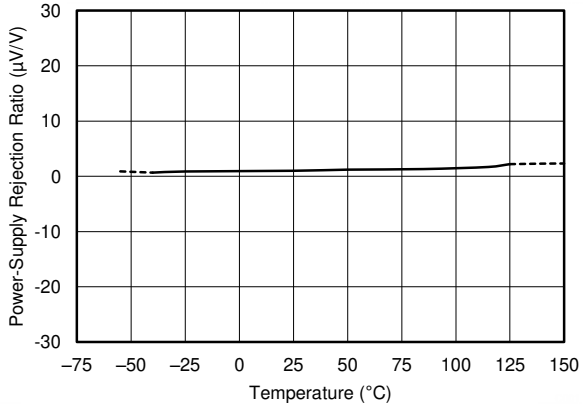


図 42. Common-Mode Rejection Ratio vs Temperature

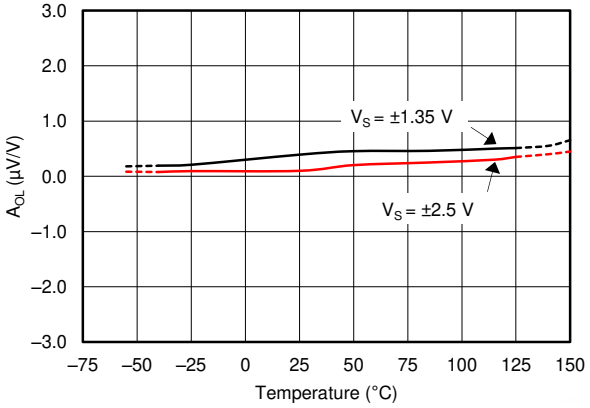
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



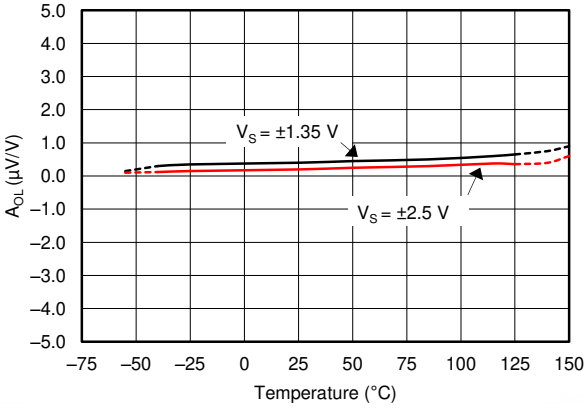
2.7 V ≤ V_S ≤ 5.5 V

図 43. Power-Supply Rejection Ratio vs Temperature



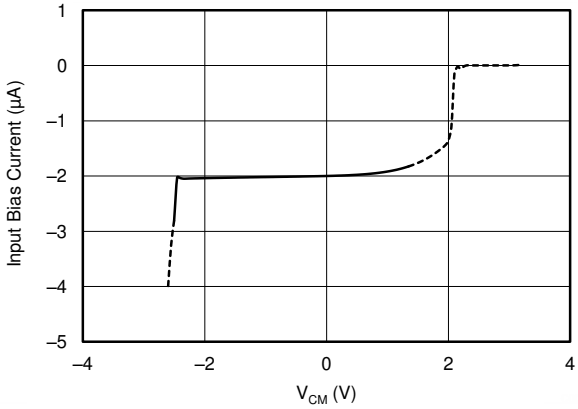
R_{LOAD} = 10 kΩ

図 44. Open-Loop Gain vs Temperature With 10-kΩ Load



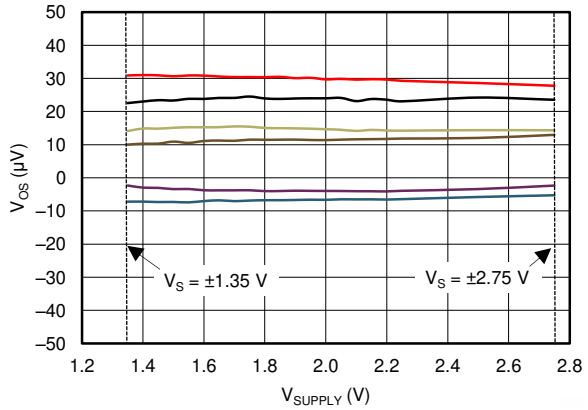
R_{LOAD} = 600 Ω

図 45. Open-Loop Gain vs Temperature With 600-Ω Load



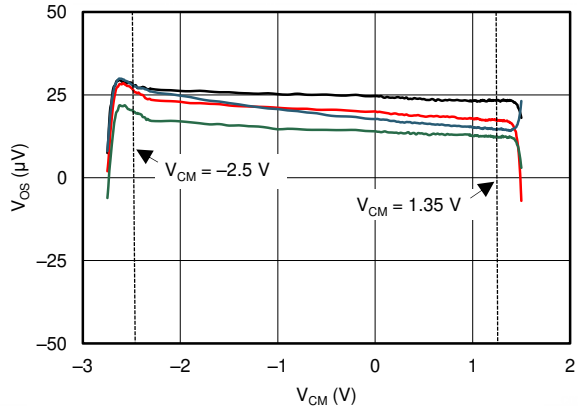
V_S = ±2.5 V

図 46. Input Bias Current vs Input Common-Mode Voltage



6 typical units shown, V_S = ±1.35 V to ±2.75 V

図 47. Input Offset Voltage vs Power-Supply Voltage



6 typical units shown, V_S = ±2.5 V

図 48. Input Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

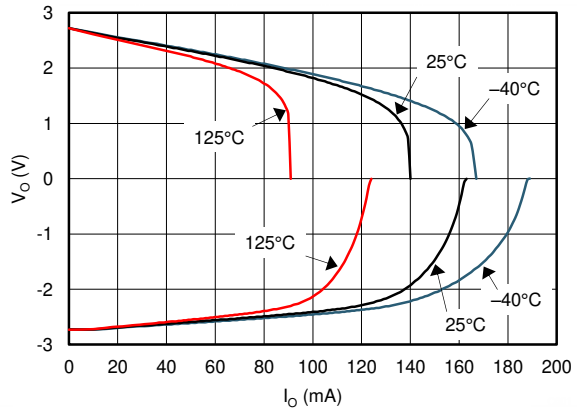


図 49. Output Voltage vs Output Current

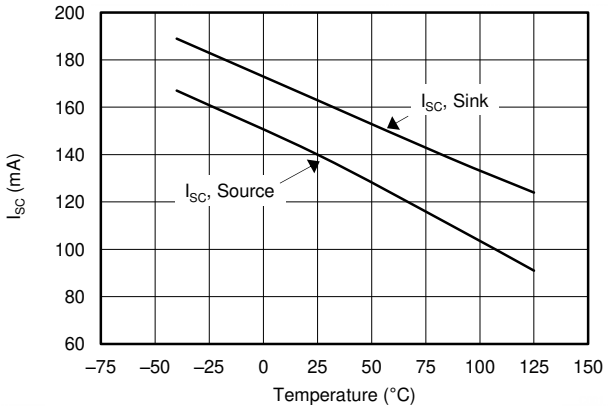


図 50. Short-Circuit Current vs Temperature

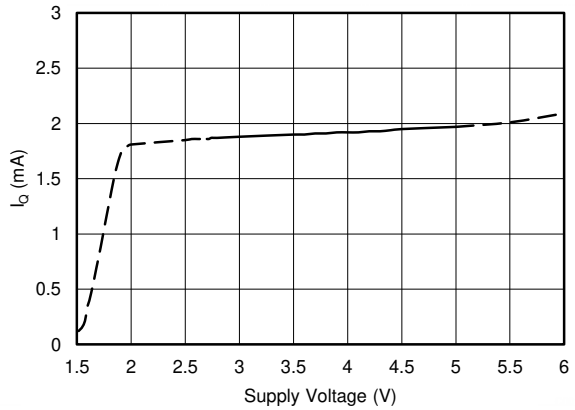


図 51. Quiescent Current vs Power-Supply Voltage

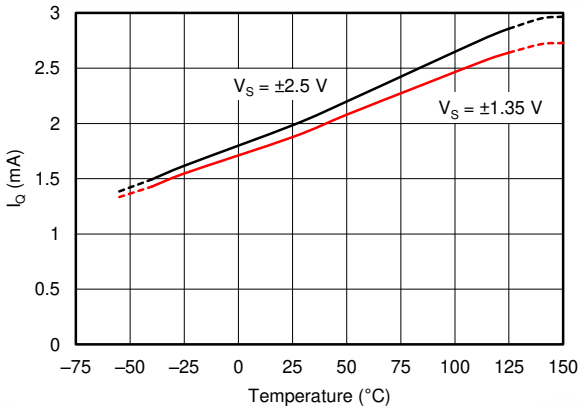
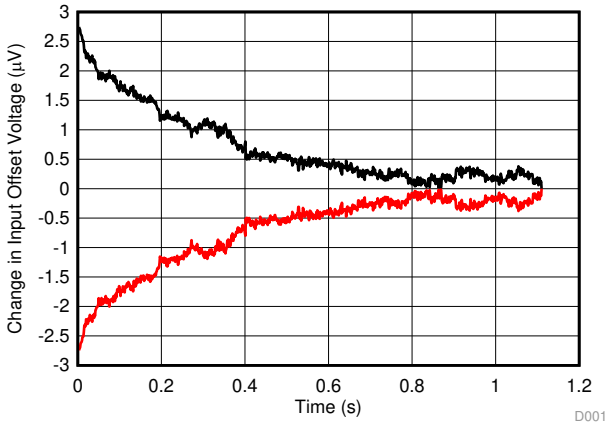


図 52. Quiescent Current vs Temperature



Powered on at t = 0 s, PCB dimensions: 4 in^2, 2 layer, FR4

図 53. Warm-Up Time

7 Parameter Measurement Information

7.1 DC Parameter Measurements

The circuit shown in 図 54 measures the dc input offset related parameters of the OPA2626. Input offset voltage, power-supply rejection ratio, common-mode rejection ratio, and open-loop gain can be measured with this circuit. The basic test procedure requires setting the inputs (the power-supply voltage, V_S, and the common-mode voltage, V_{CM}), to the desired values. V_O is set to the desired value by adjusting the loop-drive voltage while measuring V_O. After all inputs are configured, measure the input offset at the V_X measurement point. Calculate the input offset voltage by dividing the measured result by 101. Changing the voltages on the various inputs changes the input offset voltage. The input parameters can be measured according to the relationships illustrated in 式 1 through 式 5.

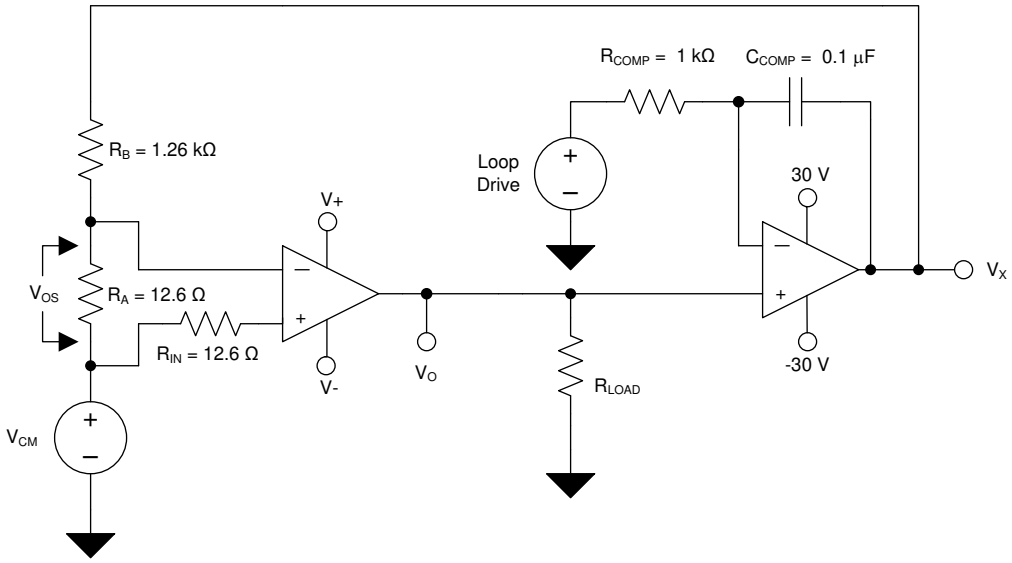


図 54. DC-Parameters Measurement Circuit

$$V_{OS} = \frac{V_X}{101} \tag{1}$$

$$V_{OSDrift} = \frac{\Delta V_{OS}}{\Delta Temperature} \tag{2}$$

$$PSRR = \frac{\Delta V_{OS}}{\Delta V_{SUPPLY}} \tag{3}$$

$$CMRR = \frac{\Delta V_{OS}}{\Delta V_{CM}} \tag{4}$$

$$AOL = \frac{\Delta V_O}{\Delta V_{OS}} \tag{5}$$

7.2 Transient Parameter Measurements

The circuit shown in 図 55 measures the transient response of the OPA2626. Configure V+, V–, R_{ISO}, R_{LOAD}, and C_{LOAD} as desired. Monitor the input and output voltages on an oscilloscope or other signal analyzer. Use this circuit to measure large-signal and small-signal transient response, slew rate, overshoot, and capacitive-load stability.

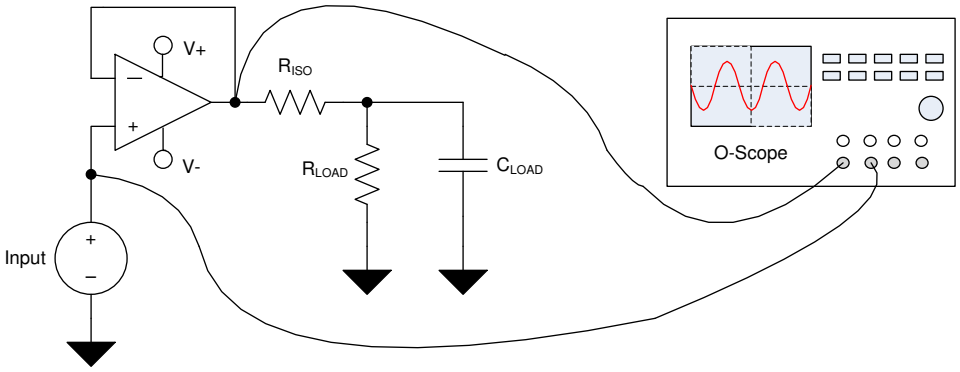


図 55. Pulse-Response Measurement Circuit

7.3 AC Parameter Measurements

The circuit shown in 図 56 measures the ac parameters of the OPA2626. Configure V+, V–, and C_{LOAD} as desired. The THS4271 family is used to buffer the input and output of the OPA2626 to prevent loading by the gain phase analyzer. Monitor the input and output voltages on a gain phase analyzer. Use this circuit to measure the gain bandwidth product, and open-loop gain versus frequency versus capacitive load.

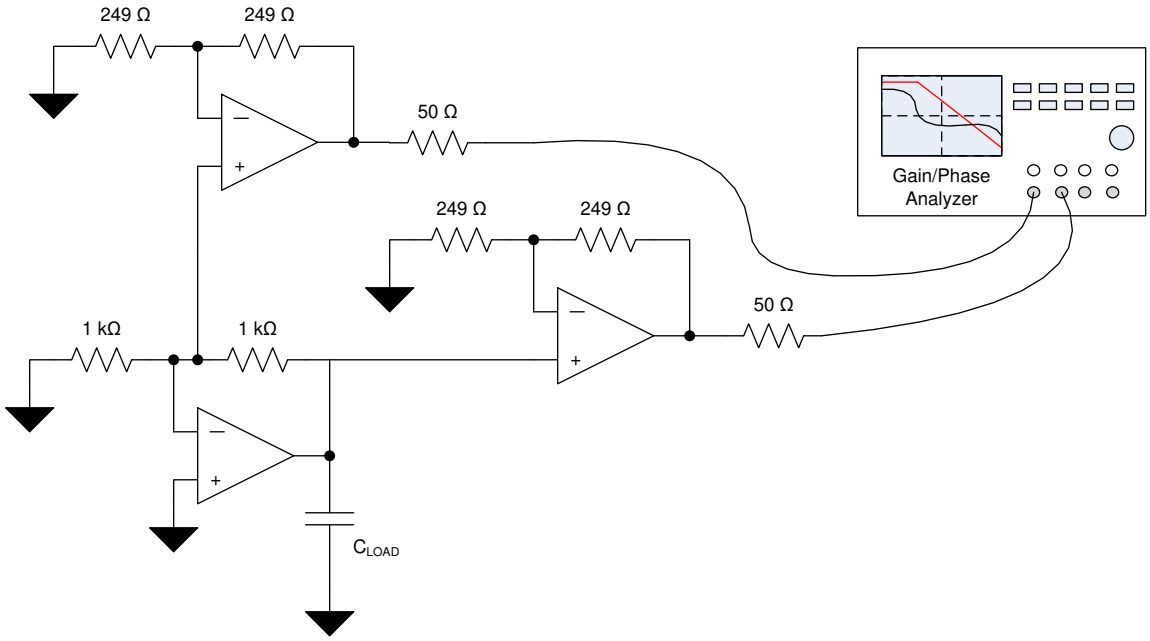


図 56. AC-Parameters Measurement Circuit

7.4 Noise Parameter Measurements

The circuit shown in 図 57 measures the voltage noise of the OPA2626. Configure V+, V–, and C_{LOAD} as desired.

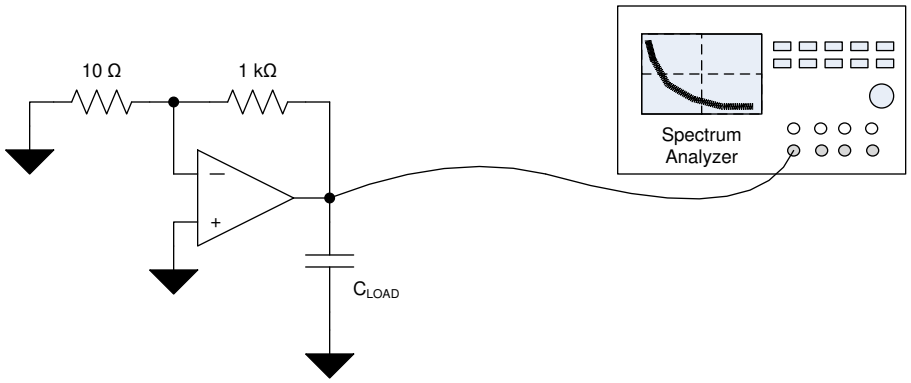


図 57. Voltage Noise Measurement Circuit

The circuit shown in 図 58 measures the current noise of the OPA2626. Configure V+, V– and C_{LOAD} as desired.

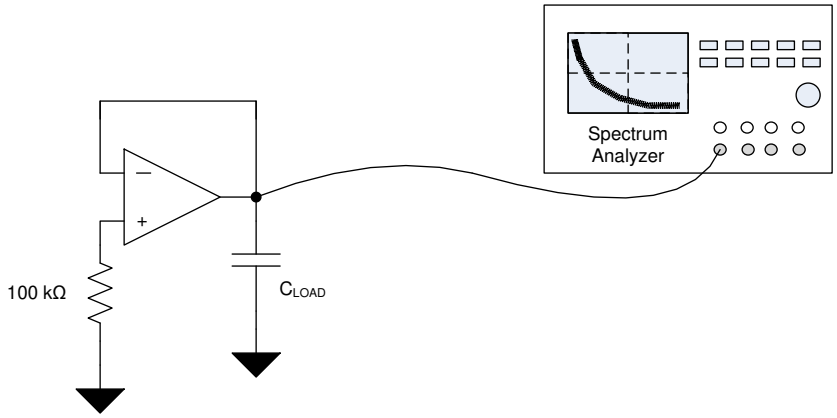


図 58. Current Noise Measurement Circuit

The circuit shown in 図 59 measures the 0.1-Hz to 10-Hz voltage noise of the OPA2626. Configure V+, V–, and C_{LOAD} as desired.

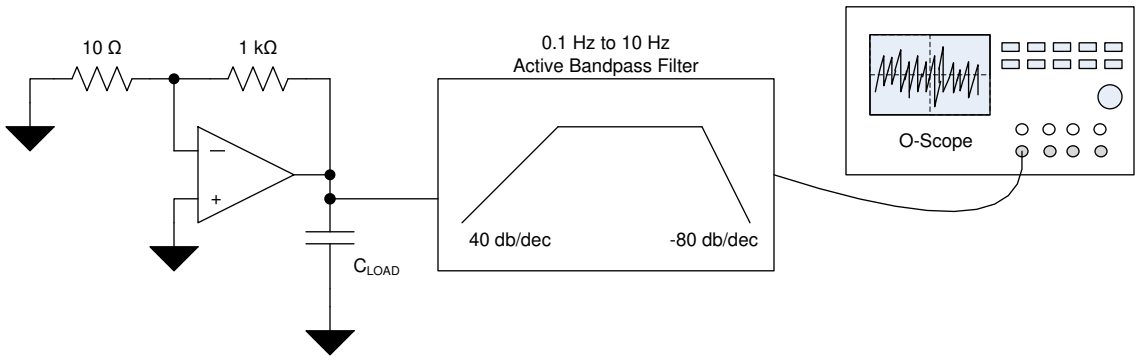


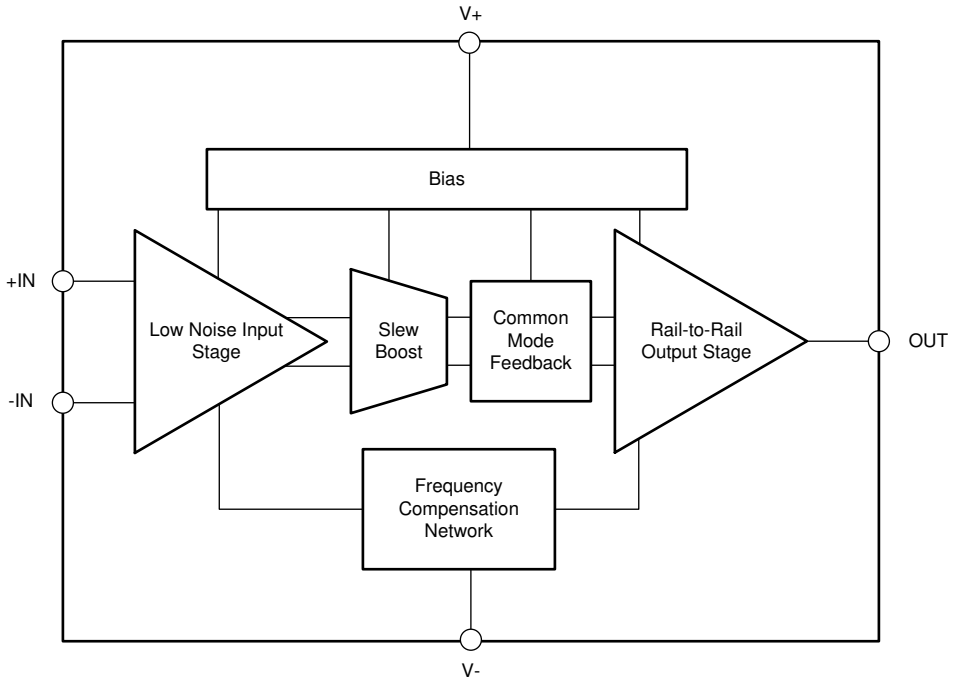
図 59. 0.1-Hz to 10-Hz Voltage-Noise Measurement Circuit

8 Detailed Description

8.1 Overview

The OPA2626 is a fast-settling, high slew rate, high-bandwidth, voltage-feedback operational amplifier. Low offset and low offset drift combine with the superior dynamic performance and low output impedance of this device, resulting in an amplifier suited for driving 16-bit and 18-bit SAR ADCs, and buffering precision voltage references in industrial applications. The OPA2626 includes low-noise input, slew boost, and rail-to-rail output stages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 SAR ADC Driver

The OPA2626 is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low output impedance, low THD, low noise, and fast settling time make the OPA2626 the ideal choice for driving both the SAR ADC inputs, as well as the reference input to the ADC. Internal slew boost circuitry increases the slew rate as a function of the input signal magnitude, resulting in settling from a 4-V step input to 16-bit levels within 280 ns. Low output impedance (1 Ω at 1 MHz) ensures capacitive load stability with minimal overshoot.

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly. A good understanding of this basic ESD circuitry and how the ESD circuitry relates to an electrical overstress event is helpful. 図 60 provides a diagram of the ESD circuits contained in the OPA2626. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

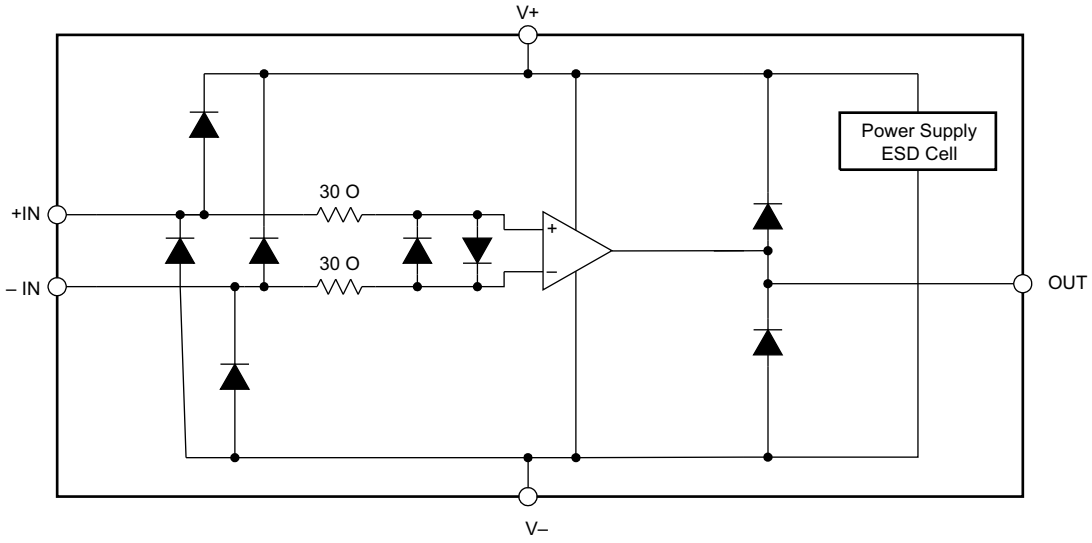


図 60. Simplified ESD Circuit

8.4 Device Functional Modes

The OPA2626 has a single functional mode and is operational when the power supply voltage, V_S, is between 2.7 V (±1.35 V) and 5.5 V (±2.75 V).

8.4.1 High-Drive Mode

The OPA2626 has a 120-MHz gain bandwidth, 2.5-nV/√Hz input-referred noise, and consumes 2 mA of quiescent current. Additionally, the OPA2626 has an offset voltage of 100 µV (maximum) and an offset voltage drift of 1 µV/°C (typical). This combination of high precision, high speed, and low noise makes this device suitable for use as an input driver for high-precision, high-throughput SAR ADCs such as the ADS88xx family of SAR ADCs, as illustrated in 図 61.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA2626 consists of precision, high-speed, voltage-feedback operational amplifiers. Fast settling to 16-bit and 18-bit levels, low THD, and low noise make the OPA2626 suitable for driving SAR ADC inputs and buffering precision voltage references. With a wide power-supply voltage range from 2.7 V to 5.5 V, and operating from –40°C to +125°C, the OPA2626 is suitable for a variety of high-speed, industrial applications. The following sections show application information for the OPA2626. For simplicity, power-supply decoupling capacitors are not shown in these diagrams.

9.2 Typical Applications

9.2.1 Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

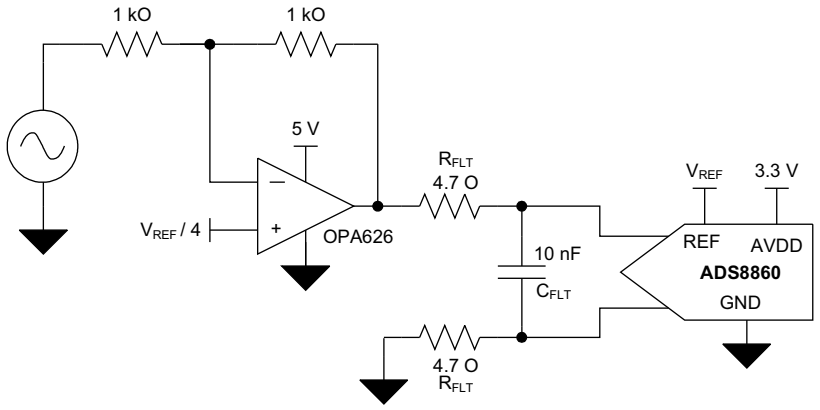


図 61. Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

Typical Applications (continued)

9.2.1.1 Design Requirements

A SAR ADC, such as the ADS8860 device, uses sampling capacitors on the data converter input. During the signal acquisition phase, these sampling capacitors are connected to the ADC analog input terminals AINP and AINN (pins 3 and 4), through a set of switches. After the acquisition period has elapsed, the internal sampling capacitors are disconnected from the input terminals (pins 3 and 4) and connected to the ADC input through a second set of switches, during this period the ADC is performing the analog-to-digital conversion. 図 62 shows this architecture.

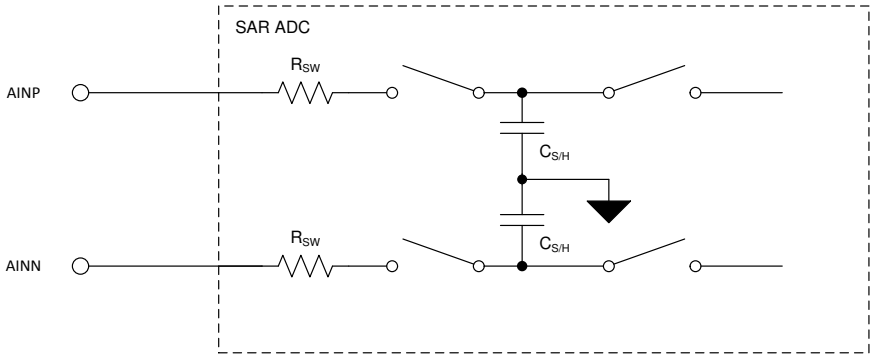


図 62. Simplified SAR ADC Input

The SAR ADC inputs and sampling capacitors must be driven by the OPA2626 to 16-bit levels within the acquisition time of the ADC. For the example illustrated in 図 61, the OPA2626 is used to drive the ADS8860 at a sample rate of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The circuit illustrated in 図 61 consists of the SAR ADC driver, a low-pass filter, and the SAR ADC. The SAR ADC driver circuit consists of an OPA2626 configured in an inverting gain of 1. The filter consists of R_{FLT} and C_{FLT}, connected between the OPA2626 output and the ADS8860 input. Selecting the proper values for each of these passive components is critical to obtain the best performance from the ADC. Capacitor C_{FLT} serves as a charge reservoir, providing the necessary charge to the ADC sampling capacitors. The dynamic load presented by the ADC creates a glitch on the filter capacitor, C_{FLT}. To minimize the magnitude of this glitch, choose a value for C_{FLT} large enough to maintain a glitch amplitude of less than 100 mV. Maintaining such a low glitch amplitude at the amplifier output makes sure that the amplifier remains in the linear operating region, and results in a minimum settling time. Using 式 6, a 10-nF capacitor is selected for C_{FLT}.

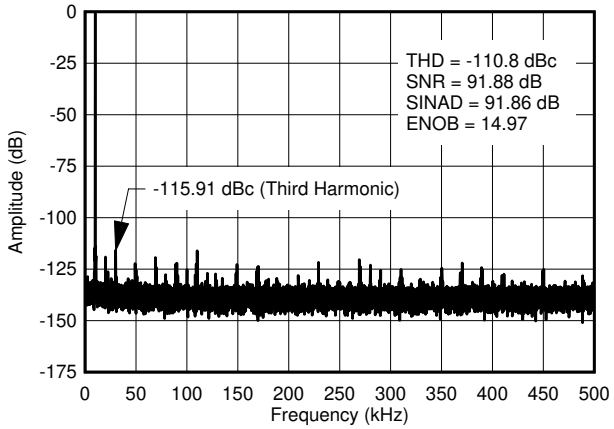
$$C_{FLT} \geq 15 \times C_{SH} \tag{6}$$

Connecting a 10-nF capacitor directly to the OPA2626 output degrades the OPA2626 phase margin and results in stability and settling-time problems. To properly drive the 10-nF capacitor, use a series resistor (R_{FLT}) to isolate the capacitor, C_{FLT}, from the OPA2626. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, consider the impact upon the THD resulting from the voltage divider effect from R_{FLT} reacting with the switch resistance (R_{SW}) of the ADC input circuit, as well as the impact of the output impedance upon amplifier stability. In this example, 4.7-Ω resistors are selected. In this design example, 図 13 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, and in this example is equivalent to $2 \times R_{FLT}$.

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to the *Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design* reference guide.

9.2.1.3 Application Curve

図 63 shows the performance of the circuit in 図 61.



4096-point FFT at 1 MSPS, f_{IN} = 10 kHz , V_{IN} = 1.5 V_{RMS}

図 63. ADC Output FFT for 図 61

9.2.2 Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

In order to operate a high-resolution, 16-bit ADC at its maximum throughput, the full-scale voltage step must settle to better than 16-bit accuracy at the ADC inputs within the minimum specified acquisition time (t_{ACQ}). This settling imposes very stringent requirements on the driver amplifier in terms of large-signal bandwidth, slew rate, and settling time. 図 64 shows a typical multiplexed ADC driver application using the OPA2626.

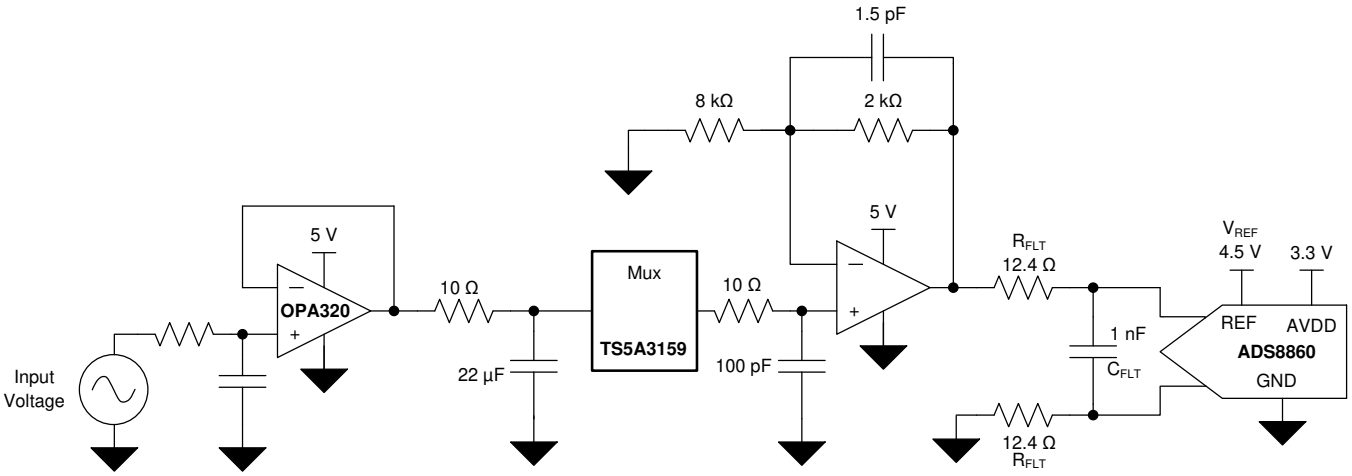


図 64. Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

9.2.2.1 Design Requirements

To optimize this circuit for performance, this design does not allow any large signal input transients at the driver circuit inputs for a small quiet-time period (t_{QT}) towards the end of the previous conversion. The input step voltage can appear anytime from the beginning of conversion (CONVST rising edge) until the elapse of a half cycle time ($0.5 \times t_{CYC}$). This timing constraint on the input step allows a minimum settling time of ($t_{QT} + t_{ACQ}$) for the ADC input to settle within the required accuracy, in the worst-case scenario. $t_{QT} + t_{ACQ}$ is the total time in which the output of the amplifier has to slew and settle within the required accuracy before the next conversion starts. 図 65 shows this timing sequence.

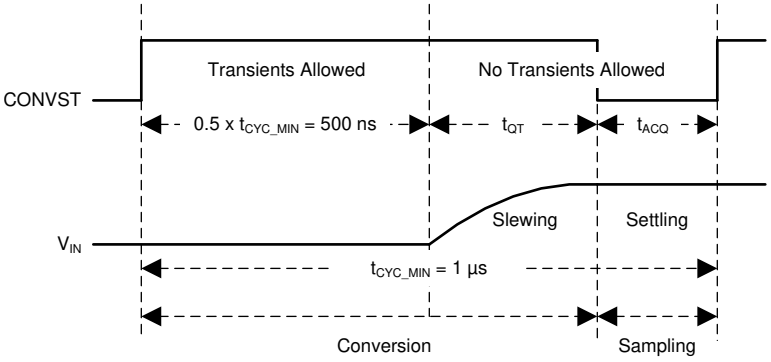


図 65. Timing Diagram for Input Signals

9.2.2.2 Detailed Design Procedure

An ADC input driver circuit consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and the low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC and acts as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven by the following requirements:

- The R_{FLT} and C_{FLT} filter bandwidth must be low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system
- The overall system bandwidth must be large enough to accommodate optimal settling of the input signal at the ADC input before the conversion starts

C_{FLT} is chosen based upon 式 7. C_{FLT} is chosen to be 1 nF.

$$C_{FLT} \geq 15 \times C_{SH} \tag{7}$$

Connecting a 1-nF capacitor directly to the output of the OPA2626 degrades the OPA2626 phase margin and results in stability and settling time problems. To properly drive the 1-nF capacitor, a series resistor, R_{FLT}, is used to isolate the capacitor, C_{FLT}, from the OPA2626. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, the system designer must consider the impact upon the THD resulting from the voltage divider effect from R_{FLT} reacting with the switch resistance, R_{SW}, of the ADC input circuit as well as the impact of the output impedance upon amplifier stability. In this example 12.4-Ω resistors are selected. In this design example, 図 12 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, which in this example is equivalent to 2 × R_{FLT}.

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to the *18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response* reference guide.

9.2.2.3 Application Curves

図 66 and 図 67 show the performance of the circuit in 図 64.

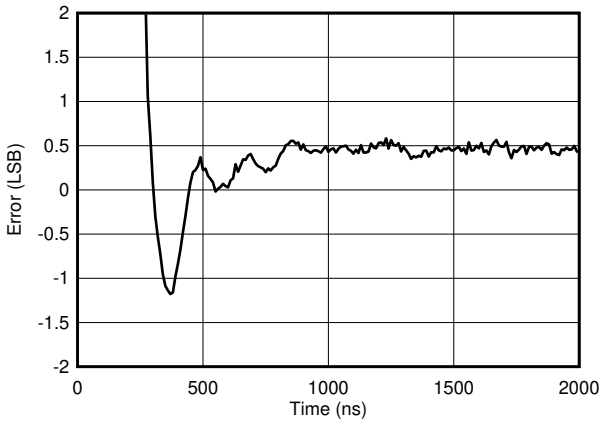


図 66. Positive Transient Response for 図 64

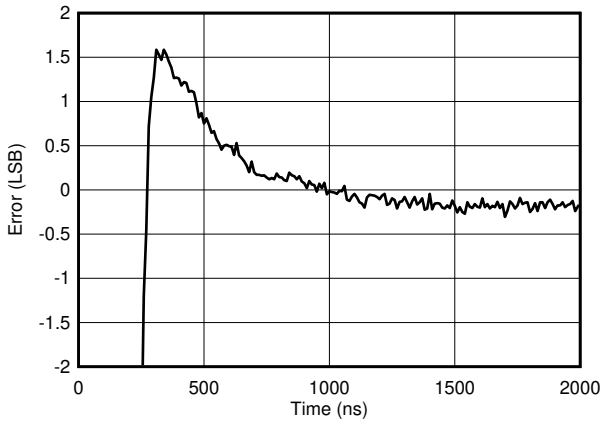


図 67. Negative Transient Response for 図 64

10 Power Supply Recommendations

The OPA2626 is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section. Place bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

注意

Supply voltages larger than 6 V can cause permanent damage to the device. See the *Absolute Maximum Ratings* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Use bypass capacitors to reduce the noise coupled from the power supply. Connect low ESR, ceramic, bypass capacitors between the power-supply pins (V+ and V–) and the ground plane. Place the bypass capacitors as close to the device as possible with the 100-nF capacitor closest to the device, as indicated in 図 68. For single-supply applications, bypass capacitors on the V– pin are not required.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. (For more details, see the *Circuit Board Layout Techniques* chapter extract.)
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicular is better as opposed to in parallel with the noisy trace.
- Minimize parasitic coupling between +IN and OUT for best ac performance.
- Place the external components as close to the device as possible. As illustrated in 図 68, keeping RF, CF, and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

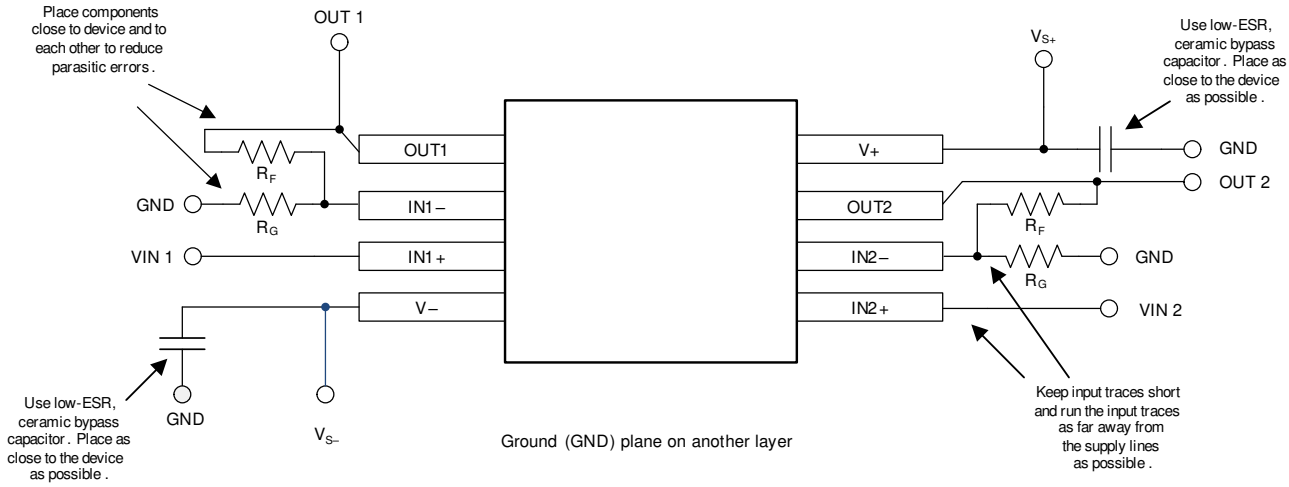


図 68. PCB Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

12.1.1.2 TI Precision Designs

TI Precision Designs は、http://www.ti.com/ww/en/analog/precision-designs/ からオンラインで入手できます。TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『Fast Settling 16-bit 1MSPS Multiplexed Data Acquisition Reference Design』*デザイン・ガイド (英語)
- テキサス・インスツルメンツ、*『Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design』*リファレンス・ガイド (英語)
- テキサス・インスツルメンツ、*『18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response』*リファレンス・ガイド (英語)
- テキサス・インスツルメンツ、*『Circuit Board Layout Techniques』*チャプター抜粋 (英語)
- テキサス・インスツルメンツ、*『THS427x LOW NOISE, HIGH SLEW RATE, UNITY GAIN STABLE VOLTAGE FEEDBACK AMPLIFIER』*データシート (英語)
- テキサス・インスツルメンツ、*『ADS8860 16 ビット、1MSPS、シリアル・インターフェイス、micropower、小型、シングルエンド入力の SAR アナログ / デジタル・コンバータ』*データシート

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商標

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TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2626IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6
OPA2626IDGKR.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6
OPA2626IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6
OPA2626IDGKT.Z	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

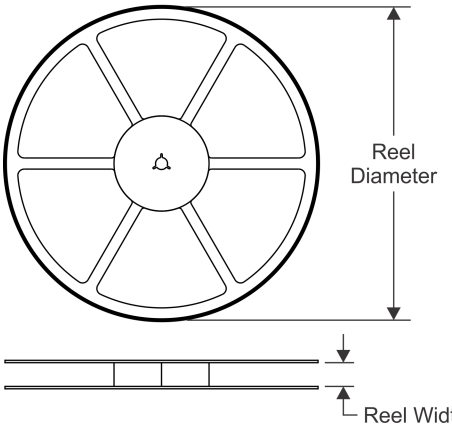
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

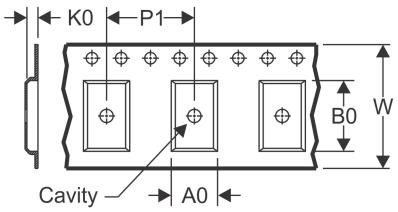
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

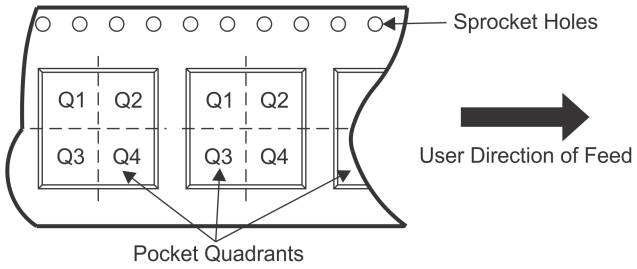


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

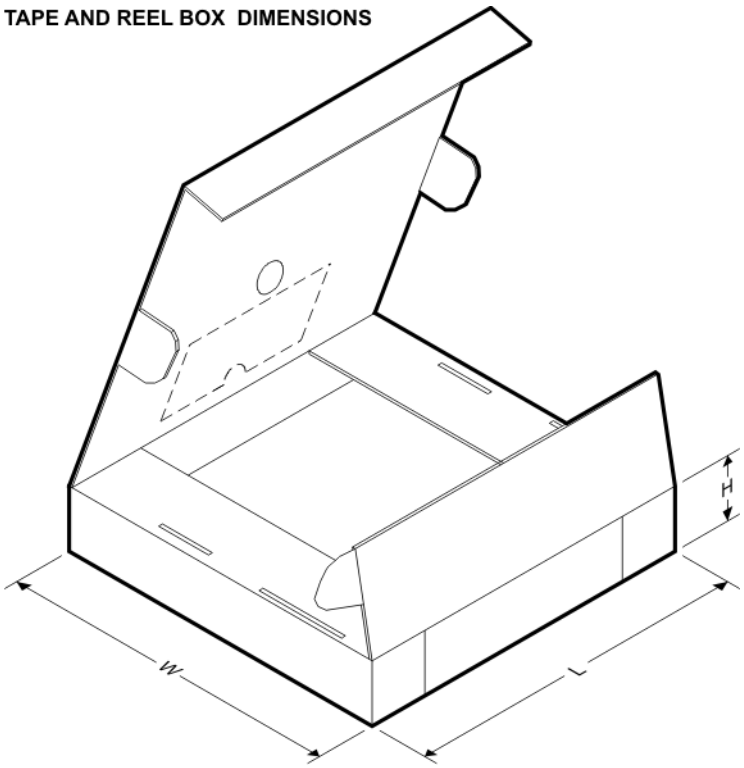
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2626IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2626IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

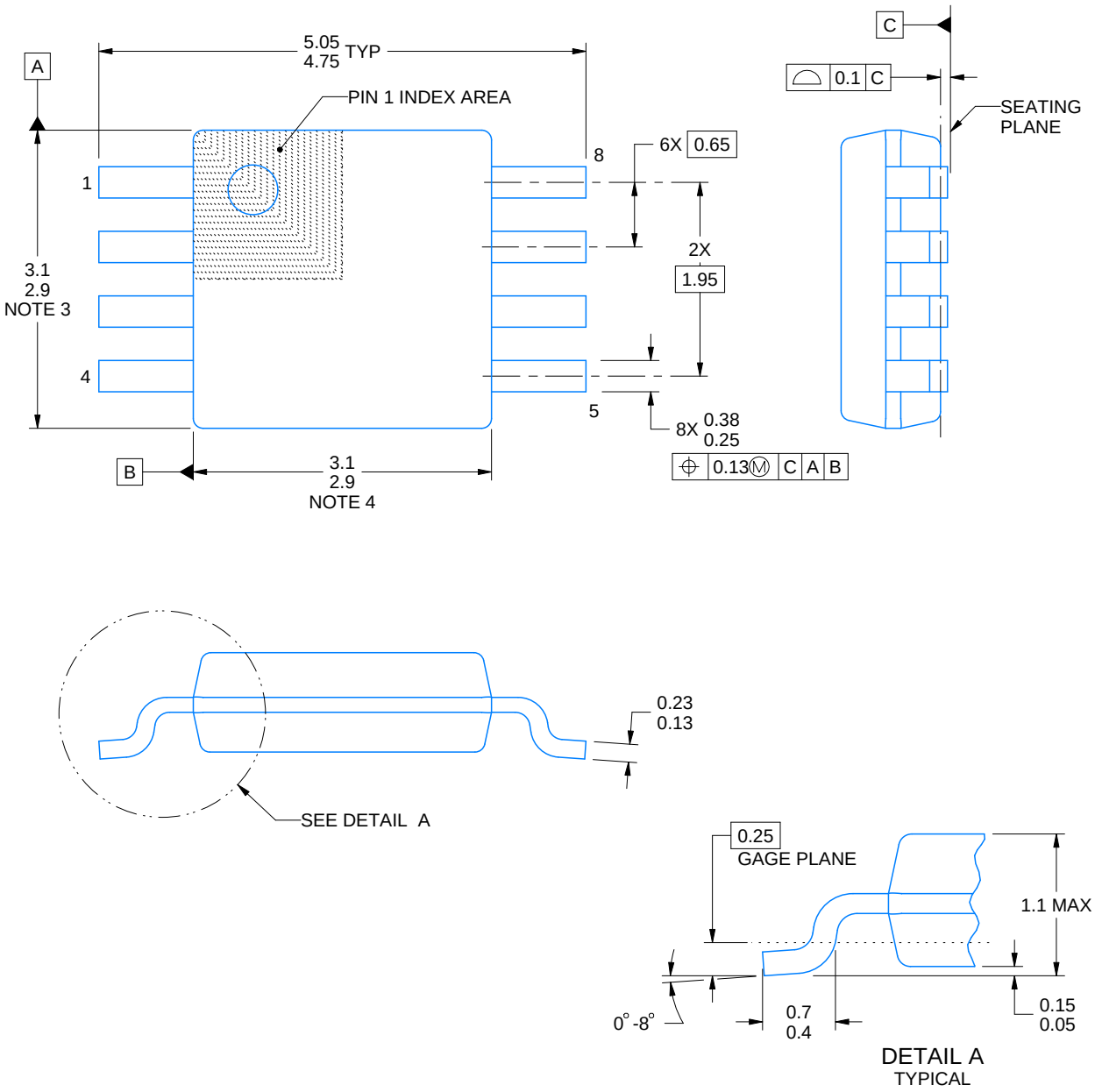
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2626IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2626IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

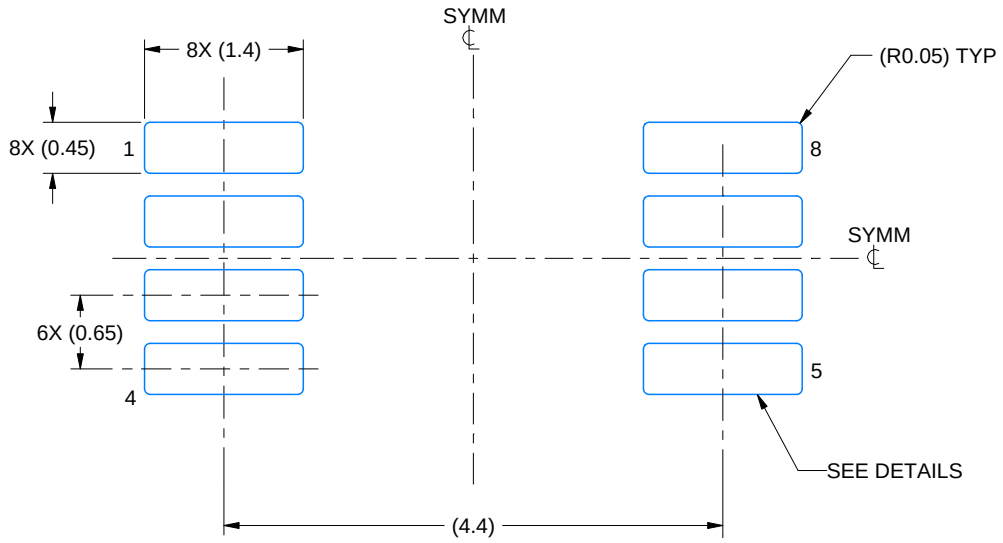
SMALL OUTLINE PACKAGE



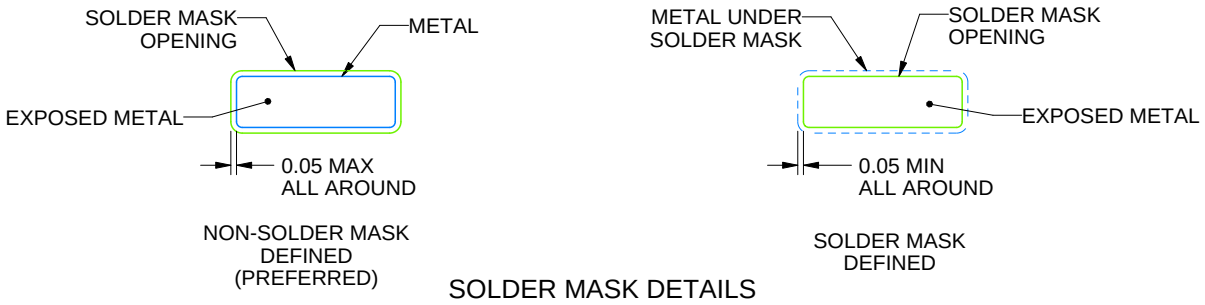
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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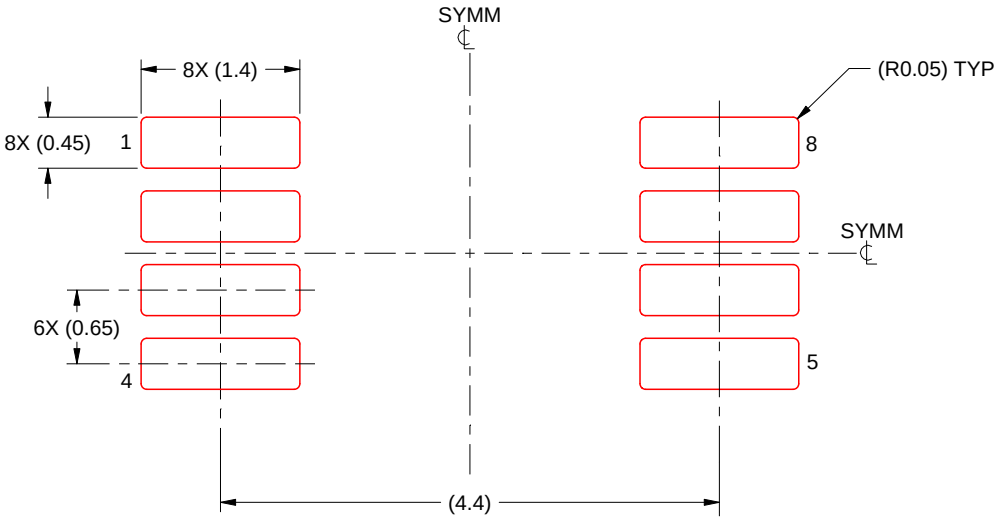
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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