PCM1798 24-Bit, 192-kHz Sampling, Advanced Segment, Audio Stereo Digital-to-Analog Converter

1 Features

- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range: 123 dB
  - THD+N: 0.0005%
- Differential Current Output: 4 mAp-p
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –98 dB
  - Pass-Band Ripple: ±0.0002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect
- Accepts 16- and 24-Bit Audio Data
- PCM Data Formats: Standard, I2S, and Left-Justified
- Interface Available for Optional External Digital Filter or DSP
- Digital De-Emphasis
- Digital Filter Rolloff: Sharp or Slow
- Soft Mute
- Zero Flag
- Dual-Supply Operation: 5-V Analog, 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small 28-Lead SSOP Package
- Pin Assignment Compatible With PCM1794

2 Applications

- A/V Receivers
- DVD Players
- Musical Instruments
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 24-Bit Audio

3 Description

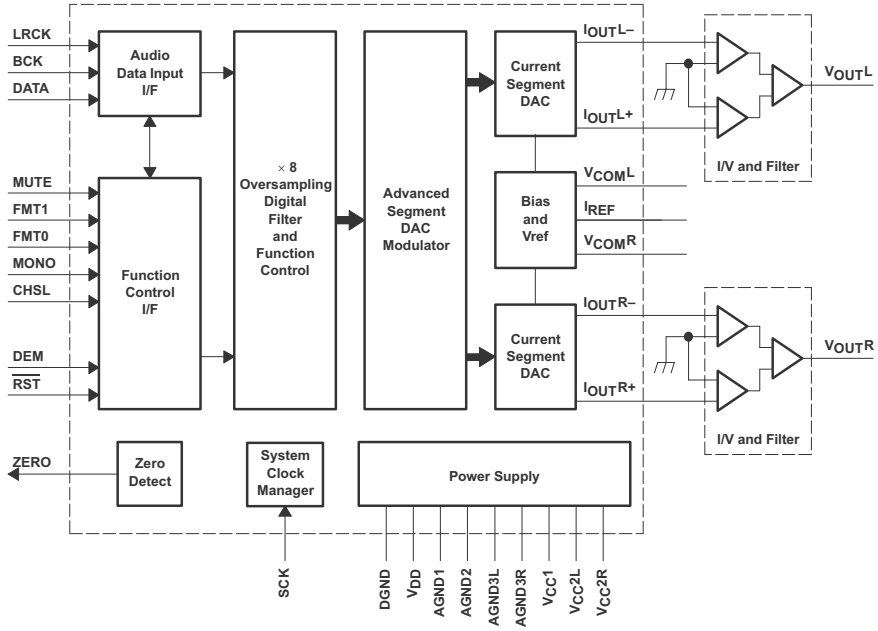
The PCM1798 device is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters (DACs) and support circuitry in a small 28-lead SSOP package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1798 device provides balanced current outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1798	SSOP (28)	10.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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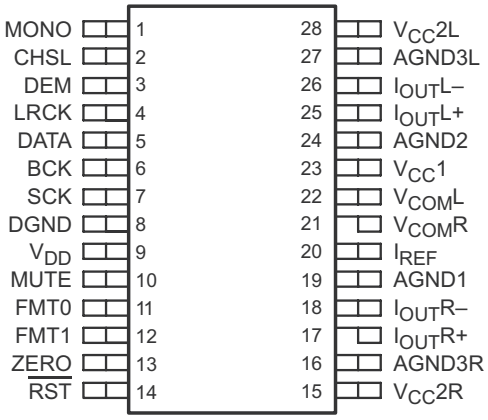
4 Revision History

Changes from Revision A (November 2006) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DB Package
28-Lead SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND1	19	—	Analog ground (internal bias)
AGND2	24	—	Analog ground (internal bias)
AGND3L	27	—	Analog ground (L-channel DACFF)
AGND3R	16	—	Analog ground (R-channel DACFF)
BCK	6	Input	Bit clock input(1)
CHSL	2	Input	L-, R-channel select(1)
DATA	5	Input	Serial audio data input(1)
DEM	3	Input	De-emphasis enable(1)
DGND	8	—	Digital ground
FMT0	11	Input	Audio data format select(1)
FMT1	12	Input	Audio data format select(1)
$I_{OUT}L+$	25	Output	L-channel analog current output +
$I_{OUT}L–$	26	Output	L-channel analog current output –
$I_{OUT}R+$	17	Output	R-channel analog current output +
$I_{OUT}R–$	18	Output	R-channel analog current output –
I_{REF}	20	—	Output current reference bias pin
LRCK	4	Input	Left and right clock (f_S) input(1)
MONO	1	Input	Monaural mode enable(1)
MUTE	10	Input	Mute control(1)
$\overline{RST}$	14	Input	Reset(1)
SCK	7	Input	System clock input(1)
$V_{CC}1$	23	—	Analog power supply, 5 V
$V_{CC}2L$	28	—	Analog power supply (L-channel DACFF), 5 V
$V_{CC}2R$	15	—	Analog power supply (R-cahnnel DACFF), 5 V
$V_{COM}L$	22	—	L-channel internal bias decoupling pin
$V_{COM}R$	21	—	R-channel internal bias decoupling pin
V_{DD}	9	—	Digital power supply, 3.3 V
ZERO	13	Output	Zero flag

(1) Schmitt-trigger input, 5-V tolerant

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	–0.3	6.5	V
	V_{DD}	–0.3	4	
Supply voltage differences: $V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$			±0.1	V
Ground voltage differences: AGND1, AGND2, AGND3L, AGND3R, DGND			±0.1	V
Digital input voltage	LRCK, DATA, BCK, SCK, FMT1, FMT0, MONO, CHSL, DEM, MUTE, $\overline{RST}$	–0.3	6.5	V
	ZERO	–0.3	(V_{DD} + 0.3 V) < 4	
Analog input voltage		–0.3	(V_{CC} + 0.3 V) < 6.5	V
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature			150	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD Digital supply voltage		3.0	3.3	3.6	V
VCC1	Analog supply voltage	4.7525	5	5.25	V
VCC2L					
VCC2R					
Operating temperature		–25		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		PCM1798 DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	
ψ_{JT}	Junction-to-top characterization parameter	3.1	
ψ_{JB}	Junction-to-board characterization parameter	31.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

All specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				24		Bits
DATA FORMAT						
	Audio data interface format			Standard, I^2S, left-justified		
	Audio data bit length			16-, 24-bit selectable		
	Audio data format			MSB first, 2s complement		
f_S	Sampling frequency		10		200	kHz
	System clock frequency			128, 192, 256, 384, 512, 768 f_S		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			VDC
V_{IL}					0.8	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –2 mA	2.4			VDC
V_{OL}		I_{OL} = 2 mA			0.4	
DYNAMIC PERFORMANCE(1)(2)						
	THD+N at VOUT = 0 dB	f_S = 44.1 kHz		0.0005%	0.001%	
		f_S = 96 kHz		0.00%		
		f_S = 192 kHz		0.0015%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	120	123		dB
		EIAJ, A-weighted, f_S = 96 kHz		123		
		EIAJ, A-weighted, f_S = 192 kHz		123		
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	120	123		dB
		EIAJ, A-weighted, f_S = 96 kHz		123		
		EIAJ, A-weighted, f_S = 192 kHz		123		
	Channel separation	f_S = 44.1 kHz	116	119		dB
		f_S = 96 kHz		118		
		f_S = 192 kHz		117		
	Level linearity error	V_{OUT} = –120 dB		±1		dB
DYNAMIC PERFORMANCE (MONO MODE)(1)(2)(3)						
	THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0005%		
		f_S = 96 kHz		0.001%		
		f_S = 192 kHz		0.0015%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		126		dB
		EIAJ, A-weighted, f_S = 96 kHz		126		
		EIAJ, A-weighted, f_S = 192 kHz		126		
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		126		dB
		EIAJ, A-weighted, f_S = 96 kHz		126		
		EIAJ, A-weighted, f_S = 192 kHz		126		

(1) Filter conditions:
THD+N: 20-Hz HPF, 20-kHz AES17 LPF
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(2) Dynamic performance and dc accuracy are specified at the output of the post amplifier as shown in Figure 32.
(3) Dynamic performance and dc accuracy are specified at the output of the measurement circuit as shown in Figure 33.

Electrical Characteristics (continued)

All specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2L = V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Gain error		–7	±2	7	% of FSR
	Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
	Bipolar zero error	At BPZ	–2	±0.5	2	% of FSR
	Output current	Full scale (0 dB)		4		mAp-p
	Center current	At BPZ		–3.5		mA
DIGITAL FILTER PERFORMANCE						
	De-emphasis error				±0.1	dB
FILTER CHARACTERISTICS–1: SHARP ROLLOFF						
		±0.0002 dB			0.454 f_S	
	Pass band	–3 dB			0.49 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple				±0.0002	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–98			dB
	Delay time			38/f_S		s
FILTER CHARACTERISTICS–2: SLOW ROLLOFF						
	Pass band	±0.001 dB			0.21 f_S	
		–3 dB			0.448 f_S	
	Stop band		0.79 f_S			
	Pass-band ripple				±0.001	dB
	Stop-band attenuation	Stop band = 0.732 fS	–80			dB
	Delay time			38/f_S		s
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		36	3.3	3.6	VDC
$V_{CC}1$						
$V_{CC}2L$			4.7525	5	5.25	
$V_{CC}2R$						
I_{DD}	Supply current(4)	f_S = 44.1 kHz		7	9	mA
		f_S = 96 kHz		13		
		f_S = 192 kHz		25		
I_{CC}		f_S = 44.1 kHz		18	23	mA
		f_S = 96 kHz		19		
		f_S = 192 kHz		20		
	Power dissipation(4)	f_S = 44.1 kHz		115	150	mW
		f_S = 96 kHz		140		
		f_S = 192 kHz		180		
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C

(4) Input is BPZ data.

6.6 Timing Requirements

		MIN	MAX	UNIT
SYSTEM CLOCK INPUT TIMING				
$t_{(SCY)}$	System clock pulse cycle time	13		ns
$t_{(SCKH)}$	System clock pulse duration, HIGH	$0.4t_{(SCY)}$		ns
$t_{(SCKL)}$	System clock pulse duration, LOW	$0.4t_{(SCY)}$		ns
EXTERNAL RESET TIMING				
$t_{(RST)}$	Reset pulse duration, Low	20		ns
TIMING OF AUDIO INTERFACE				
$t_{(BCY)}$	BCK pulse cycle time	70		ns
$t_{(BCL)}$	BCK pulse duration, LOW	30		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	30		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns
	LRCK clock data	50% ± 2 bit clocks		
AUDIO INTERFACE TIMING FOR EXTERNAL DIGITAL FILTER				
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(BCL)}$	BCK pulse duration, LOW	7		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA setup time	5		ns
$t_{(DH)}$	DATA hold time	5		ns

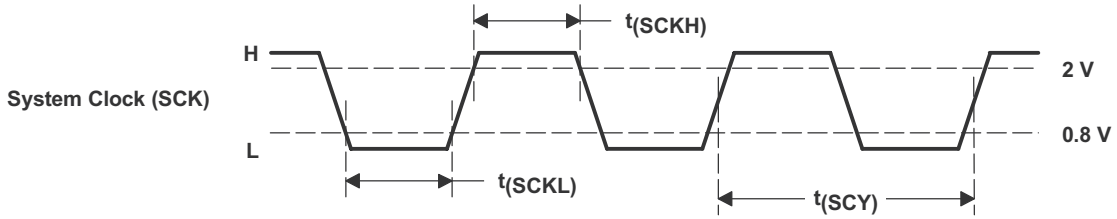


Figure 1. System Clock Input Timing

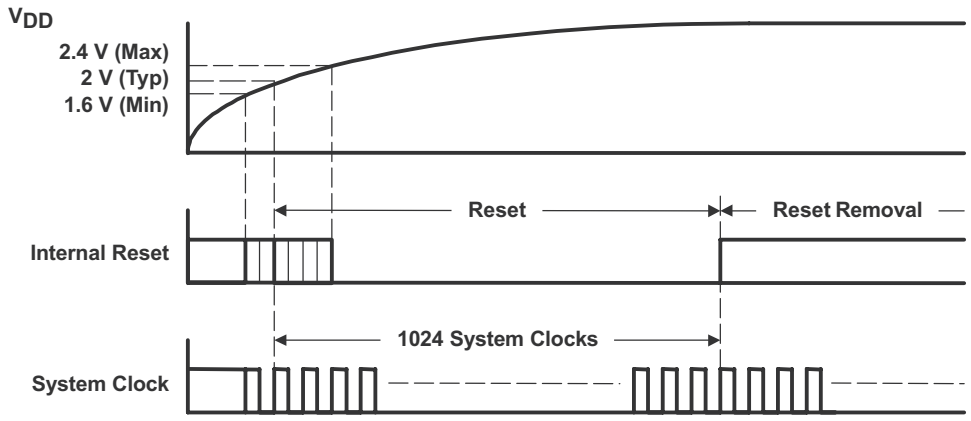


Figure 2. Power-On Reset Timing

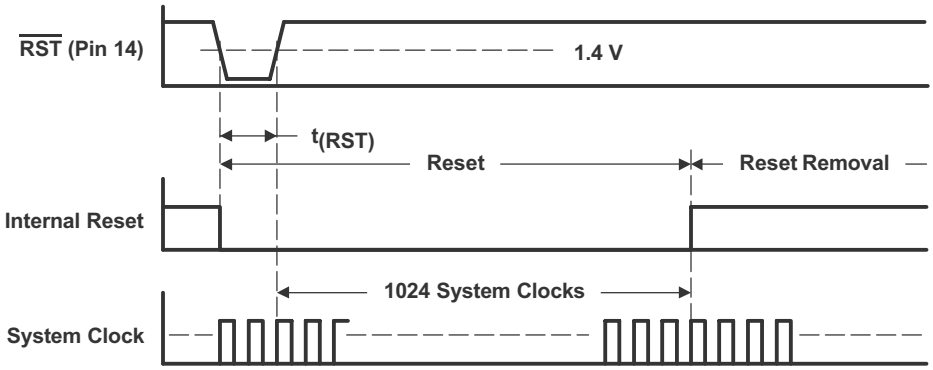


Figure 3. External Reset Timing

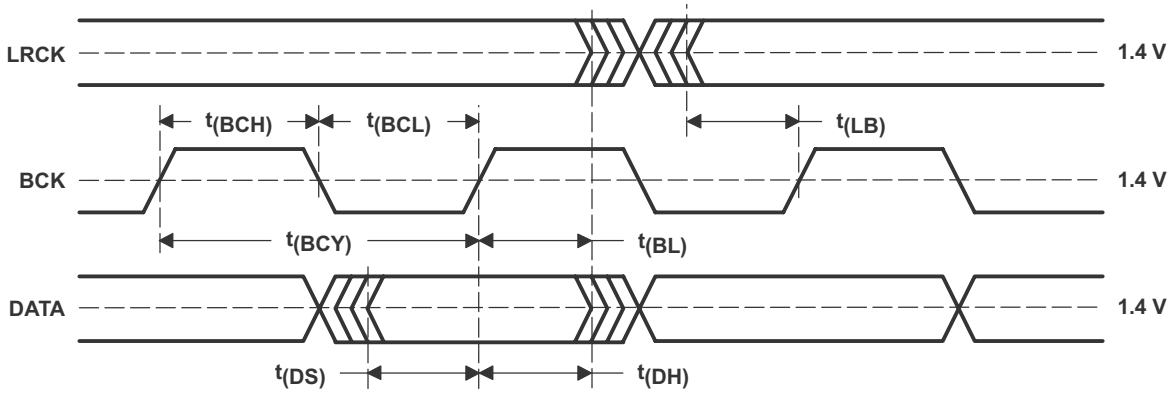
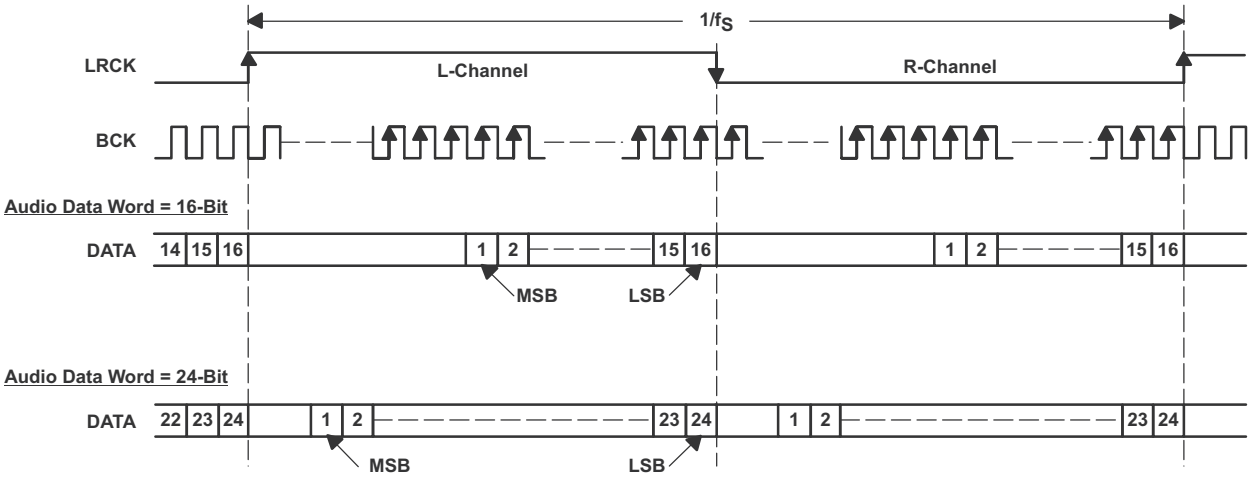
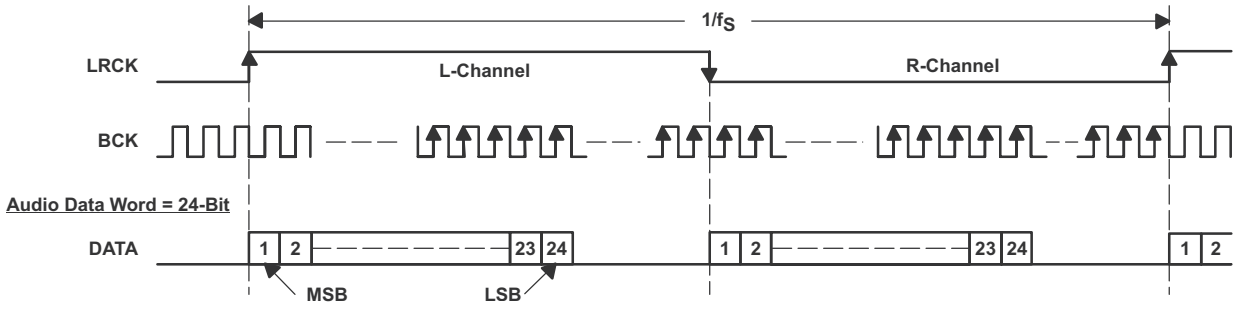


Figure 4. Timing of Audio Interface



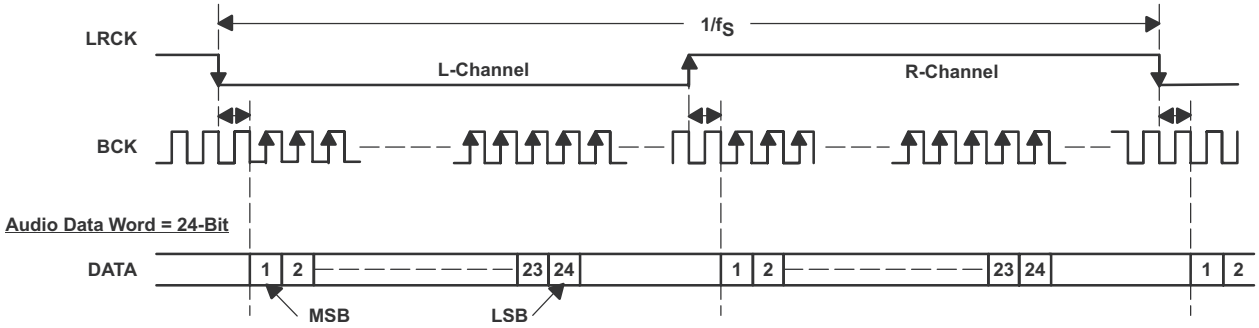
(1) Standard Data Format (Right-Justified); L-Channel = HIGH, R-Channel = LOW

Figure 5. Auto Data Input Format (1 of 3)



(2) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

Figure 6. Auto Data Input Format (2 of 3)



(3) I^2S Data Format; L-Channel = LOW, R-Channel = HIGH

Figure 7. Auto Data Input Format (3 of 3)

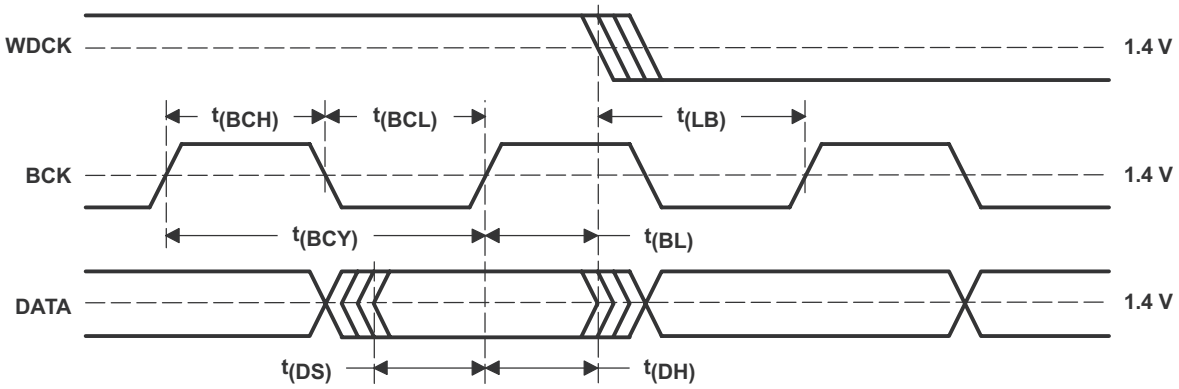
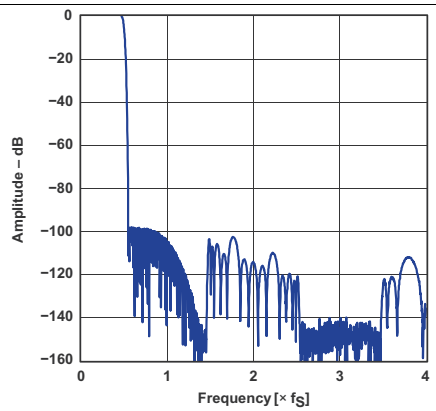


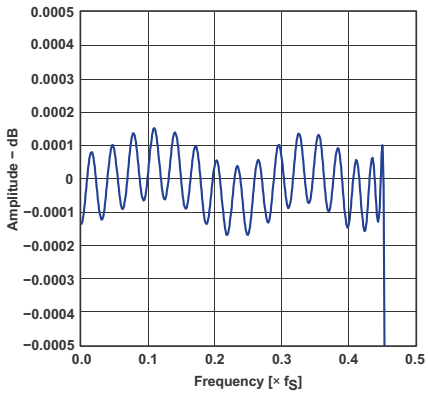
Figure 8. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

6.7 Typical Characteristics for Digital Filter



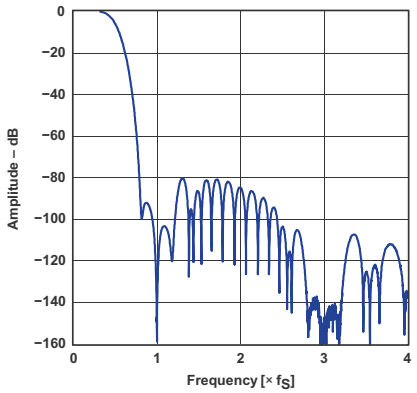
Frequency Response, Sharp Rolloff

Figure 9. Amplitude vs Frequency



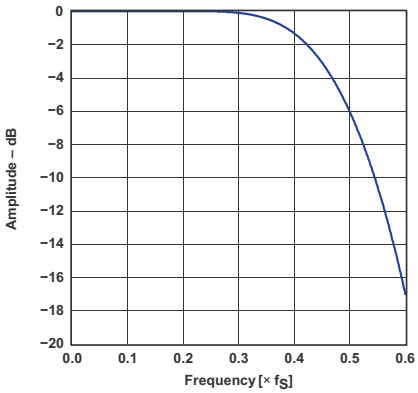
Pass-Band Ripple, Sharp Rolloff

Figure 10. Amplitude vs Frequency



Frequency Response, Slow Rolloff

Figure 11. Amplitude vs Frequency



Transition Characteristics, Slow Rolloff

Figure 12. Amplitude vs Frequency

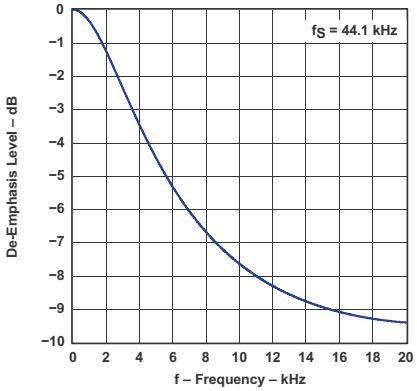


Figure 13. De-emphasis Level vs Frequency

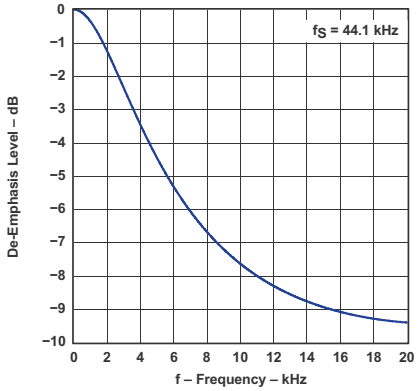
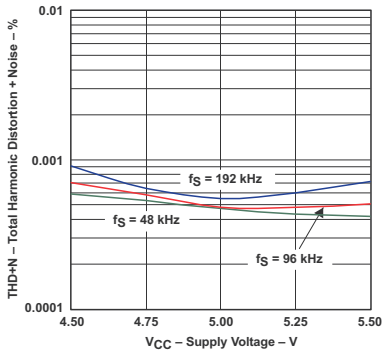


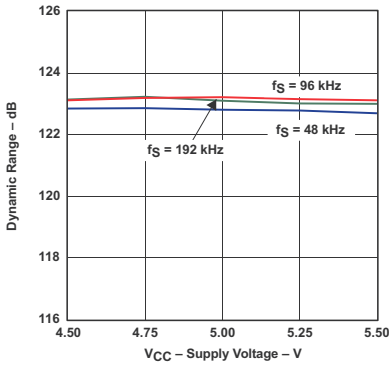
Figure 14. De-emphasis Error vs Frequency

6.7.1 Analog Dynamic Performance



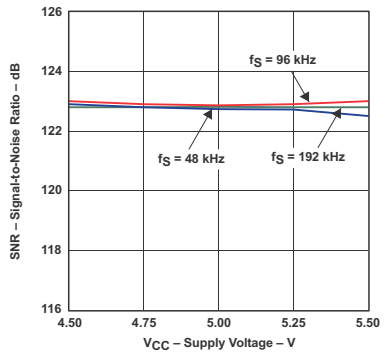
NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 32.

Figure 15. Total Harmonic Distortion + Noise vs Supply Voltage



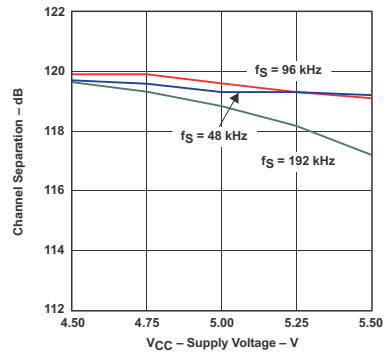
NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 32.

Figure 16. Dynamic Range vs Supply Voltage



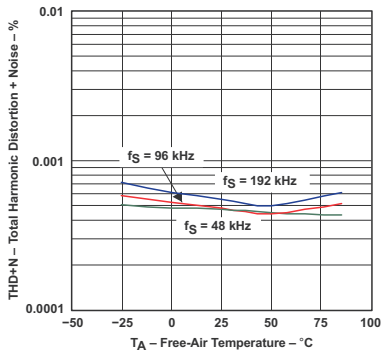
NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 32.

Figure 17. Signal-to-Noise Ratio vs Supply Voltage



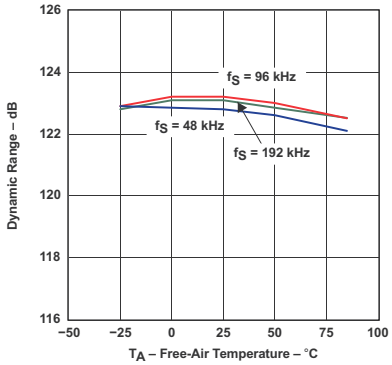
NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 32.

Figure 18. Channel Separation vs Supply Voltage



NOTE: PCM mode, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

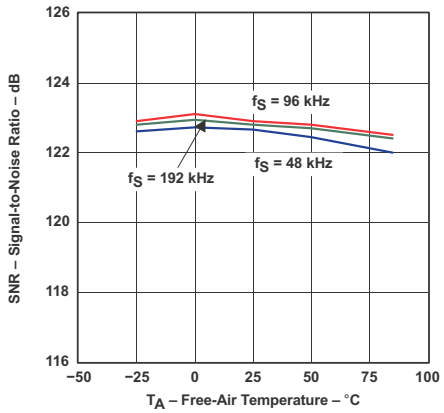
Figure 19. Total Harmonic Distortion + Noise vs Free-air Temperature



NOTE: PCM mode, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

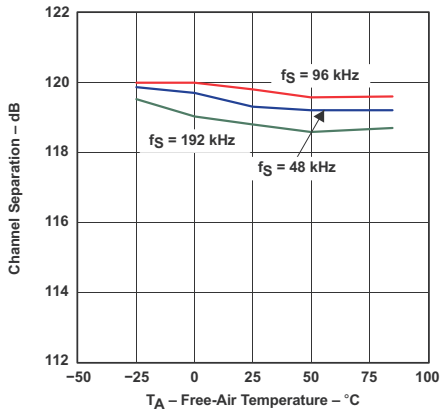
Figure 20. Dynamic Range vs Free-air Temperature

Analog Dynamic Performance (continued)



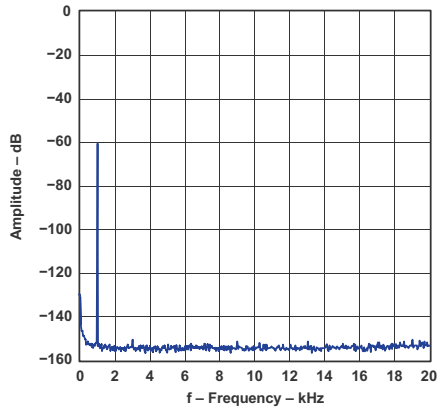
NOTE: PCM mode, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

Figure 21. Signal-to-noise Ratio vs Free-air Temperature



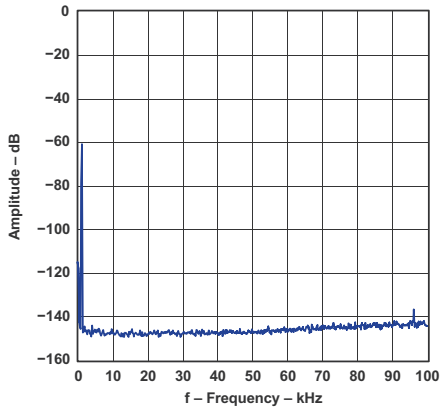
NOTE: PCM mode, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

Figure 22. Channel Separation vs Free-air Temperature



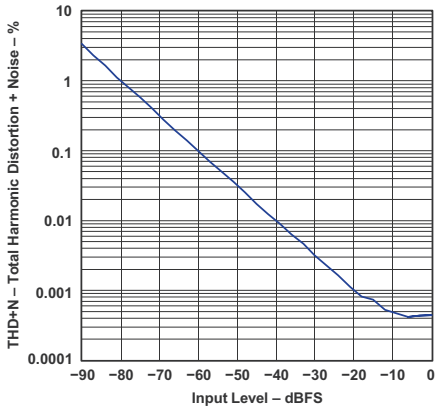
NOTE: f_S = 48 kHz, 32768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

Figure 23. Amplitude vs Frequency



NOTE: f_S = 96 kHz, 32768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

Figure 24. Amplitude vs Frequency



NOTE: f_S = 48 kHz, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 32.

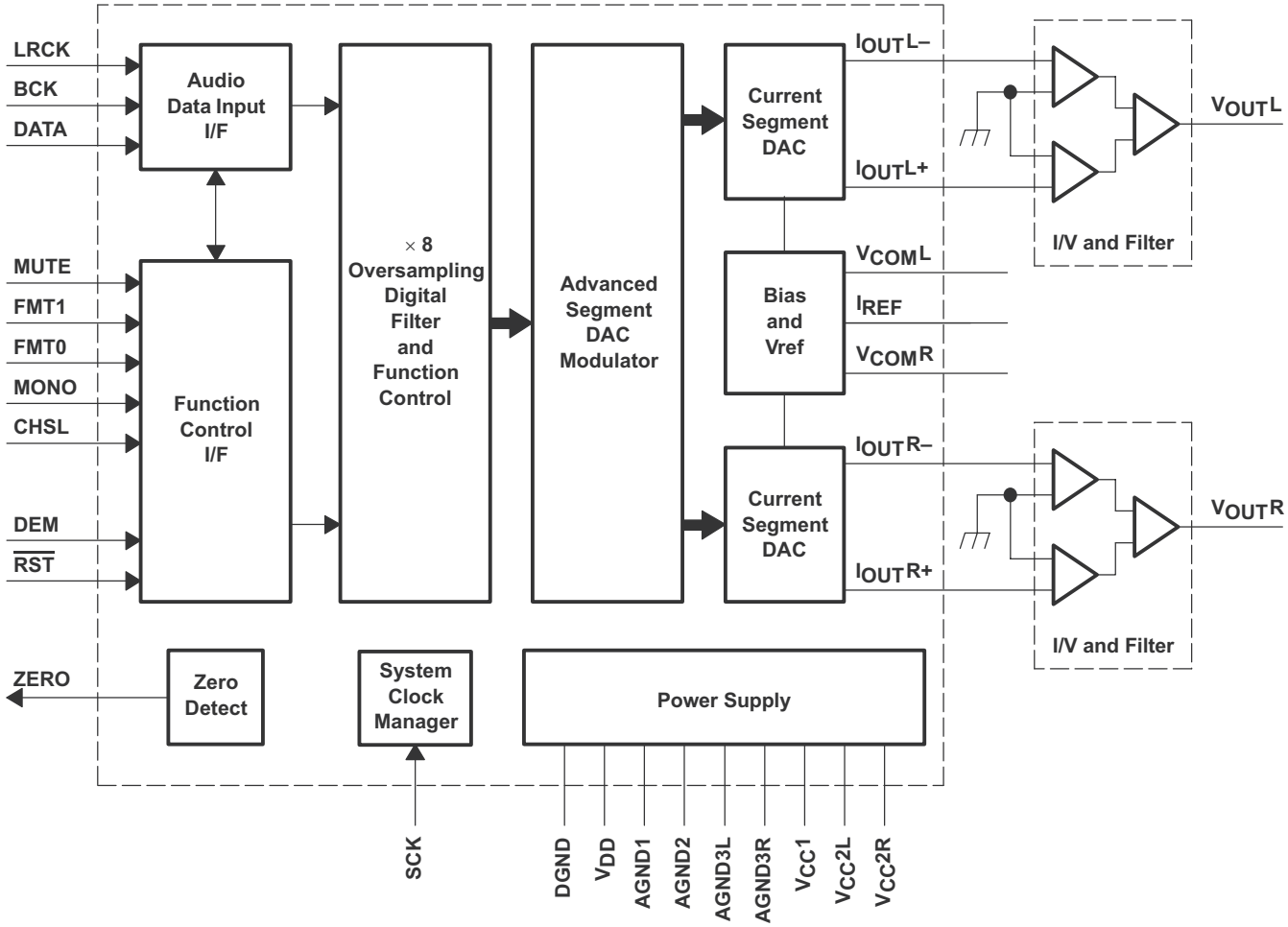
Figure 25. Total Harmonic Distortion + Noise vs Input Level

7 Detailed Description

7.1 Overview

The PCM1798 is a 24-bit, 192-kHz, differential current output DAC that comes in a 28-pin SSOP package. The PCM1798 is a hardware controlled and utilizes the advanced segment DAC architecture from TI in order to perform with a Stereo Dynamic Range of 123 dB (126 dB Mono) and SNR of 123 dB (126 dB Mono) with a THD of 0.0005%. The PCM1798 will use the SCK input as its system clock and automatically detect the sampling rate of the Digital Audio input and has a high tolerance for clock jitter. The internal filter can be bypassed to allow for an external digital filter to be used.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 System Clock and Reset Functions

7.3.1.1 System Clock Input

The PCM1798 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1798 has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Feature Description (continued)

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments PLL1700 family of multiclock generators is an excellent choice for providing the PCM1798 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (fSCK) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	See (1)	See (1)

(1) This system clock rate is not supported for the given sampling frequency.

7.3.2 Power-On and External Reset Functions

The PCM1798 includes a power-on reset function. Figure 2 shows the operation of this function. With V_{DD} > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V.

The PCM1798 also includes an external reset capability using the $\overline{RST}$ input (pin 14). This allows an external controller or master reset circuit to force the PCM1798 to initialize to its default reset state.

Figure 3 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1798 power up and system clock activation.

7.3.3 Audio Data Interface

7.3.3.1 Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1798 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1798 requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ±6 BCK, internal operation is initialized within $1/f_S$ and the analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

7.3.3.2 PCM Audio Data Formats and Timing

The PCM1798 supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 5, Figure 6, and Figure 7. Data formats are selected using FMT0 (pin 11) and FMT1 (pin 12) as shown in Table 2. All formats require binary twos-complement, MSB-first audio data. Figure 4 shows a detailed timing diagram for the serial audio interface.

7.3.4 Function Descriptions

7.3.4.1 Audio Data Format

Audio format is selected using FMT0 (pin 11) and FMT1 (pin 12). The PCM1798 also supports monaural mode and DF bypass mode using MONO (pin 1) and CHSL (pin 2). The PCM1798 can select the DF rolloff characteristics.

Table 2. Audio Data Format Select

MONO	CHSL	FMT1	FMT0	FORMAT	STEREO/MONO	DF ROLLOFF
0	0	0	0	I^2S	Stereo	Sharp
0	0	0	1	Left-justified format	Stereo	Sharp
0	0	1	0	Standard, 16-bit	Stereo	Sharp
0	0	1	1	Standard, 24-bit	Stereo	Sharp
0	1	0	0	I^2S	Stereo	Slow
0	1	0	1	Left-justified format	Stereo	Slow
0	1	1	0	Standard, 16-bit	Stereo	Slow
0	1	1	1	Digital filter bypass	Mono	—
1	0	0	0	I^2S	Mono, L-channel	Sharp
1	0	0	1	Left-justified format	Mono, L-channel	Sharp
1	0	1	0	Standard, 16-bit	Mono, L-channel	Sharp
1	0	1	1	Standard, 24-bit	Mono, L-channel	Sharp
1	1	0	0	I^2S	Mono, R-channel	Sharp
1	1	0	1	Left-justified format	Mono, R-channel	Sharp
1	1	1	0	Standard, 16-bit	Mono, R-channel	Sharp
1	1	1	1	Standard, 24-bit	Mono, R-channel	Sharp

7.3.4.2 Soft Mute

The PCM1798 supports mute operation. When MUTE (pin 10) is set to HIGH, both analog outputs are transitioned to the bipolar zero level in –0.5-dB steps with a transition speed of $1/f_S$ per step. This system provides pop-free muting of the DAC output.

7.3.4.3 De-Emphasis

The PCM1798 has a de-emphasis filter for the sampling frequency of 44.1 kHz. The de-emphasis filter is controlled using DEM (pin 3).

7.3.4.4 Zero Detection

When the PCM1798 detects that the audio input data in the L-channel and the R-channel is continuously zero for 1024 LRCKs in the PCM mode, or that the audio input data is continuously zero for 1024 WDCKs in the external filter mode, the PCM1798 sets ZERO (pin 13) to HIGH.

7.4 Device Functional Modes

The PCM1798 is a hardware controlled device. The pins CHSL, DEM, FMT0, FMT1, MONO, and MUTE control the functionality of this part. See the Pin Functions table or the Feature Description section for more detail.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1798 device is a hardware-controlled, differential current output DAC that can accept multiple formats of 16- or 24-bit PCM audio data. Because the PCM1798 is a current output part, in most cases a current to voltage stage is required before the signal is passed to the amplifier stage. A microcontroller or DSP can use GPIO to manipulate the control pins CHSL, DEM, FMT0, FMT1, MONO, and MUTE. The PCM1798 requires a 5-V analog supply, as well as a 3.3-V digital supply.

8.2 Typical Applications

8.2.1 Application for External Digital Filter Interface

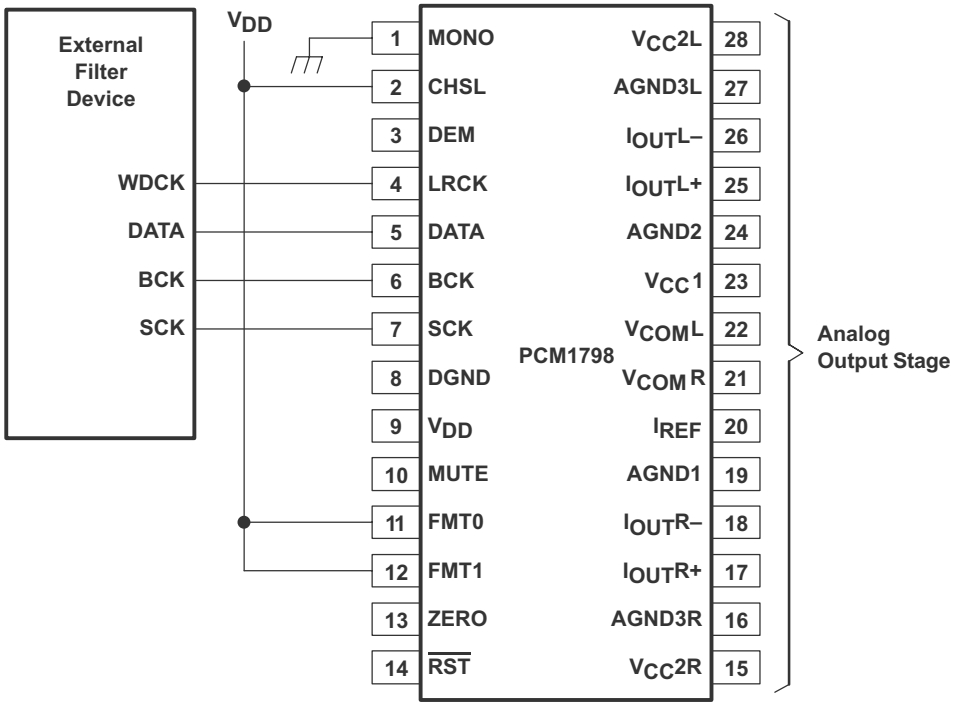


Figure 26. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application

8.2.1.1 Design Requirements

- Control: Host controller with SPI communication
- Audio Output: I/V output circuitry
- Audio Input: Digital Audio Filter with I2S or DSD output

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use a programmable digital signal processor as an external digital filter to perform the interpolation function. The following pin settings enable the external digital filter application mode.

Typical Applications (continued)

- MONO (pin 1) = LOW
- CHSL (pin 2) = HIGH
- FMT0 (pin 11) = HIGH
- FMT1 (pin 12) = HIGH

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 26. The word clock (WDCK) must be operated at 8× or 4× the desired sampling frequency, f_S.

Pin assignment when using the external digital filter interface:

- LRCK (pin 4): WDCK as word clock input
- DATA (pin 5): Monaural audio data input
- BCK (pin 6): Bit clock input

8.2.1.2.2 Audio Format

The PCM1798 in the external digital filter interface mode supports the 24-bit right-justified audio format as shown in Figure 27.

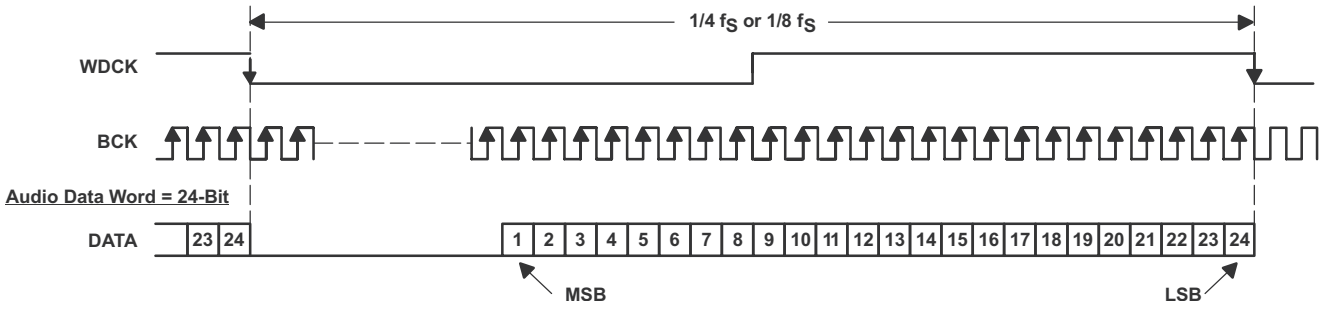


Figure 27. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application

8.2.1.2.3 Analog Output

Table 3 and Figure 28 show the relationship between the digital input code and analog output.

Table 3. Analog Output Current and Voltage(1)

	800000 (–FS)	000000 (BPZ)	7FFFFF (+FS)
$I_{OUT}N$ [mA]	–1.5	–3.5	–5.5
$I_{OUT}P$ [mA]	–5.5	–3.5	–1.5
$V_{OUT}N$ [V]	–1.23	–2.87	–4.51
$V_{OUT}P$ [V]	–4.51	–2.87	–1.23
V_{OUT} [V]	–2.98	0	2.98

(1) $V_{OUT}N$ is the output of U1, $V_{OUT}P$ is the output of U2, and V_{OUT} is the output of U3 in the measurement circuit of Figure 23.

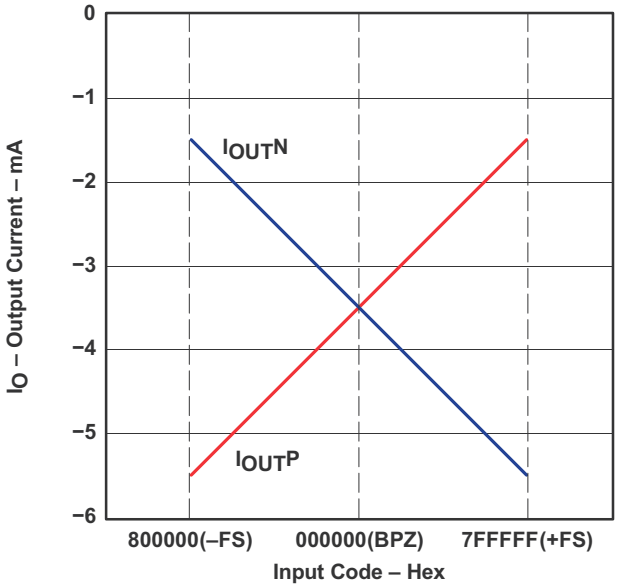
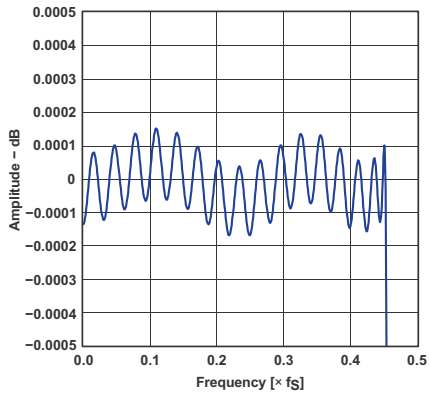


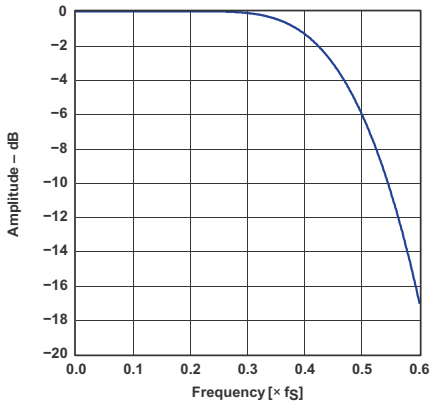
Figure 28. Relationship Between Digital Input and Analog Output

8.2.1.3 Application Curves



Pass-Band Ripple, Sharp Rolloff

Figure 29. Amplitude vs Frequency



Transition Characteristics, Slow Rolloff

Figure 30. Amplitude vs Frequency

8.2.2 PCM1798 Typical Application

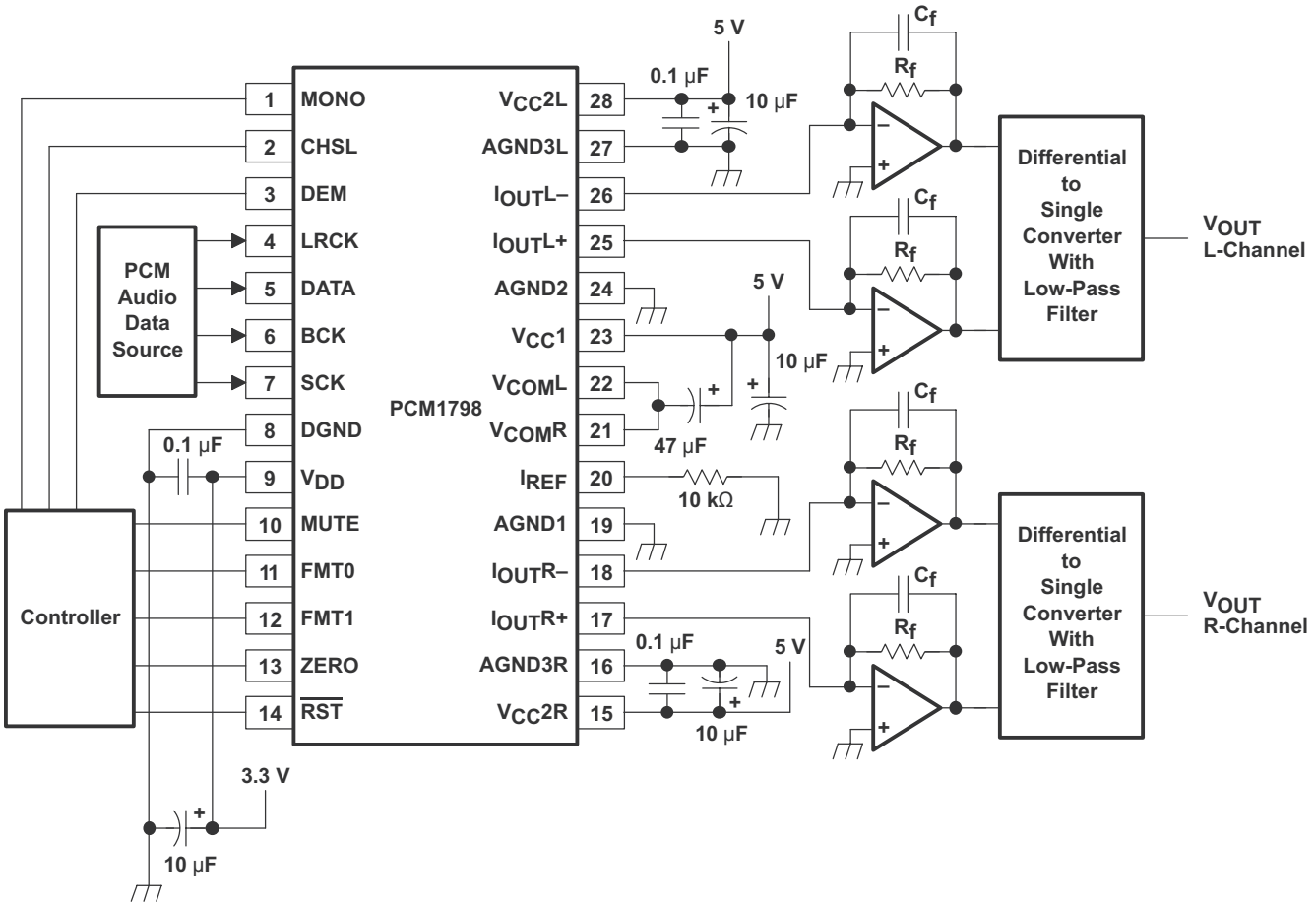


Figure 31. Typical Application Circuit

8.2.2.1 Design Requirements

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1798 is capable. This is because noise and distortion that are generated in an application circuit are not negligible.

In the third-order LPF circuit of Figure 32, the output level is 2.1 V RMS, and 123 dB S/N is achieved.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 I/V Section

The current of the PCM1798 on each of the output pins ($I_{OUT}L+$, $I_{OUT}L–$, $I_{OUT}R+$, $I_{OUT}R–$) is 4 mA p-p at 0 dB (full scale). The voltage output level of the I/V converter (Vi) is given by following equation:

$$V_I = 4\ mAp–p \times R_f\ (R_f : \text{feedback resistance of I/V converter}) \quad (1)$$

TI recommends an NE5534 operational amplifier for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

8.2.2.2.2 Differential Section

The PCM1798 voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the differential circuit is the low-noise type.

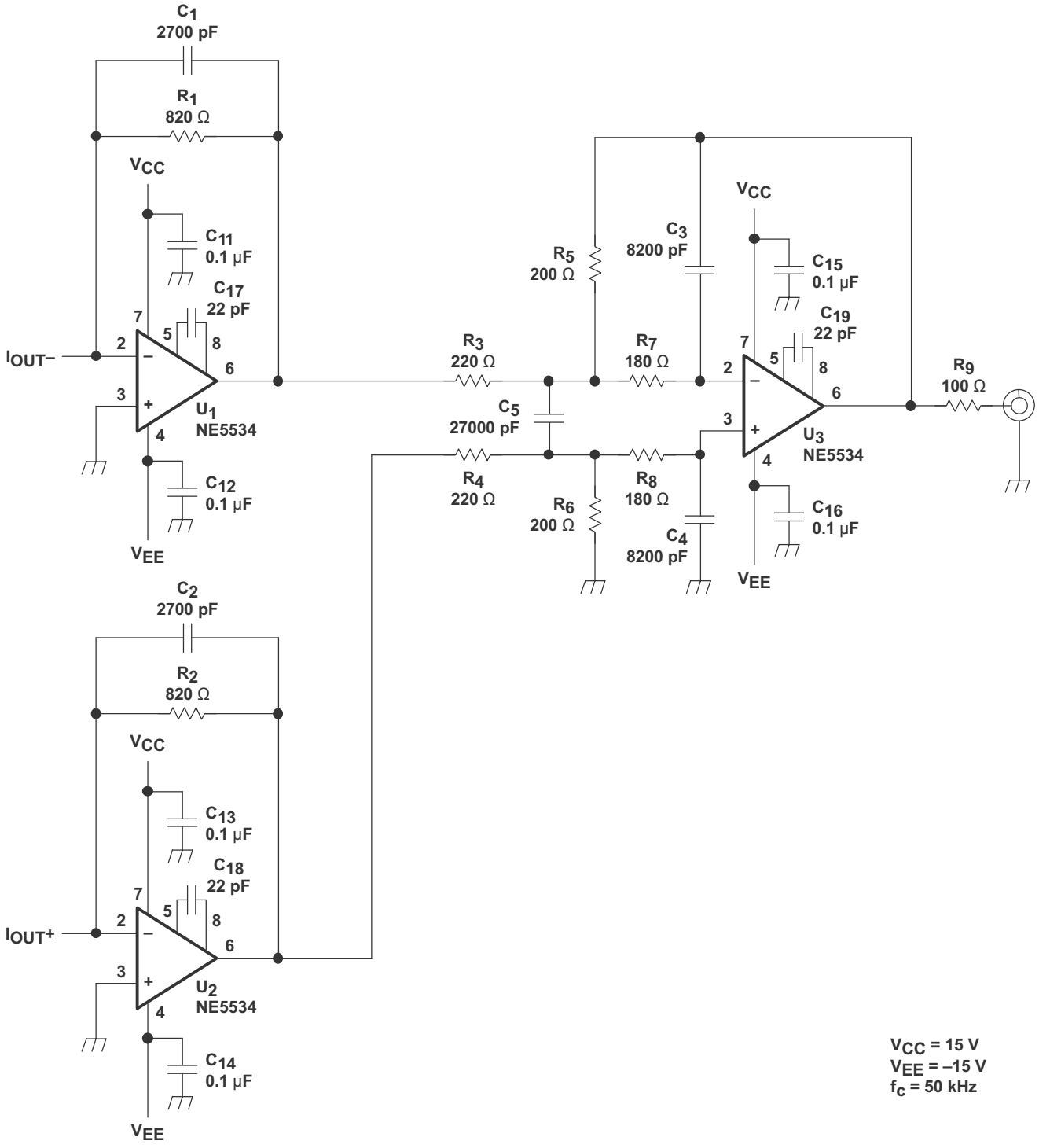


Figure 32. Measurement Circuit

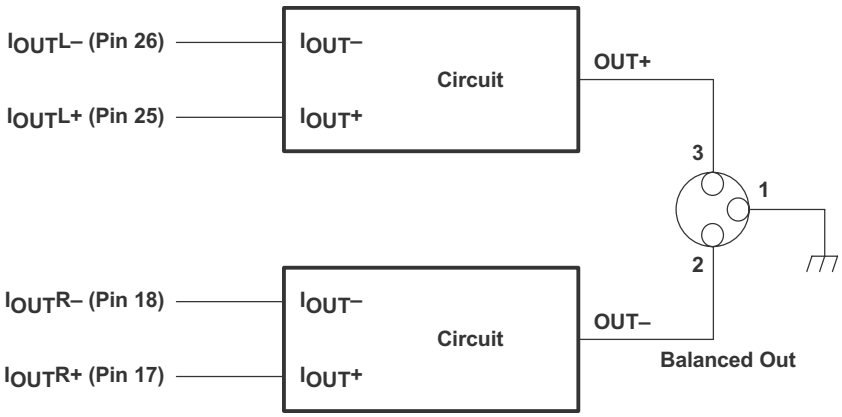


Figure 33. Measurement Circuit for Monaural Mode

9 Power Supply Recommendations

The PCM1798 requires a 5-V nominal supply and a 3.3-V nominal supply. The 5-V supply is for the analog circuitry powered by pins VCC1, VCC2L, and VCC2R pins. The 3.3-V supply is for the digital circuitry powered by the Vdd pin. The decoupling capacitors for the power supplies should be placed close to the device terminals.

10 Layout

10.1 Layout Guidelines

Designers should try to use the same ground between AGND and DGND to avoid any potential voltage difference between them. Ensure that the return currents for digital signals will avoid the AGND pin or the input signals to the I/V stage. Avoid running high frequency clock and control signals near AGND, or any of the Vout pins where possible. The pin layout of the PCM1798 partitions into two parts - analog section and digital section. Providing the system is partitioned in such a way that digital signals are routed away from the analog sections, then no digital return currents (for example, clocks) should be generated in the analog circuitry.

- Decoupling capacitors should be placed as close to the $V_{CC}1$, $V_{CC}2L$, $V_{CC}R2$, $V_{COM}L$, $V_{COM}R$, and V_{DD} pins as possible.
- Further guidelines can be found in Figure 34.

10.2 Layout Example

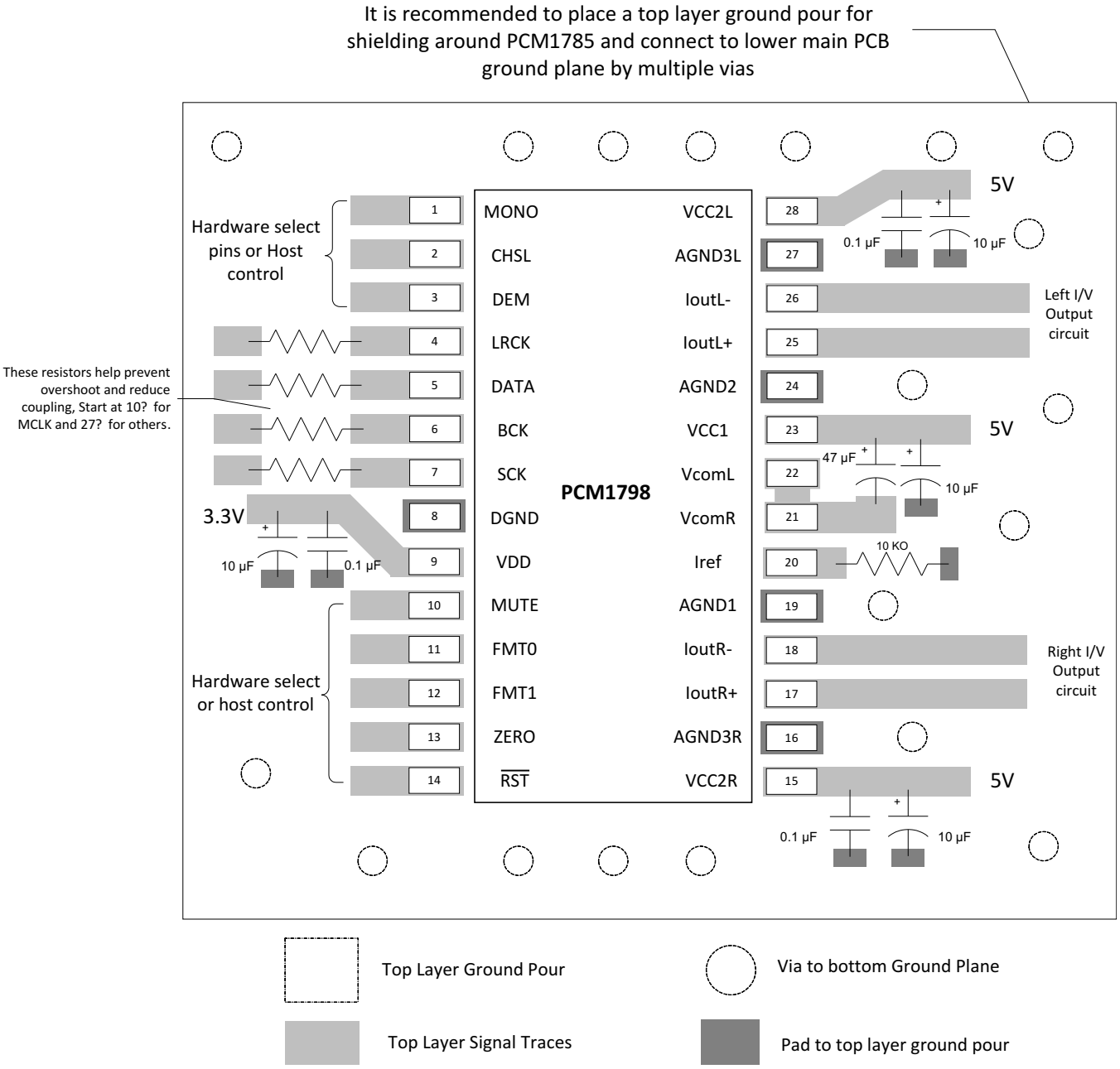


Figure 34. PCM1785 Layout Example

11 Device and Documentation Support

11.1 Trademarks

System Two, Audio Precision are trademarks of Audio Precision, Inc.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1798DB	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1798
PCM1798DB.B	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1798
PCM1798DBG4	Active	Production	SSOP (DB) | 28	47 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1798
PCM1798DBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1798
PCM1798DBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1798

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

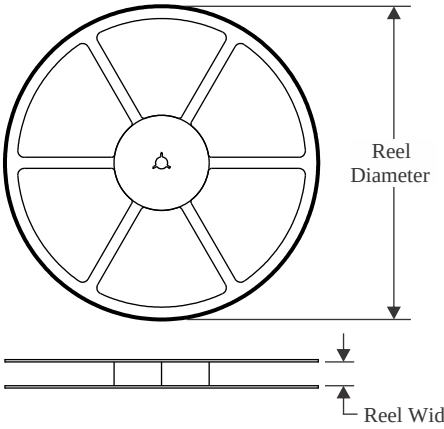
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

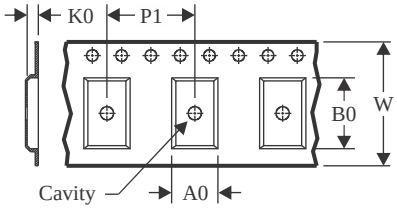
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

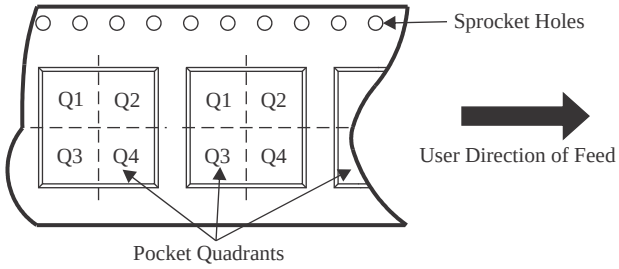


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

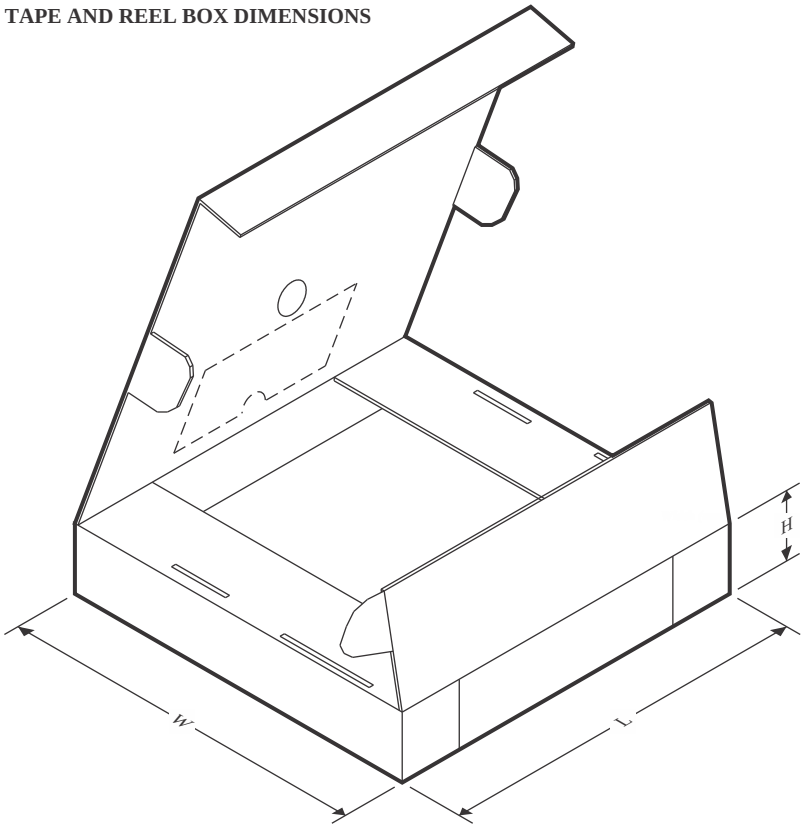
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1798DBR	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

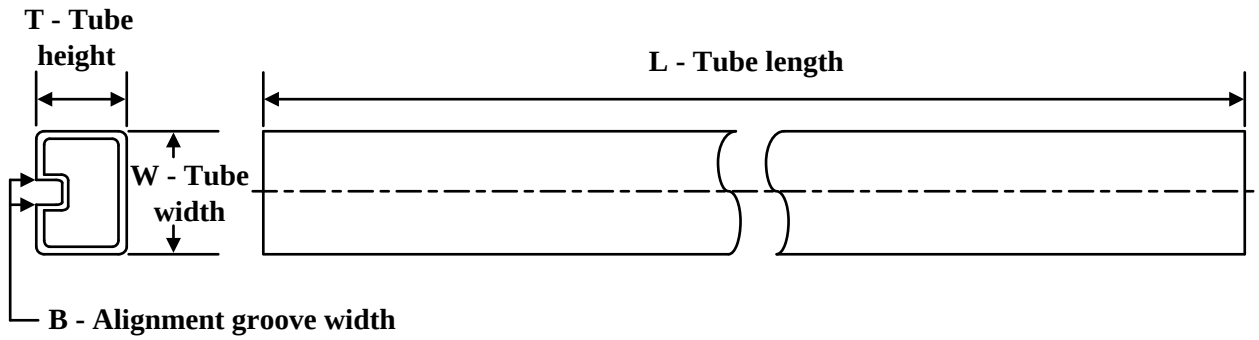
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1798DBR	SSOP	DB	28	2000	336.6	336.6	28.6

TUBE



*All dimensions are nominal

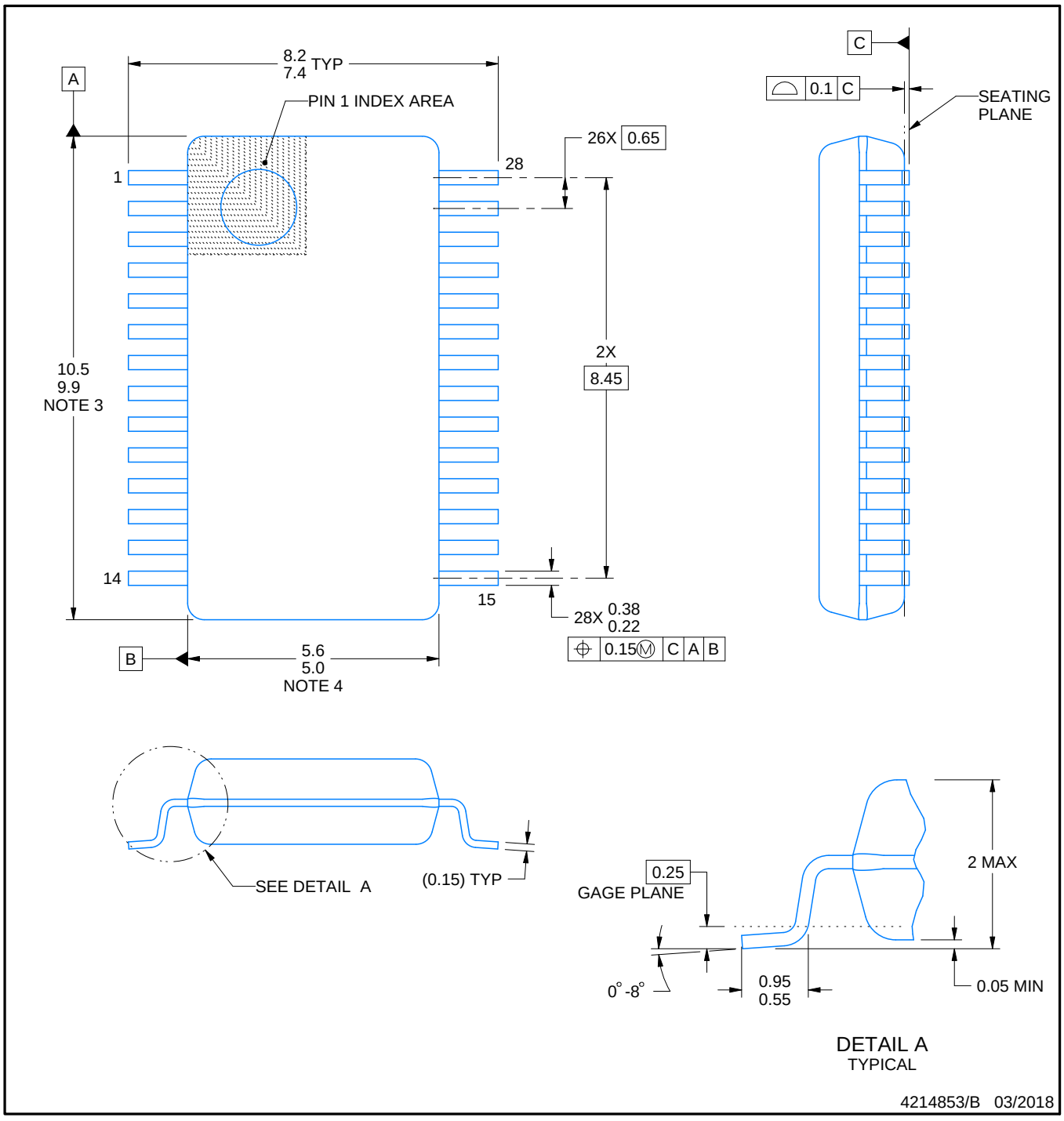
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1798DB	DB	SSOP	28	47	500	10.6	500	9.6
PCM1798DB.B	DB	SSOP	28	47	500	10.6	500	9.6
PCM1798DBG4	DB	SSOP	28	47	500	10.6	500	9.6

PACKAGE OUTLINE

DB0028A

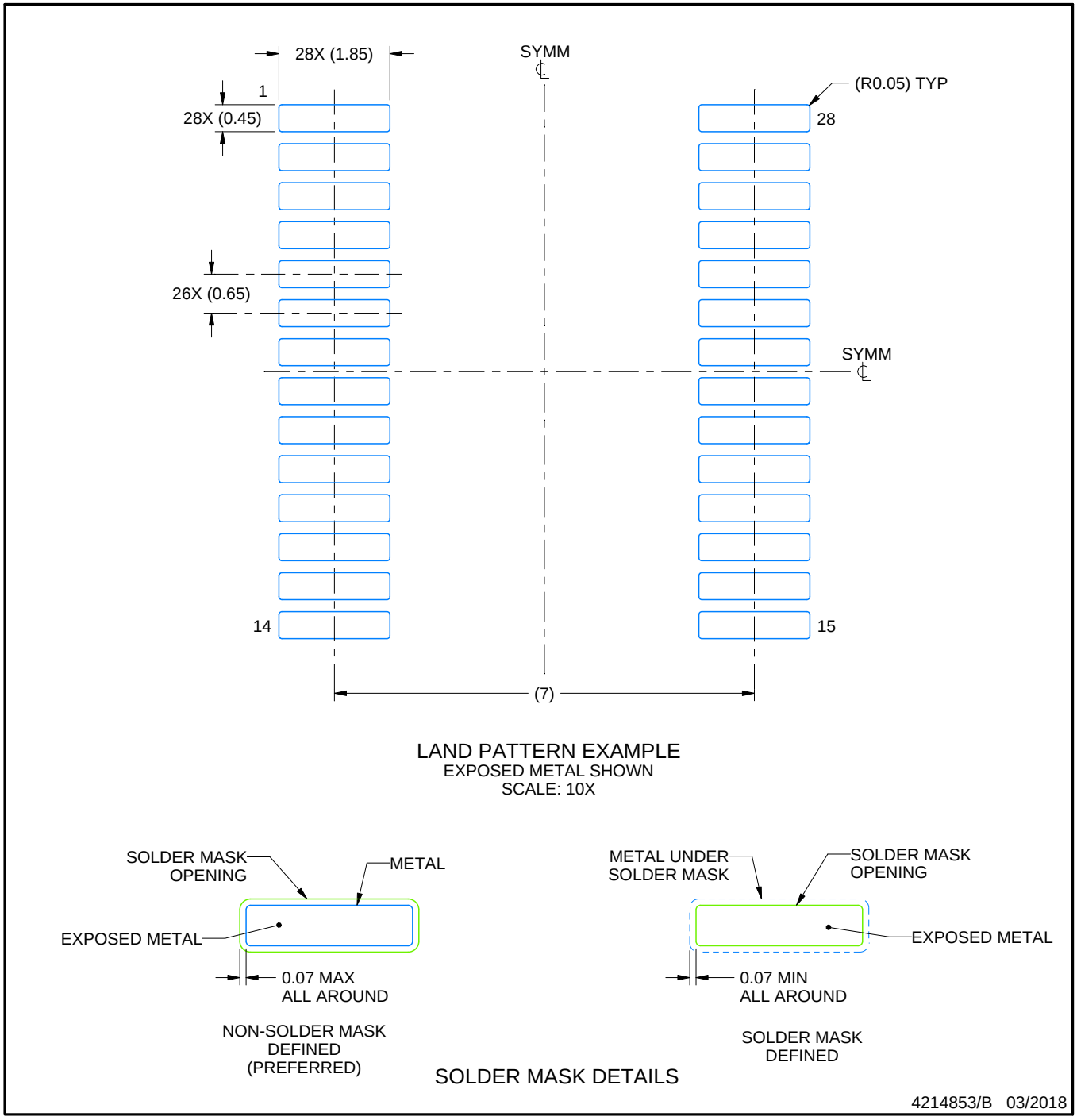
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



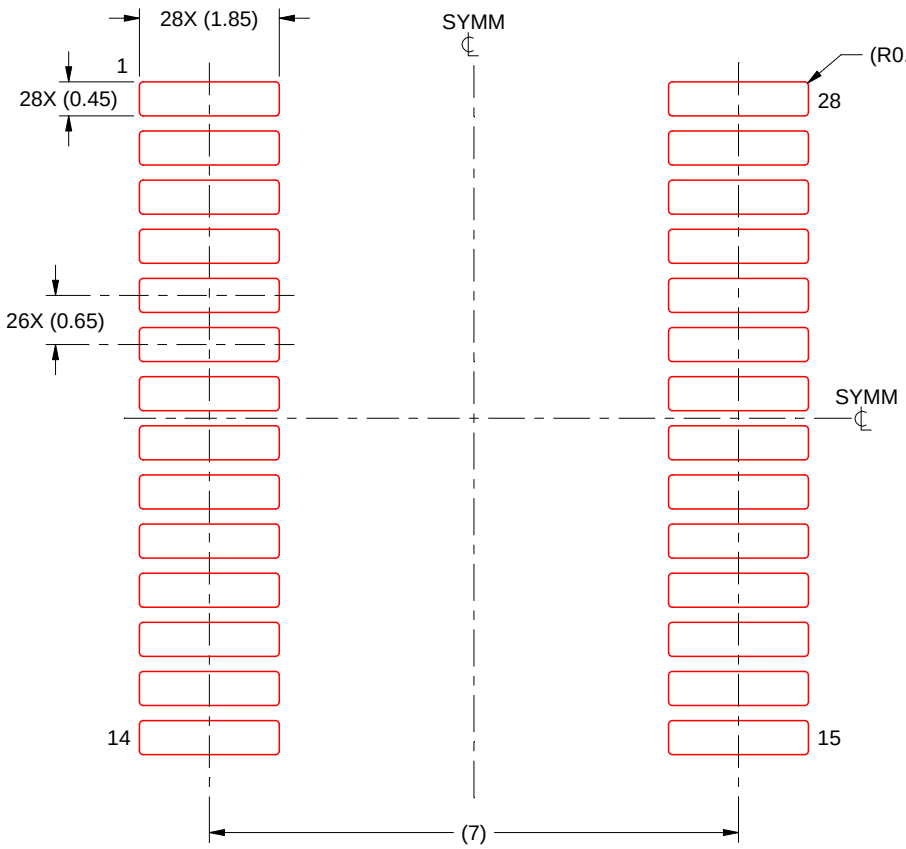
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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