SN74ALVC164245 16-Bit 2.5-V to 3.3-V or 3.3-V to 5-V Level-Shifting Transceiver With 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Maximum t_{pd} of 5.8 ns at 3.3 V
- ±24-mA Output Drive at 3.3 V
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Electronic Points of Sale
- Printers and Other Peripherals
- Motor Drives
- Wireless and Telecom Infrastructures
- Wearable Health and Fitness Devices

3 Description

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has V_{CCB}, which is set to operate at 3.3 V and 5 V. A port has V_{CCA}, which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses. The control circuitry (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) is powered by V_{CCA}.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

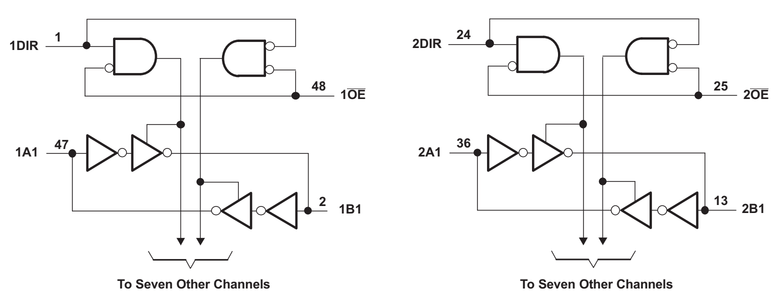
The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74ALVC164245	TSSOP (48)	12.50 mm × 6.10 mm
	SSOP (48)	15.88 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm
	BGA MICROSTAR JUNIOR (54)	8.00 mm × 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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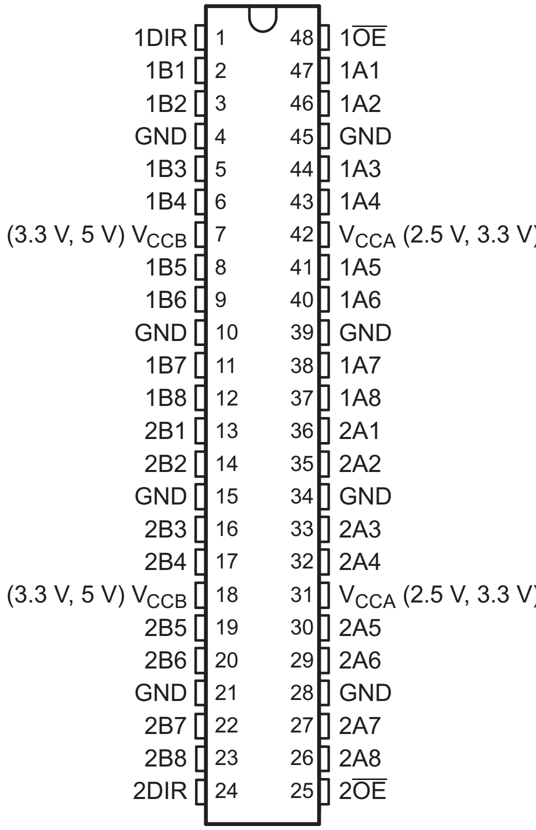
4 Revision History

Changes from Revision P (November 2005) to Revision Q	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see POA at the end of the data sheet	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	8

5 Pin Configuration and Functions

DGG and DL Packages
48-Pin TSSOP and BGA MICROSTAR JUINIOR
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1DIR	—	Direction Pin 1
2	1B1	I/O	1B1 input or output
3	1B2	I/O	1B2 input or output
4	GND	—	Ground pin
5	1B3	I/O	1B3 input or output
6	1B4	I/O	1B4 input or output
7	V_{CCB} (3.3 V, 5 V)	—	Power pin
8	1B5	I/O	1B5 input or output
9	1B6	I/O	1B6 input or output
10	GND	—	Ground pin
11	1B7	I/O	1B7 input or output
12	1B8	I/O	1B8 input or output
13	2B1	I/O	2B1 input or output
14	2B2	I/O	2B2 input or output
15	GND	—	Ground pin
16	2B3	I/O	2B3 input or output

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
17	2B4	I/O	2B4 input or output
18	V_{CCB} (3.3 V, 5 V)	—	Power pin
19	2B5	I/O	2B5 input or output
20	2B6	I/O	2B6 input or output
21	GND	—	Ground pin
22	2B7	I/O	2B7 input or output
23	2B8	I/O	2B8 input or output
24	2DIR	—	Direction pin 2
25	$2\overline{OE}$	I	Output Enable 2
26	2A8	I/O	2A8 input or output
27	2A7	I/O	2A7 input or output
28	GND	—	Ground pin
29	2A6	I/O	2A6 input or output
30	2A5	I/O	2A5 input or output
31	V_{CCA} (2.5 V, 3.3 V)	—	Power pin
32	2A4	I/O	2A4 input or output
33	2A3	I/O	2A3 input or output
34	GND	—	Ground pin
35	2A2	I/O	2A2 input or output
36	2A1	I/O	2A1 input or output
37	1A8	I/O	1A8 input or output
38	1A7	I/O	1A7 input or output
39	GND	—	Ground pin
40	1A6	I/O	1A6 input or output
41	1A5	I/O	1A5 input or output
42	V_{CCA} (2.5 V, 3.3 V)	—	Power pin
43	1A4	I/O	1A4 input or output
44	1A3	I/O	1A3 input or output
45	GND	—	Ground pin
46	1A2	I/O	1A2 input or output
47	1A1	I/O	1A1 input or output
48	$1\overline{OE}$	I	Output Enable 1

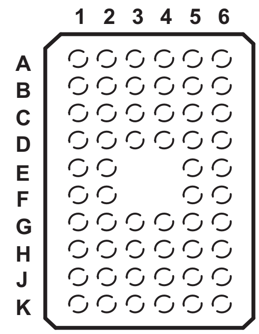


Table 1. Pin Assignments(1) (56-Ball GQL or ZQL Package)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{\text{OE}}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7	—	—	1A7	1A8
F	2B1	2B2	—	—	2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{\text{OE}}$

(1) NC – No internal connection

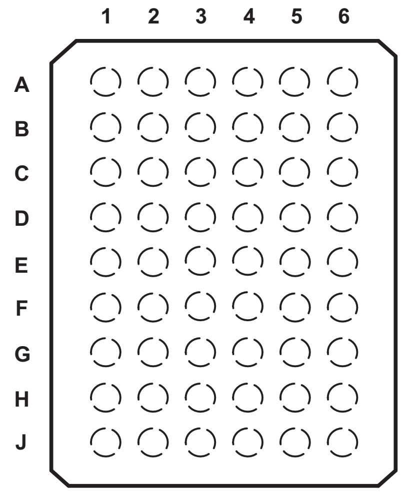


Table 2. Pin Assignments(1) (54-Ball GRD or ZRD Package)

	1	2	3	4	5	6
A	1B1	NC	1DIR	1$\overline{OE}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V_{CCB}	V_{CCA}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V_{CCB}	V_{CCA}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2$\overline{OE}$	NC	2A8

(1) NC – No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CCA}	–0.5	4.6	V
		V_{CCB}	–0.5	6	
V_I	Input voltage	Except I/O ports(2)	–0.5	6	V
		I/O port A(3)	–0.5	V_{CCA} + 0.5	
		I/O port B(2)	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) This value is limited to 4.6 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions: V_{CCB} at 3.3 V

for V_{CCB} at 3.3 V and 5 V(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		3	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage	V_{CCB} = 3 V to 3.6 V		0.7	V
		V_{CCB} = 4.5 V to 5.5 V		0.8	
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. see the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Recommended Operating Conditions: V_{CCA} at 2.5 V

for V_{CCA} at 2.5 V and 3.3 V(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 2.3 V to 2.7 V	1.7		V
		V_{CCA} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CCA} = 2.3 V to 2.7 V		0.7	V
		V_{CCA} = 3 V to 3.6 V		0.8	
V_{IA}	Input voltage		0	V_{CCA}	V
V_{OA}	Output voltage		0	V_{CCA}	V
I_{OH}	High-level output current	V_{CCA} = 2.3 V		–18	mA
		V_{CCA} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCA} = 2.3 V		18	mA
		V_{CCA} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

6.5 Thermal Information

THERMAL METRIC(1)		SN74ALVC164245				UNIT
		DGG (TSSOP)	DL (SSOP)	ZQL (BGA MICROSTAR JUNIOR)	ZRD (BGA MICROSTAR JUNIOR)	
		48 PINS	48 PINS	56 PINS	54 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.7	63.6	54.5	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.3	30.1	19.1	17.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	36.2	21.7	20.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	8.1	0.5	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.6	35.6	21.7	19.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: V_{CCA} = 2.7 V to 3.6 V

over recommended operating free-air temperature range for V_{CCA} = 2.7 V to 3.6 V and V_{CCB} = 4.5 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP[(1)]	MAX	UNIT
V_{OH}	B to A	I_{OH} = –100 µA	2.7 V to 3.6 V		V_{CC} – 0.2			V
		I_{OH} = –12 mA	2.7 V		2.2			
			3 V		2.4			
		I_{OH} = –24 mA	3 V		2			
	A to B	I_{OH} = –100 µA		4.5 V	4.3			
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL}	B to A	I_{OL} = 100 µA	2.7 V to 3.6 V				0.2	V
		I_{OL} = 12 mA	2.7 V				0.4	
		I_{OL} = 24 mA	3 V				0.55	
	A to B	I_{OL} = 100 µA		4.5 V to 5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V to 5.5 V			0.55	
I_I	Control inputs	V_I = V_{CCA}/V_{CCB} or GND	3.6 V	5.5 V			±5	µA
I_{OZ}[(2)]	A or B port	V_O = V_{CCA}/V_{CCB} or GND	3.6 V	5.5 V			±10	µA
I_{CC}		V_I = V_{CCA}/V_{CCB} or GND, I_O = 0	3.6 V	5.5 V			40	µA
ΔI_{CC}[(3)]		One input at V_{CCA}/V_{CCB} – 0.6 V, Other inputs at V_{CCA}/V_{CCB} or GND	3 V to 3.6 V	4.5 V to 5.5 V			750	µA
C_i	Control inputs	V_I = V_{CCA}/V_{CCB} or GND	3.3 V	5 V		6.5		pF
C_{io}	A or B port	V_O = V_{CCA}/V_{CCB} or GND	3.3 V	3.3 V		8.5		pF

(1) Typical values are measured at V_{CCA} = 3.3 V and V_{CCB} = 5 V, T_A = 25°C.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(3) This is the supply current increase for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC}.

6.7 Electrical Characteristics: V_{CCA} = 2.3 V to 2.7 V

over recommended operating free-air temperature range for V_{CCA} = 2.3 V to 2.7 V and V_{CCB} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{OH}	B to A	I_{OH} = –100 µA	2.3 V to 2.7 V	3 V to 3.6 V	V_{CCA} – 0.2		V
		I_{OH} = –8 mA	2.3 V	3 V to 3.6 V	1.7		
		I_{OH} = –12 mA	2.7 V	3 V to 3.6 V	1.8		
	A to B	I_{OH} = –100 µA	2.3 V to 2.7 V	3 V to 3.6 V	V_{CCB} – 0.2		
		I_{OH} = –18 mA	2.3 V to 2.7 V	3 V	2.2		
V_{OL}	B to A	I_{OL} = 100 µA	2.3 V to 2.7 V	3 V to 3.6 V		0.2	V
		I_{OL} = 12 mA	2.3 V	3 V to 3.6 V		0.6	
	A to B	I_{OL} = 100 µA	2.3 V to 2.7 V	3 V to 3.6 V		0.2	
		I_{OL} = 18 mA	2.3 V	3 V		0.55	
I_I	Control inputs	V_I = V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3 V to 3.6 V		±5	µA
I_{OZ} (1)	A or B port	V_O = V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3 V to 3.6 V		±10	µA
I_{CC}		V_I = V_{CCA}/V_{CCB} or GND, I_O = 0	2.3 V to 2.7 V	3 V to 3.6 V		20	µA
ΔI_{CC} (2)		One input at V_{CCA}/V_{CCB} – 0.6 V, Other inputs at V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3 V to 3.6 V		750	µA

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC}.

6.8 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V				UNIT
			V_{CCA} = 2.5 V ± 0.2 V		V_{CCA} = 2.7 V		V_{CCA} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		7.6		5.9	1	5.8	ns
	B	A		7.6		6.7	1.2	5.8	
t_{en}	$\overline{OE}$	B		11.5		9.3	1	8.9	ns
t_{dis}	$\overline{OE}$	B		10.5		9.2	2.1	9.5	ns
t_{en}	$\overline{OE}$	A		12.3		10.2	2	9.1	ns
t_{dis}	$\overline{OE}$	A		9.3		9	2.9	8.6	ns

6.9 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
				V_{CCA} = 2.5 V	V_{CCA} = 3.3 V	
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled (B)	C_L = 50 pF, f = 10 MHz	55	56	pF
		Outputs disabled (B)		27	6	
		Outputs enabled (A)	C_L = 50 pF, f = 10 MHz	118	56	
		Outputs disabled (A)		58	6	

6.10 Typical Characteristics

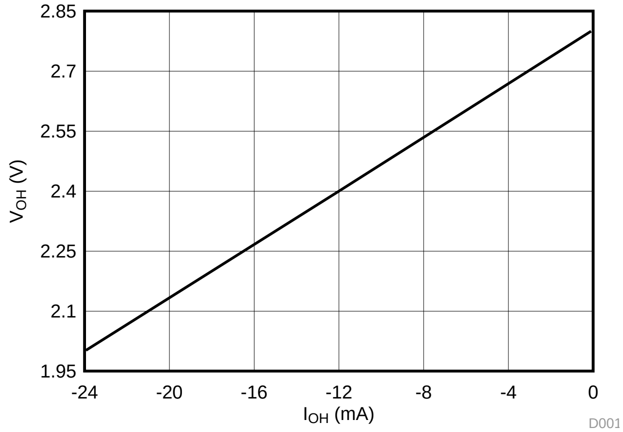
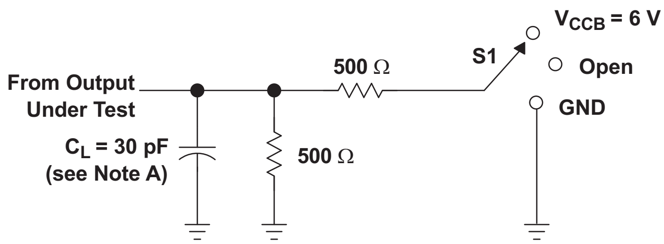


Figure 1. V_{OH} vs I_{OH}

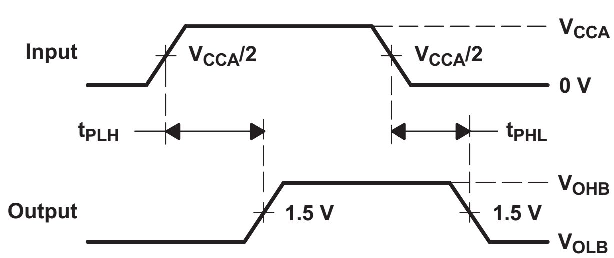
7 Parameter Measurement Information

7.1 V_{CCA} = 2.5 V ± 0.2 V to V_{CCB} = 3.3 V ± 0.3 V

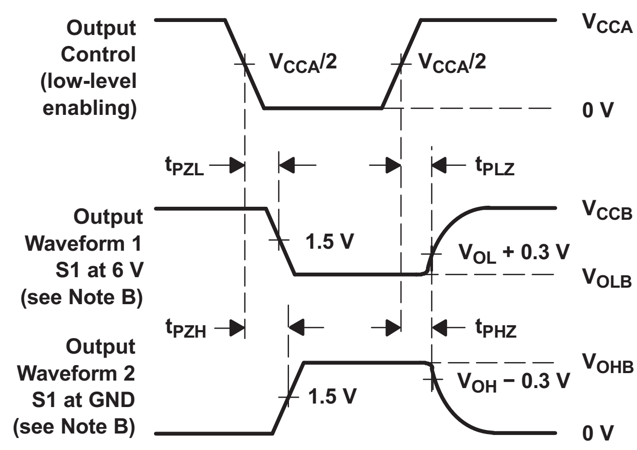


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{CCB} = 6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

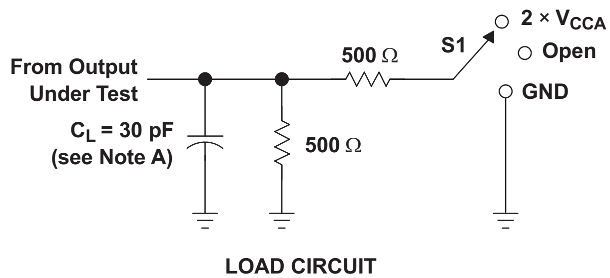


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

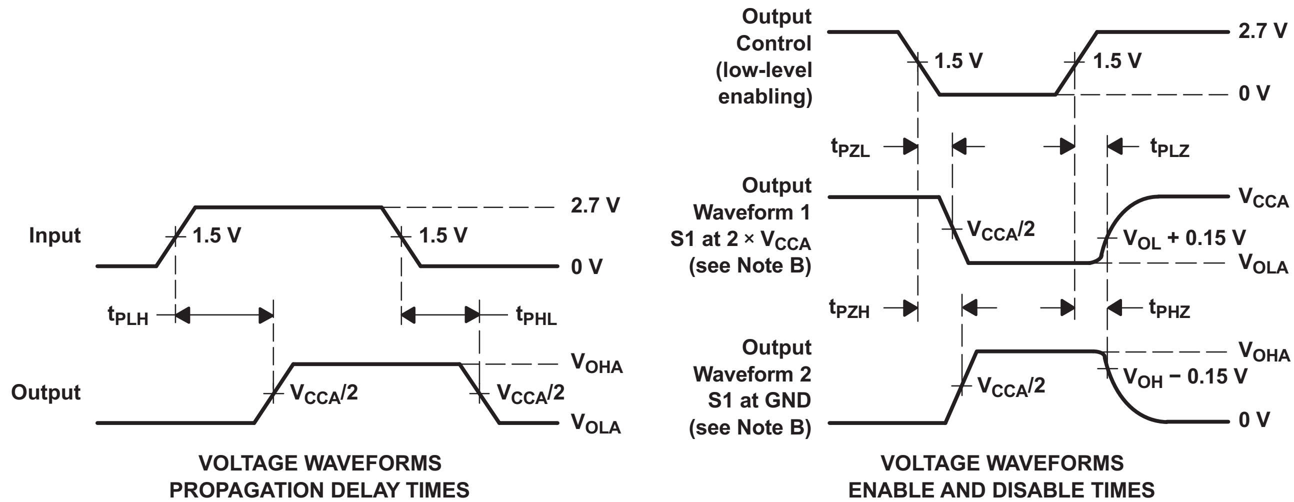
NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f≤2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

7.2 V_{CCB} = 3.3 V ± 0.3 V to V_{CCA} = 2.5 V ± 0.2 V



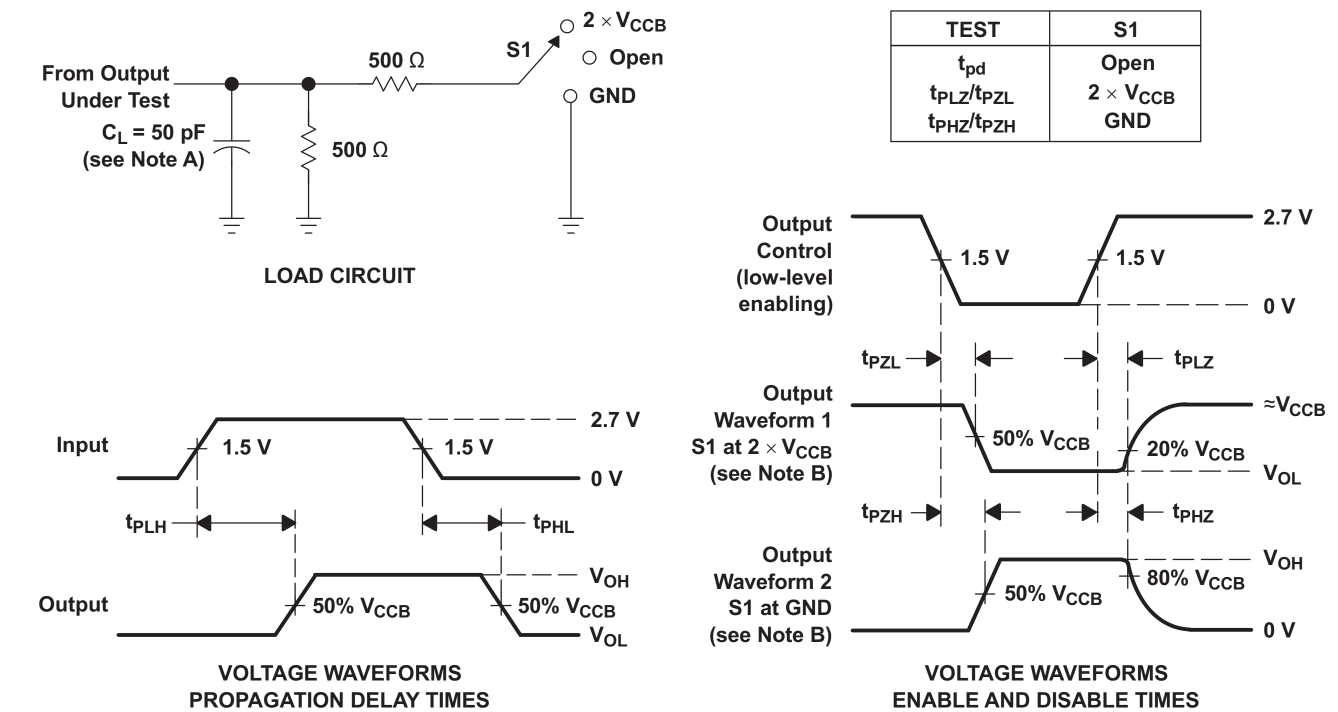
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCA}
t_{PHZ}/t_{PZH}	GND



NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

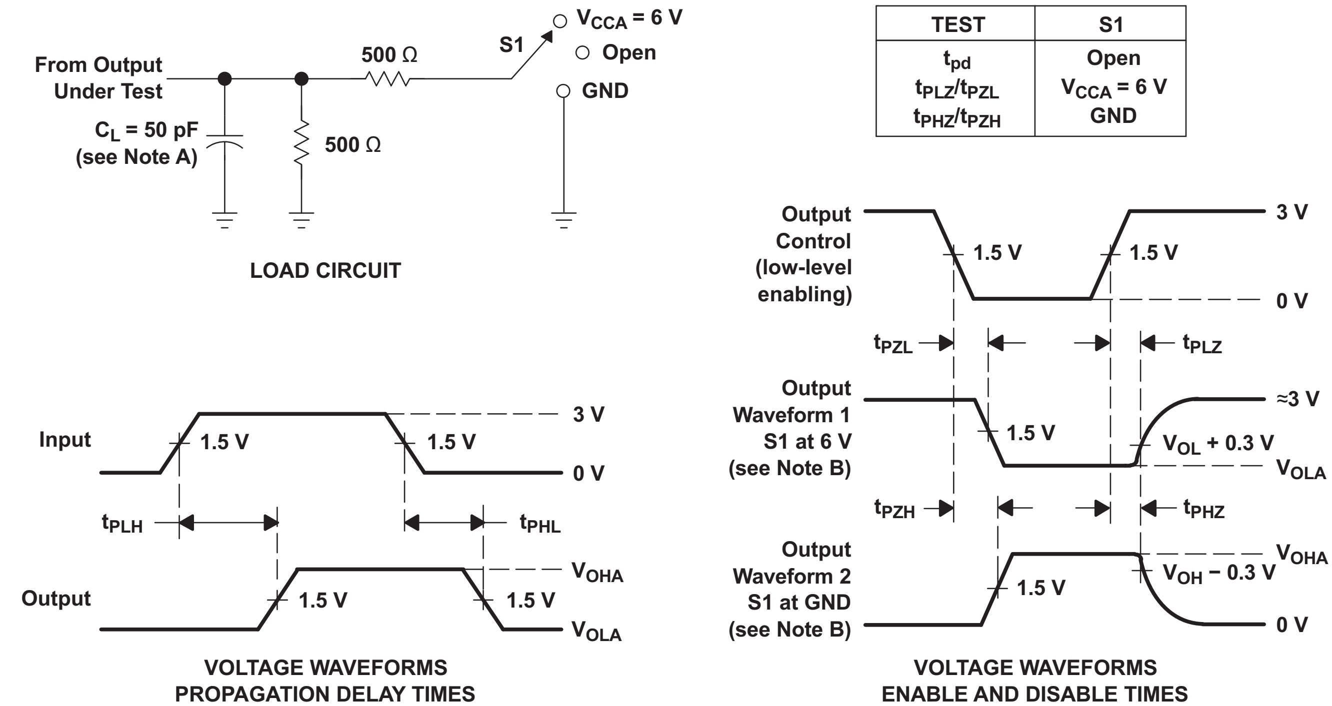
7.3 V_{CCA} = 3.3 V ± 0.3 V to V_{CCB} = 5 V ± 0.5 V



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Load Circuit and Voltage Waveforms

7.4 V_{CCB} = 5 V ± 0.5 V to V_{CCA} = 2.7 V and 3.3 V ± 0.3 V



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{CCA} = 6 V
t_{PHZ}/t_{PZH}	GND

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74ALVC16245 device is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V and 5-V system environment.

8.2 Functional Block Diagram

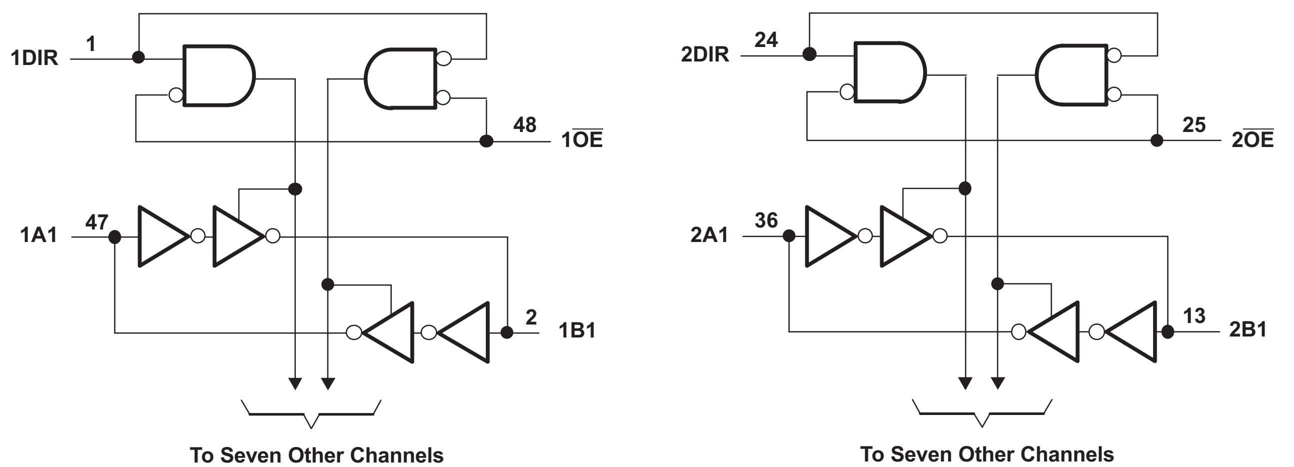


Figure 6. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74ALVC164245 can output 24 mA drive at 3.3V V_{CC}. This device allows down voltage translations and accepts input voltages to V_{CC} + 0.5V. This device is useful for high-speed applications because of the low t_{pd}.

8.4 Device Functional Modes

Table 3 lists the functions of the device.

Table 3. Function Table(1) (Each 8-Bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74ALVC16245 device is a 16-bit bidirectional transceiver. This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. This allows it to be used in multi-power systems and for down translation as well.

9.2 Typical Application

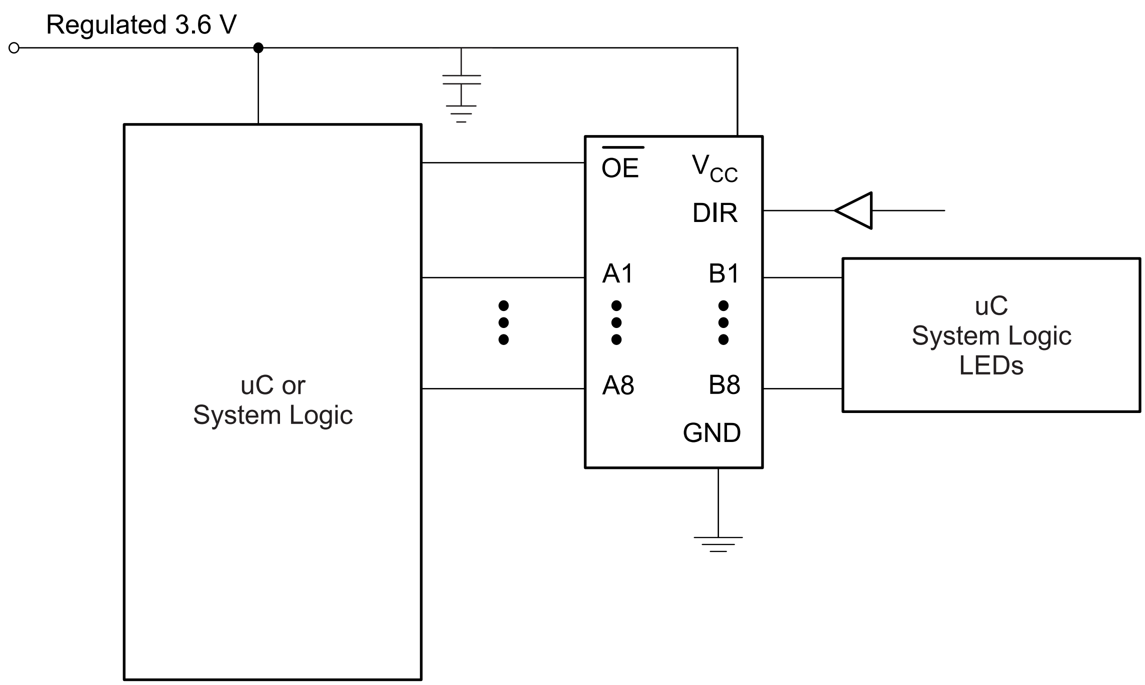


Figure 7. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in *Recommended Operating Conditions: V_{CCB} at 3.3 V*.
   - Specified high and low levels: See (V_{IH} and V_{IL}) in *Recommended Operating Conditions: V_{CCB} at 3.3 V*.
2. Recommend Output Conditions
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve

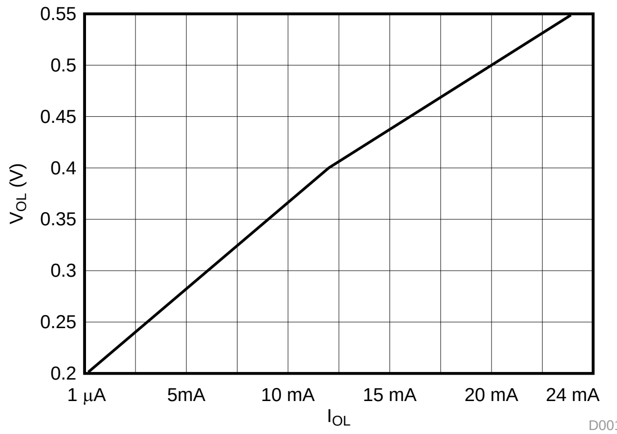


Figure 8. V_{OH} vs I_{OH}

10 Power Supply Recommendations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence must always be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

For more information, see the TI application report, *Texas Instruments Voltage-Level-Translation Devices* (SCEA021).

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the Figure 9 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

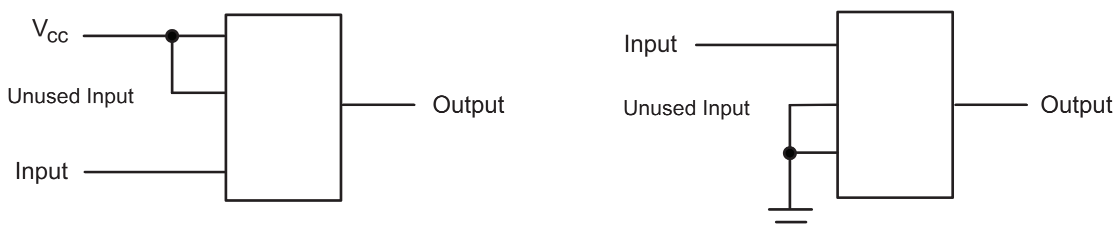


Figure 9. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Texas Instruments Voltage-Level-Translation Devices* (SCEA021)
- *Implications of Slow or Floating CMOS Inputs* (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

Widebus, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ALVC164245DGGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245
74ALVC164245DLRG4	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245
SN74ALVC164245DGG	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	ALVC164245
SN74ALVC164245DGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245
SN74ALVC164245DGGT	Active	Production	TSSOP (DGG) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245
SN74ALVC164245DL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245
SN74ALVC164245DLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC164245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ALVC164245 :

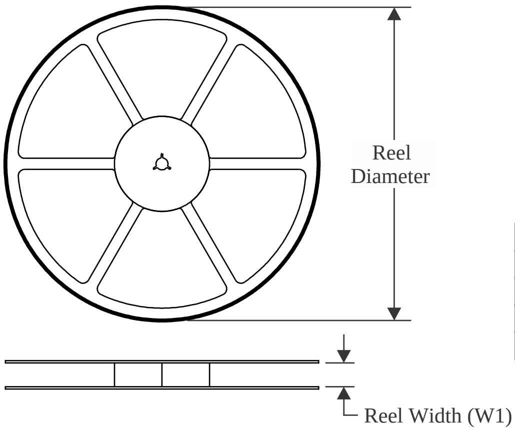
- Enhanced Product : SN74ALVC164245-EP

NOTE: Qualified Version Definitions:

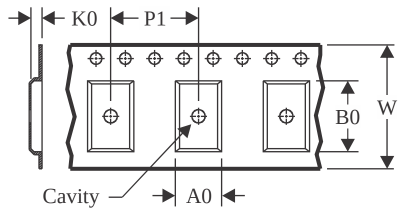
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

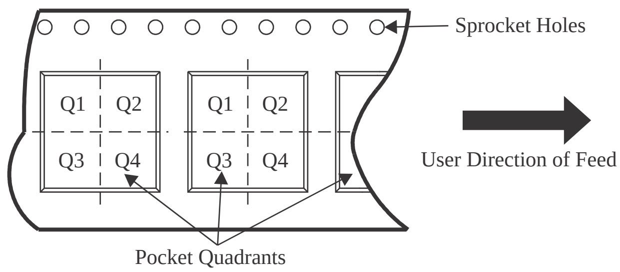


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

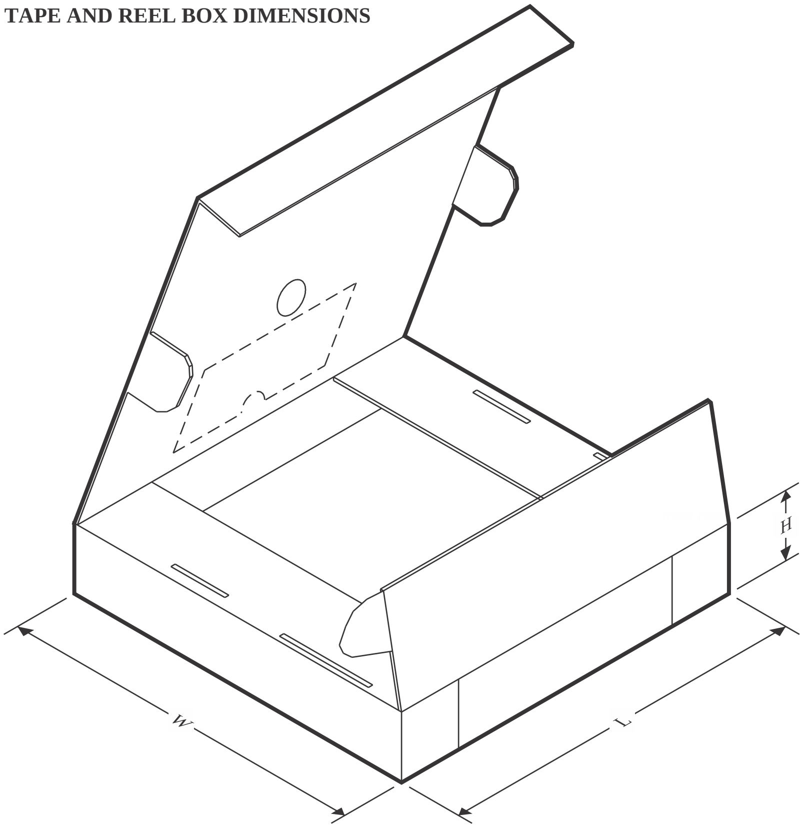
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC164245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVC164245DGGT	TSSOP	DGG	48	250	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVC164245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

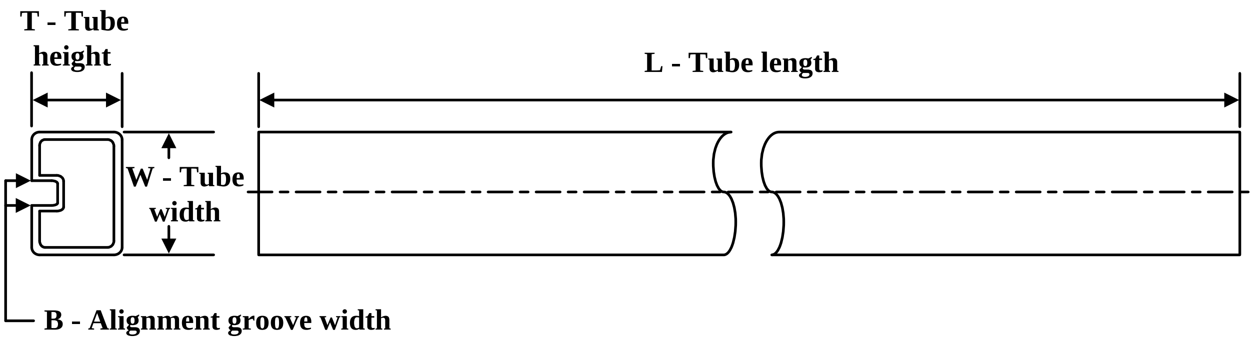
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC164245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVC164245DGGT	TSSOP	DGG	48	250	367.0	367.0	45.0
SN74ALVC164245DLR	SSOP	DL	48	1000	367.0	367.0	55.0

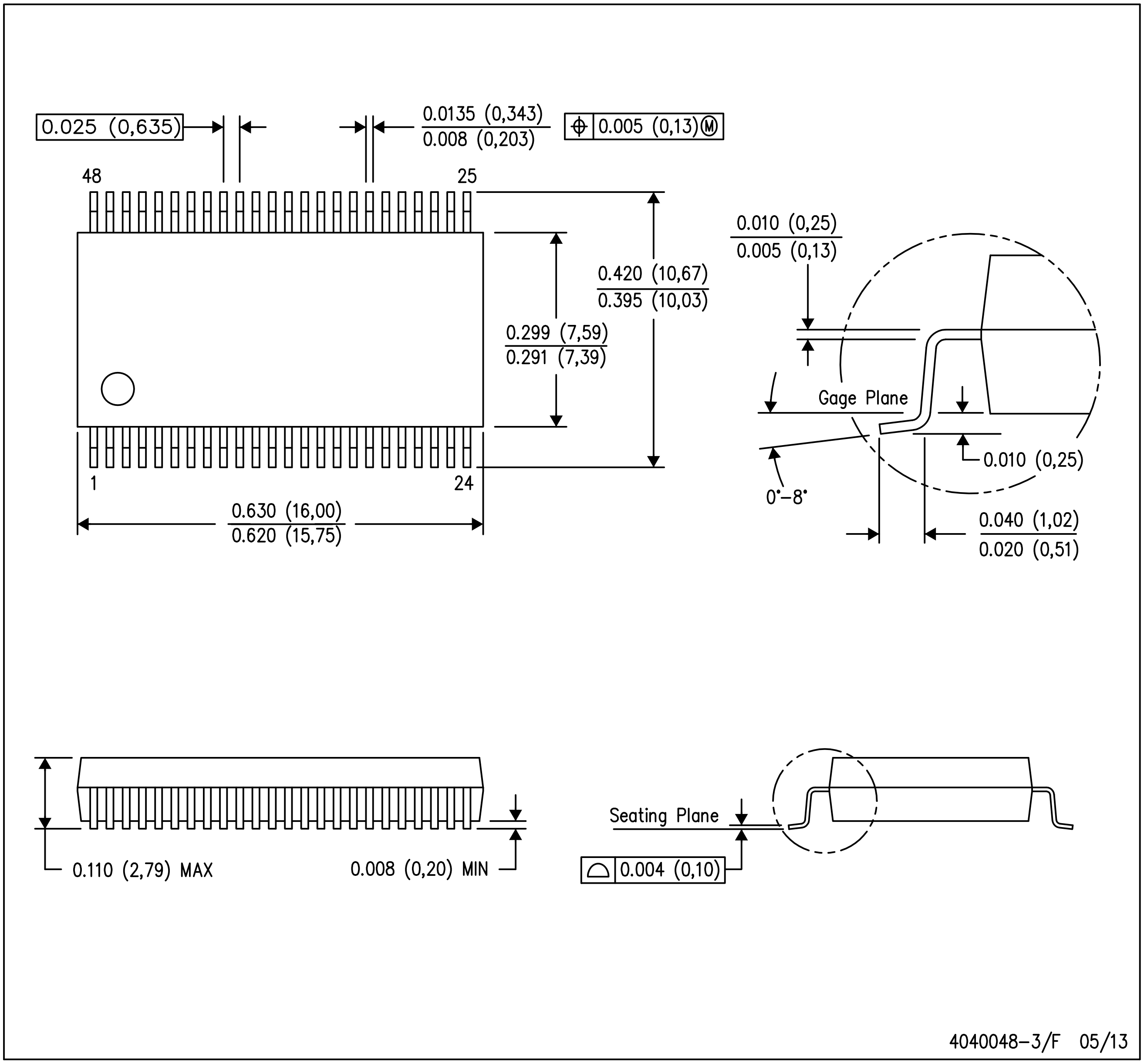
TUBE



*All dimensions are nominal

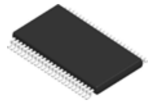
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74ALVC164245DLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ALVC164245DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN74ALVC164245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

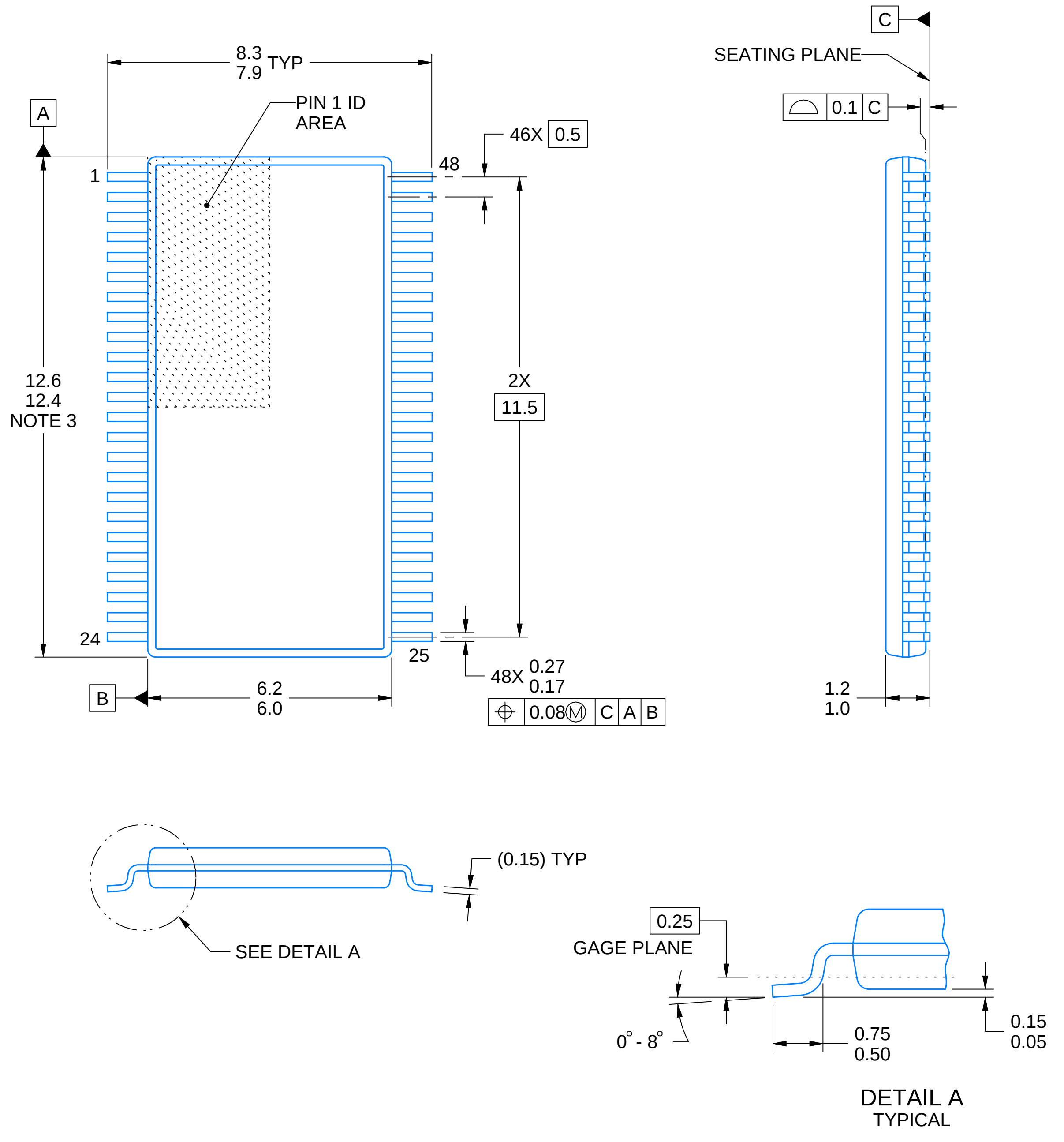
DL (R-PDSO-G48) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

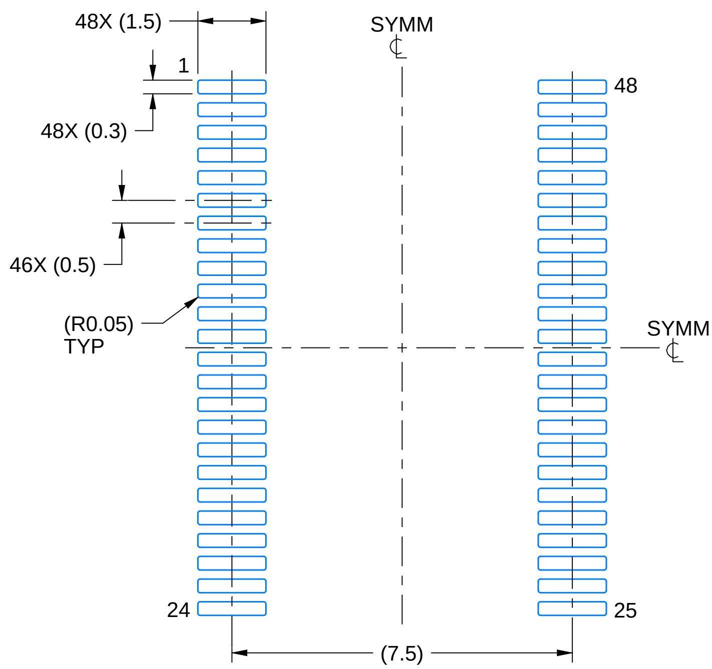
PowerPAD is a trademark of Texas Instruments.



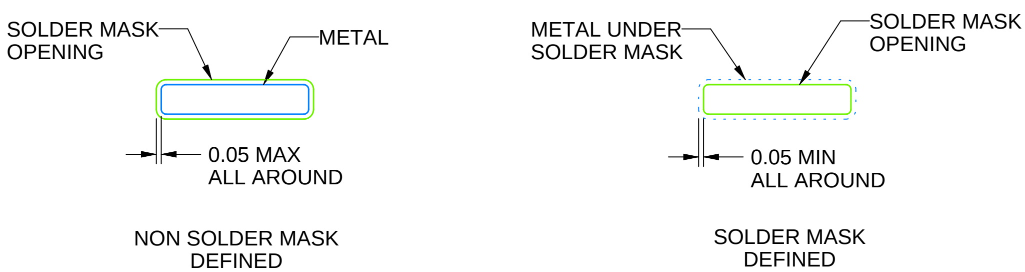


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

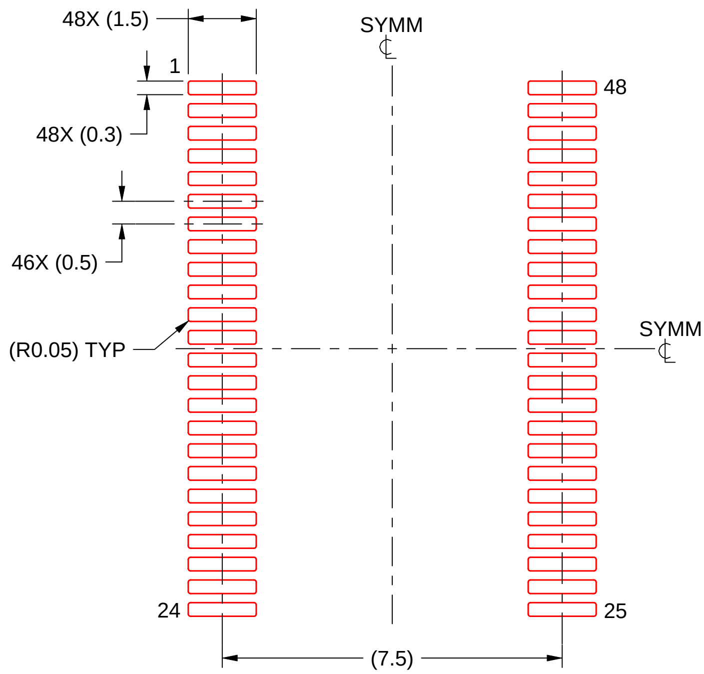


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

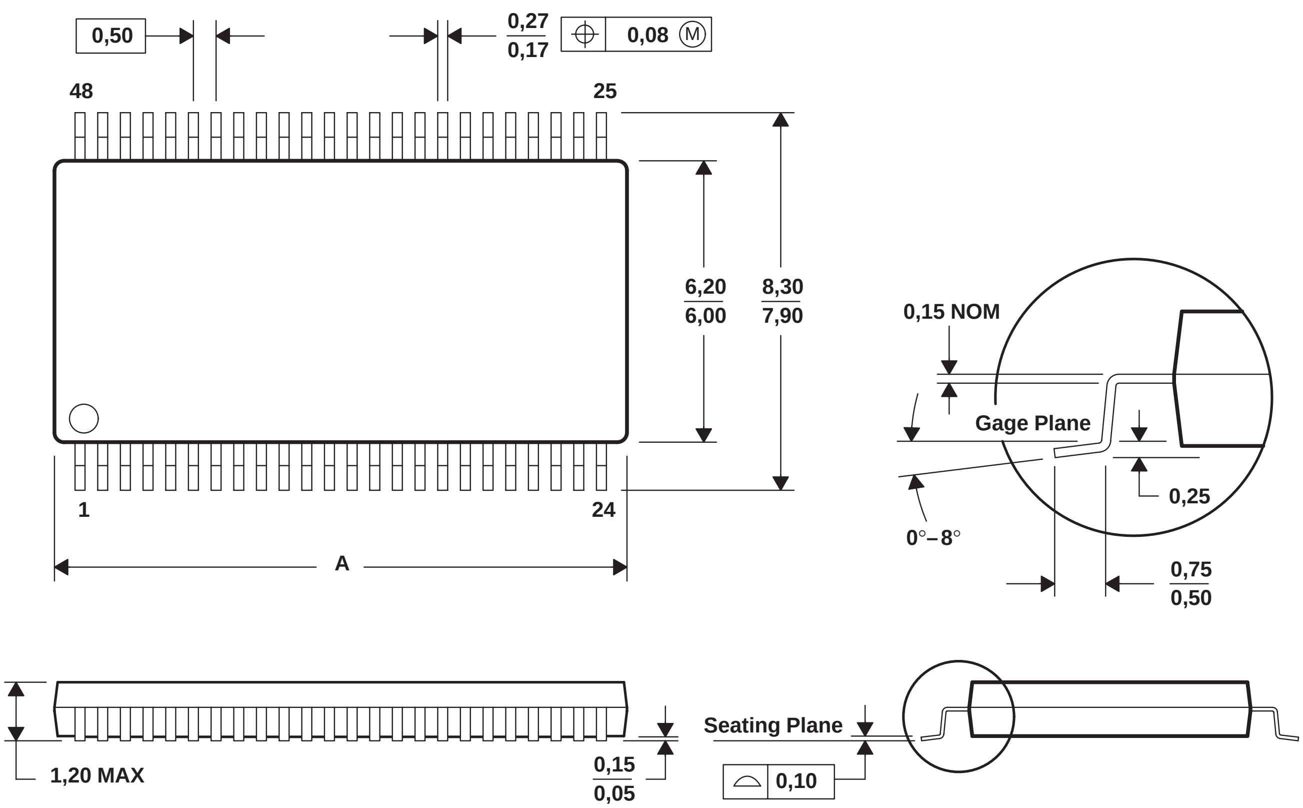
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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