TEXAS INSTRUMENTS

SNx4HC112 クリアとプリセット搭載、デュアル、J-K、ネガティブ・エッジ・トリガ・フリップ・フロップ

1 特長

- 幅広い動作電圧範囲:2V～6V
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低消費電力、I_{CC}:40μA 以下
- t_{pd} = 13ns (標準値)
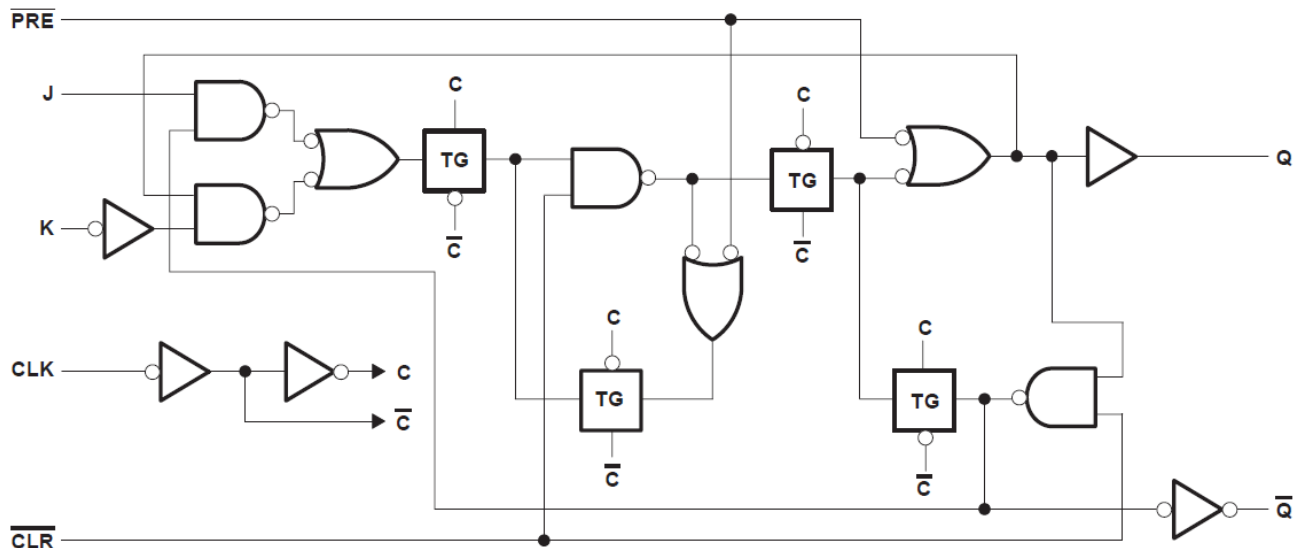- 5V で ±4mA の出力駆動能力
- 低い入力電流:最大 1μA

2 概要

HC112 デバイスには、2 つの独立した J-K ネガティブ・エッジ・トリガ・フリップ・フロップが含まれています。その他の入力のレベルに関係なく、プリセット (PRE) 入力を LOW レベルにすると出力は HIGH になり、クリア ($\overline{CLR}$) 入力を LOW レベルにすると出力は LOW になります。PRE と $\overline{CLR}$ が非アクティブ (HIGH) の場合、セットアップ時間の要件を満たす J 入力と K 入力のデータは、クロック (CLK) パルスの負方向エッジで出力に転送されます。クロックのトリガは電圧レベルで発生し、CLK パルスの立ち下がり時間とは直接関係しません。ホールド時間が経過した後、J 入力と K 入力のデータは、出力のレベルに影響を及ぼさずに変化させることができます。これらの汎用フリップ・フロップは、J と K を HIGH に接続することで、トグル・フリップ・フロップとしての動作を実行します。

製品情報

部品番号	パッケージ[1]	本体サイズ (公称)
SN54HC112J	CDIP (16)	24.38mm × 6.92mm
SN74HC112D	SOIC (16)	9.90mm × 3.90mm
SN74HC112N	PDIP (16)	19.31mm × 6.35mm
SN54HC112FK	LCCC (20)	8.89mm × 8.45mm
SN54HC112W	CFP (16)	10.16mm × 6.73mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図

English Data Sheet: SCLS099

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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (February 2022) to Revision H (June 2022)	Page
• Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, N was 67 is now 89.1........4	

Changes from Revision F (September 2003) to Revision G (February 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新...........................1	

Product Folder Links: *SN54HC112 SN74HC112*

4 Pin Configuration and Functions

1CLK	1	16	V$_{CC}$
1K	2	15	1$\overline{CLR}$
1J	3	14	2$\overline{CLR}$
1$\overline{PRE}$	4	13	2CLK
1Q	5	12	2K
1$\overline{Q}$	6	11	2J
2$\overline{Q}$	7	10	2$\overline{PRE}$
GND	8	9	2Q
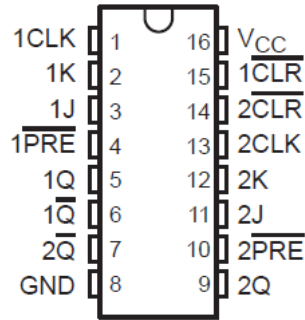
J, D, N, W package
16-Pin CDIP, SOIC, PDIP, CFP
Top View

FK Package pinout (20-Pin LCCC, Top View):

Top row pins: 1K (3), 1CLK (2), NC (1), Vcc (20), 1$\overline{CLR}$ (19)

Left side: 1J (4), 1$\overline{PRE}$ (5), NC (6), 1Q (7), 1$\overline{Q}$ (8)

Right side: 2$\overline{CLR}$ (18), 2CLK (17), NC (16), 2K (15), 2J (14)

Bottom row: 2$\overline{Q}$ (9), GND (10), NC (11), 2Q (12), 2$\overline{PRE}$ (13)
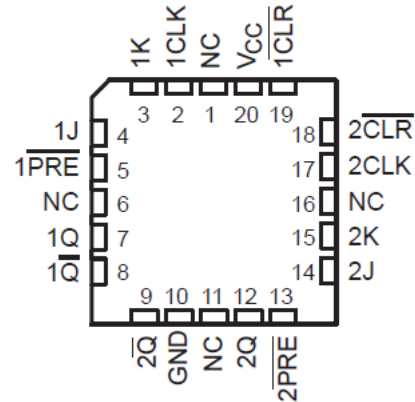
NC – No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	mA
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions[2]

			SN54HC112			SN74HC112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			0.5	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 6$ V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t [1]	Input transition (rise and fall) time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

(1) If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

(2) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

		D (SOIC)	N (PDIP)	
THERMAL METRIC		**16 PINS**	**16 PINS**	**UNIT**
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	117.2	89.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.6	47.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.1	11.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.3	47	°C/W

Product Folder Links: *SN54HC112 SN74HC112*

5.3 Thermal Information (continued)

THERMAL METRIC		D (SOIC)	N (PDIP)	
		16 PINS	**16 PINS**	**UNIT**
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

Product Folder Links: *SN54HC112 SN74HC112*

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98	4.3			3.7		3.84	
		I_{OH} = −5.2 mA	6 V	5.48	5.8			5.2		5.34	
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			4		80		40	μA
C_i			2 V to 6 V		3	10		10		10	pF

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC112		SN74HC112		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		5		3.4		4	MHz
			4.5 V		25		17		20	
			6 V		29		20		24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK ↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK ↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	10		3.4		4		MHz
			4.5 V	25	50		17		20		
			6 V	29	60		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		54	165		245		205	ns
			4.5 V		16	33		49		41	
			6 V		13	28		42		35	
	CLK	Q or $\overline{Q}$	2 V		56	125		185		155	
			4.5 V		16	25		37		31	
			6 V		13	21		31		26	
t_t		Q or $\overline{Q}$	2 V		29	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

5.7 Operating Characteristics

T_A = 25℃

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

Product Folder Links: *SN54HC112 SN74HC112*

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
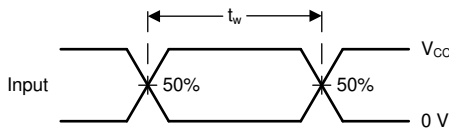
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
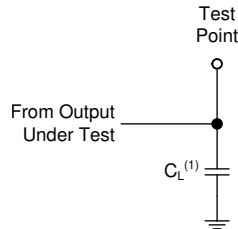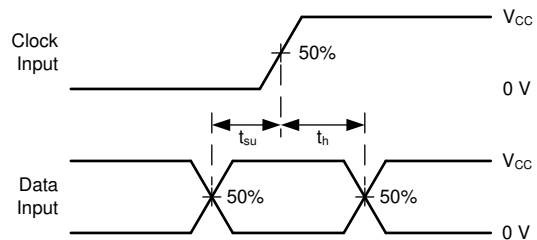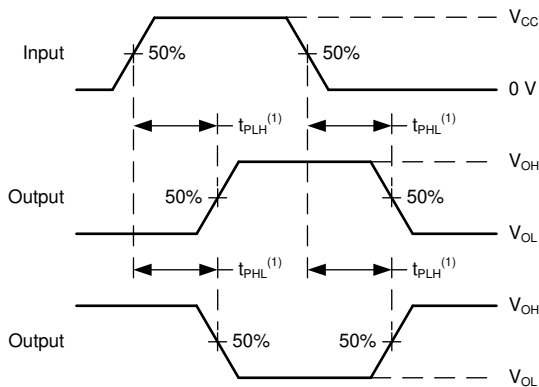
(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for Push-Pull Outputs

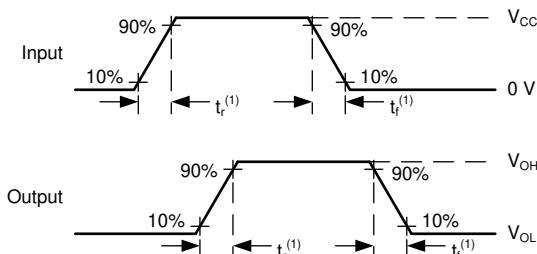**図 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration**

図 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times

(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs

(1) The greater between t_r and t_f is the same as t_t.

図 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

Product Folder Links: *SN54HC112 SN74HC112*

7 Detailed Description

7.1 Overview

The 'HC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the CLK pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

7.2 Functional Block Diagram
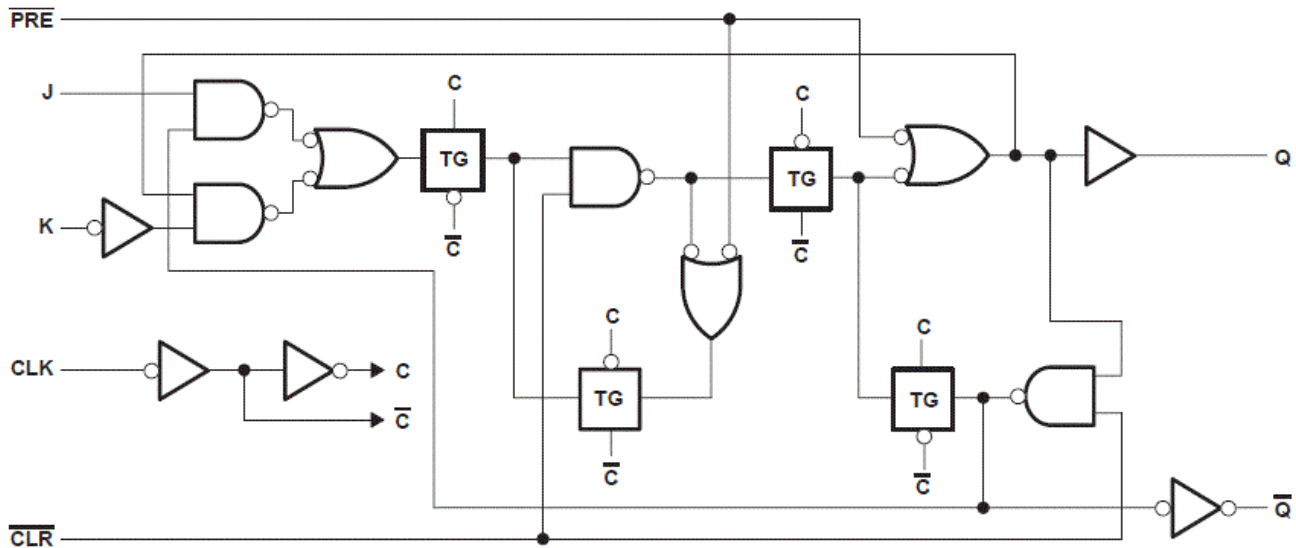
7.3 Device Functional Modes

表 7-1. Function Table

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	H
H	L	X	X	X	L	H
L	L	X	X	X	H[1]	H[1]
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84088012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84088012A SNJ54HC 112FK	Samples
8408801EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408801EA SNJ54HC112J	Samples
8408801FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408801FA SNJ54HC112W	Samples
JM38510/65305BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65305BEA	Samples
M38510/65305BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65305BEA	Samples
SN54HC112J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC112J	Samples
SN74HC112DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 85	HC112	Samples
SN74HC112N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC112N	Samples
SNJ54HC112FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84088012A SNJ54HC 112FK	Samples
SNJ54HC112J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408801EA SNJ54HC112J	Samples
SNJ54HC112W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408801FA SNJ54HC112W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC112, SN74HC112 :

- Catalog : SN74HC112

- Military : SN54HC112

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC112DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC112DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC112DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC112DR	SOIC	D	16	2500	366.0	364.0	50.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
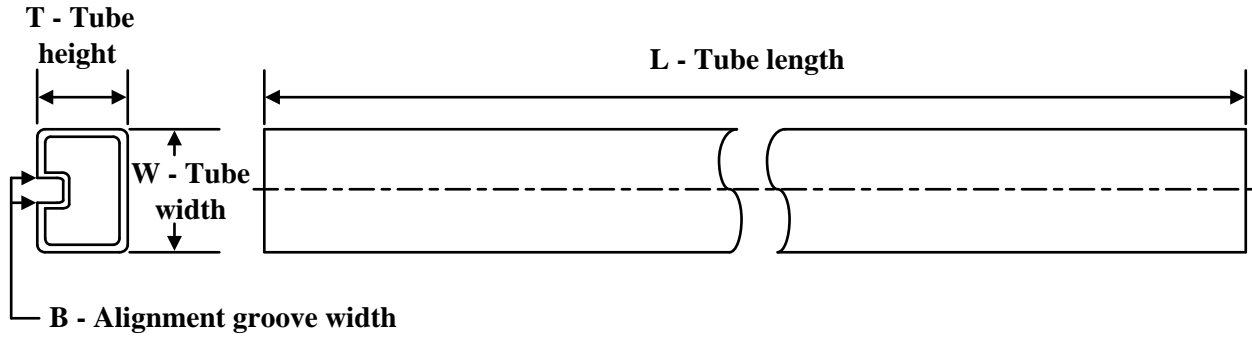
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84088012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8408801FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC112N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC112N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC112FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC112W	W	CFP	16	25	506.98	26.16	6220	NA

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) | Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

⬠ | 0.004 (0,10)

Gauge Plane

0.010 (0,25)   0°−8°

Seating Plane

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          △D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AC.

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W (R-GDFP-F16)   CERAMIC DUAL FLATPACK
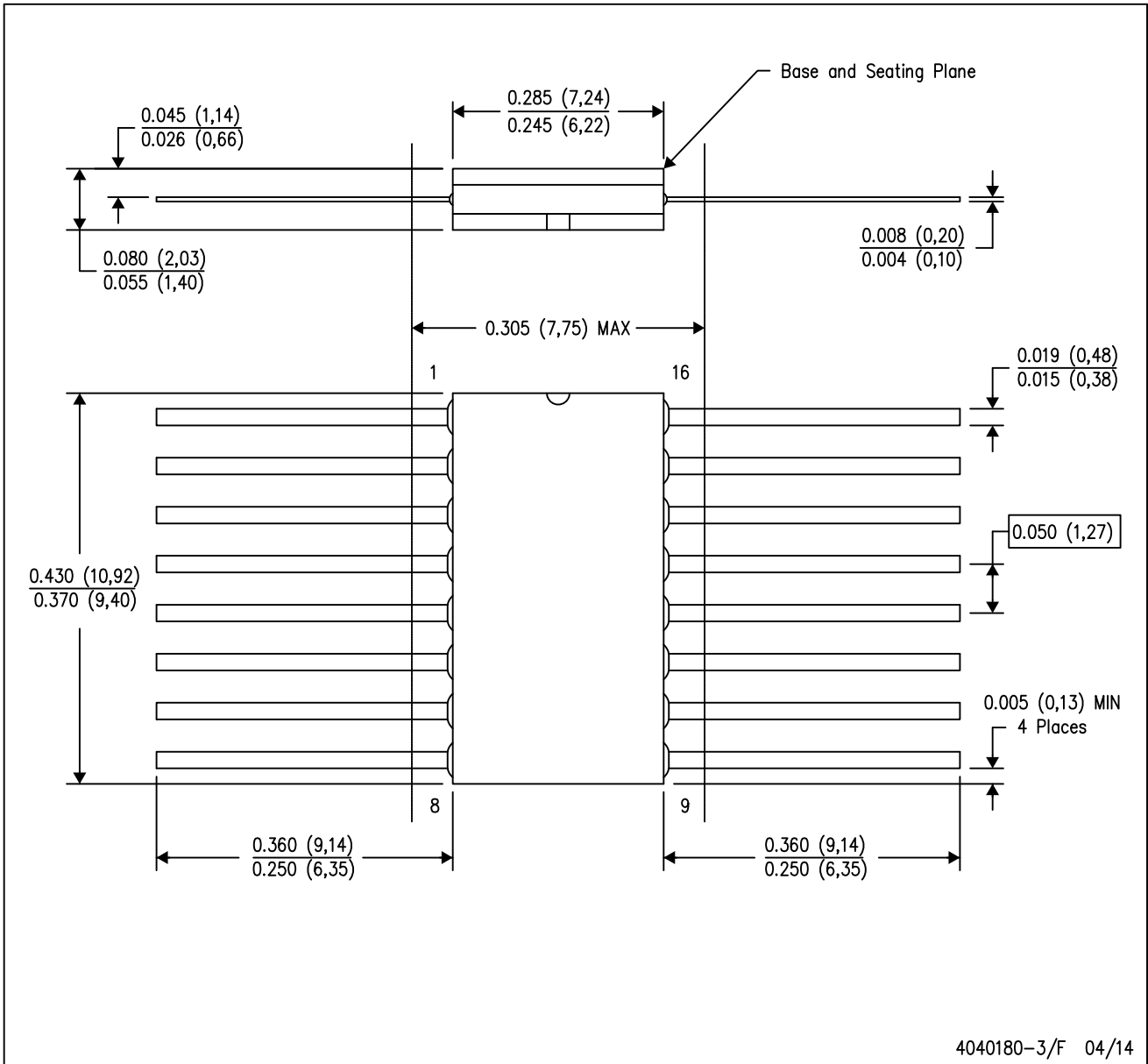
0.045 (1,14)
0.026 (0,66)

0.285 (7,24)
0.245 (6,22)

Base and Seating Plane

0.080 (2,03)
0.055 (1,40)

0.008 (0,20)
0.004 (0,10)

0.305 (7,75) MAX

0.019 (0,48)
0.015 (0,38)

1   16

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180-3/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
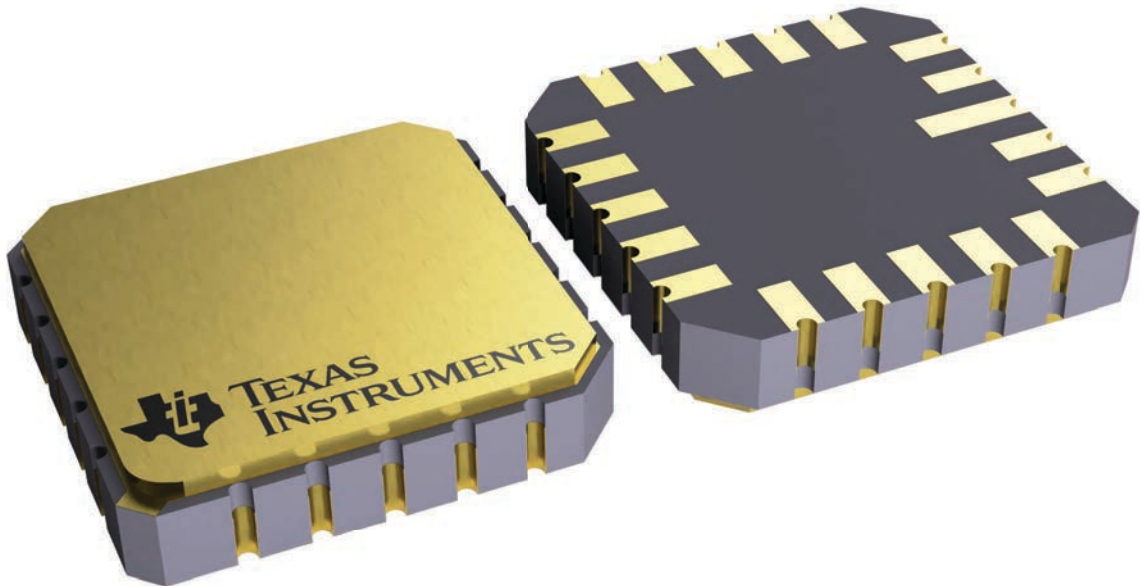   E. Falls within MIL STD 1835 GDFP2-F16

FK 20

8.89 x 8.89, 1.27 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4229370VA\
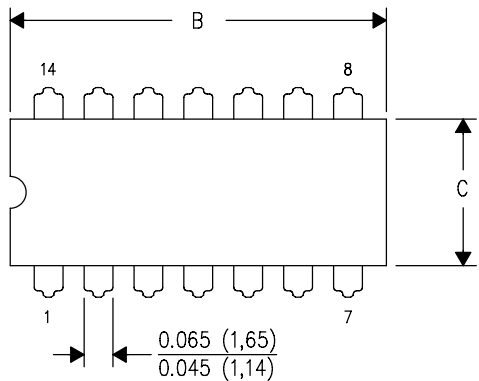
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

C

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°—15°

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R–PDIP–T**)
16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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