15-W STEREO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **10-W/ch into an 4-Ω Load From a 17-V Supply**
- **15-W/ch into an 8-Ω Load From a 28-V Supply**
- **Operates from 10 V to 30 V**
- **Efficient Class-D Operation**
- **Four Selectable, Fixed Gain Settings**
- **Internal Oscillator (No External Components Required)**
- **Single Ended Analog Inputs**
- **Thermal and Short-Circuit Protection with Auto Recovery Feature**
- **20-pin DIP Package**

APPLICATIONS

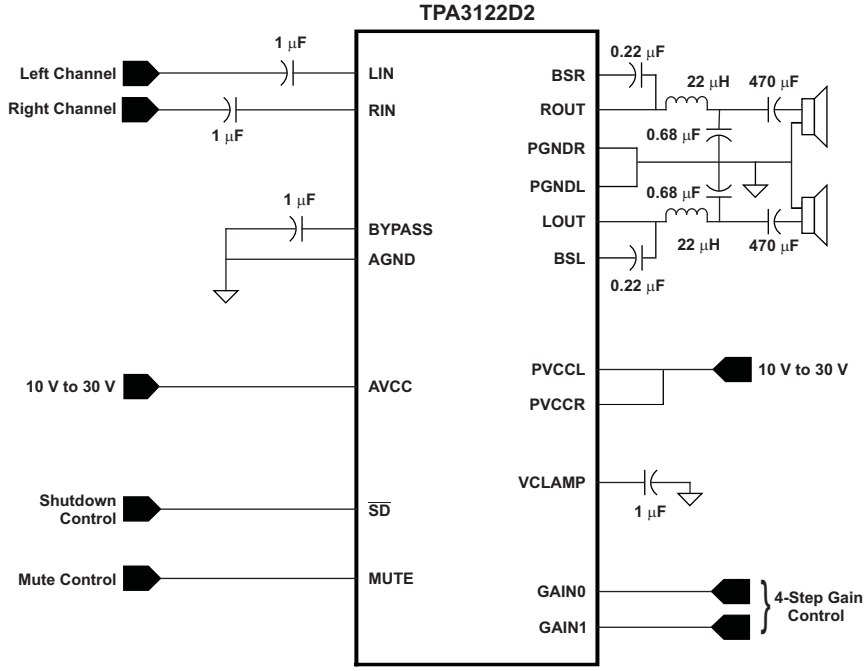
- **Televisions**

DESCRIPTION

The TPA3122D2 is a 15-W (per channel) efficient, Class-D audio power amplifier for driving stereo single ended speakers or mono bridge tied load. The TPA3122D2 can drive stereo speakers as low as 4Ω. The efficiency of the TPA3122D2 eliminates the need for an external heat sink when playing music.

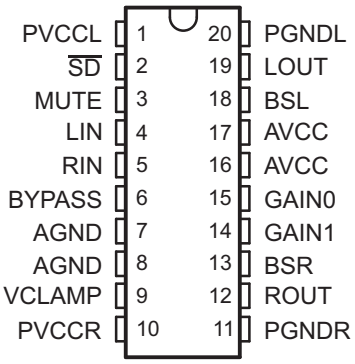
The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, and 36 dB.

SIMPLIFIED APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

N (DIP) PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	20-PIN (DIP)		
$\overline{SD}$	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC.
RIN	5	I	Audio input for right channel.
LIN	4	I	Audio input for left channel.
GAIN0	15	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	14	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
MUTE	3	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle; low = outputs enabled). TTL logic levels with compliance to AVCC.
BSL	18	I/O	Bootstrap I/O for left channel.
PVCCL	1		Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
LOUT	19	O	Class-D -H-bridge positive output for left channel.
PGNDL	20		Power ground for left channel H-bridge.
VCLAMP	9		Internally generated voltage supply for bootstrap capacitors.
BSR	13	I/O	Bootstrap I/O for right channel.
ROUT	12	O	Class-D -H-bridge negative output for right channel.
PGNDR	11		Power ground for right channel H-bridge.
PVCCR	10		Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
AGND	8		Analog ground for digital/analog cells in core.
AGND	7		Analog Ground for analog cells in core.
BYPASS	6	O	Reference for pre-amplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
AVCC	16, 17		High-voltage analog power supply. Not internally connected to PVCCR or PVCCL

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_{CC}	Supply voltage, AVCC, PVCC		–0.3 to 36	V
V_I	Logic input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1	–0.3 to V_{CC} +0.3 –0.3 to V_{CC} +0.3	V
V_{IN}	Analog input voltage	RIN, LIN	–0.3 to 7	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		-65 to 150	°C
R_L	Load resistance (Minimum value)		3.2	kV
ESD	Electrostatic Discharge	Human body model (all pins)	±2	kV
		Charged-device model (all pins)	±500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE(1)	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
20-pin DIP	1.87 W	15 mW/°C	1.20 W	0.97 W

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	10	30	V
V_{IH}	High-level input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, MUTE, GAIN0, GAIN1		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, $V_I = V_{CC}$, V_{CC} = 30 V		125	µA
		MUTE, $V_I = V_{CC}$, V_{CC} = 30 V		125	
		GAIN0, GAIN1, $V_I = V_{CC}$, V_{CC} = 24 V		125	
I_{IL}	Low-level input current	$\overline{SD}$, V_I = 0, V_{CC} = 30 V		1	µA
		MUTE, V_I = 0 V, V_{CC} = 30 V		1	
		GAIN0, GAIN1, V_I = 0 V, V_{CC} = 24 V		1	
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 4Ω (unless otherwise noted)

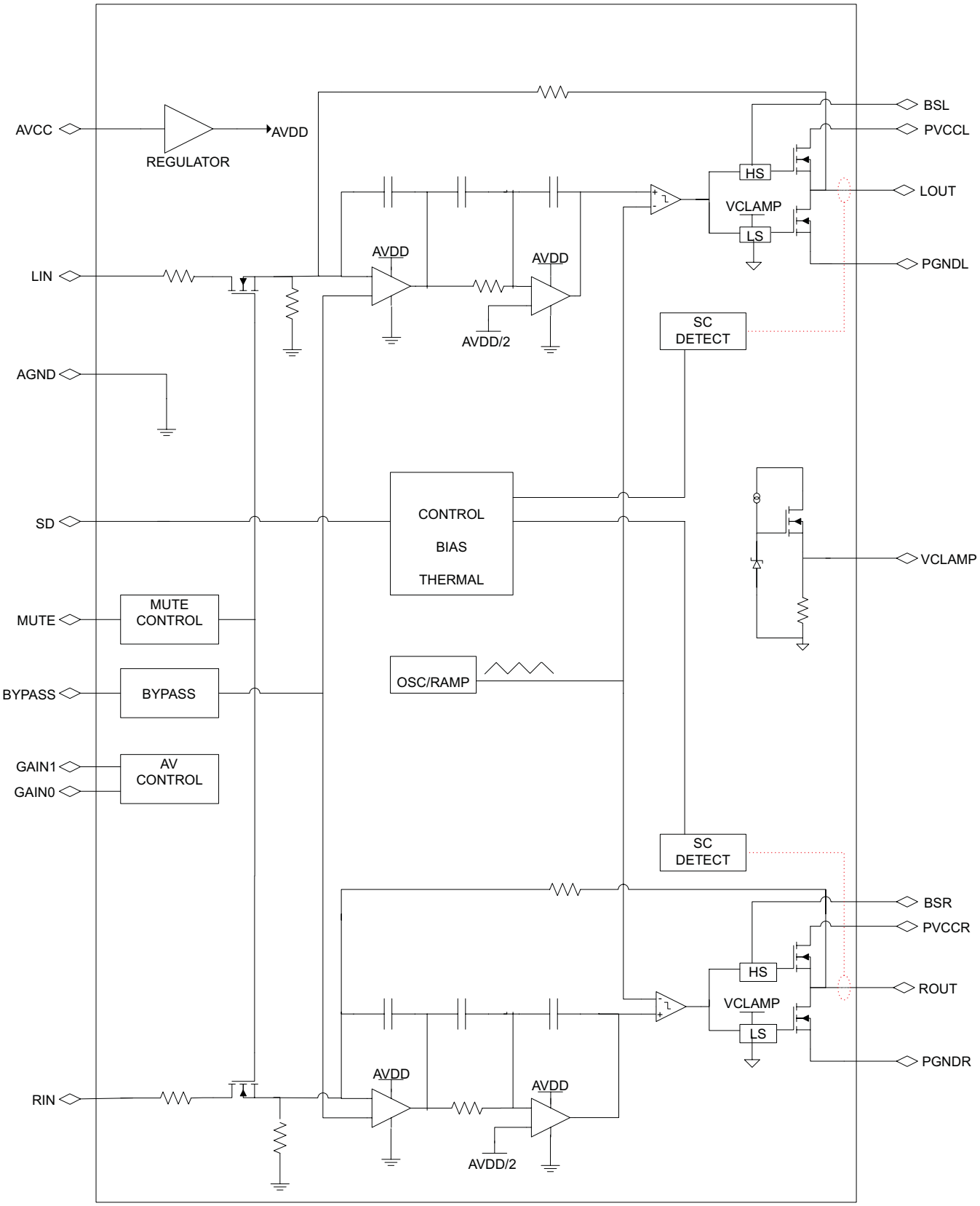
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, A_V = 36 dB			7.5	50	mV
$V_{(BYPASS)}$	Bypass output voltage	No load			$AV_{CC}/8$		V
$I_{CC(q)}$	Quiescent supply current	$\overline{SD}$ = 2 V, MUTE = 0 V, No load			23	37	mA
$I_{CC(q)}$	Quiescent supply current in mute mode	MUTE = 2 V, No load			23		mA
$I_{CC(q)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V , No load			0.39	1	mA
$r_{DS(on)}$	Drain-source on-state resistance				200		mΩ
G	Gain	Gain1 = 0.8 V	Gain0 = 0.8 V	18	20	22	dB
			Gain0 = 2 V	24	26	28	
		Gain1 = 2 V	Gain0 = 0.8 V	30	32	34	
			Gain0 = 2 V	34	36	38	
	Mute Attenuation	V_I = 1Vrms			–82		

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24V, R_L = 4Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	V_{CC} = 12 V, V_{ripple} = 200 mV_{PP} Gain = 20 dB	100 Hz		–30		dB
			1 kHz		-48		dB
P_O	Output Power at 1% THD+N	V_{CC} = 12 V, R_L = 4 Ω, f = 1 kHz			4		W
		V_{CC} = 24 V, R_L = 8 Ω, f = 1 kHz			8		
	Output Power at 10% THD+N	V_{CC} = 12 V, R_L = 4 Ω, f = 1 kHz			5		
		V_{CC} = 24 V, R_L = 8 Ω, f = 1 kHz			10		
THD+N	Total harmonic distortion + noise	R_L = 4 Ω, f = 1 kHz, P_O = 1 W			0.1%		
		R_L = 8 Ω, f = 1 kHz, P_O = 1 W			0.06%		
V_n	Output integrated noise floor	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB			85		µV
					–80		dB
	Crosstalk	P_O = 1 W, f = 1kHz; Gain = 20 dB			–60		dB
SNR	Signal-to-noise ratio	Max Output at THD+N < 1%, f = 1 kHz, Gain = 20 dB			99		dB
	Thermal trip point				150		°C
	Thermal hysteresis				30		°C
f_{OSC}	Oscillator frequency	10 V ≤ V_{CC}		230	250	270	kHz
Δt	mute delay	time from mute input switches high until outputs muted			120		msec
	unmute delay	time from mute input switches low until outputs unmuted			120		msec

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (SE)

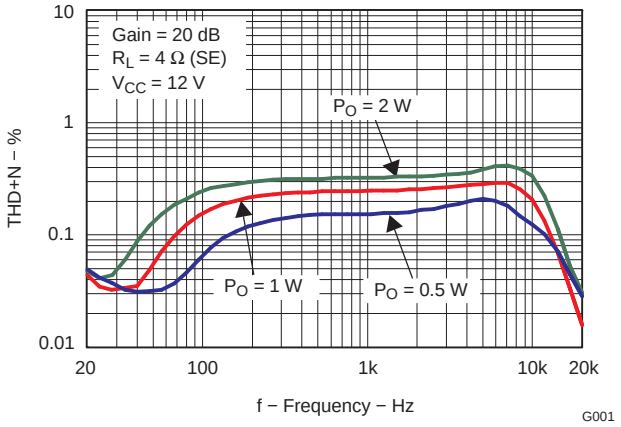


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (SE)

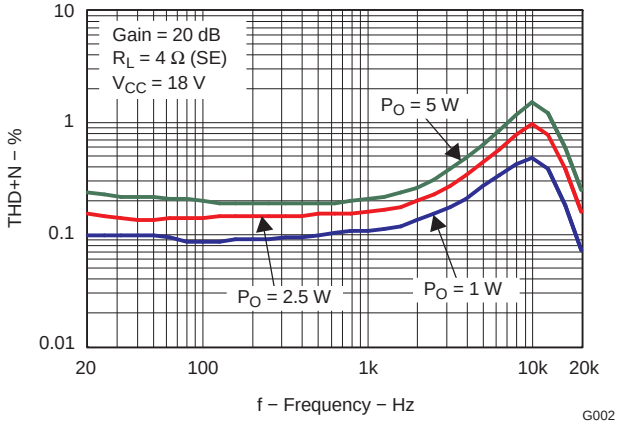


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (SE)

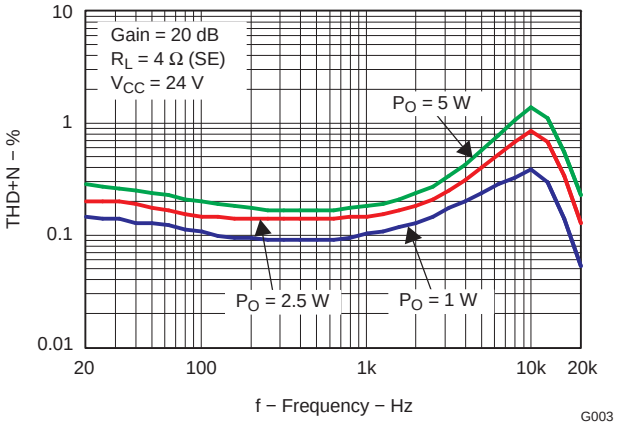


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (SE)

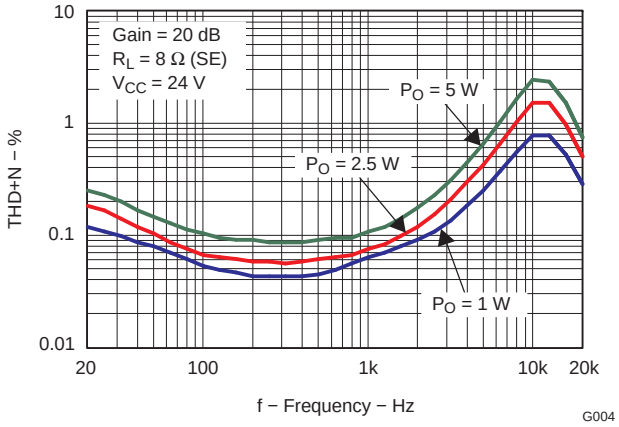


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (SE)

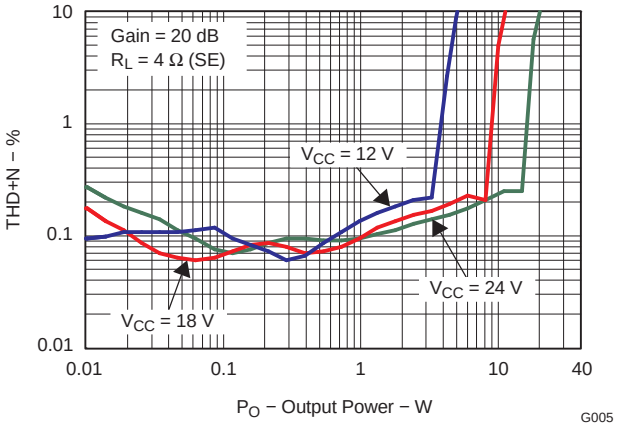


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (SE)

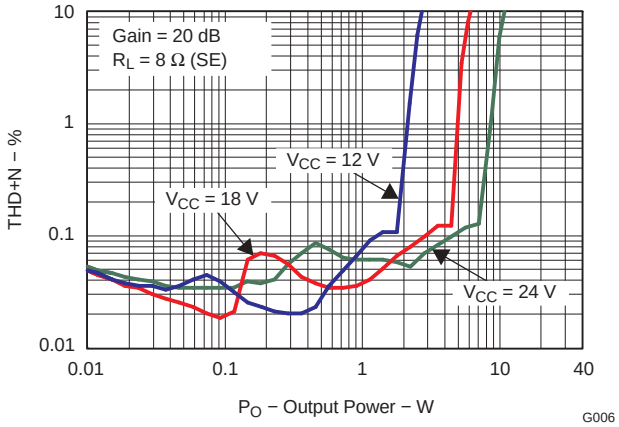


Figure 6.

TYPICAL CHARACTERISTICS (continued)

CROSSTALK vs FREQUENCY (SE)

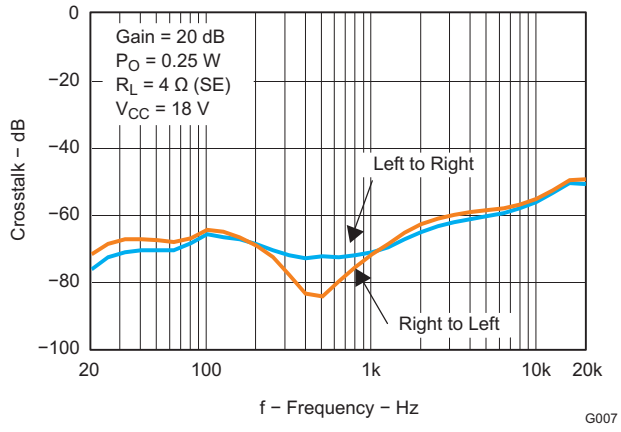


Figure 7.

CROSSTALK vs FREQUENCY (SE)

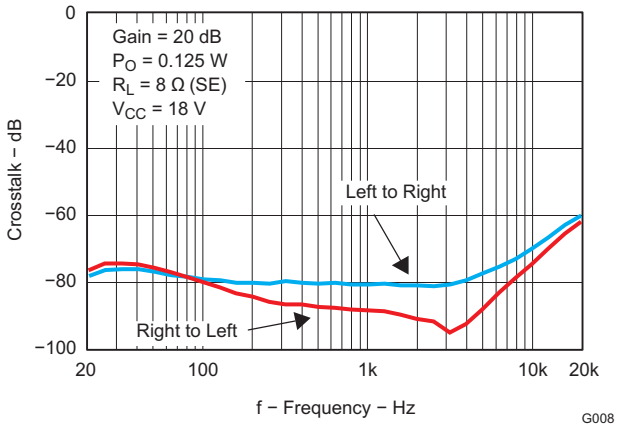


Figure 8.

GAIN/PHASE vs FREQUENCY (SE)

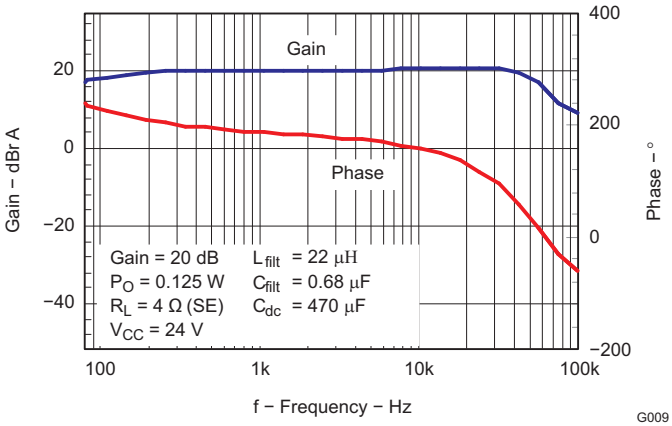


Figure 9.

GAIN/PHASE vs FREQUENCY (SE)

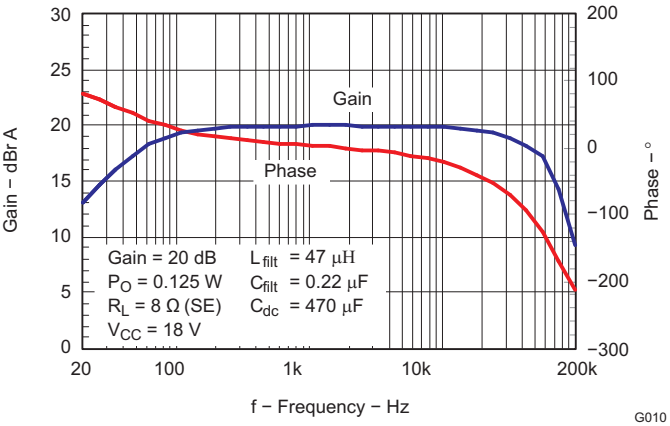
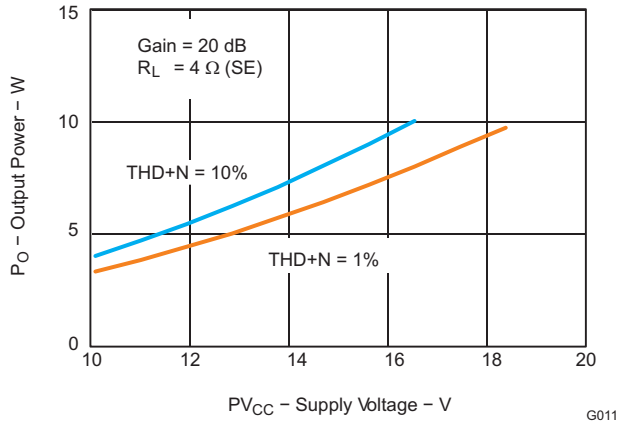


Figure 10.

OUTPUT POWER vs SUPPLY VOLTAGE (SE)



NOTE: Dashed line = Thermally limited

Figure 11.

OUTPUT POWER vs SUPPLY VOLTAGE (SE)

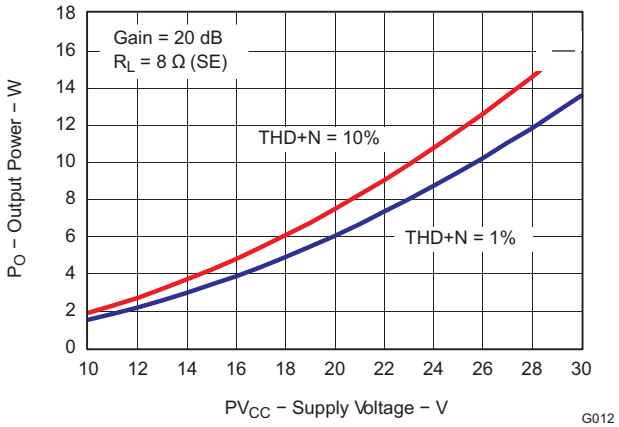


Figure 12.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs OUTPUT POWER (SE)

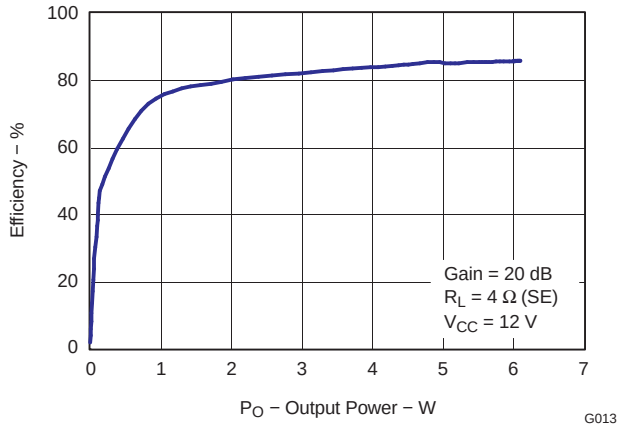


Figure 13.

EFFICIENCY vs OUTPUT POWER (SE)

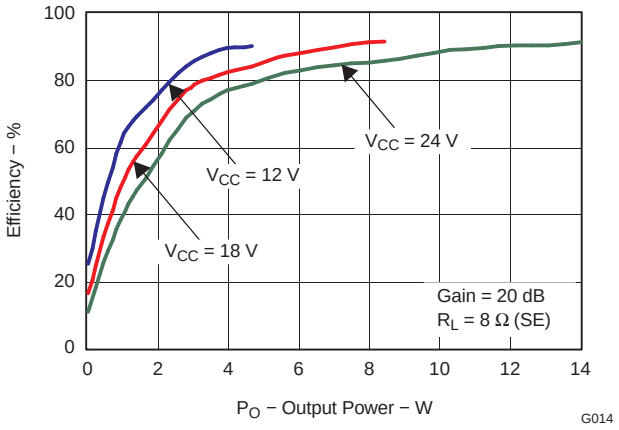


Figure 14.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (SE)

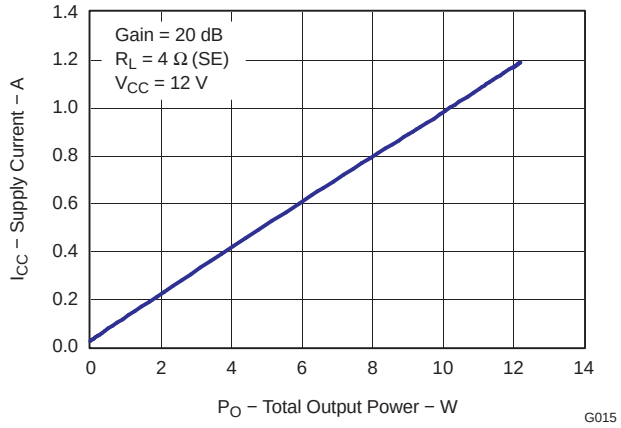


Figure 15.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (SE)

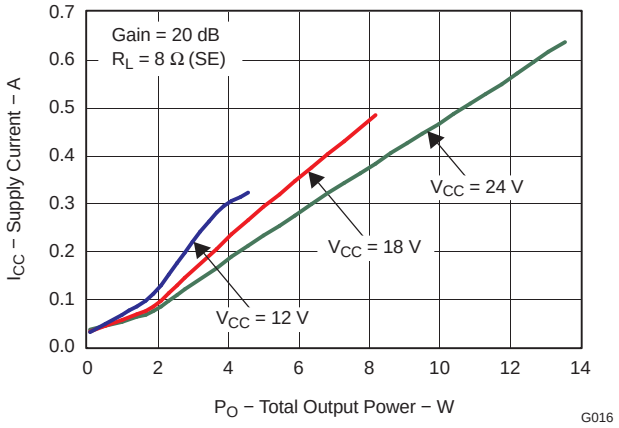


Figure 16.

POWER SUPPLY REJECTION RATIO vs FREQUENCY (SE)

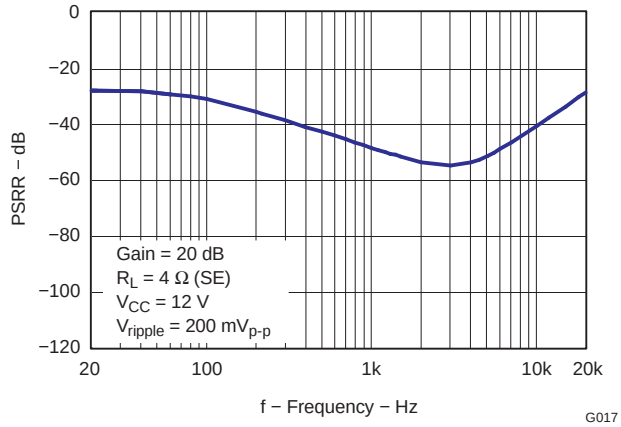


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (BTL)

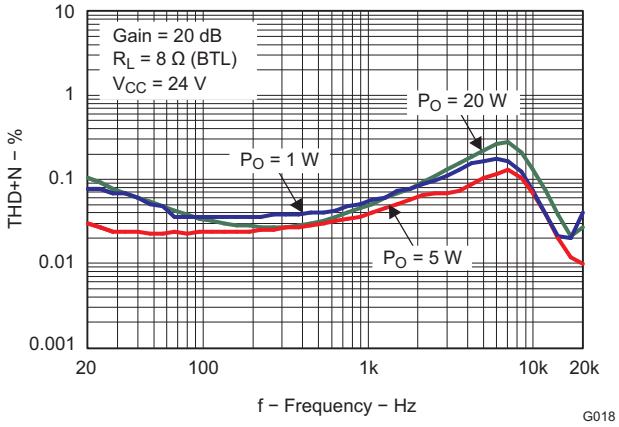


Figure 18.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (BTL)

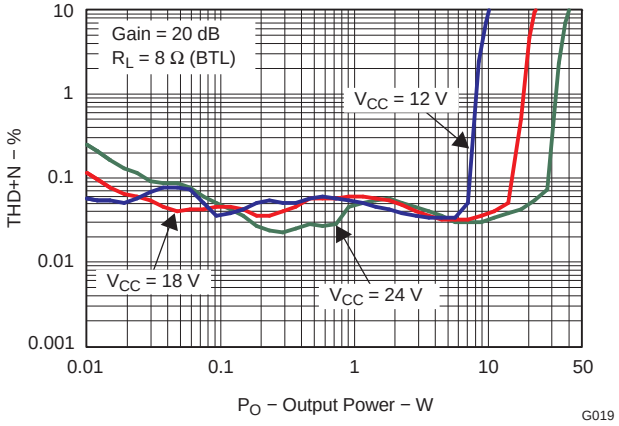


Figure 19.

GAIN/PHASE vs FREQUENCY (BTL)

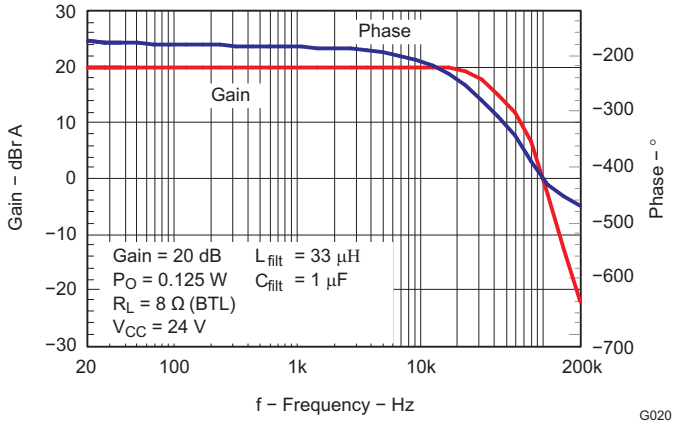


Figure 20.

OUTPUT POWER vs SUPPLY VOLTAGE (BTL)

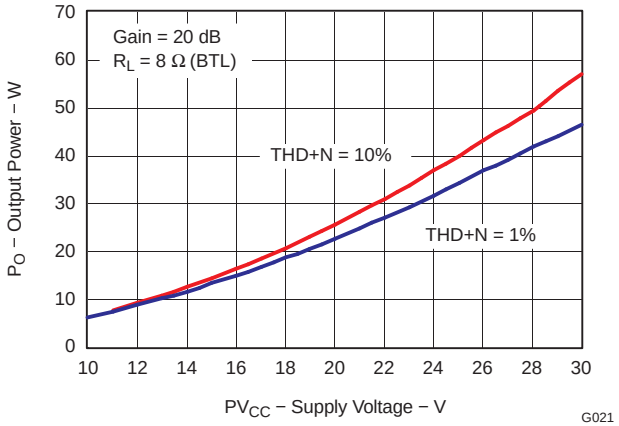


Figure 21.

EFFICIENCY vs OUTPUT POWER (BTL)

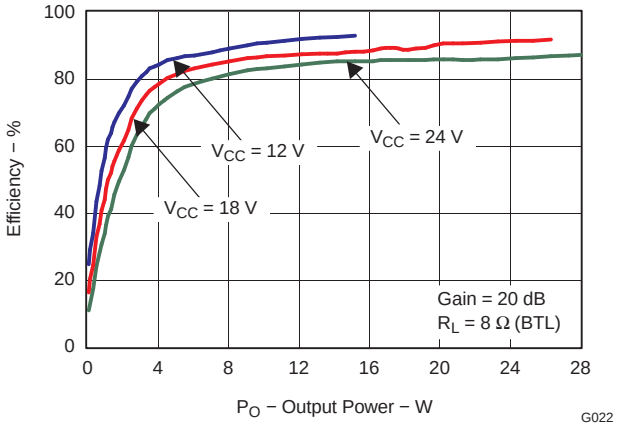


Figure 22.

SUPPLY CURRENT vs TOTAL OUTPUT POWER (BTL)

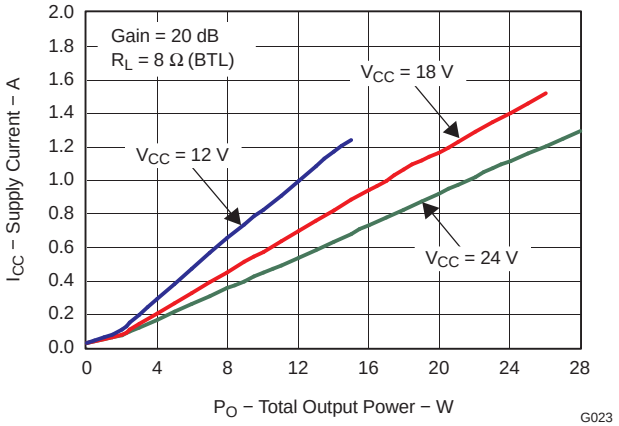


Figure 23.

POWER SUPPLY REJECTION RATIO vs FREQUENCY (BTL)

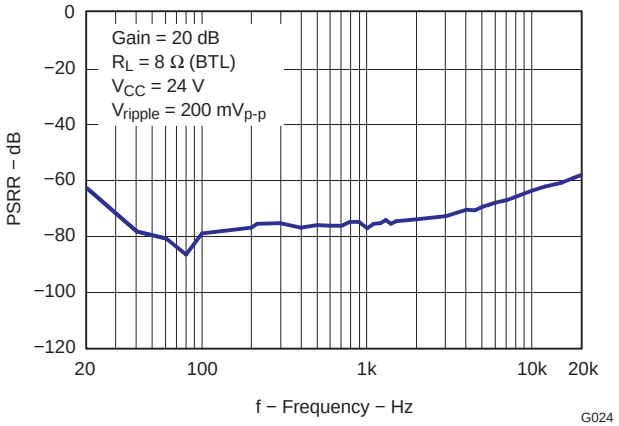


Figure 24.

APPLICATION INFORMATION

CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3122D2.

Traditional Class-D Modulation Scheme

The TPA3122D2 operates in AD mode. There are two main configurations that may be used. For stereo operation, the TPA3122D2 should be configured in a single-ended (SE) half bridge amplifier. For mono applications, TPA3122D2 may be used as a bridge tied load (BTL) amplifier. The traditional class-D modulation scheme, which is used in the TPA3122D2 BTL configuration, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential pre-filtered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 25.

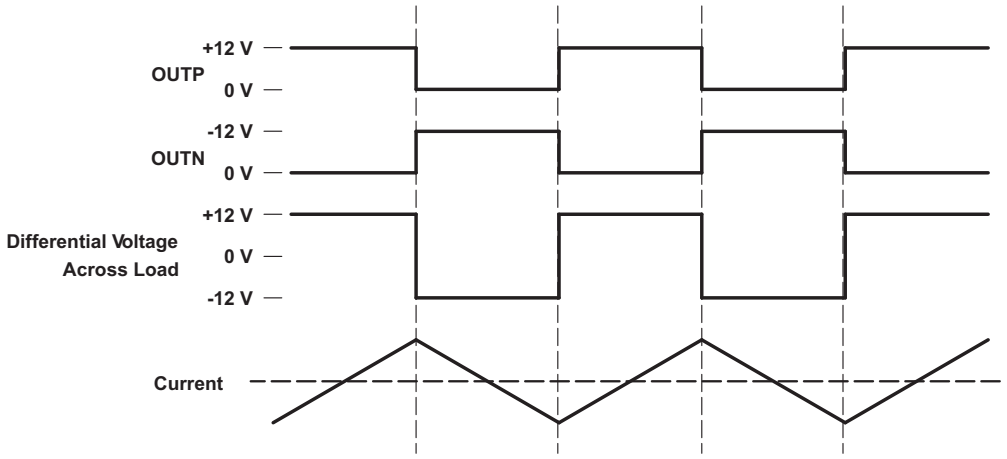


Figure 25. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms into an Inductive Load With No Input

Supply Pumping

One issue encountered in single-ended (SE) class-D amplifier designs is supply pumping. Power-supply pumping is a rise in the local supply voltage due to energy being driven back to the supply by operation of the class-D amplifier. This phenomenon is most evident at low audio frequencies and when both channels are operating at the same frequency and phase. At low levels, power-supply pumping results in distortion in the audio output due to fluctuations in supply voltage. At higher levels, pumping can cause the overvoltage protection to operate, which temporarily shuts down the audio output.

Several things can be done to relieve power-supply pumping. The lowest impact is to operate the two inputs out of phase 180° and reverse the speaker connections. Because most audio is highly correlated, this causes the supply pumping to be out of phase and not as severe. If this is not enough, the amount of bulk capacitance on the supply must be increased. Also, improvement is realized by hooking other supplies to this node, thereby, sinking some of the excess current. Power-supply pumping should be tested by operating the amplifier at low frequencies and high output levels.

Gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA3122D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

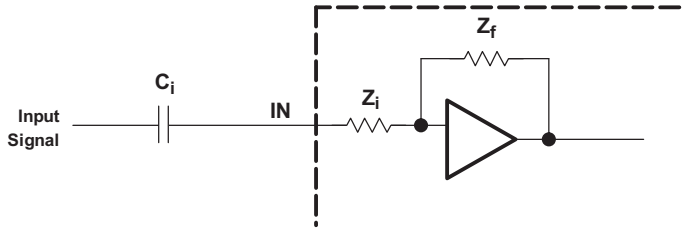
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 8 kΩ, which is the absolute minimum input impedance of the TPA3122D2. At the higher gain settings, the input impedance could increase as high as 72 kΩ

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYPICAL	TYPICAL
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

INPUT RESISTANCE

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 10 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



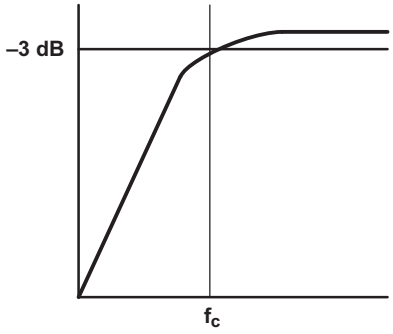
The -3-dB frequency can be calculated using Equation 1. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

INPUT CAPACITOR, C_I

In the typical application, an input capacitor ($_I$) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (2)$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example, C_I is 0.4 µF; so, one would likely choose a value of 0.47 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network ($_I$) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially

in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

Single Ended Output Capacitor, C_o

In single ended (SE) applications, the DC blocking capacitor forms a high pass filter with speaker impedance. The frequency response rolls of with decreasing frequency at a rate of 20dB/decade. The cutoff frequency is determined by

$$fc = 1/2\times\pi C_o Z_L$$

Table 2 shows some common component values and the associated cutoff frequencies:

Table 2. Common Filter Responses

Speaker Impedance (Ω)	C_{SE} – DC Blocking Capacitor (μF)		
	f_c = 60 Hz	f_c = 40 Hz	f_c = 20 Hz
4	680	1000	2200
8	330	470	1000

Output Filter and Frequency Response

For the best frequency response, a flat passband output filter (second order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the LOUT and ROUT pins. There are several possible configurations depending on the speaker impedance and whether the output configuration is Single Ended (SE) or Bridge Tied Load (BTL). Table 3 list several possible arrangements.

Table 3. Recommended Filter Output Components

Output Configuration	Speaker Impedance (Ω)	Filter Inductor (μH)	Filter Capacitor (nF)
Single Ended (SE)	4	22	680
	8	47	390
Bridge Tied Load	4	10	1500
	8	22	680

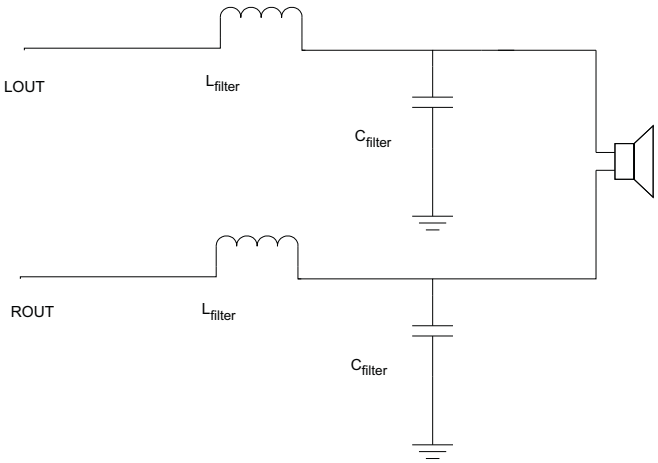


Figure 26. BTL Filter Configuration

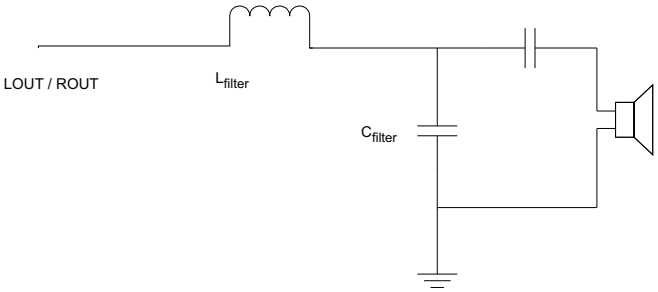


Figure 27. SE Filter Configuration

Power Supply Decoupling, C_S

The TPA3122D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended. The 220-µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-µF or larger capacitor should be placed on each PVCC terminal. A 10-µF capacitor on the AVCC terminal is adequate.

BSN and BSP Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220-nF capacitor must be connected from LOUT to BSL, and one 220-nF capacitor must be connected from ROUT to BSR.

The bootstrap capacitors connected between the BSx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. One 1-µF capacitor must be connected from VCLAMP (pin 11 for PWP and pin 9 for DIP package) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminal may vary with V_{CC} and may not be used for powering any other circuitry.

V_{BYP} Capacitor Selection

The scaled supply reference (V_{BYP}) nominally provides an AVcc/8 internal bias for the preamplifier stages. The external capacitor for this reference C_{BYP}) is a critical component and serves several important functions. During start-up or recovery from shutdown mode, C_{BSP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling with the output drive signal. This noise could result in degraded PSRR and THD + N.

The circuit is designed for a C_{BSP} value of 1 µF for best pop performance. The inputs caps should be the same value. A ceramic or tantalum low-ESR capacitor is recommended.

$\overline{\text{SHUTDOWN}}$ OPERATION

The TPA3122D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-up pop performance, place the amplifier in the shutdown or mute mode prior to applying the power supply voltage.

MUTE Operation

The MUTE pin is an input for controlling the output state of the TPA3122D2. A logic high on this terminal causes the outputs to run at a constant 50% duty cycle. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or switching between different audio sources.

The MUTE terminal should never be left floating. For power conservation, the $\overline{\text{SHUTDOWN}}$ terminal should be used to reduce the quiescent current to the absolute minimum level.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

SHORT-CIRCUIT PROTECTION

The TPA3122D2 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts and output-to-GND shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is an unlatched fault. Normal operation is restored when the fault is removed.

THERMAL PROTECTION

Thermal protection on the TPA3122D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3122D2 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 0.1µF decoupling capacitors should be placed as close to the PVCC (pins 1 and 10) and AVCC (pins 16 and 17) terminals as possible. The VBYP (pin 6) capacitor and VCLAMP (pin 9) capacitor should also be placed as close to the device as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3122D2 on the PVCCL and PVCCR terminals.
- Grounding—The AVCC (pins 16 and 17) decoupling capacitor and VBYP (pin 6) capacitor should each be grounded to analog ground (AGND, pins 7 and 8). The PVCCx decoupling capacitors and VCLAMP capacitors should each be grounded to power ground (PGND, pins 11 and 20). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3122D2.
- Output filter—The EMI filter (L1, L2, C9, and C16) should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.

For an example layout, see the TPA3122D2 Evaluation Module (TPA3122D2EVM) User Manual, (SLOU214). Both the EVM user manual and the thermal pad application note are available on the TI Web site at http://www.ti.com.

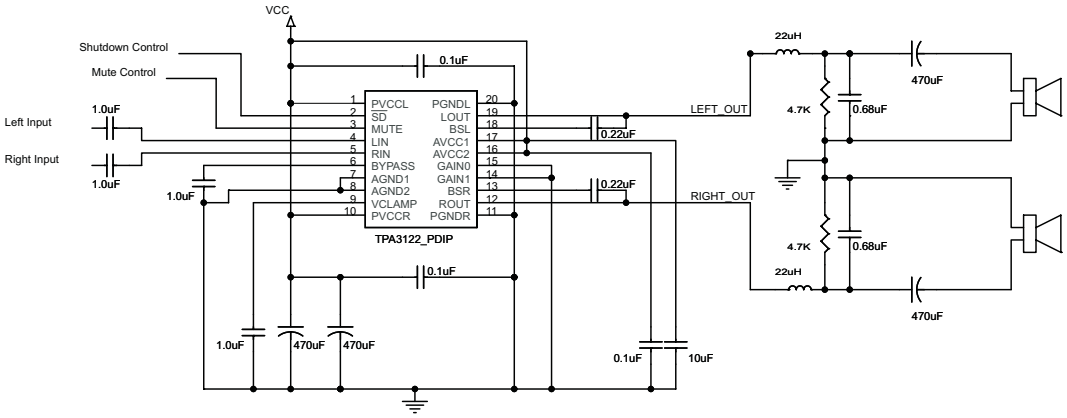


Figure 28. SE 4-Ω Application Schematic

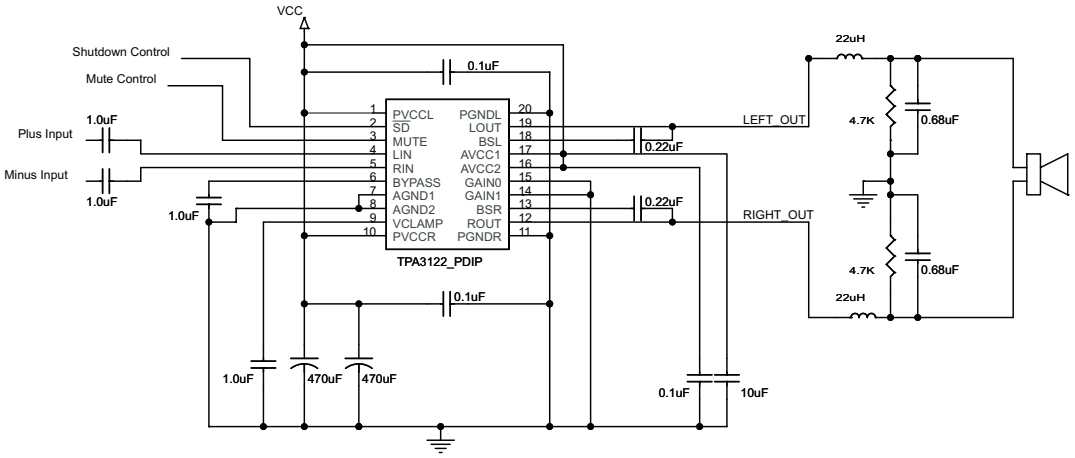


Figure 29. BTL 8-Ω Application Schematic

BASIC MEASUREMENT SYSTEM

This application note focuses on methods that use the basic equipment listed below:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 30 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer-input impedance should be high. The output resistance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 30(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 30(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.

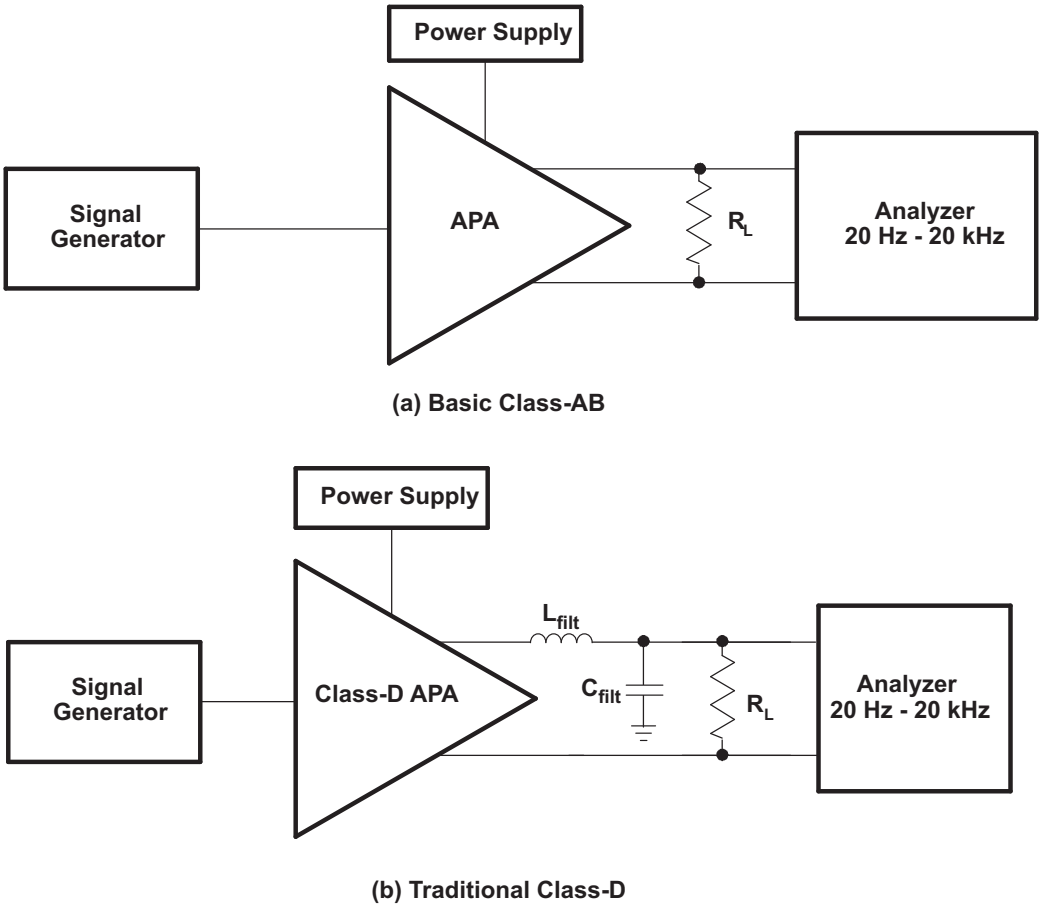


Figure 30. Audio Measurement Systems

SE Input and SE Output (TPA3122D2 Stereo Configuration)

The SE input and output configuration is used with class-AB amplifiers. A block diagram of a fully SE measurement circuit is shown in Figure 31. SE inputs normally have one input pin per channel. In some cases, two pins are present; one is the signal and the other is ground. SE outputs have one pin driving a load through an output ac coupling capacitor and the other end of the load is tied to ground. SE inputs and outputs are considered to be unbalanced, meaning one end is tied to ground and the other to an amplifier input/output.

The generator should have unbalanced outputs, and the signal should be referenced to the generator ground for best results. Unbalanced or balanced outputs can be used when floating, but they may create a ground loop that will effect the measurement accuracy. The analyzer should have balanced inputs to cancel out any common-mode noise in the measurement.

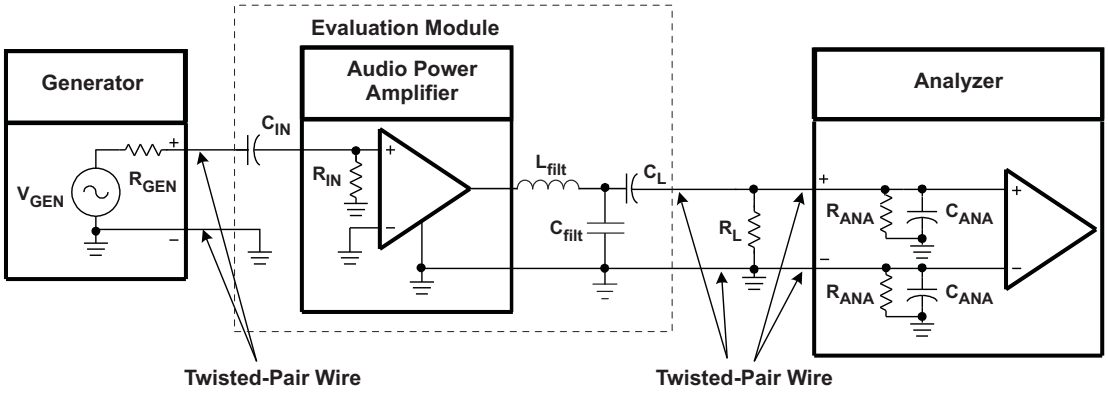


Figure 31. SE Input—SE Output Measurement Circuit

The following general rules should be followed when connecting to APAs with SE inputs and outputs:

- Use an unbalanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 4)

DIFFERENTIAL INPUT AND BTL OUTPUT (TPA3122D2 Mono Configuration)

Many of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 32. The differential input is a balanced input, meaning the positive (+) and negative (-) pins have the same impedance to ground. Similarly, the SE output equates to a balanced output.

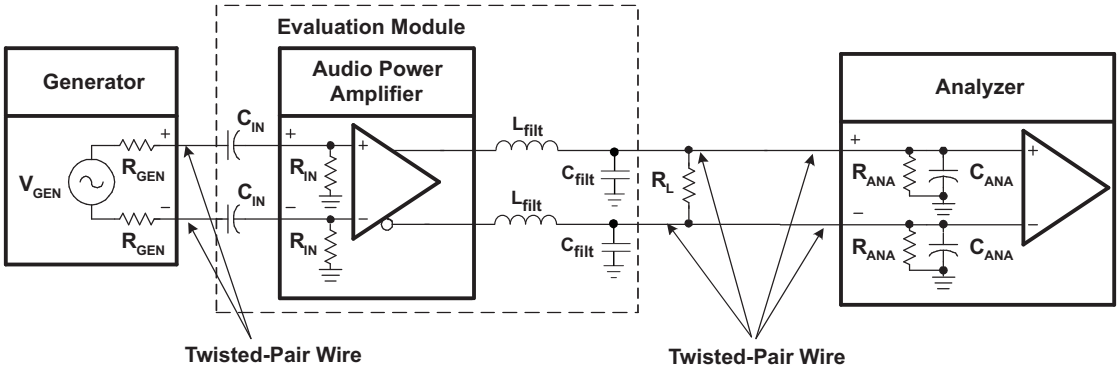


Figure 32. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 4).

Table 4 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

Table 4. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L(Ω)	AWG Size		DC POWER LOSS (MW)		AC POWER LOSS (MW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3122D2N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TPA3122D2
TPA3122D2N.Z	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TPA3122D2

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

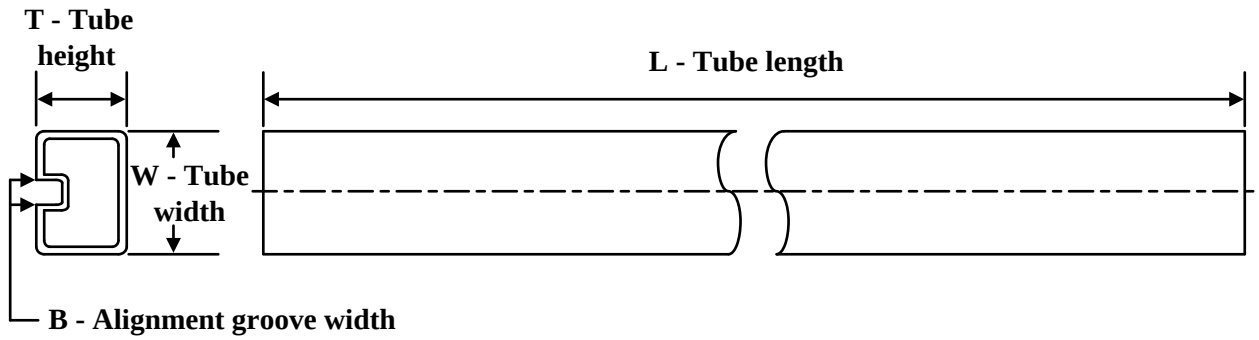
(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



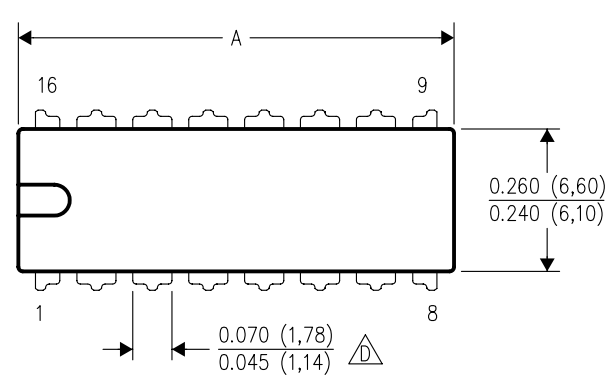
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3122D2N	N	PDIP	20	20	506	13.97	11230	4.32
TPA3122D2N.Z	N	PDIP	20	20	506	13.97	11230	4.32

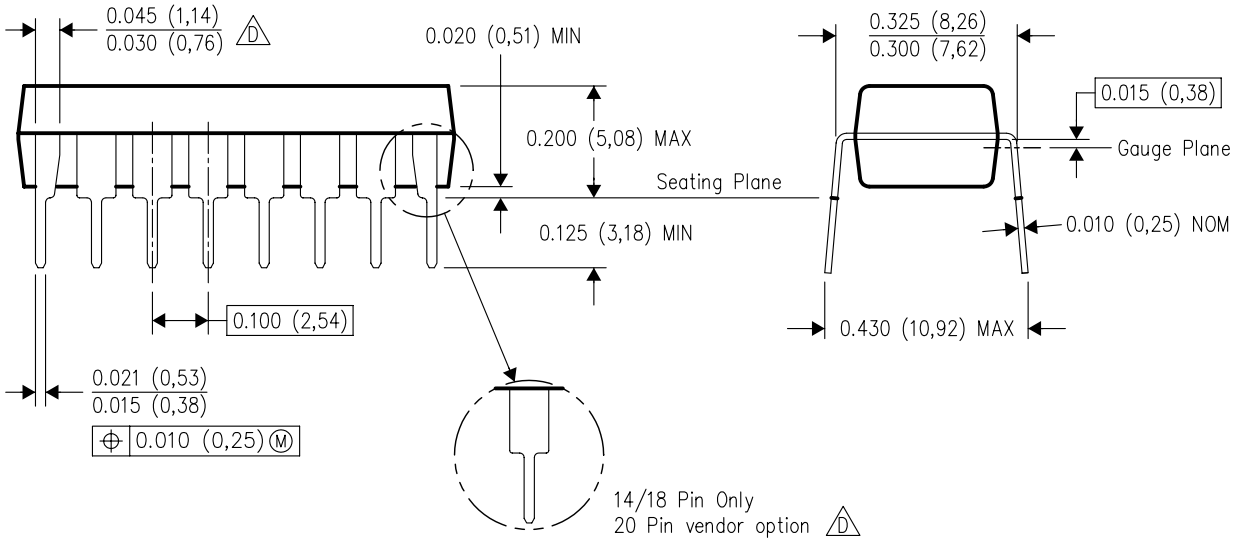
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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