TPS1H100-Q1 40V、100mΩ、シングルチャネル、スマート・ハイサイド・パワー・スイッチ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 –40°C～125°C
  - デバイス HBM ESD 分類レベル H3A
  - デバイス CDM ESD 分類レベル C4B
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 包括的な診断機能を備えたシングルチャネルのスマート・ハイサイド・パワー・スイッチ
  - バージョン A:オープン・ドレインのステータス出力
  - バージョン B:電流センス・アナログ出力
- 広い動作電圧範囲：3.5 ～ 40V
- 非常に低いスタンバイ電流：0.5µA 未満
- 動作時接合部温度範囲：–40～150°C
- 入力制御、3.3V および 5V ロジック互換
- 高精度電流センス：±30mA (1A 時)、±4mA (5mA 時)
- 外付け抵抗によるプログラマブル電流制限：±20% (0.5A 時)
- 診断イネーブル機能によって MCU のアナログ / デジタル・インターフェイスの多重化が可能
- AECQ100-12 グレード A に従ってテスト済み、100 万回の GND 短絡テスト
- 過渡電圧耐性に対する ISO7637-2 および ISO16750-2 の認定
- 保護
  - 過負荷および短絡保護
  - 誘導性負荷の負電圧クランプ
  - 低電圧誤動作防止 (UVLO) 保護
  - 自己回復可能なサーマル・シャットダウン / スイング
  - GND 喪失、電源喪失保護
  - 外部回路によるバッテリ逆極性保護
- 診断機能
  - オンおよびオフ状態での出力開放およびバッテリ短絡の検出
  - 過負荷およびグランド短絡検出、電流制限
  - サーマル・シャットダウン / スイング検出
- 熱特性強化型 14 ピン PWP パッケージ

2 アプリケーション

- サブモジュール用ハイサイド・パワー・スイッチ
- 低電力ランプ用パワー・スイッチ
- ハイサイド・リレーおよびソレノイド
- PLC デジタル出力パワー・スイッチ
- 一般的な抵抗性、誘導性、容量性負荷

3 概要

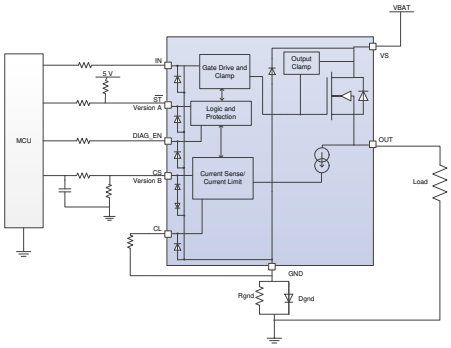
TPS1H100-Q1デバイスは各種の保護機能を搭載したハイサイド・パワー・スイッチで、NMOSパワーFETとチャージ・ポンプを内蔵して、抵抗性、誘導性、容量性の各種負荷をインテリジェントに制御することを目標にしています。高精度の電流センスとプログラマブル電流制限機能により、市場での差別化に役立ちます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS1H100-Q1	HTSSOP (14)	4.40mm×5.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (June 2018) から Revision D に変更 — **Page**

- 「*特長*」セクションに機能安全対応のリンクを追加 ... 1

Revision B (June 2015) から Revision C に変更 — **Page**

- Changed the *Pin Functions* table to alphabetical order and created separate columns for the Version A and Version B devices ... 3
- Added tablenotes to the *Electrical Characteristics* table ... 7
- 「*ドキュメントの更新通知を受け取る方法*」セクションを追加 ... 39

Revision A (January 2015) から Revision B に変更 — **Page**

- Updated Figure 6 and Figure 7 ... 10
- Updated Figure 38 ... 25
- Updated Figure 39 ... 26
- Updated Figure 40 ... 27
- 「*コミュニティ・リソース*」を追加 ... 39

2014年10月発行のものから更新 — **Page**

- デバイス・ステータスをプレビューから量産データに更新 ... 1

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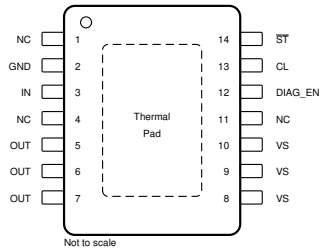
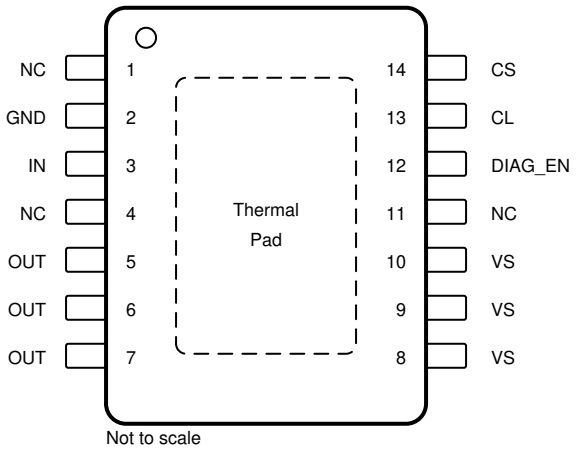
5 Pin Configuration and Functions

PWP Package Version A
14-Pin HTSSOP
Top View



PWP Package Version B
14-Pin HTSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VER. A	VER. B		
CL	13	13	O	Programmable current-limit pin. Connect to device GND if external current limit is not used.
CS	—	14	O	Current-sense output. Leave floating if not used.
DIAG_EN	12	12	I	Enable and disable pin for diagnostic functions. Connect to device GND if not used.
GND	2	2	—	Ground pin
IN	3	3	I	Input control for channel activation
NC	1, 4, 11	1, 4, 11	—	No-connect pin; leave floating.
OUT	5, 6, 7	5, 6, 7	O	Output, connected to load (NMOS source)
$\overline{ST}$	14	—	O	Open-drain diagnostic status output. Leave floating if not used.
VS	8, 9, 10	8, 9, 10	I	Power supply; battery voltage
Thermal pad	—	—	—	Thermal pad. Connect to device GND or leave floating.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1][2][3]

	MIN	MAX	UNIT
Supply voltage[4], t < 400 ms		48	V
Reverse polarity voltage[5]	–18		V
Continuous drain current	Internally limited		A
Reverse current on GND	–50	20	mA
Reverse current on GND, t < 120 s	–250	20	mA
Voltage on IN/DIAG_EN pin	–0.3	7	V
Current on IN /DIAG_EN pin	–30	2	mA
Voltage on $\overline{ST}$ pin	–0.3	7	V
Current on $\overline{ST}$ pin	–30	10	mA
IN pin PWM frequency		2	KHz
Voltage on CL pin	–0.3	7	V
Current on CL pin	–2	30	mA
Voltage on CS pin	–2.7	6.5	V
Current on CS pin	–2	30	mA
Inductive load switch-off energy dissipation, single pulse[6]		70	mJ
Operating ambient temperature	–40	125	°C
Operating junction temperature	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute negative voltage on these terminals is not to go below –0.3 V.
(4) Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.
(5) Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-kΩ resistor in parallel with diode.
(6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-µm Cu, 2- × 35-µm Cu. 600-mm^2 thermal pad copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) AEC-Q100 Classification Level H3A[1]	VS, OUT, GND	±5000	V
		Human body model (HBM) AEC-Q100 Classification Level H2[1]	Other pins	±4000	
		Charged device model (CDM), per AEC Q100-011[2]		±750	

(1) The human-body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
(2) The charged-device model is tested according to AEC_Q100-011C.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Operating voltage	5	40	V
	Voltage on IN/DIAG_EN pin	0	5	V
	Voltage on $\overline{ST}$ pin	0	5	V
$I_{o,nom}$	Nominal DC load current	0	4	A
T_J	Operating junction temperature range	–40	150	°C

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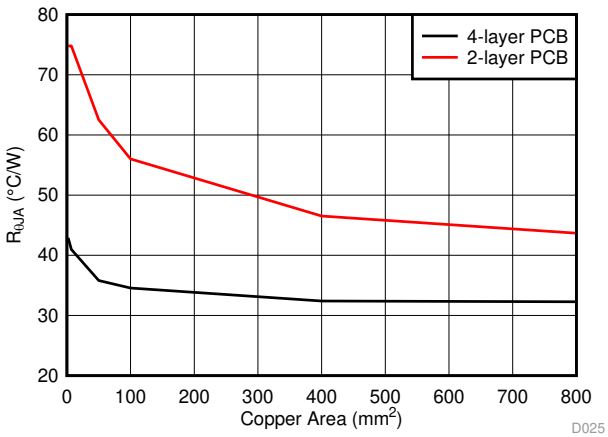
6.4 Thermal Information

THERMAL METRIC[1]		TPS1H100-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	41	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.



(1) 4-layer board: FR4 2s2p board, 2.8-mil copper (top/bottom), 1.4-mil copper (internal layers). 76.4- × 114.3- × 1.5-mm board size.

(2) 2-layer board: FR4 2s0p board, 2.8-mil copper (top/bottom). 76.4- × 114.3- × 1.5-mm board size.

Figure 1. $R_{\theta JA}$ Value vs Copper Area

6.5 Electrical Characteristics

5 V < V_S < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{S,nom}$	Nominal operating voltage		5		40	V
$V_{S,op}$	Extended operating voltage	$R_{DS(on)}$ value increases maximum 20%, compared to 5 V, see $R_{DS(on)}$ parameter	3.5		5	V
$V_{S,UVR}$	Undervoltage restart	V_S rises up, V_S > $V_{S,UVR}$, device turn on	3.5	3.7	4	V
$V_{S,UVF}$	Undervoltage shutdown	V_S falls down, V_S < $V_{S,UVF}$, device shuts off	3	3.2	3.5	V
$V_{UV,hys}$	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
I_{nom}	Nominal operating current	V_{IN} = 5 V, V_{DIAG_EN} = 0 V, no load			5	mA
		V_{IN} = 5 V, V_{DIAG_EN} = 0 V, 10-Ω load			10	mA
I_{off}	Standby current	V_S = 13.5 V, V_{IN} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTPUT} = 0 V, T_J = 25°C			0.5	µA
		V_S = 13.5 V, V_{IN} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTPUT} = 0 V, T_J = 125°C			5	µA
$I_{off,diag}$	Standby current with diagnostic enabled	V_{IN} = 0 V, V_{DIAG_EN} = 5 V			1.2	mA
$t_{off,deg}$	Standby mode deglitch time(1)	IN from high to low, if deglitch time > $t_{off,deg}$, enters into standby mode.		2		ms
$I_{leak,out}$	Off-state output leakage current	V_S = 13.5 V, V_{IN} = V_{OUTPUT} = 0, T_J = 25°C			0.5	µA
		V_S = 13.5 V, V_{IN} = V_{OUTPUT} = 0, T_J = 125°C			3	µA
POWER STAGE						
R_{DS-ON}	On-state resistance	V_S > 5 V, T_J = 25°C		80	100	mΩ
		V_S > 5 V, T_J = 150°C			166	mΩ
		V_S = 3.5 V, T_J = 25°C			120	mΩ
$I_{lim,nom}$	Internal current limit		7		13	A
$II_{im,tsd}$	Current limit during thermal shutdown	Internal current limit, thermal cycling condition		5		A
		External current limit, thermal cycling condition; Percentage of current limit set value		50%		
V_{DS}	Clamp drain-to-source voltage internally clamped		50		70	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain-to-source diode voltage	V_{IN} = 0, I_{OUT} = −0.2 A		0.7		V
I_{rev1}	Continuous reverse current when reverse polarity(2)	t < 60 s, V_S = 13.5 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. See I_{rev1} test condition (Figure 6).		4		A
I_{rev2}	Continuous reverse current when V_{OUT} > V_S + V_{diode}(2)	t < 60 s, V_S = 13.5 V. T_J = 25°C. See I_{rev2} test condition (Figure 7).		2		A
LOGIC INPUT (IN AND DIAG_EN)						
$V_{logic,h}$	Input or DIAG_EN high-level voltage		2			V
$V_{logic,l}$	Input or DIAG_EN low-level voltage				0.8	V
$V_{logic,hys}$	Input or DIAG_EN hysteresis voltage			250		mV
$R_{pd,in}$	Input pulldown resistor			500		kΩ
$R_{pd,diag}$	Diag pulldown resistor			150		kΩ

(1) Value is specified by design, not subject to production test.
(2) Value is based on the minimum value of the 10 pcs/3 lots samples.

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Electrical Characteristics (continued)

5 V < V_S < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
$I_{loss,gnd}$	Loss-of-ground output leakage current				100	µA
$V_{ol,off}$	Open-load detection threshold in off-state	V_{IN} = 0 V, When V_S – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.	1.4	1.8	2.6	V
$I_{ol,off}$	Off-state output sink current with open load	V_{IN} = 0 V, V_S = V_{OUT} = 13.5 V, T_J = 125°C.			–50	µA
$t_{ol,off}$	Open-load detection-threshold deglitch time in off state	V_{IN} = 0 V, When V_S – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.		600		µs
$I_{ol,on}$	Open-load detection threshold in on state	V_{IN} = 5 V, when I_{OUT} < $I_{ol,on}$, duration longer than $t_{ol,on}$. Open load detected. Version A only	2	6	10	mA
$t_{ol,on}$	Open-load detection-threshold deglitch time in on-state	V_{IN} = 5 V, when I_{OUT} < $I_{ol,on}$, duration longer than $t_{ol,on}$. Open load detected. Version A only		700		µs
V_{ST}	Status low output voltage	I_{ST} = 2 mA Version A only			0.4	V
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD,rst}$	Thermal shutdown status reset			155		
T_{sw}	Thermal swing shutdown threshold			60		
T_{hys}	Hysteresis for resetting the thermal shutdown and swing			10		
CURRENT SENSE (VERSION B) AND CURRENT LIMIT						
K	Current sense current ratio			500		
K_{CL}	Current limit current ratio			2000		
dK/K	Current-sense accuracy	I_{load} ≥ 5 mA	–80		80	%
		I_{load} ≥ 25 mA	–10		10	
		I_{load} ≥ 50 mA	–7		7	
		I_{load} ≥ 0.1 A	–5		5	
		I_{load} ≥ 1 A	–3		3	
dK_{CL}/K_{CL}	External current-limit accuracy (3) (4)	I_{limit} ≥ 0.5 A	–20		20	%
		I_{limit} ≥ 1.6 A	–14		14	
$V_{CS,lin}$	Linear current sense voltage range (1)	V_S ≥ 5 V	0		4	V
$I_{OUT,lin}$	Linear output current range (1)	V_S ≥ 5 V, $V_{CS,lin}$ ≤ 4 V	0		4	A
$V_{CS,H}$	Current-sense fault high voltage	V_S ≥ 7 V	4.3	4.75	4.9	V
		V_S ≥ 5 V	Min(V_S – 0.8, 4.3)		4.9	
$I_{CS,H}$	Current sense fault condition current	V_{CS} = 4.3 V, V_S > 7 V	10			mA
$V_{CL,th}$	Current limit internal threshold voltage (1)			1.233		V
$I_{CS,leak}$	Current sense leakage current in disabled mode	V_{IN} = 5 V, R_{load} = 10 Ω, V_{DIAG_EN} = 0 V, T_J = 125°C			1	µA
		V_{IN} = 0 V, V_{DIAG_EN} = 0 V, T_J = 125°C			1	µA

(3) External current-limit accuracy is only applicable to overload conditions greater than 1.5× the current-limit setting.
(4) External current-limit setting is recommended to be higher than 500 mA.

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6.6 Timing Requirements – Current Sense Characteristics(1)

			MIN	NOM	MAX	UNIT
$t_{CS,off1}$	CS settling time from DIAG disabled	V_{IN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 5 to 0 V. CS to 10% of sense value.			10	µs
$t_{CS,on1}$	CS settling time from DIAG enabled	V_{IN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 0 to 5 V. CS to 90% of sense value.			10	µs
$t_{CS,off2}$	CS settling time from IN falling edge	V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. IN from 5 to 0 V. CS to 10% of sense value.			10	µs
		V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. IN from 5 to 0 V. Current limit triggered.			180	µs
$t_{CS,on2}$	CS settling time from IN rising edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{load} ≥ 100 mA. V_{IN} from 0 to 5 V. CS to 90% of sense value.			150	µs

(1) Value specified by design, not subject to production test.

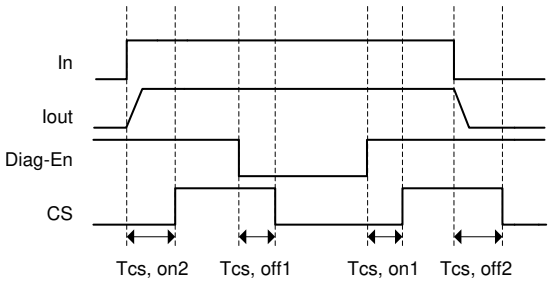

Figure 2. CS Delay Characteristics

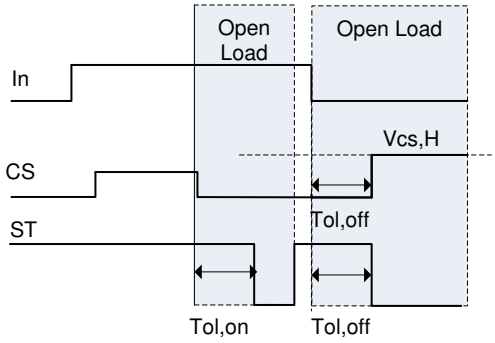

Figure 3. Open-Load Blanking Time Characteristics

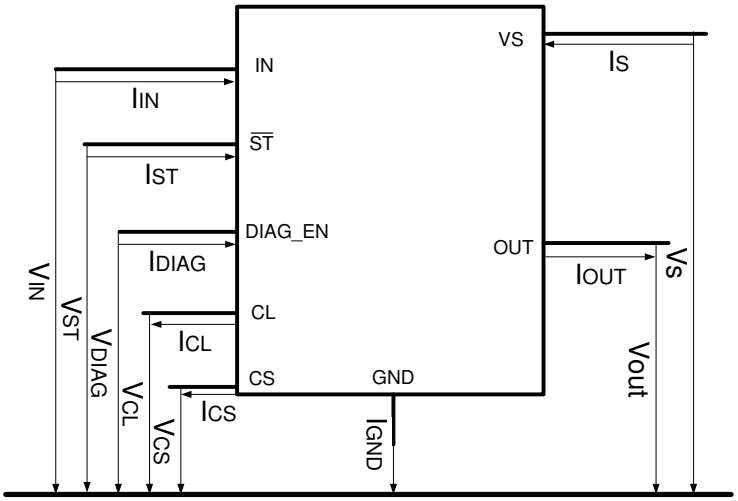

Figure 4. Pin Current and Voltage Conventions

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6.7 Switching Characteristics

V_{VS} = 13.5 V, R_{load} = 10 Ω, over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d,ON}$	Turn-on delay time	IN rising edge to V_{OUT} = 10%, DIAG_EN high	20		50	µs
$t_{d,OFF}$	Turn-off delay time	IN falling edge to V_{OUT} = 90%, DIAG_EN high	20		50	µs
dV/dt_{ON}	Slew rate on	V_{OUT} = 10% to 90%, DIAG_EN high	0.1		0.5	V/µs
dV/dt_{OFF}	Slew rate off	V_{OUT} = 90% to 10%, DIAG_EN high	0.1		0.5	V/µs
	Slew rate on and off matching		–0.15		0.15	V/µs

(1) Value specified by design, not subject to production test.

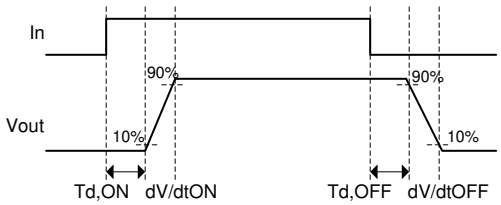

Figure 5. Switching Characteristics Diagram

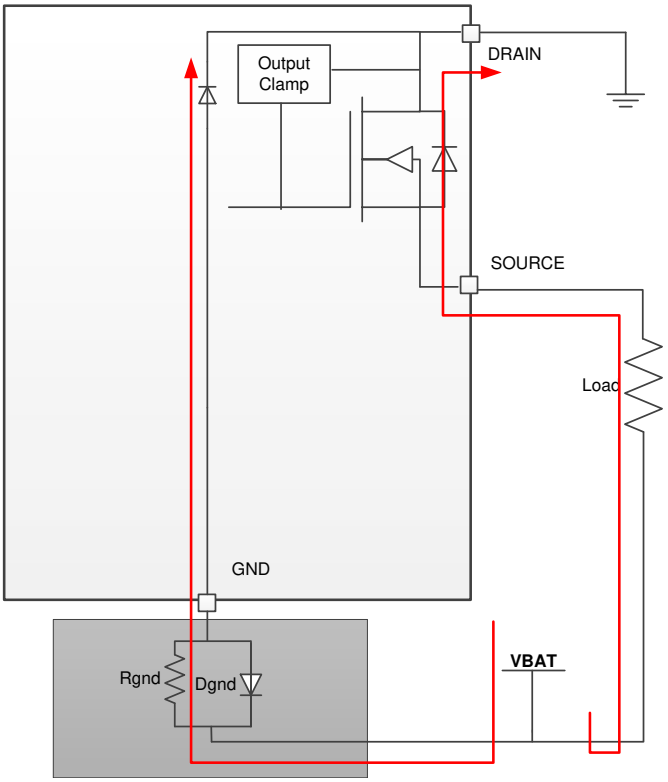

Figure 6. I_{rev1} Test Condition

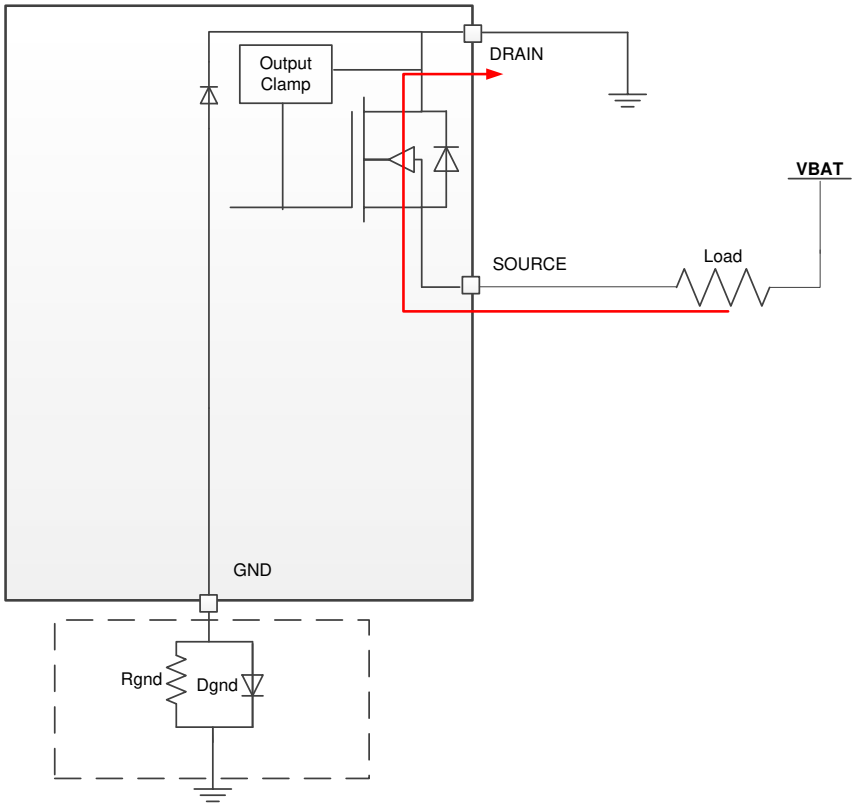

Figure 7. I_{rev2} Test Condition

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6.8 Typical Characteristics

All the following data are based on the mean value of the three lots samples, V_{VS} = 13.5 V if not specified.

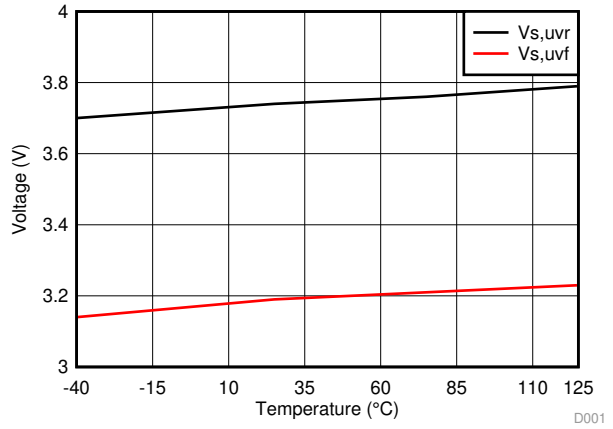

Figure 8. $V_{VS,UVR}$ and $V_{VS,UVF}$

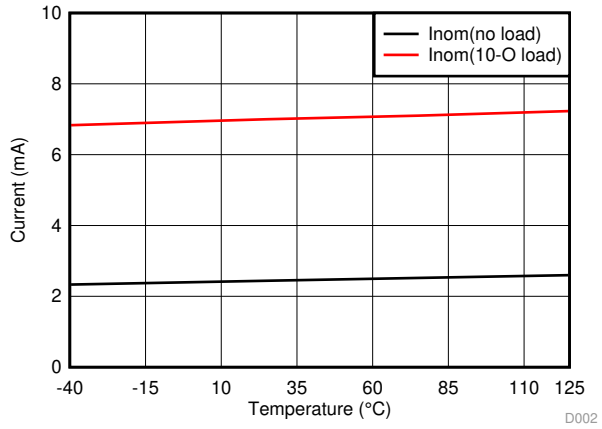

Figure 9. I_{nom} With No Load and 10-Ω Load

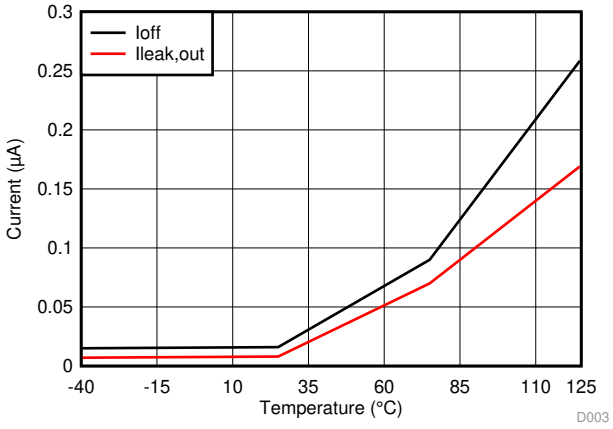

Figure 10. I_{off} and $I_{leak,out}$

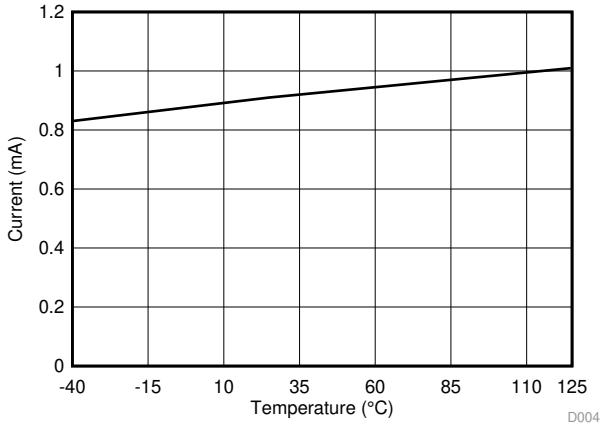

Figure 11. $I_{off,diag}$

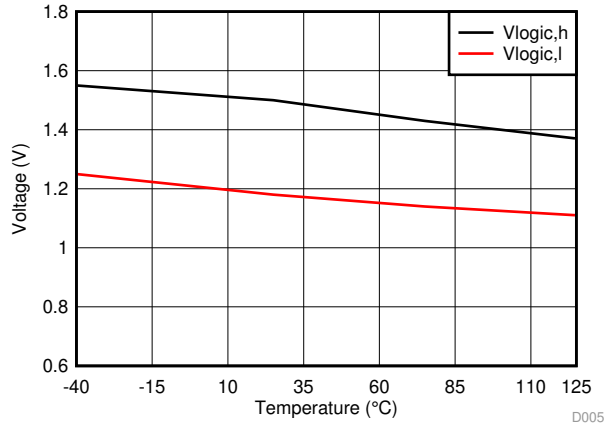

Figure 12. $V_{logic,h}$ and $V_{logic,l}$

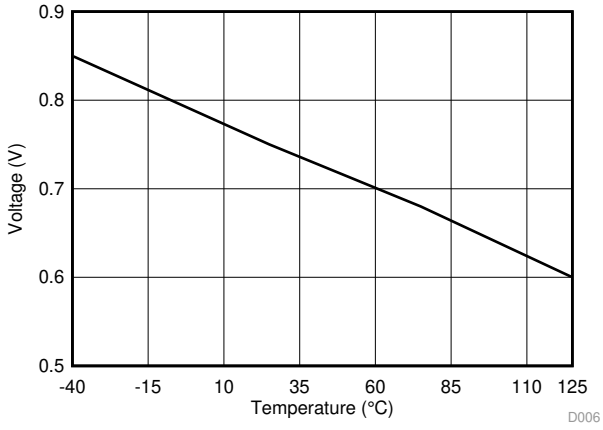

Figure 13. VF

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Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VS} = 13.5 V if not specified.

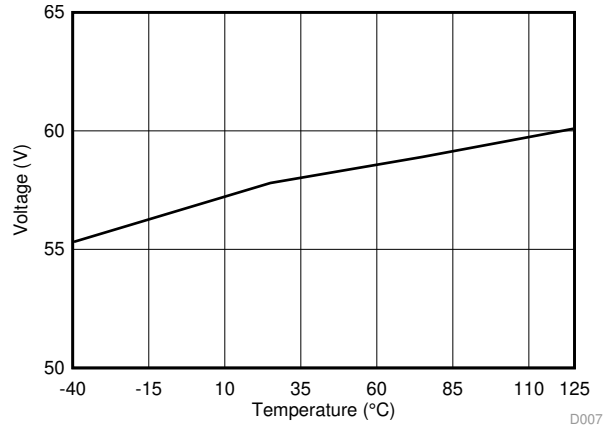

Figure 14. $V_{DS,\ clamp}$

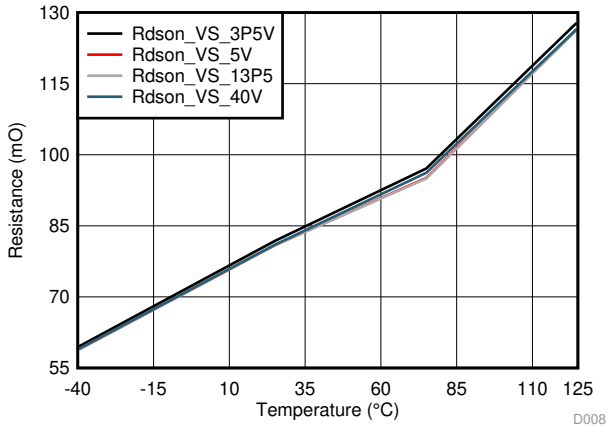

Figure 15. R_{DSON}

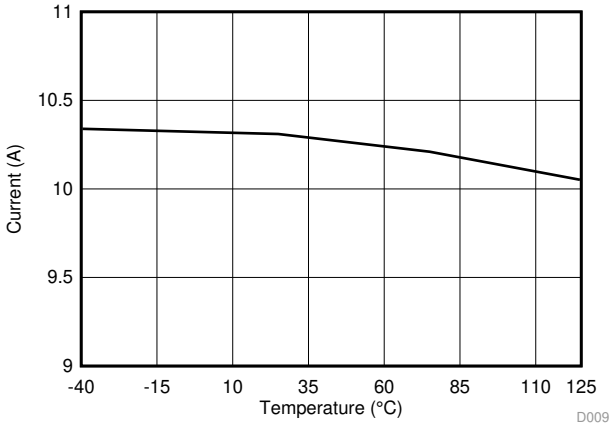

Figure 16. $I_{lim,nom}$

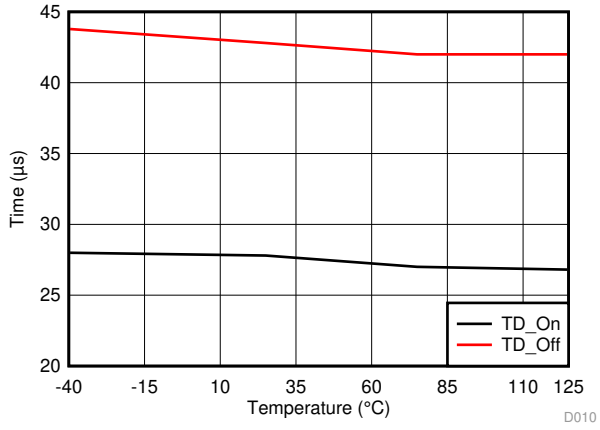

Figure 17. TDon and TDoff

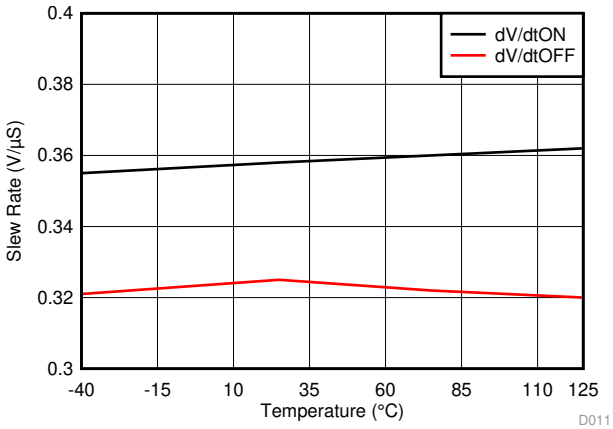

Figure 18. dV/dtON and dV/dtOFF

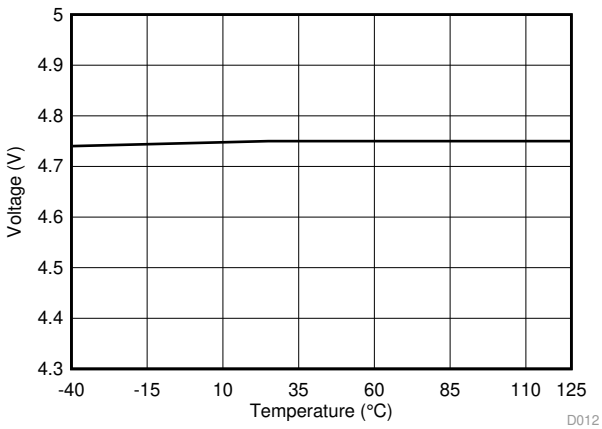

Figure 19. $V_{CS,h}$

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Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VS} = 13.5 V if not specified.

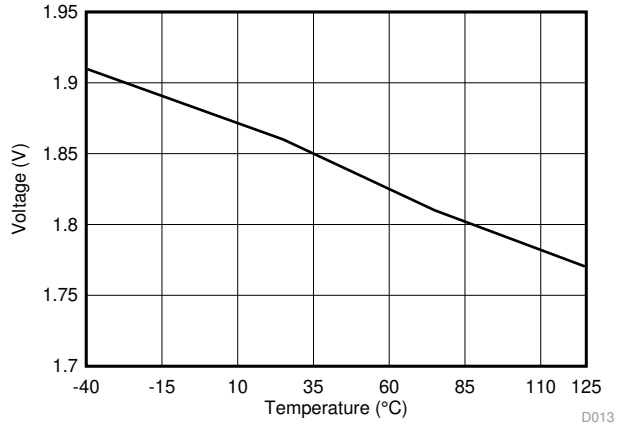

Figure 20. $V_{ol,off}$

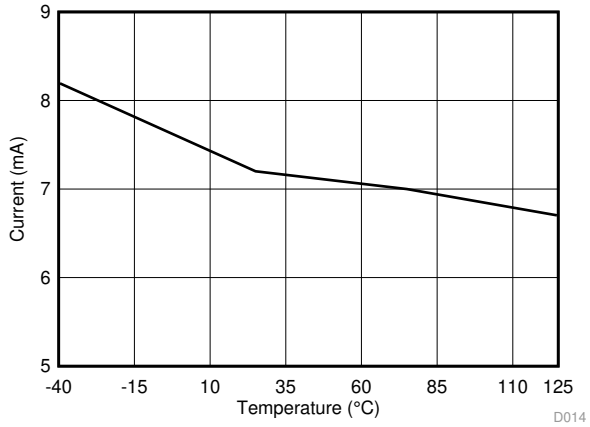

Figure 21. $I_{ol,on}$

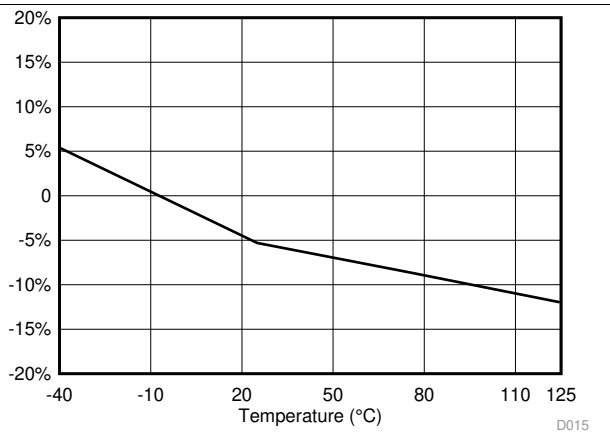

Figure 22. K_{CS} = 5 mA, 13.5 V

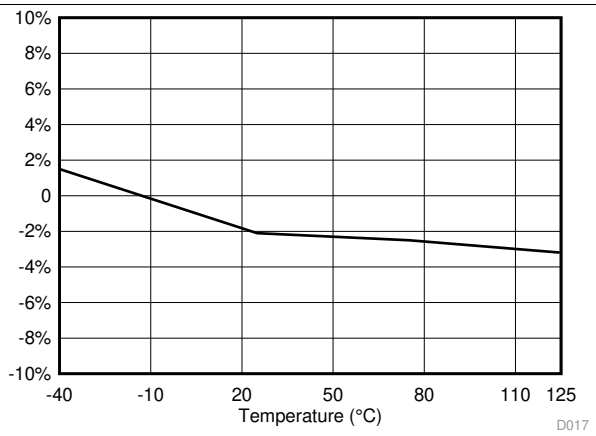

Figure 23. K_{CS} = 25 mA, 13.5 V

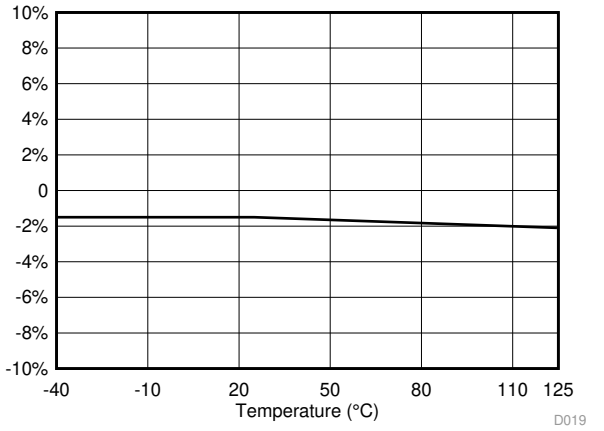

Figure 24. K_{CS} = 50 mA, 13.5 V

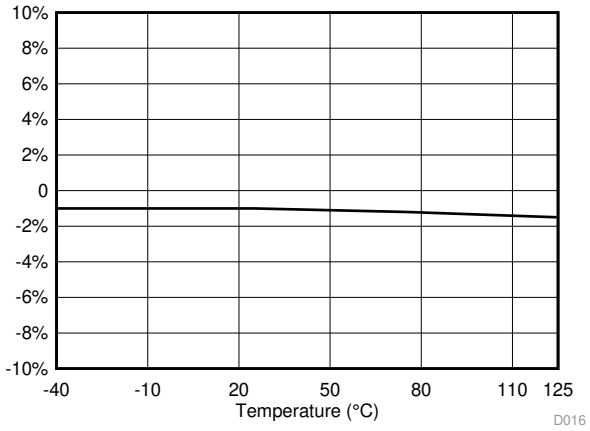

Figure 25. K_{CS} = 100 mA, 13.5 V

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Typical Characteristics (continued)

All the following data are based on the mean value of the three lots samples, V_{VS} = 13.5 V if not specified.

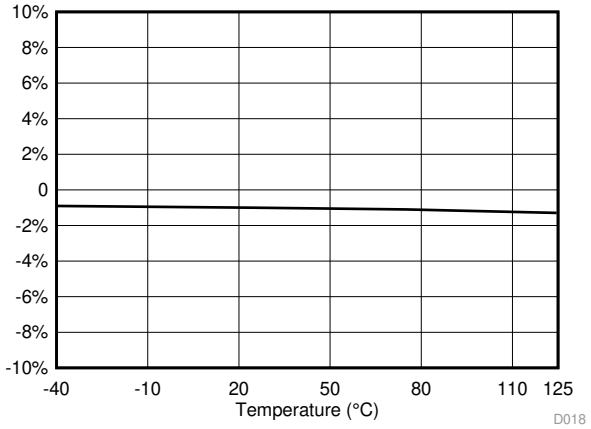

Figure 26. K_{CS} = 1 A, 13.5 V

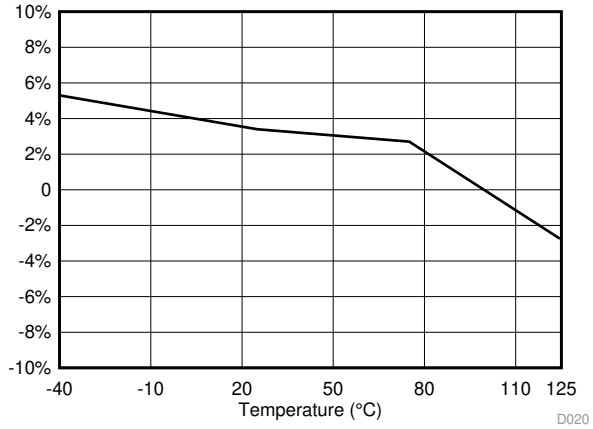

Figure 27. K_{CL} = 0.5 A, 13.5 V

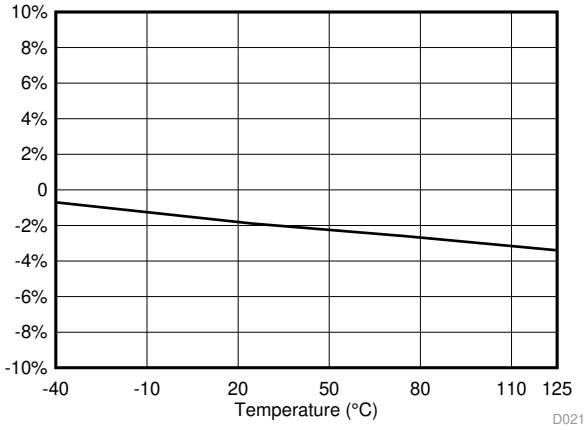

Figure 28. K_{CL} = 1.6 A, 13.5 V

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7 Detailed Description

7.1 Overview

The TPS1H100-Q1 is a single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital status and analog current-sense output, both of which can be set to the high-impedance state when diagnostics are disabled, for multiplexing the MCU analog or digital interface among devices.

For version A, the digital status report is implemented with an open-drain structure. When a fault condition occurs, it pulls down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. For version B, high-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K of the load current, which is reflected as voltage on the CS pin. K is a constant value across the temperature and supply voltage. The current-sensing function operates normally within a wide linear region from 0 to 4 V. The CS pin can also report a fault by pulling up the voltage of $V_{CS,h}$.

The external high-accuracy current limit allows setting the current limit value by application. It highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, it can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit is also implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain and source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, the TPS1H100-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. See *Inductive-Load Switching-Off Clamp* for more details.

Short-circuit reliability is critical for smart high-side power-switch devices. The standard of AEC-Q100-012 is to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

The TPS1H100-Q1 device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

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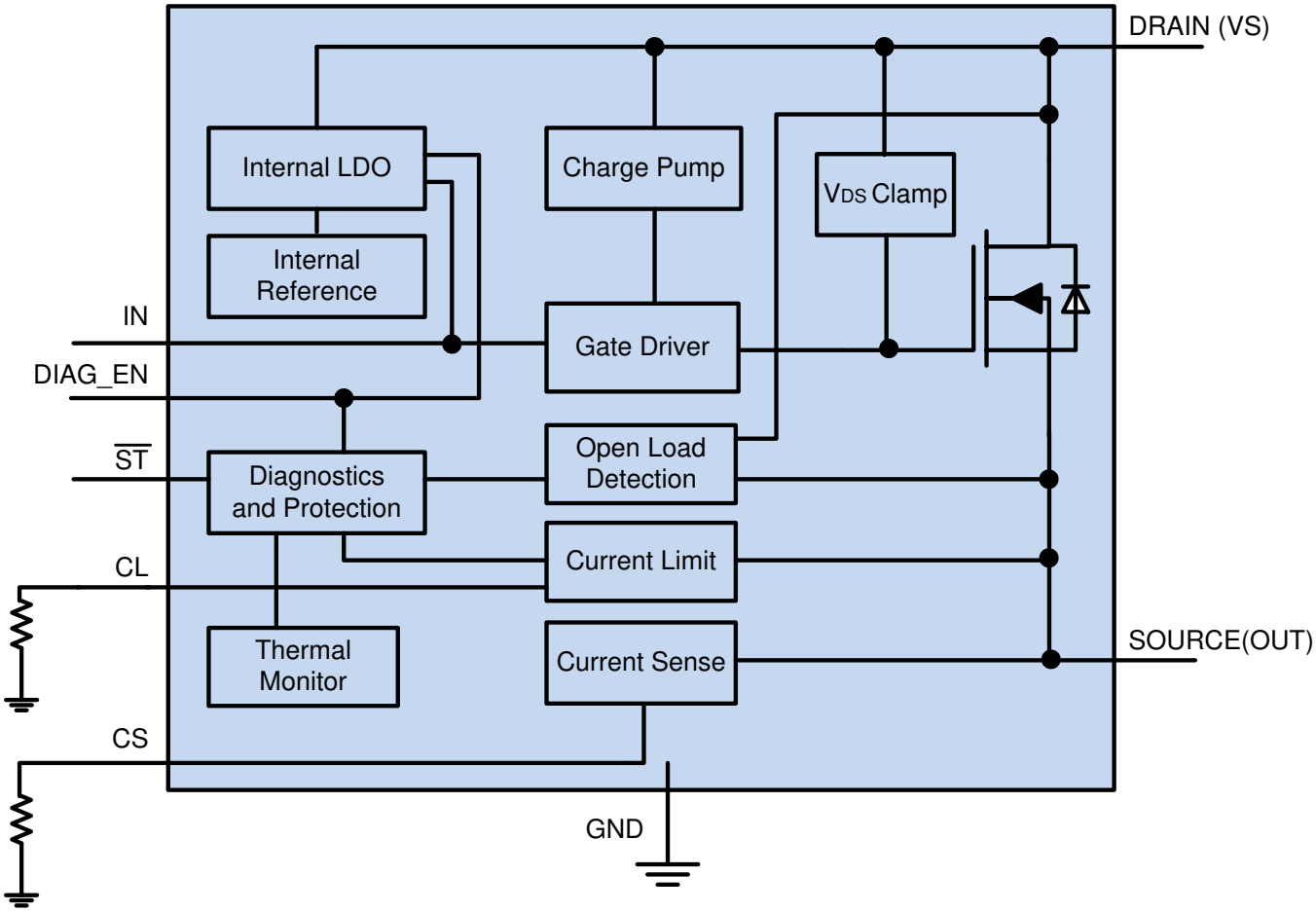
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Accurate Current Sense

For version B, the high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K of the load current, flowing out to the external resistor between the CS pin and GND, and reflected as voltage on the CS pin.

K is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

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Feature Description (continued)

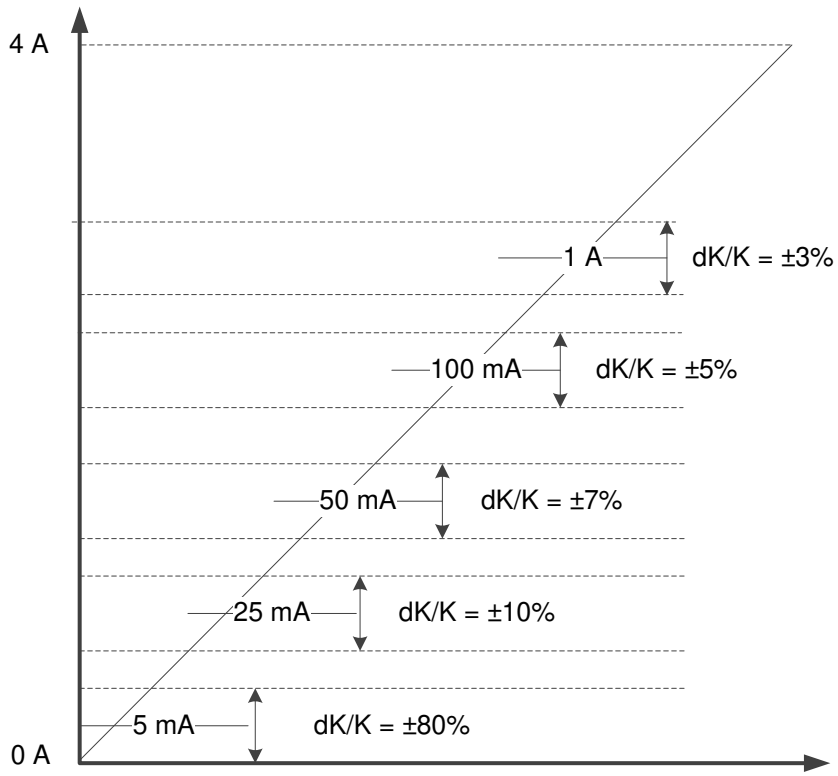

Figure 29. Current-Sense Accuracy

Ensure the CS voltage is in the linear region (0 to 4 V) during normal operation. Calculate R_{CS} with Equation 1.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K}{I_{out}} \tag{1}$$

Also, when a fault condition occurs, CS works as a diagnostics report pin. When an open load or short to battery occurs in the on-state, V_{CS} almost equals 0. When current limit, thermal shutdown/swing, open load, or short to battery in the off-state occurs, the voltage is pulled up to $V_{CS,h}$. Figure 30 shows a typical current-sense voltage according to the operating conditions, including fault conditions.

Feature Description (continued)

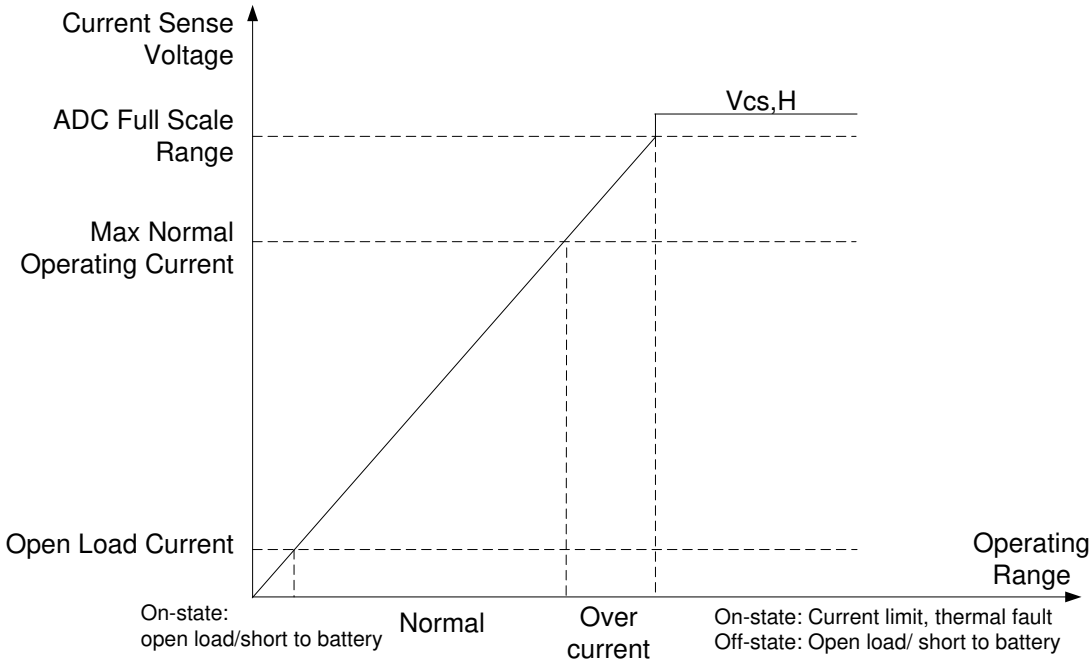

Figure 30. Voltage Indication on the Current-Sense Pin

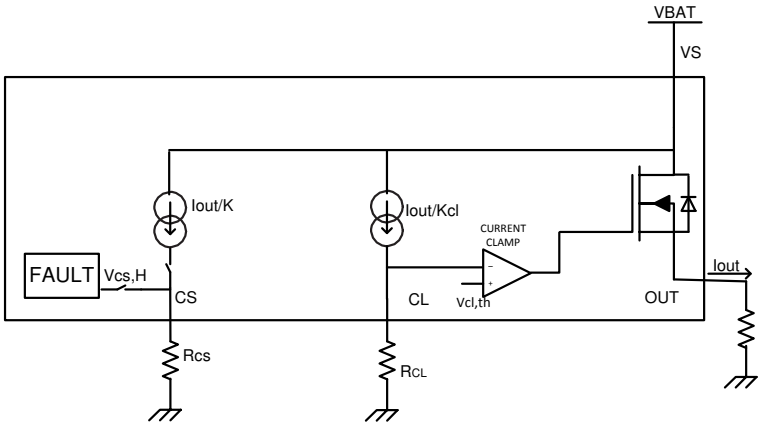

Figure 31. Current-Sense and Current-Limit Block Diagram

7.3.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, it can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from overstressing to the load and integrated power FET. Current limit holds the current at the set value, and pulls up the CS pin to $V_{CS,h}$ as a diagnostic report. The two current-limit thresholds are:

- External programmable current limit -- An external resistor is used to convert a proportional load current into a voltage, which is compared with an internal reference voltage, $V_{th,cl}$. When the voltage on the CL pin exceeds $V_{th.cl}$, a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{ds} voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

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Feature Description (continued)

- Internal current limit -- The internal current limit is fixed and typically 10 A. To use the internal current limit for large-current applications, tie the CL pin directly to the device GND.

Both the internal current limit ($I_{lim,nom}$) and external programmable current limit are always active when V_{VS} is powered and IN is high. The lower one (of $I_{lim,nom}$ and the external programmable current limit) is applied as the actual current limit.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the CL pin must be connected with device GND. Calculate R_{CL} with Equation 2.

$$I_{CL} = \frac{V_{CL,th}}{R_{CL}} = \frac{I_{out}}{K_{CL}} \rightarrow R_{CL} = \frac{V_{CL,th} \times K_{CL}}{I_{out}} \tag{2}$$

For better protection from a hard short-to-GND condition (when V_S and input are high and a short to GND happens suddenly), an open-loop fast-response behavior is set to turn off the channel, before the current-limit closed loop is set up. The open-loop response time is around 1 µs. With this fast response, the device can achieve better inrush-suppression performance.

7.3.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,clamp}$, the clamp diode between the drain and gate.

$$V_{DS,clamp} = V_{BAT} - V_{OUT} \tag{3}$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \tag{4}$$

From the high-side power switch's view, E_{HSD} equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \tag{5}$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \tag{6}$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{7}$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \tag{8}$$

Feature Description (continued)

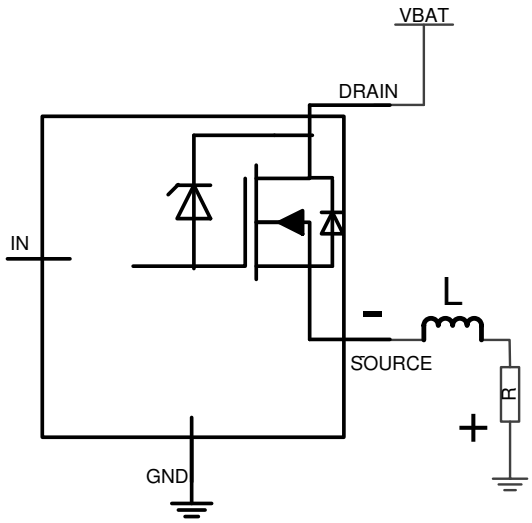

Figure 32. Driving Inductive Load

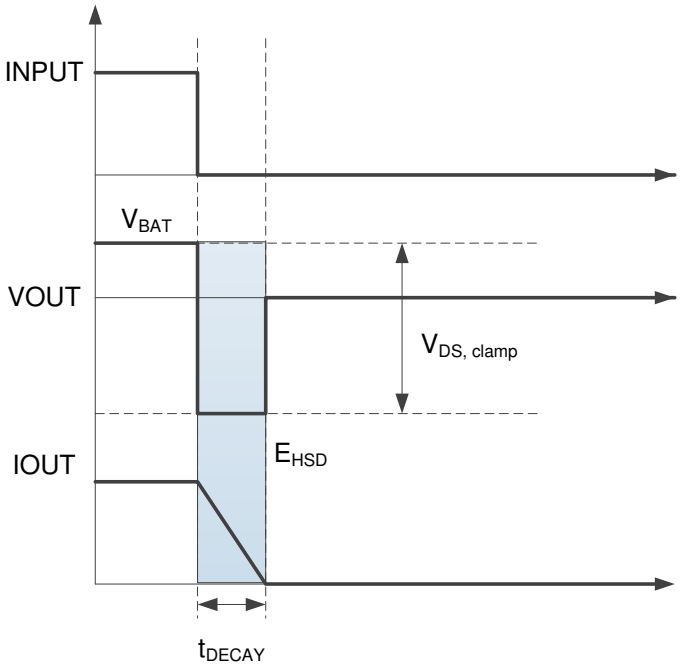

Figure 33. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition. TI provides the upper limit of single-pulse energy that devices can tolerate under the test condition: V_{VS} = 13.5 V, inductance from 0.1 mH to 400 mH, R = 0 Ω, FR4 2s2p board, 2- × 70-µm copper, 2- × 35-µm copper, thermal pad copper area 600 mm^2.

For one dedicated inductance, see Figure 34. If the maximum switching-off current is lower than the current value shown on the curve, the internal clamp function can be used for the demagnetization energy dissipation. If not, external free-wheeling circuitry is necessary for device protection.

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Feature Description (continued)

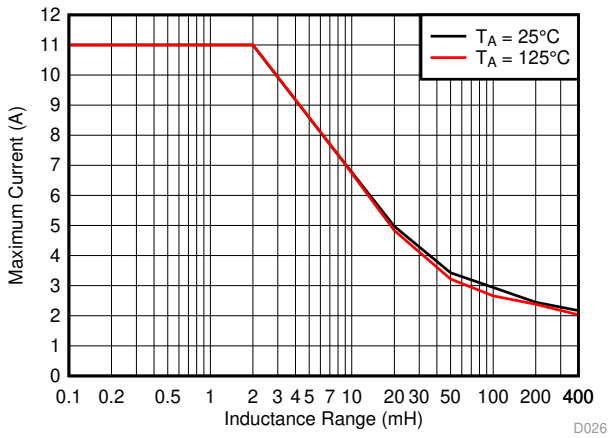

Figure 34. Maximum Current vs Inductance Range

7.3.4 Full Protections and Diagnostics

Table 1 is when DIAG_EN enabled. When DIAG_EN is low, current sense or ST is disabled accordingly. The output is in high-impedance mode. Refer to Table 2 for details.

Table 1. Fault Table

CONDITIONS	IN	OUT	CRITERION	$\overline{ST}$ (Version A)	CS (Version B)	Diagnostics Recovery
Normal	L	L		H	0	
	H	H		H	In linear region	
Short to GND	H	L	Current limit triggered.	L	$V_{CS,h}$	AUTO
Open load(1) Short to battery Reverse polarity	H	H	Version A: Output current < $I_{ol,on}$ Version B: Judged by users	L (deglitch)	Almost 0	AUTO
	L	H	$V_{VS} - V_{OUT} < V_{ol,off}$	L (deglitch)	$V_{CS,h}$ (deglitch)	AUTO
Thermal shutdown	H		TSD triggered	L	$V_{CS,h}$	Recovery when temp < $T_{SD,rst}$
Thermal swing	H		T_{sw} triggered	L	$V_{CS,h}$	AUTO

(1) Need external pullup resistor during off-state

Table 2. DIAG_EN Logic Table

DIAG_EN	IN Condition	Protections and Diagnostics
HIGH	ON	See Table 1
	OFF	See Table 1
LOW	ON	Diagnostics disabled, protection normal CS or $\overline{ST}$ is high Impedance
	OFF	Diagnostics disabled, no protections CS or $\overline{ST}$ is high impedance

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7.3.4.1 Short-to-GND and Overload Detection

In the on state, the short-to-GND fault is reported as the low status output or $V_{CS,h}$ on CS, when a current limit is triggered. The lower one of the internal and external set values is applied for the actual current limit. It is in auto-recovery when the fault condition is cleared. If not cleared, thermal shutdown triggers to protect the power FET.

7.3.4.2 Open-Load Detection

In the on state for version A, if the current flowing through the output is less than $I_{ol,on}$, the device recognizes an open-load fault. For version B, faults are diagnosed by reading the voltage on the CS pin and judged by the user. A benefit of high-accuracy current sense down to a verylow current range, this device can achieve a very low open-load detection threshold, which correspondingly expands the normal operation region. TI suggests 10 mA as the upper limit for the open-load detection threshold and 25 mA as the lower limit for the normal operation current. In Figure 35, the recommended open-load detection region is shown as the dark-shaded region and the light-shaded region is for normal operation. As a guideline, do not overlap these two regions.

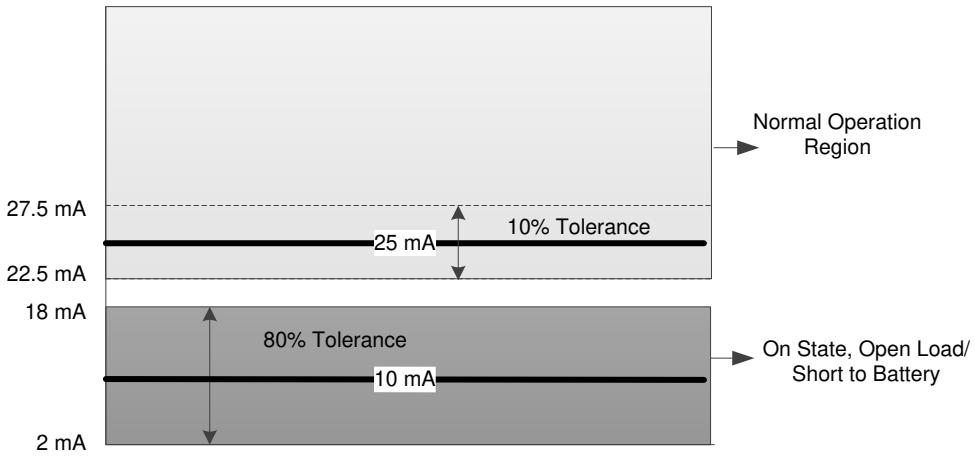

Figure 35. On-State Open-Load Detection and Normal-Operation Diagram

In the off state, if a load is connected, the output voltage is pulled to 0 V. In the case of an open load, the output voltage is close to the supply voltage, $V_S - V_{OUT} < V_{ol,off}$. For version A, the ST pin goes low to indicate the fault to the MCU. For version B, the CS pin is pulled up to $V_{CS,h}$. There is always a leakage current $I_{ol,off}$ present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current. This pullup current should be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI recommends always to use a switch in series with? the pullup resistor. TI recommends $R_{pu} \leq 15\ k\Omega$.

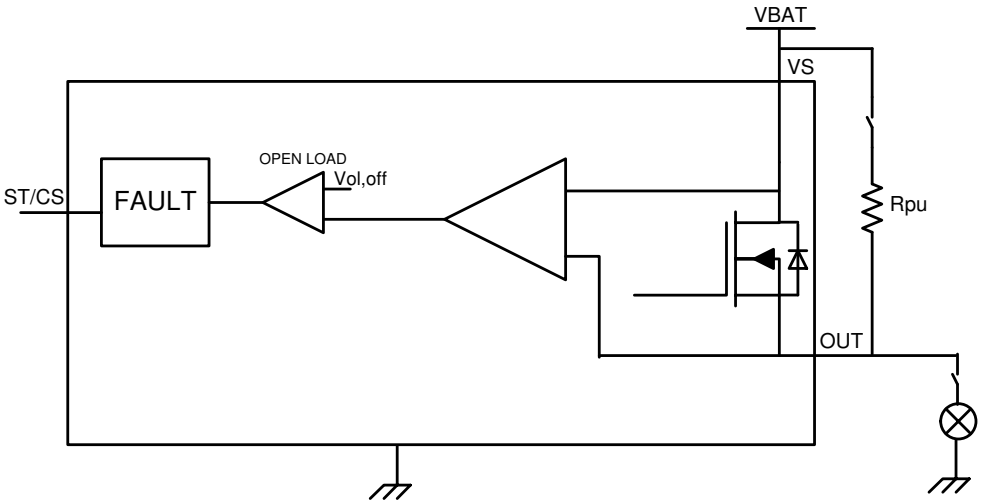

Figure 36. Open-Load Detection Circuit

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7.3.4.3 Short-to-Battery Detection

Short-to-battery detectioin has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. See the fault truth table, Table 1, for more details. In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case for off-state is when reverse current occurs. In the off-state, if $V_{OUT} – V_{VS} < V_F$, short to battery can be detected. (V_F is the body diode forward voltage and typically 0.7 V.) However, the reverse current does not occur. If $V_{OUT} – V_{VS} > V_F$, short to battery can be detected, and the reverse current should be lower than I_{rev2} to ensure the survival of the device. TI recommends switching on the input for lower power dissipation or the reverse block circuitry for the supply. See *Reverse Current Protection* for more external protection circuitry information.

7.3.4.4 Reverse-Polarity Detection

Reverse-polarity detection has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. See the fault truth table, Table 1, for more details. In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case off-state is when reverse current occurs. In off-state, the reverse current should be lower than I_{rev1} to ensure the survival of the device. See *Reverse Current Protection* for more external protection circuitry information.

7.3.4.5 Thermal Protection Behavior

Both the absolute temperature thermal shutdown and the dynamic temperature thermal swing diagnostic and protection are built into the device to increase the maximum reliability of the power FET. Thermal swing is active when the temperature of the power FET is increasing sharply, that is $\Delta T = T_{DMOS} – T_{Logic} > T_{sw}$, then the output is shut down, and the ST pin goes low, or the CS pin is pulled up to $V_{CS,h}$. It auto-recovers and clears the fault signal until $\Delta T = T_{DMOS} – T_{Logic} < T_{sw} – T_{hys}$. Thermal swing function improves device reliability against repetitive fast thermal variation, as shown in Figure 37. Multiple thermal swings are triggered before thermal shutdown happens. Thermal shutdown is active when absolute temperature $T > T_{SD}$. When active, the output is shut down, and the ST pin goes low, or the CS pin is pulled up to $V_{CS,h}$. The output is auto-recovered when $T < T_{SD} – T_{hys}$; the current limit is reduced to $I_{lim,tsd}$, or half of the programmable current limit value, to avoid repeated thermal shutdown. However, the thermal shutdown fault signal and half-current limit value are not cleared until the junction temperature decreases to less than $T_{SD,rst}$.

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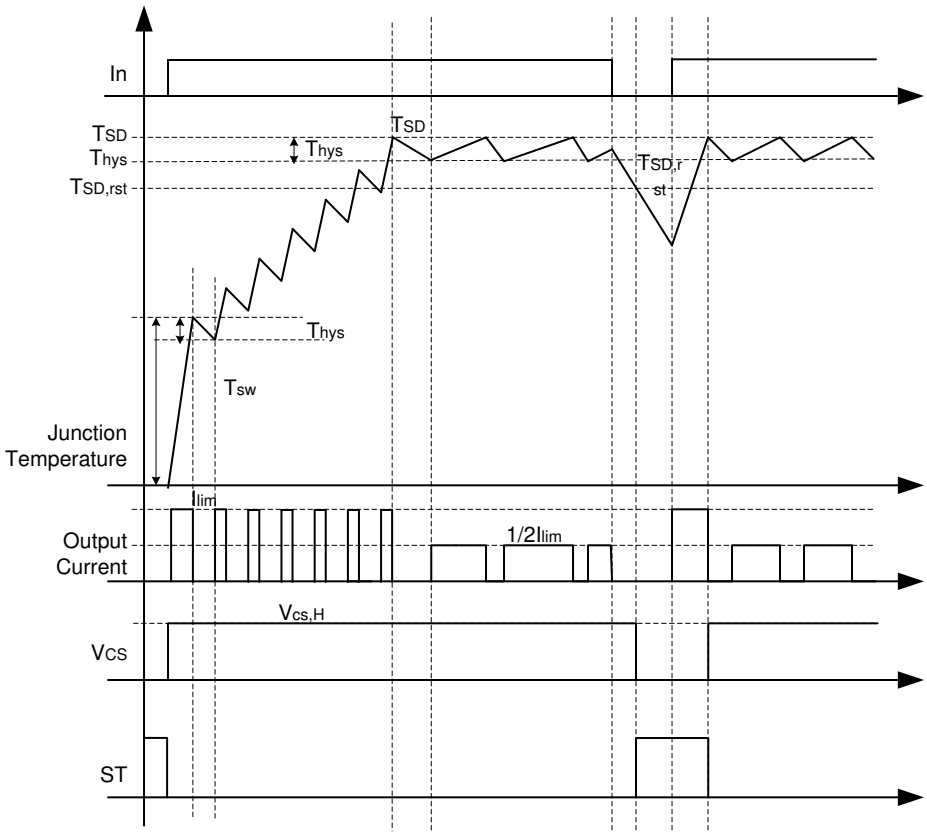

Figure 37. Thermal Behavior

7.3.4.6 UVLO Protection

The device monitors the supply voltage V_{VS} to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to $V_{VS,UVF}$, the output stage is shut down automatically. When the supply rises up to $V_{VS,UVR}$, the device turns on.

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7.3.4.7 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of device GND): Loss of GND protection is active when the Tab, I_{C_GND}, and current limit GND are one trace connected to the board GND, as shown in Figure 38. Tab floating is also a choice.

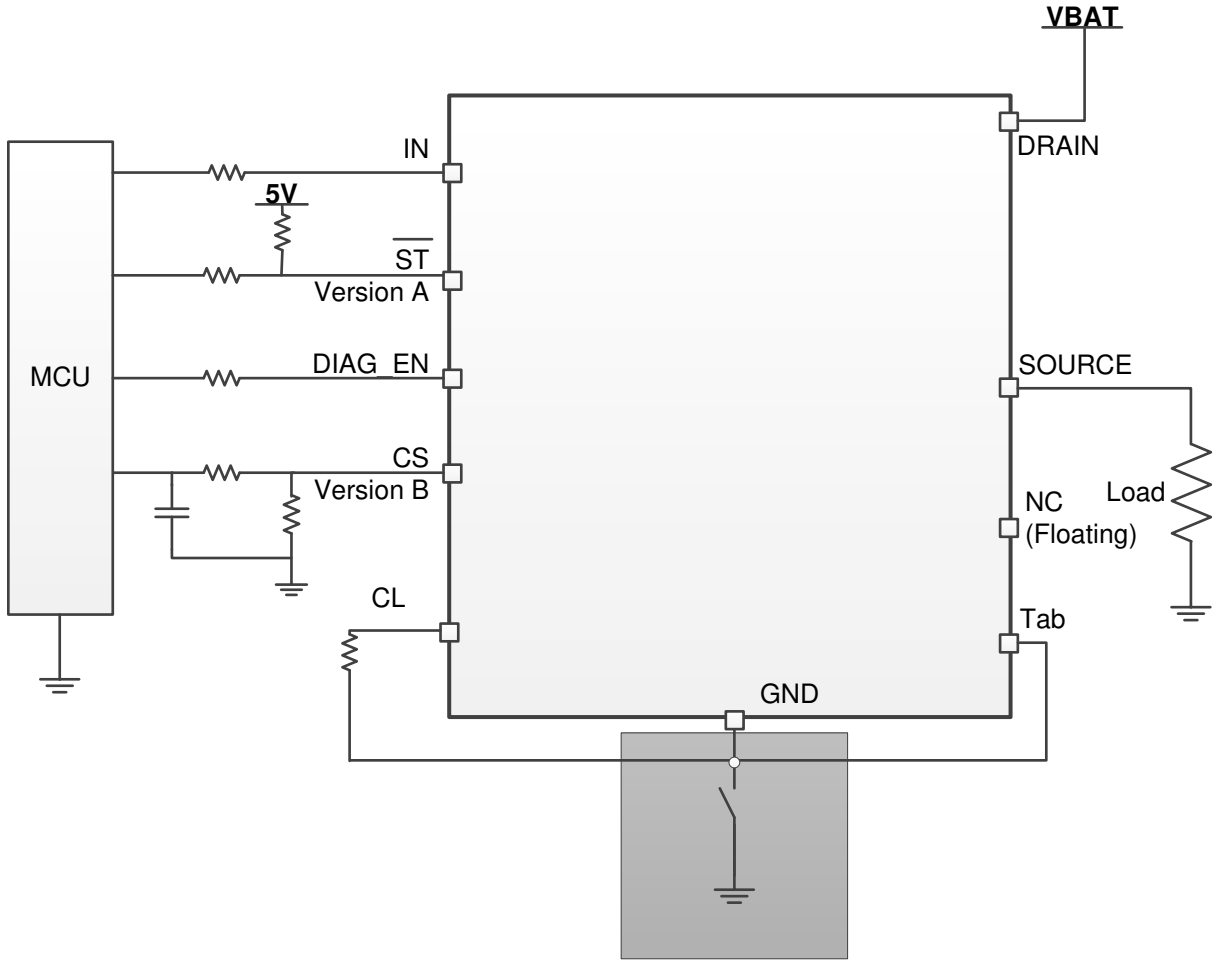

Figure 38. Loss of Device GND

Case 2 (loss of module GND): When the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

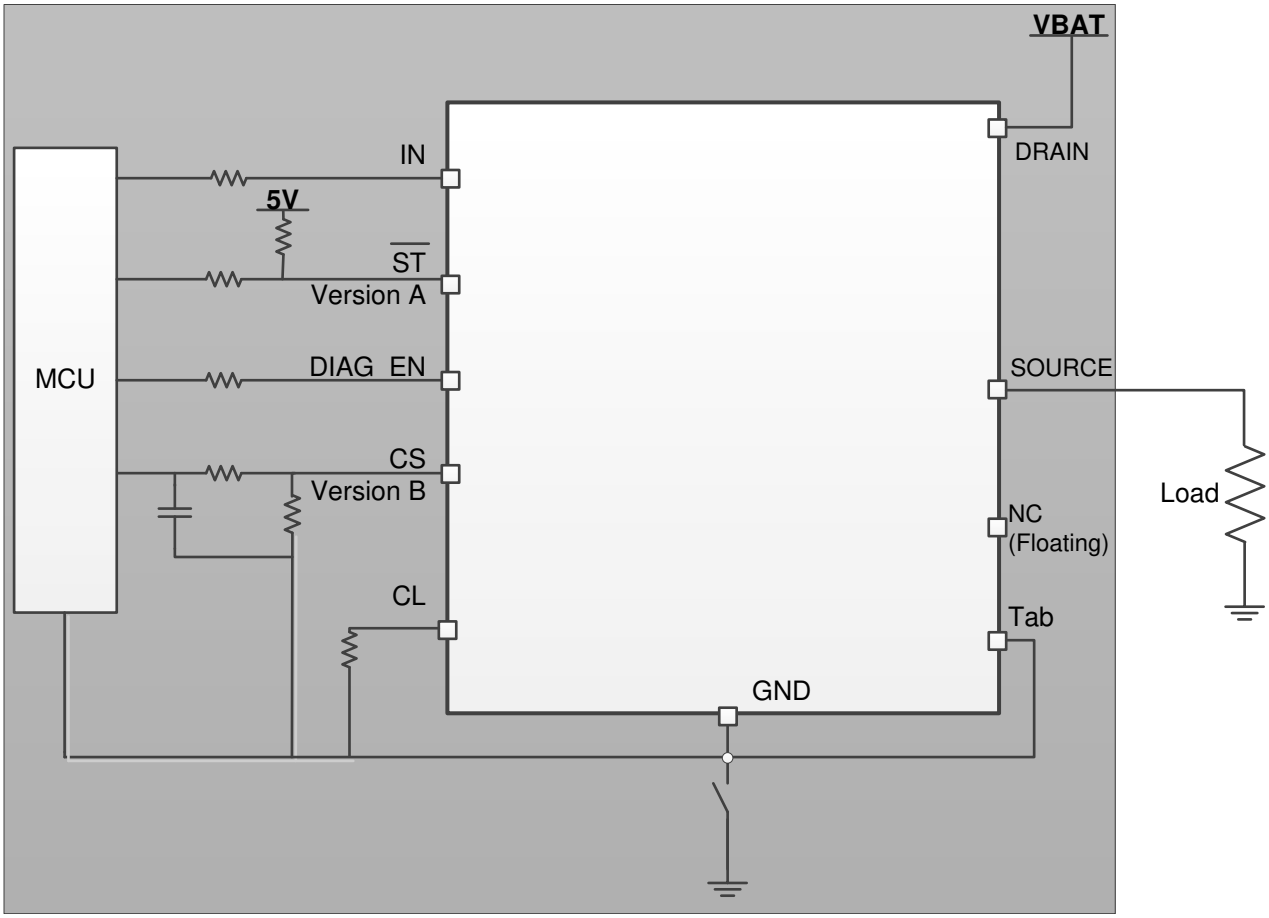

Figure 39. Loss of Module GND

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7.3.4.8 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss-o-supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

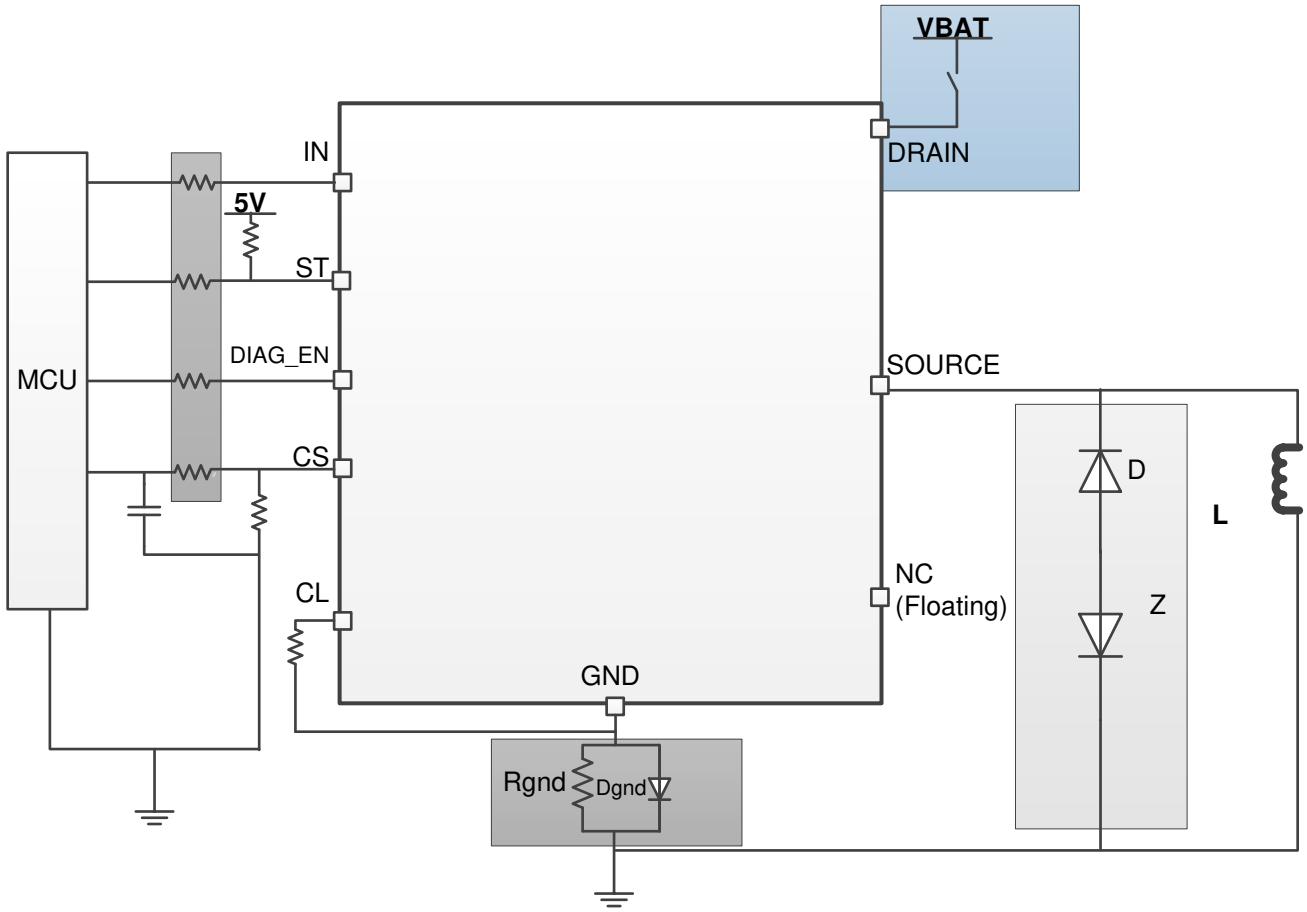

Figure 40. Loss of Battery

7.3.4.9 Reverse Current Protection

Method 1: Block diode connected with V_S. Both the device and load are protected when in reverse polarity.

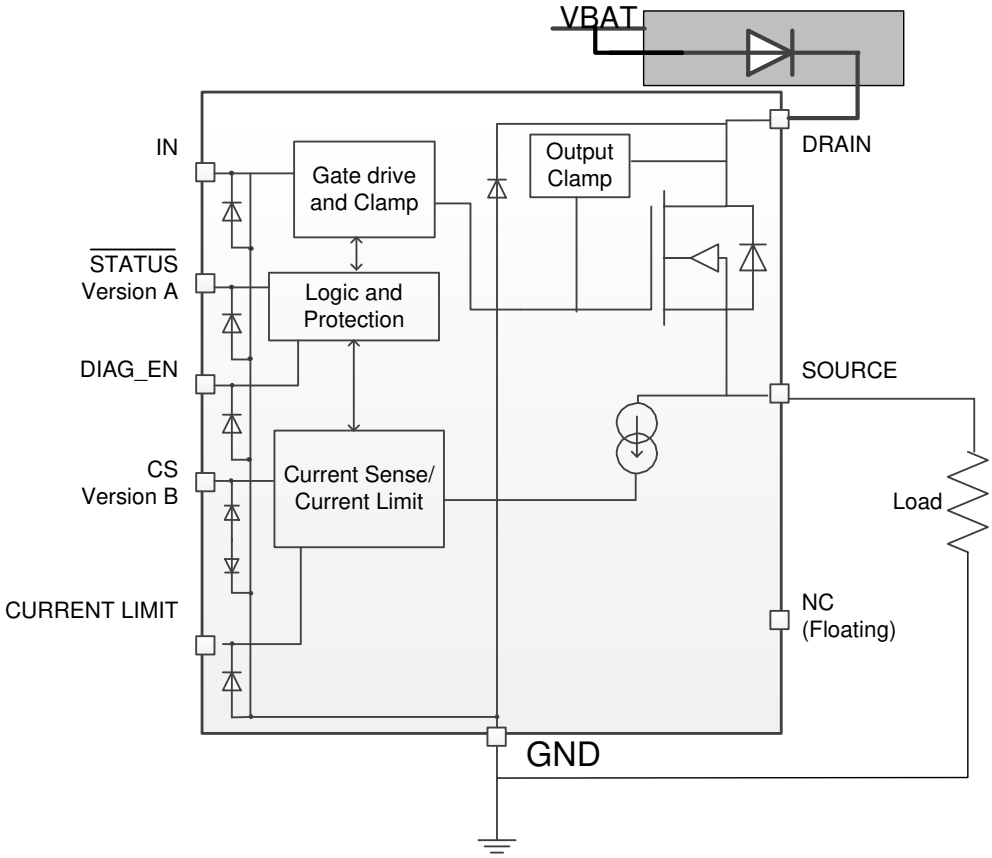

Figure 41. Reverse Protection With Block Diode

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Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse loop is limited by the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET should be less than I_{rev}. Of the three types of ground pin networks, TI strongly recommends type 3 (the resistor and diode in parallel). No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Leave the NC pin floating or connect to the device GND. TI recommends to leave floating.
- Connect the current limit programmable resistor to the device GND.

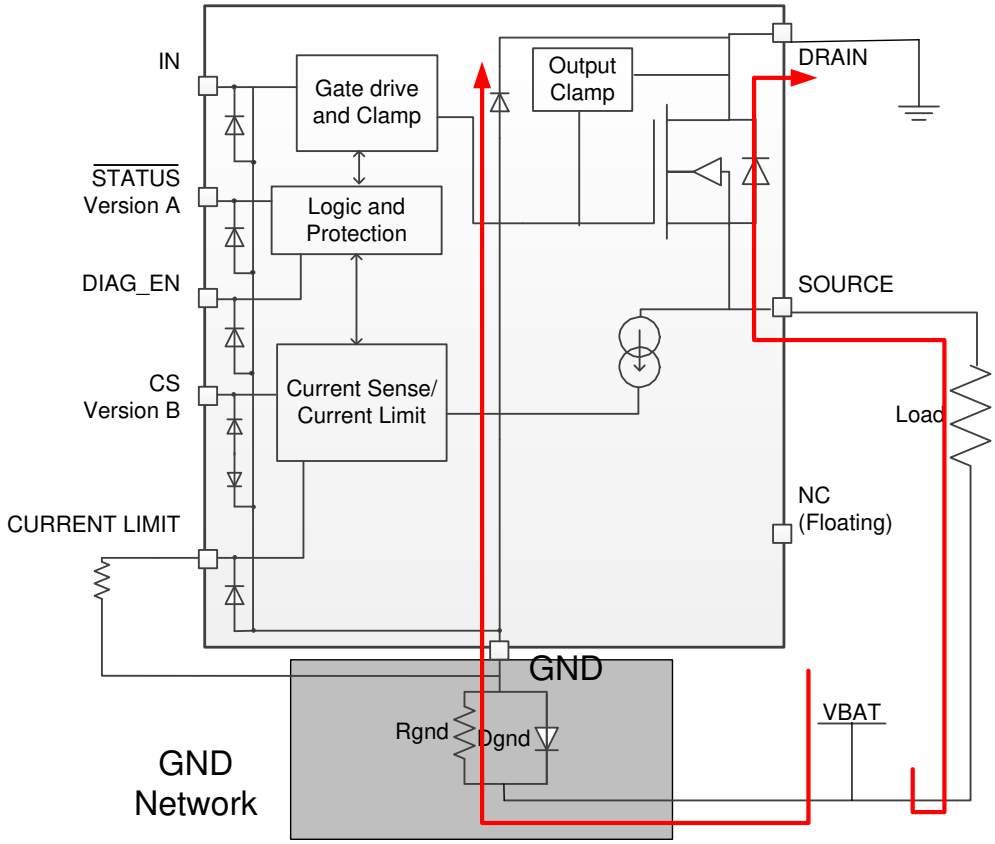

Figure 42. Reverse Protection With GND Network

- **Type 1 (resistor):** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses. However, it leads to higher GND shift during normal operation mode. Also, consider the resistor's power dissipation.

$$R_{GND} \le \frac{V_{GNDshift}}{I_{nom}}$$
$$R_{GND} \ge \frac{(-V_{CC})}{(-I_{GND})} \quad (9)$$

where

- $V_{GNDshift}$ is the maximum value for the GND shift, determined by the HSD and microcontroller. TI suggests a value ≤ 0.6 V.
- I_{nom} is the nominal operating current.
- $-V_{CC}$ is the maximum reverse voltage seen on the battery line.
- $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*. (10)

If multiple high-side power switches are used, the resistor can be shared among devices.

- **Type 2 (diode):** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600 mV).

However, an inductive load is not acceptable to avoid an abnormal status when switching off.

- **Type 3 (resistor and diode in parallel (recommended)):** A peak negative spike may occur when the inductive load is switching off, which may damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are 1-kΩ resistor in parallel with an I_F > 100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

7.3.4.10 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin may damage the MCU I/O pins [more likely, the internal circuitry connected to the pins]. Therefore, the serial resistors between MCU and HSD are required.

Also, for proper protection against loss of GND, TI recommends 4.7 kΩ when using 3.3-V MCU I/Os; 10 kΩ is for 5-V applications.

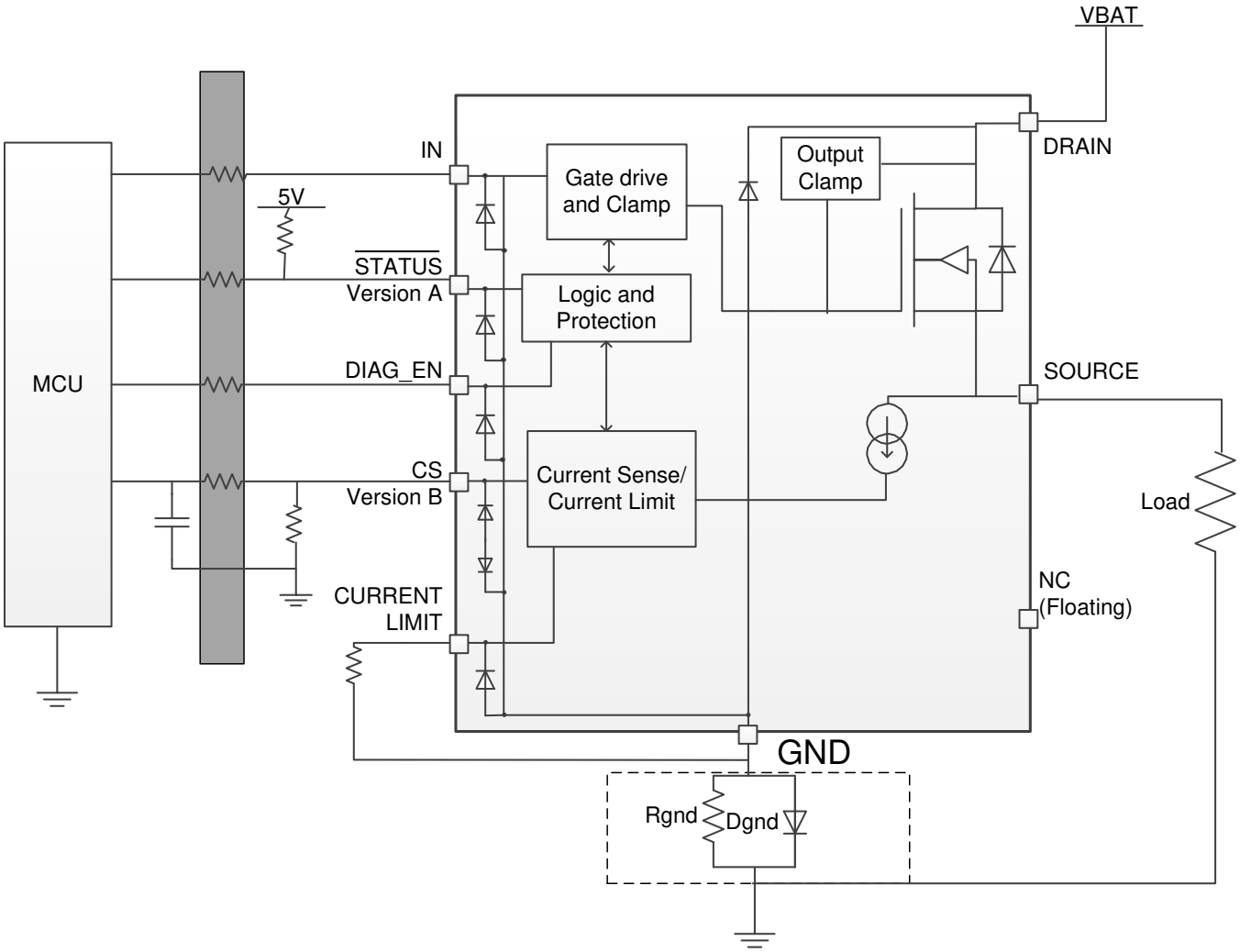

Figure 43. MCU IO Protections

7.3.5 Diagnostic Enable Function

The diagnostic enable pin, DIAG_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

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In addition, during the output-off period, the diagnostic disable function lowers the current consumption for the standby condition. The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If off-state power saving is required in the system, the standby current is <500 nA with DIAG_EN low. If the off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high.

7.4 Device Functional Modes

7.4.1 Working Mode

The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If an off-state power saving is required in the system, the standby current is less than 500 nA with DIAG_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high. Note that to enter standby mode requires IN low and $t > t_{off,deg}$. $t_{off,deg}$ is the standby-mode deglitch time, which is used to avoid false triggering. Figure 44 shows a work-mode state-machine state diagram.

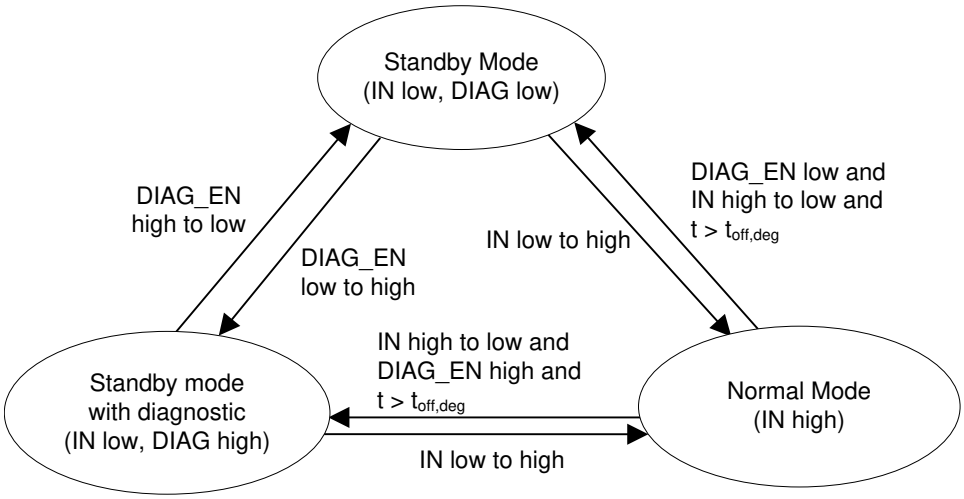

Figure 44. Work-Mode State Machine

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following discussion notes how to implement the device to distinguish the different fault modes and implement a ? transient-pulse immunity test.

In some applications, open load, short to battery, and short to GND must be distinguished from each other. This requires two steps.

8.2 Typical Application

Figure 45 shows an example of how to design the external circuitry parameters.

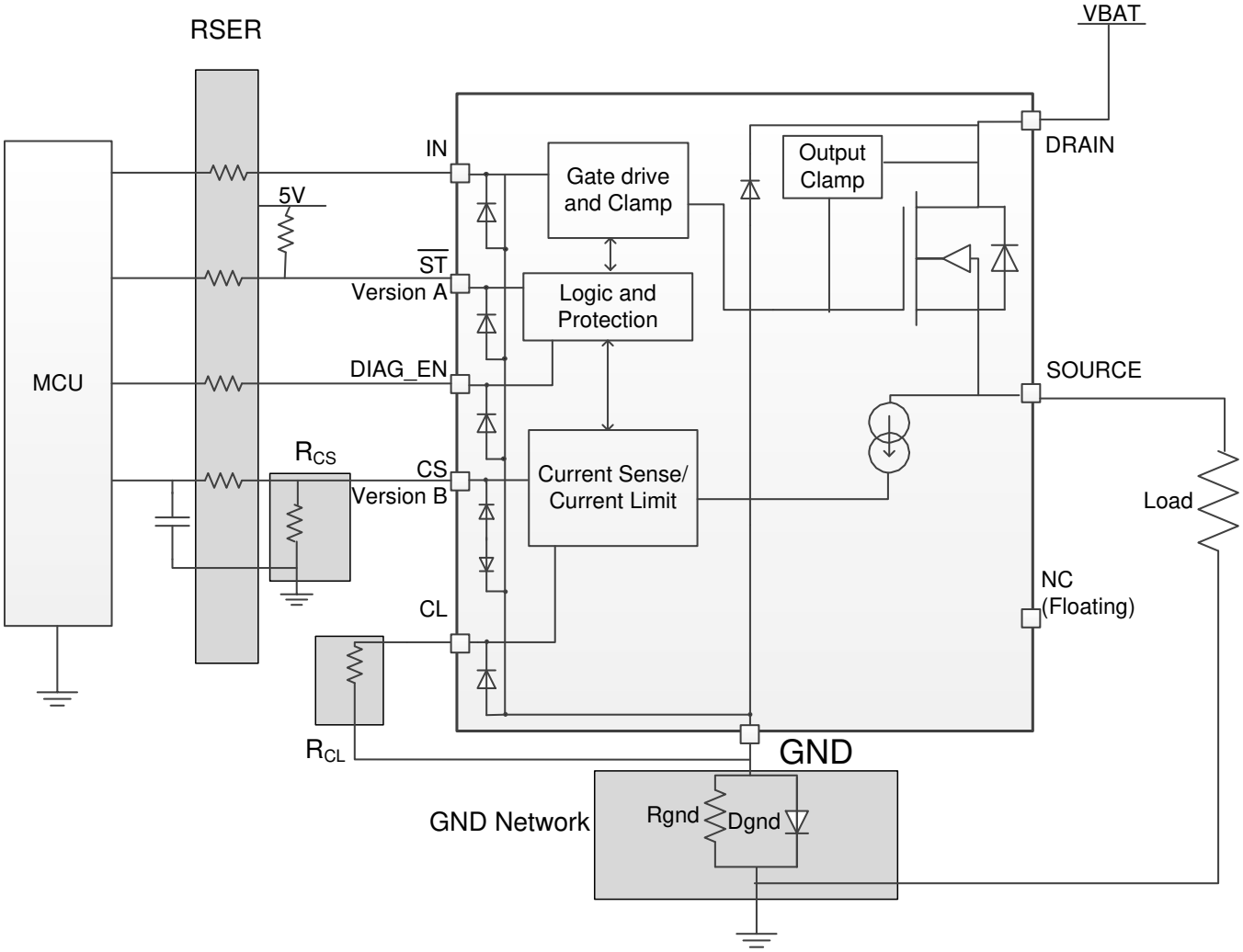

Figure 45. Typical Application Circuitry

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Typical Application (continued)

8.2.1 Design Requirements

- V_S range from 9 V to 16 V
- Nominal current of 2 A
- Current sense for fault monitoring
- Expected current limit value of 5 A
- Full diagnostics with 5-V MCU
- Reverse protection with GND network

8.2.2 Detailed Design Procedure

The R_{CS}, V_{CS} linear region is from 0 to 4 V. To keep the 2-A nominal current in the 0- to 3-V range, calculate the R_{CS} as in Equation 11. To achieve better current sense accuracy, a 1% accuracy or better resistor is preferred.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K}{I_{OUT}} = \frac{3 \times 500}{2} = 750\ \Omega \tag{11}$$

R_{CL}, $V_{CL,th}$ is the current-limit internal threshold, 1.233 V. To set the programmable current limit value at 5 A, calculate the R_{CL} as in Equation 12.

$$R_{CL} = \frac{V_{cl,th} \times K_{CL}}{I_{OUT}} = \frac{1.233 \times 2000}{5} = 493.2\ \Omega \tag{12}$$

TI recommends R_{SER} = 10 kΩ for 5-V MCU.

TI recommends a 1-kΩ resistor and 200-V, 0.2-A diode for the GND network.

8.2.2.1 Distinguishing of Different Fault Modes

Some applications require that open load, short to battery, and short to GND can be distinguished from each other. This requires two steps:

1. In the on-state, for the current-sense version device (version B), on-state open load and short to battery are recognized as an extremely-low voltage level on the current-sense pin, whereas short to GND is reported as a pulled-up voltage $V_{CS,h}$. Therefore, the user can find a short to GND (see Figure 46).
2. If reported as an on-state open-load or short-to-battery fault in the first step, turn off the input signal. In the off-state, with an external pulldown resistor, open load and short to battery can be easily distinguished. When the output pulls down, the short to battery is still reported as an off-state fault condition, whereas the open load is ignored.

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Typical Application (continued)

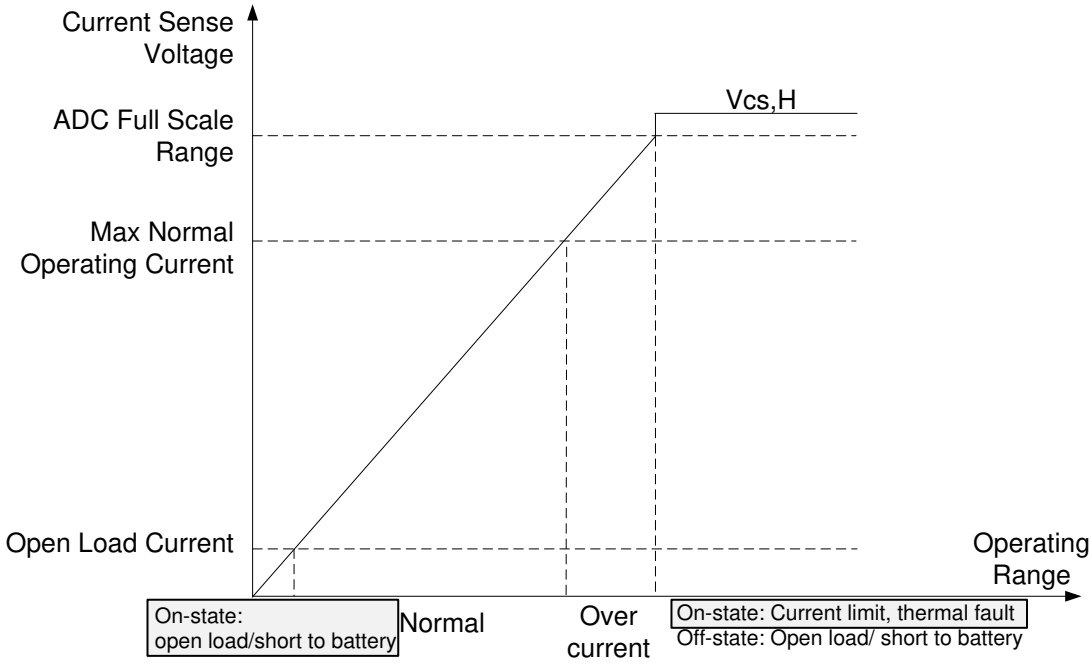

Figure 46. Step 1: Short-to-GND Detection in the On-State

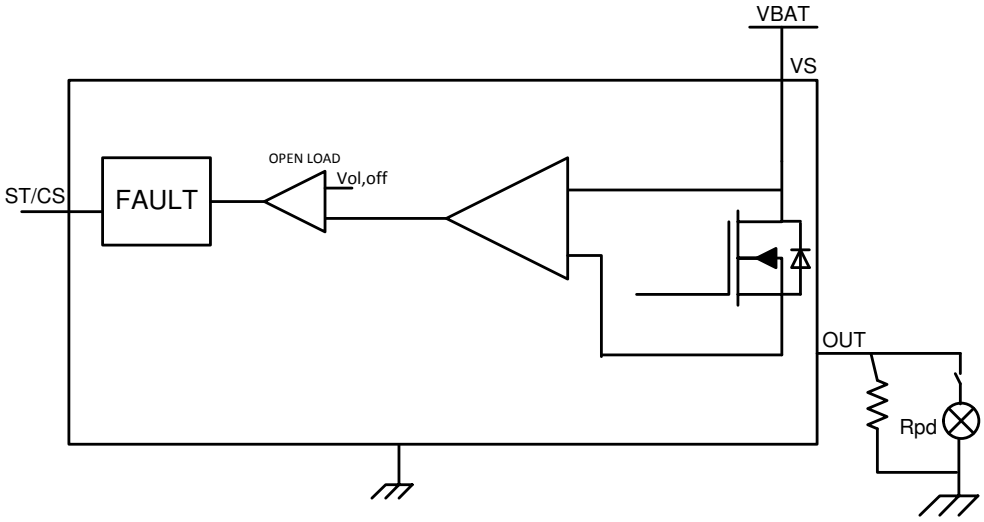

Figure 47. Step 2: Short-to-Battery Detection in the Off-State

8.2.2.2 AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The AEC-Q100-012 standard is used to determine the reliability of the devices when operating in a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level, Grade A, 1 million times short-to-GND certification.

Three test modes are defined in the AEC Q100-012 standard. See Table 3 for cold repetitive short-circuit test – long pulse, cold repetitive short-circuit test – short pulse, and hot repetitive short-circuit test.

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Typical Application (continued)

Table 3. Tests

Test Items	Test Condition	Test Cycles
Cold repetitive short-circuit test – short pulse	–40°C, 10-ms pulse, cool down	1M
Cold repetitive short-circuit test – long pulse	–40°C, 300-ms pulse, cool down	1M
Hot repetitive short-circuit test	25°C, continuous short	1M

Different grade levels are specified according to the pass cycles. The TPS1H100-Q1 device gets the certification of Grade A level, 1 million short-to-GND cycles, which is the highest test standard in the market.

Table 4. Grade Levels

Grade	Number of Cycles	Lots,Samples Per Lot	Number of Fails
A	>1000000	3, 10	0
B	>300000 to 1000000	3, 10	0
C	>100000 to 300000	3, 10	0
D	>30000 to 100000	3, 10	0
E	>10000 to 30000	3, 10	0
F	>3000 to 10000	3, 10	0
G	>1000 to 3000	3, 10	0
H	300 to 1000	3, 10	0
O	<300	3, 10	0

8.2.2.3 EMC Transient Disturbances Test

Due to the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high-side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards. The TPS1H100-Q1 device is tested and certificated by a third-party organization.

Table 5. ISO 7637-2:2011(E) in 12-V System(1)(2)(3)(4)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst-Cycle Pulse-Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN	MAX		
1	III	–112	2 ms	500 pulses	0.5 s	e s	10	Status II
2a	III	55	50 µs	500 pulses	0.2 s	5 s	2	Status II
2b	IV	10	0.2 to 2 s	10 pulses	0.5 s	5 s	0 to 0.05	Status II
3a	IV	–220	0.1 µs	1h	90 ms	100 ms	50	Status II
3b	IV	150	0.1 µs	1h	90 ms	100 ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) Considering the worst test condition, it is tested without any filter capacitors in V_S and V_{OUT}.
(3) GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

Table 6. ISO 16750-2:2010(E) Load Dump Test B in 12-V System(1)(2)(3)(4)(5)

Test Item	Test Pulse Severity Level and vs Accordingly		Pulse Duration (t_d)	Minimum Number of Pulses or Test Time	Burst Cycle/Pulse Repetition Time		Input Resistance (Ω)	Function Performance Status Classification
	Level	Vs/V			MIN (s)	MAX (s)		
Test B		45	40 to 400 ms	5 pulses	60	e	0.5 to 4	Status II

(1) Tested both under input low condition and high condition. [DIAG_EN, IN, and VS are all classified as inputs. Which one?
(2) Considering the worst test condition, the device is tested without any filter capacitors on VS and OUT.
(3) The GND pin network is a 1-kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.
(5) Select a 45-V external suppressor.

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8.2.3 Application Curves

Figure 48 shows a test example of initial short-circuit inrush-current limit. Test conditions: V_S = 13.5 V, input is from low to high, load is short-to-GND or with a 470-µF capacitive load, external current limit is 2 A. CH1 is the output current. CH3 is the input step.

Figure 49 shows a test example of a hard short-circuit inrush-current limit. Test conditions: V_S= 13.5 V, input is high, load is 5 µH + 100 mΩ, external current limit is 1 A. A short to GND suddenly happens.

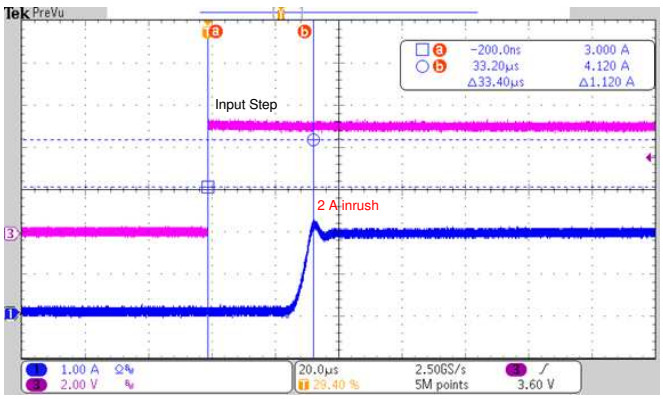

Figure 48. Initial Short-to-GND Waveform

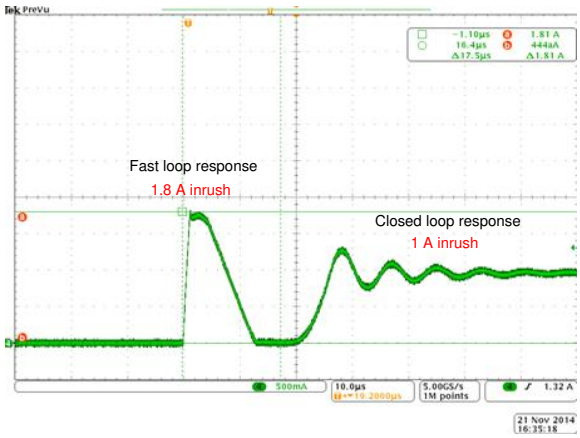

Figure 49. Hard Short-to-GND Waveform

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9 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. The supply voltage should be within the range specified in the *Recommended Operating Conditions*.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

10.2 Layout Example

10.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

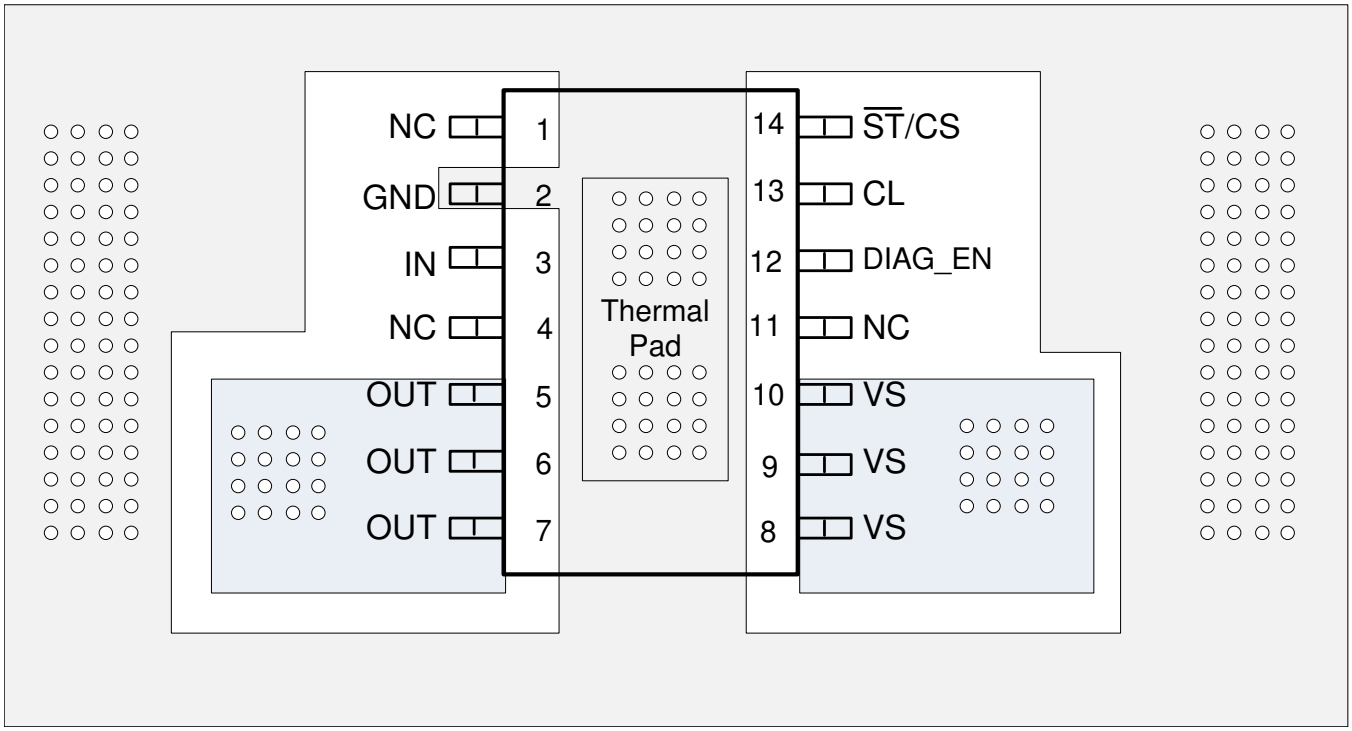

Figure 50. Layout Without a GND Network

Layout Example (continued)

10.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

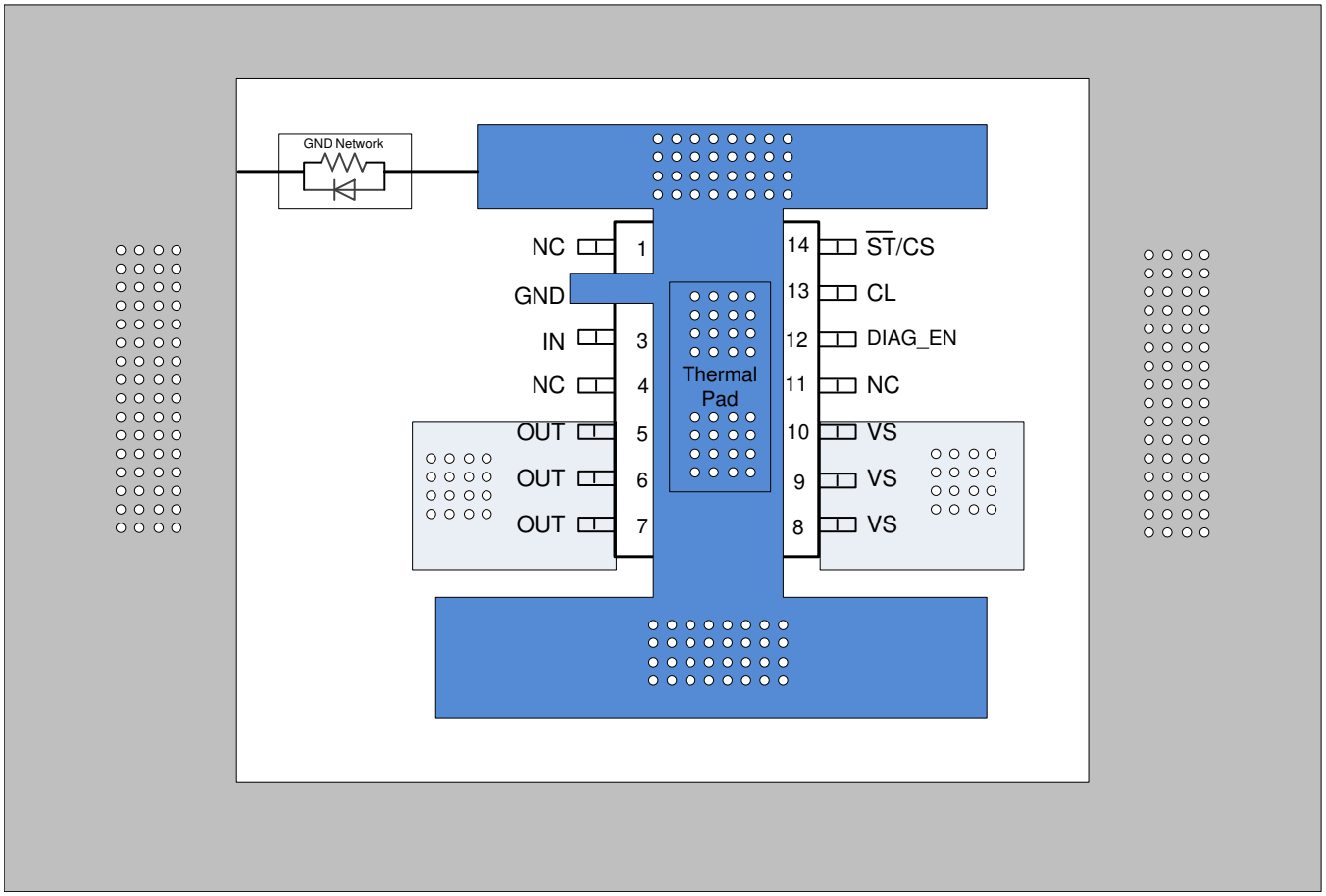

Figure 51. Layout With a GND Network

10.3 Thermal Considerations

This device possesses thermal shutdown (TSD) circuitry as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to Equation 13.

$$P_T = I_{OUT}^2 \times R_{DSON} + V_S \times I_{nom}$$

where

- P_T = Total power dissipation of the device (13)

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (14)$$

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス・プロダクト・フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1H100AQPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100AQ
TPS1H100AQPWPRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100AQ
TPS1H100BQPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100BQ
TPS1H100BQPWPRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1H100BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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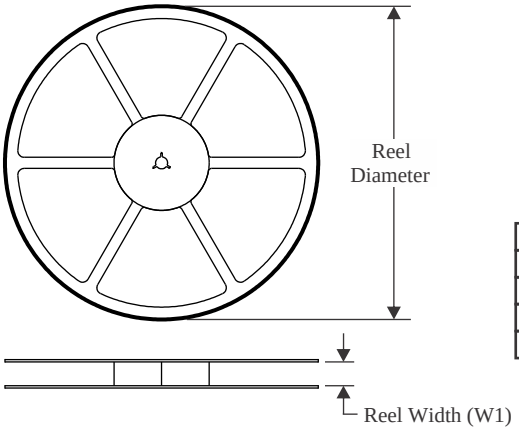
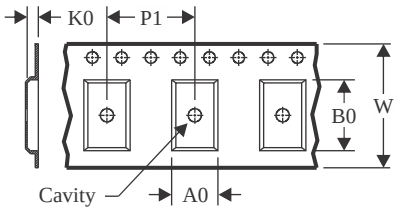
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

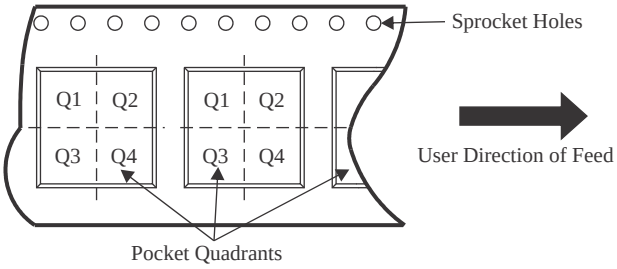


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

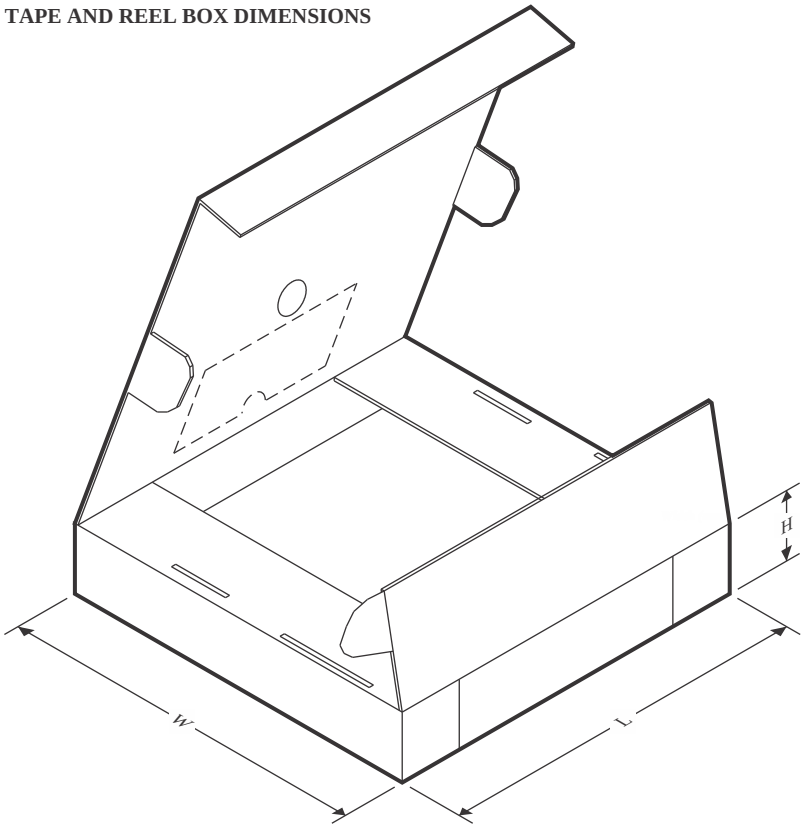
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1H100AQPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS1H100BQPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1H100AQPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS1H100BQPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

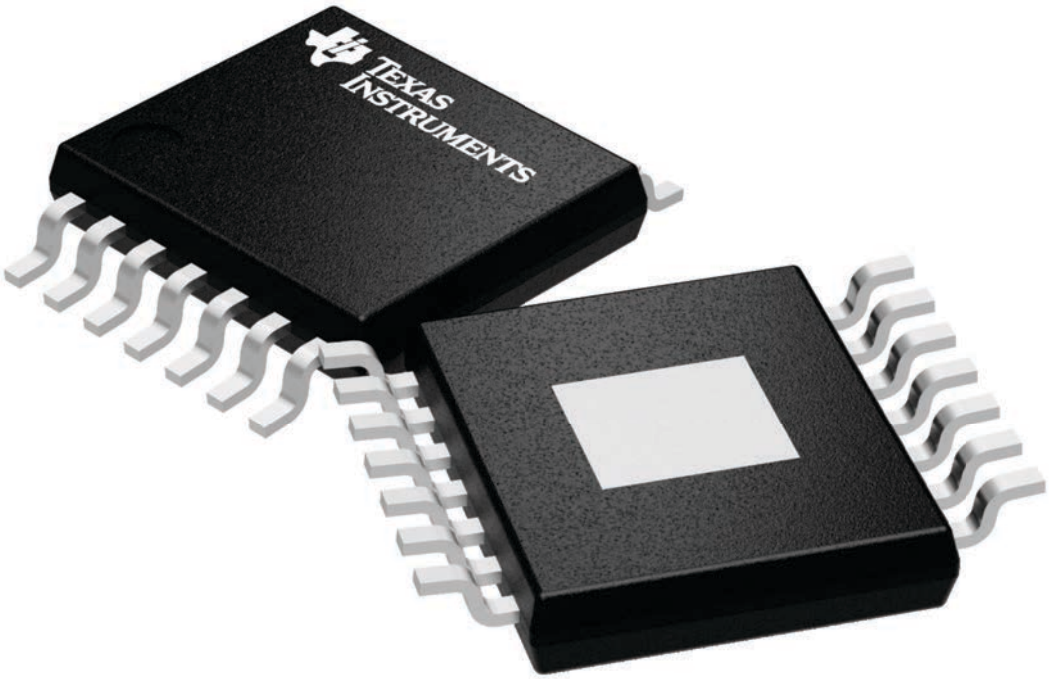
PWP 14

PowerPAD TSSOP - 1.2 mm max height

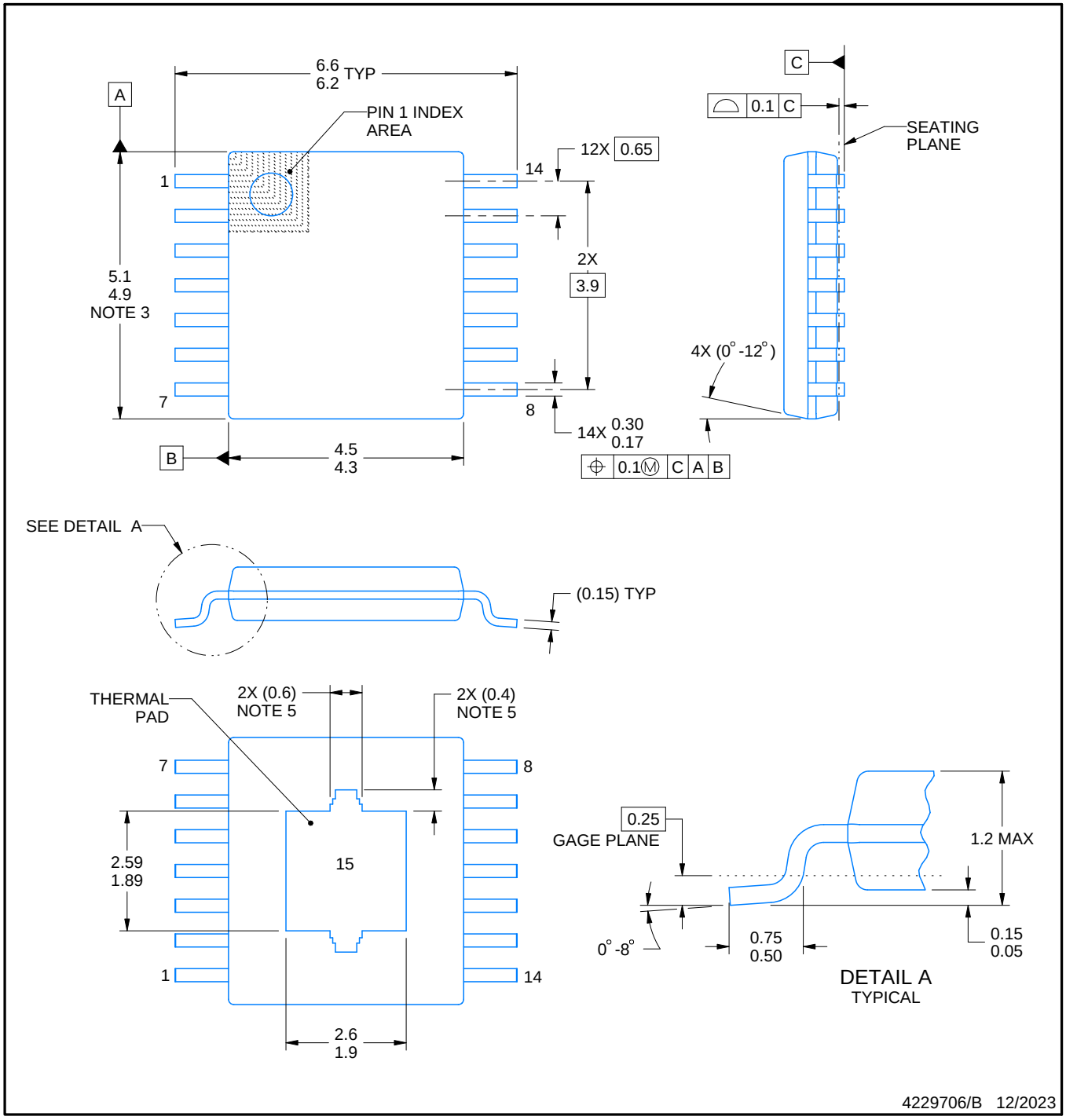
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



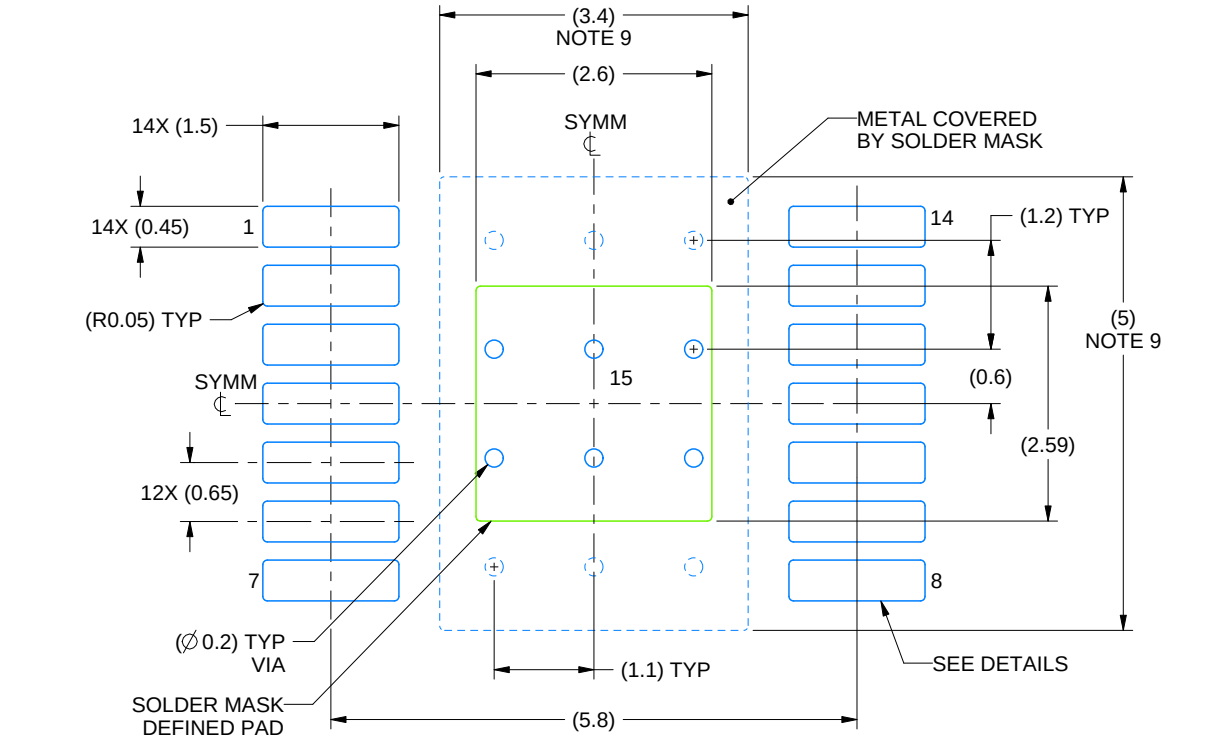
4224995/A



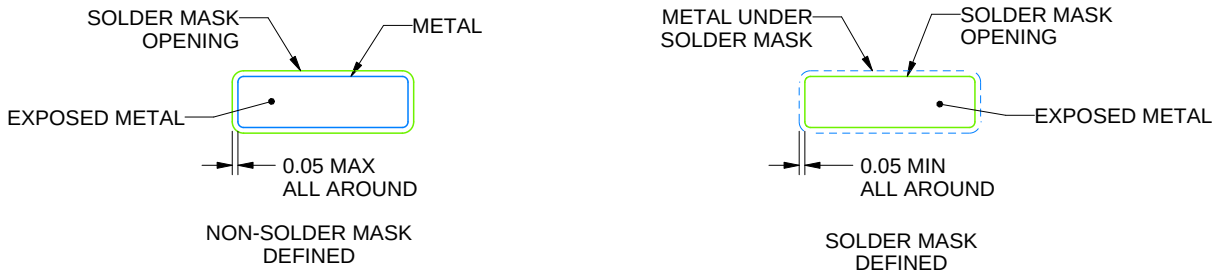
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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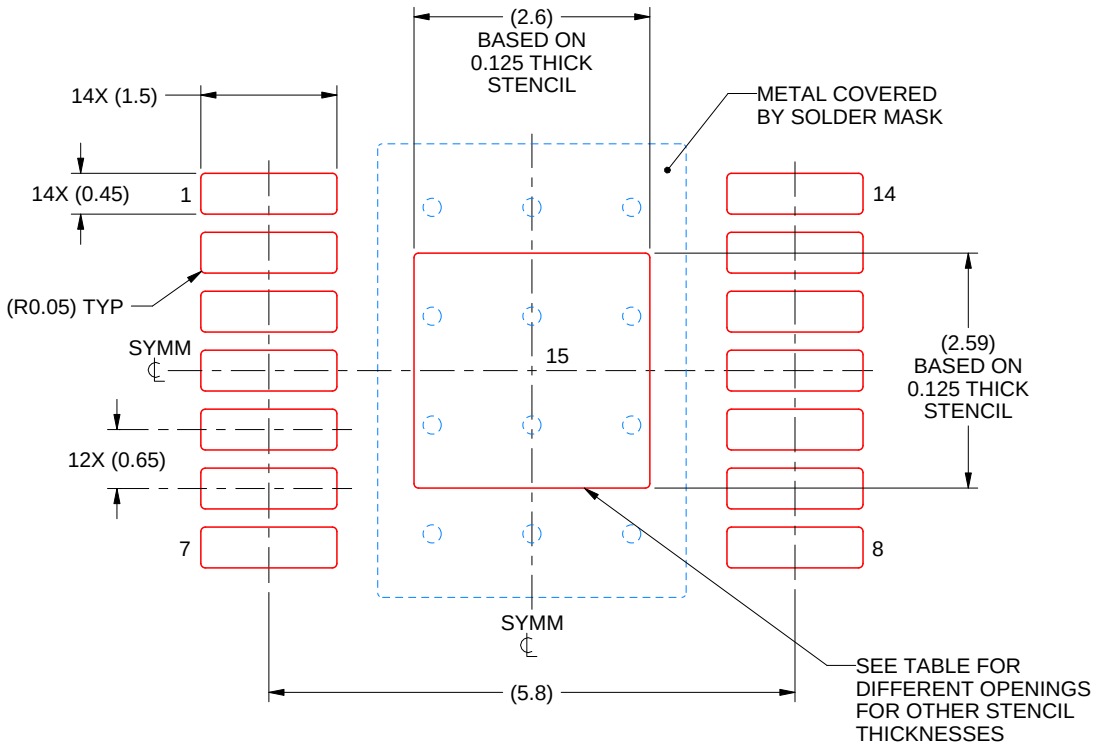
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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