**TEXAS INSTRUMENTS**

# TPS65286 デュアル電力分配スイッチ、入力電圧 4.5V〜28V、出力電流 6A の同期整流降圧レギュレータ内蔵

## 1 特長

- 内蔵デュアル電力分配スイッチ
  - 動作入力電圧範囲：2.5V〜6V
  - オン抵抗 100mΩ (標準値) のバック・ツー・バックのパワー MOSFET を内蔵
  - 75mA〜2.7A の範囲で調整可能な電流制限
  - 1.2A で ±6% の電流制限精度 (標準値)
  - ラッチオフの過電流保護バージョン
  - 逆入出力電圧に対する保護
  - ソフト・スタート機能内蔵
- 内蔵降圧 DC-DC コンバータ
  - 4.5V〜28V の広い入力電圧範囲
  - 最大連続出力負荷電流：6A
  - 帰還基準電圧：0.6V±1%
  - 500kHz の固定スイッチング周波数
  - 内蔵のソフトスタート時間：1ms
  - サイクル単位の電流制限
  - 可変電流制限スレッショルド
  - 出力過電圧保護
  - 外部クロックへの同期
  - 過熱保護

## 2 アプリケーション

- USB ポートおよび USB ハブ
- デジタル TV
- コンピュータ用電源
- ラップトップのドッキング電源
- 車載用インフォテインメント
- 監視

## 3 概要

TPS65286 は、$V_{IN}$ 4.5V〜28V、出力電流 6A のフル機能の同期整流降圧型 DC-DC コンバータであり、高い効率とハイサイドおよびローサイド MOSFET の内蔵により小型設計に最適化されています。このデバイスは、電力分配システム用のデュアル N チャネル MOSFET パワー・スイッチも内蔵しています。このデバイスは総合的な電力分配ソリューションを提供します。これらのソリューションでは、高精度の電流制限と高速な保護応答が必要です。

独立したデュアル 100mΩ 電力分配スイッチは、外付け抵抗を使用して 50mA〜2.7A (標準値) の間でプログラム可能な電流制限スレッショルドに出力電流を制限します。1.2A (標準値) において±6% の電流制限精度を達成できます。過電流および逆電圧条件では、nFAULT 出力が LOW にアサートされます。
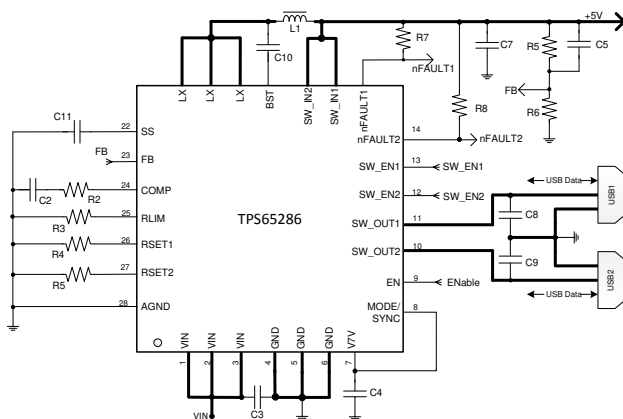
DC-DC コンバータの固定周波数ピーク電流モード制御は、補償を簡素化し、過渡応答を最適化します。サイクル単位の過電流保護とヒカップ・モード動作は、MOSFET の消費電力を抑制します。ダイ温度が熱過負荷スレッショルドを超えると、過熱保護機能がデバイスをシャットダウンします。
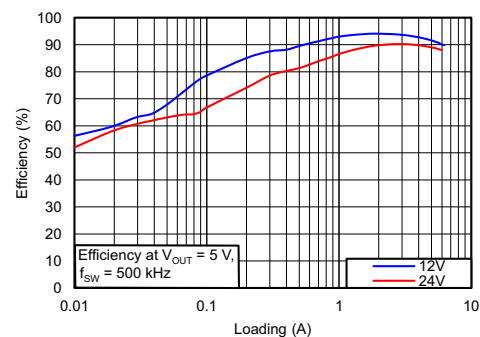
### 製品情報(1)

| 発注型番 | パッケージ | 本体サイズ |
|---|---|---|
| TPS65286 | VQFN (28) | 5.00mm×5.00mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

### 概略回路図



### 効率



Efficiency at $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz

12V / 24V

# 目次

# 4 改訂履歴

**2014年3月発行のものから更新**                                                                                                               **Page**

- Changed Ambient temperature $T_A$ to Junction temperature $T_J$ in *Recommended Operating Conditions* ............................. 5
- Changed $I_{OS}$ values when $R_{SET}$ shorted to SW_IN or open From: MIN = 1.18 TYP = 1.2 MAX = 1.34 To: MIN = 1.22 TYP = 1.31 MAX = 1.39 in the *Electrical Characteristics* ....................................................................................................... 7

# 5 Pin Configuration and Functions

**RHD Package**
**28-Pin VQFN**
**Top View**
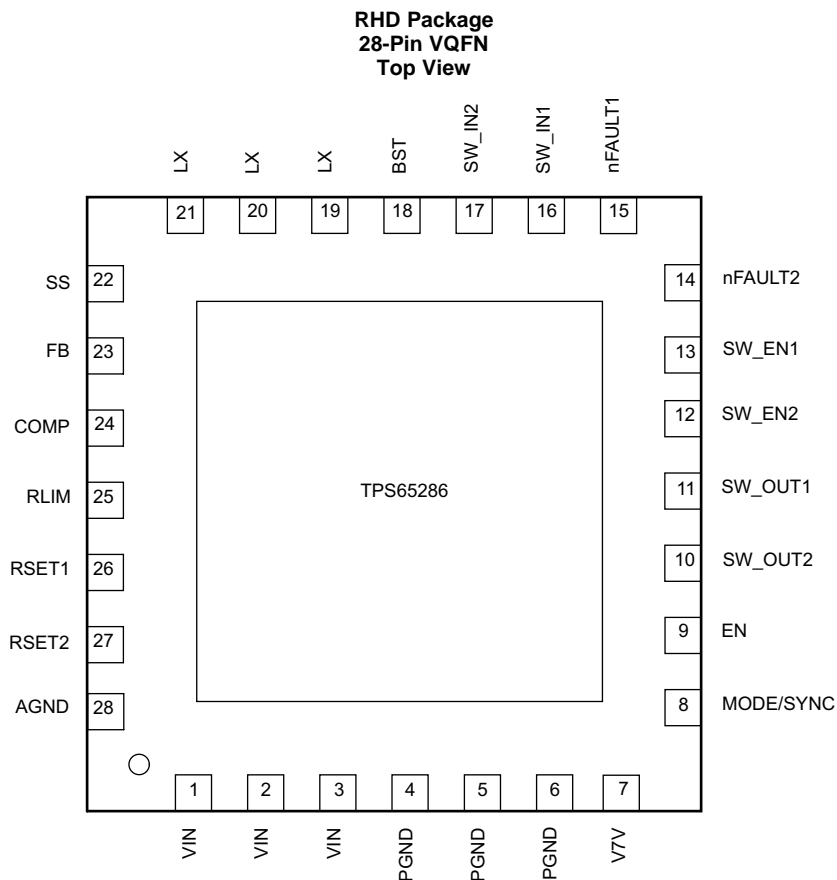


There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

## Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NUMBER | |
| VIN | 1, 2, 3 | Input power supply for buck. Connect this terminal as close as practical to the (+) terminal of an input ceramic capacitor (suggest 22 µF). |
| PGND | 4, 5, 6 | Power ground connection. Connect this terminal as close as practical to the (-) terminal of input capacitor. |
| V7V | 7 | Internal low-drop linear regulator (LDO) output. The internal driver and control circuits are powered from this voltage. Decouple this terminal to power ground with a minimum 1-M µF ceramic capacitor. The output voltage level of LDO is regulated to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor. |
| MODE/SYNC | 8 | External synchronization input to internal clock oscillator in forced continuous mode. When an external clock is applied to this terminal, the internal oscillator will force the rising edge of clock signal to be synchronized with the falling edge of the external clock. Connecting this terminal to ground forces a continuous current mode (CCM) operation in buck converter. Connecting this terminal to V7V the buck converter will automatically operate in pulse skipping mode (PSM) at light load condition to save the power. |
| EN | 9 | Enable for buck converter. Adjust the input under-voltage lockup with two resistors. |
| SW_OUT2 | 10 | Power switch 2 output |
| SW_OUT1 | 11 | Power switch 1 output |
| SW_EN2 | 12 | Enable power switch 2. There is an internal 1.25-MΩ pull-up resistor connecting this terminal to SW_IN2. |
| SW_EN1 | 13 | Enable power switch 1. There is an internal 1.25-MΩ pull-up resistor connecting this terminal to SW_IN1. |
| nFAULT2 | 14 | Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 2. |
| nFAULT1 | 15 | Active low open drain output, asserted during over-current or reverse-voltage condition of power switch 1. |
| SW_IN1 | 16 | Power switch input voltage for USB1. Connect to buck output, or other power supply input. |
| SW_IN2 | 17 | Power switch input voltage for USB2. Connect to buck output, or other power supply input. |
| BST | 18 | Bootstrapped supply to the high side floating gate driver in buck converter. Connect a capacitor (recommend 47 nF) from this terminal to LX. |
| LX | 19, 20, 21 | Switching node connection to the inductor and bootstrap capacitor for buck converter. This terminal voltage swings from a diode voltage below the ground up to $V_{IN}$ voltage. |
| SS | 22 | Soft-start and tracking input for buck converter. An internal 5.5-µA pull-up current source is connected to this terminal. An external soft-start can be programmed by connecting a capacitor between this terminal and ground. Leave the terminal floating to have a default 1ms of soft-start time. This terminal allows the start-up of buck output to track an external voltage using an external resistor divider at this terminal. |
| FB | 23 | Feedback sensing terminal for buck output voltage. Connect this terminal to the resistor divider of buck output. The feedback reference voltage is 0.6 V ±1%. |
| COMP | 24 | Error amplifier output and Loop compensation terminal for buck. Connect a series resistor and capacitor to compensate the control loop of buck converter with peak current PWM mode. |
| RLIM | 25 | BUCK current limit control terminal. An external resistor used to set current limit threshold of buck converter. Recommended 120 kΩ ≤ RLIM ≤ 450kΩ. Connect this terminal to GND, set the current limit to 8 A. |
| RSET1 | 26 | Power switch current limit control terminal. An external resistor used to set current limit threshold of power switch 1. Recommended 9.1 kΩ ≤ RLIM ≤ 300 kΩ. |
| RSET2 | 27 | Power switch current limit control terminal. An external resistor used to set current limit threshold of power switch 2. Recommended 9.1 kΩ ≤ RLIM ≤ 300 kΩ. |
| AGND | 28 | Analog ground common to buck controller and power switch controller. AGND must be routed separately from high current power grounds to the (-) terminal of bypass capacitor of internal V7V LDO output. |
| Thermal pad | – | Exposed pad beneath the IC. Connect to the power ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to pad inside the IC package. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VIN, LX | −0.3 | 30 | V |
| | LX (maximum withstand voltage transient < 20 ns) | −1 | 30 | |
| | BST referenced to LX terminal | −0.3 | 7 | |
| | SW_IN1, SW_OUT1, SW_ IN2, SW_ OUT2 | −0.3 | 7 | |
| | EN, SW_EN1, SW_EN2, nFAULT1, nFAULT2, V7V, MODE/SYNC | −0.3 | 7 | |
| | SS, COMP , RLIM, RSET1, RSET2, FB | −0.3 | 3.6 | |
| | AGND, PGND | −0.3 | 0.3 | |
| Operating virtual junction temperature range, $T_J$ | | −40 | 125 | °C |
| Storage temperature range, $T_{stg}$ | | -55 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{ESD}$[1] | Human body model (HBM) ESD stress voltage[2] | 2000 | V |
| | Charge device model (CDM) ESD stress voltage[3] | 500 | |

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. *Terminals listed as 1 kV may actually have higher performance.*
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. *Terminals listed as 250 V may actually have higher performance.*

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input operating voltage | 4.5 | | 28 | V |
| $T_J$ | Junction temperature | −40 | | 125 | °C |

## 6.4 Thermal Information

| | | TPS65286 | UNIT |
|---|---|---|---|
| | THERMAL METRIC[1] | RHD (VQFN) | |
| | | 28 PIN | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 35.6 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 24.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.9 | °C/W |
| $R_{\psi JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $R_{\psi JB}$ | Junction-to-board characterization parameter | 7.96 | °C/W |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance | 1.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

$T_J$ = 25°C, $V_{IN}$ = 24 V, $f_{SW}$ = 500 kHz, $R_{nFAULTx}$ = 100 k$\Omega$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | VIN1 and VIN2 | 4.5 | | 28 | V |
| $IDD_{SDN}$ | Shutdown supply current | EN1 = EN2 = low | | 7.60 | 15 | µA |
| $IDD_{Q\_NSW}$ | Quiescent current without buck switching | EN = high, ENx = low, FB = 1 V Without buck switching | | 0.8 | | mA |
| $IDD_{Q\_SW}$ | Input quiescent current with buck switching | EN = high, ENx = low, FB = 0.6 V With buck switching | | 26 | | mA |
| UVLO | $V_{IN}$ under voltage lockout | Rising $V_{IN}$ | 4 | 4.25 | 4.50 | V |
| | | Falling $V_{IN}$ | 3.75 | 4 | 4.25 | |
| | | Hysteresis | | 0.25 | | |
| $V_{7V}$ | Low side gate driver, controller, biasing supply | $V_{7V}$ load current = 0 A, $V_{IN}$ = 24 V | 6.10 | 6.25 | 6.4 | V |
| $I_{OCP\_7V}$ | Current limit of V7V LDO | | | 83 | | mA |
| **ENABLE** | | | | | | |
| $V_{ENR}$ | Enable threshold | Rising | | 1.21 | 1.26 | V |
| $V_{ENF}$ | Enable threshold | Falling | 1.10 | 1.17 | | V |
| $I_{ENL}$ | Enable pull-up current | EN = 1 V | | 3 | | µA |
| $I_{ENH}$ | Enable pull-up current | EN = 1.5 V | | 6 | | µA |
| $I_{ENHYS}$ | Enable hysteresis current | | | 3 | | µA |
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Switching frequency | Internal oscillator clock frequency | 400 | 500 | 600 | kHz |
| $T_{SYNC\_w}$ | Clock sync minimum pulse width | | 80 | | | ns |
| $V_{SYNC\_HI}$ | Clock sync high threshold | | | | 2 | V |
| $V_{SYNC\_LO}$ | Clock sync low threshold | | 0.8 | | | V |
| $V_{SYNC\_D}$ | Clock falling edge to LX rising edge delay | | | | 120 | ns |
| $f_{SYNC}$ | Clock sync frequency range | | 200 | | 1600 | kHz |
| **BUCK CONVERTER** | | | | | | |
| $V_{IN}$ | Input supply voltage | | 4.5 | | 28 | V |
| $V_{FB}$ | Feedback voltage | $V_{COMP}$ = 1.2 V, $T_J$ = 25°C | 0.594 | 0.6 | 0.606 | %/V |
| | | $V_{COMP}$ = 1.2 V, $T_J$ = 40°C to 125°C | 0.588 | 0.6 | 0.612 | |
| $G_{m\_EA}$ | Error amplifier trans-conductance | -4 µA < $I_{COMP}$ < 4 µA | | 1240 | | µS |
| $G_{m\_SRC}$ | COMP voltage to inductor current Gm[1] | $I_{LX}$ = 0.5 A | | 9.2 | | A/V |
| $I_{SS}$ | Soft-Start terminal charging current | SS = 1 V | | 5.5 | | µA |
| $T_{SS\_INT}$ | Internal Soft-Start time | SS terminal floats | 0.5 | 1 | 1.5 | ms |
| $I_{LIMIT}$ | Buck peak inductor current limit | $R_{LIM}$ = 0 $\Omega$ | 6.6 | 7.7 | 8.7 | A |
| | | $R_{LIM}$ = 200 k$\Omega$ | | 5.2 | | |
| $T_{ON\_MIN}$ | Minimum on time (current sense blanking) | | | 85 | 120 | ns |
| $R_{dson\_HS}$ | On resistance of high side FET | V7V = 6.25 V, includes bondwire resistance | | 55 | | m$\Omega$ |
| $R_{dson\_LS}$ | On resistance of low side FET | $V_{IN}$ = 24 V, includes bondwire resistance | | 30 | | m$\Omega$ |
| $T_{hiccupwait}$ | Hiccup wait time | | | 256 | | cycles |
| $T_{hiccup\_re}$ | Hiccup time before re-start | | | 8192 | | cycles |

(1) Ensured by design.

## Electrical Characteristics (continued)

$T_J$ = 25°C, $V_{IN}$ = 24 V, $f_{SW}$ = 500 kHz, $R_{nFAULTx}$ = 100 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER DISTRIBUTION SWITCH** | | | | | | |
| $V_{SW\_IN}$ | Power switch input voltage range | | 2.5 | | 6 | V |
| $V_{UVLO\_SW}$ | Input under-voltage lock out | $V_{SW\_IN}$ rising | 2.15 | 2.25 | 2.35 | V |
| | | $V_{SW\_IN}$ falling | 2.05 | 2.15 | 2.25 | |
| | | Hysteresis | | 0.1 | | |
| $R_{DSON\_SW}$ | Power switch NDMOS on-resistance | $V_{SW\_INx}$ = 5 V, $I_{SW\_OUTx}$ = 0.5 A, $T_J$ = 25°C, includes bondwire resistance | | 100 | | mΩ |
| | | $V_{SW\_INx}$ = 2.5 V, $I_{SW\_OUTx}$ = 0.5 A, $T_J$ = 25°C, includes bondwire resistance | | 100 | | |
| $t_{D\_on}$ | Turn-on delay time | $V_{SW\_INx}$ = 5 V, $C_L$ = 10 µF, $R_L$ = 100 Ω (see Figure 1) | | 1.26 | 1.9 | ms |
| $t_{D\_off}$ | Turn-off delay time | | | 1.17 | 1.76 | ms |
| $t_r$ | Output rise time | | | 0.86 | 1.3 | ms |
| $t_f$ | Output fall time | | | 1.37 | 2.06 | ms |
| $I_{OS}$ | Current limit threshold (Maximum DC current delivered to load) and short circuit current, SW_OUT connect to ground | $R_{SET}$ = 14.3 kΩ | 1.65 | 1.76 | 1.87 | A |
| | | $R_{SET}$ = 20 kΩ | 1.18 | 1.26 | 1.34 | |
| | | $R_{SET}$ = 50 kΩ | | 0.5 | | |
| | | $R_{SET}$ shorted to SW_IN or open | 1.22 | 1.31 | 1.39 | |
| $T_{IOS}$ | Response time to short circuit | $V_{SW\_IN}$x = 5 V | | 2 | | us |
| $T_{DEGLITCH(OCP)}$ | Switch over current fault deglitch | Fault assertion or de-assertion due to over-current condition | 7 | 10 | 13 | ms |
| $V_{L\_nFAULT}$ | nFAULTx terminal output low voltage | $I_{nFAULTx}$ = 1 mA | | | 400 | mV |
| $V_{EN\_SWH}$ | SW_EN1/2 high level input voltage | SW_EN1, SW_EN2 | 2 | | | V |
| $V_{EN\_SWL}$ | SW_EN1/2 low level input voltage | SW_EN1, SW_EN2 | | | 0.4 | V |
| $R_{DIS}$ | Discharge resistance[(2)] | $V_{SW\_INx}$ = 5 V, $V_{SW\_ENx}$ = 0 V | | 104 | | Ω |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{TRIP\_BUCK}$ | Thermal protection trip point | Rising temperature | | 160 | | °C |
| $T_{HYST\_BUCK}$ | | Hysteresis | | 20 | | °C |
| $T_{TRIP\_SW}$ | Power switch thermal protection trip point | Rising temperature | | 145 | | °C |
| $T_{HYST}$ | | Hysteresis | | 20 | | °C |

(2)   The discharge function is active when the device is disabled (when enable is de-asserted). The discharge function offers a resistive discharge path for the external storage capacitor.
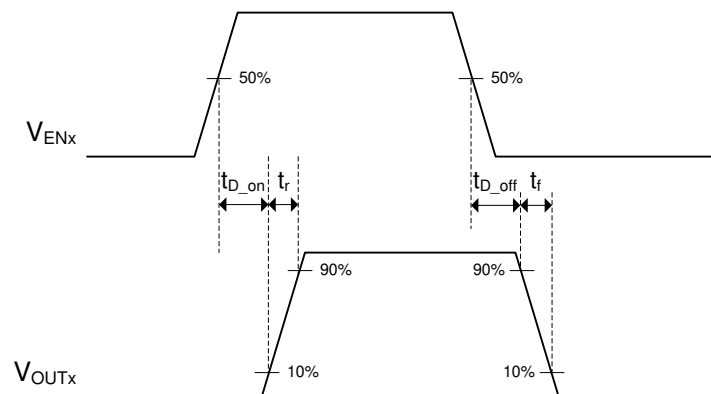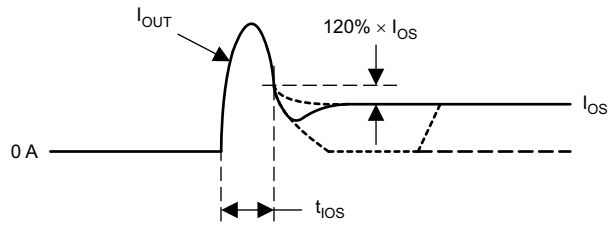


**Figure 1.  Power Switches Test Circuit and Voltage Waveforms**
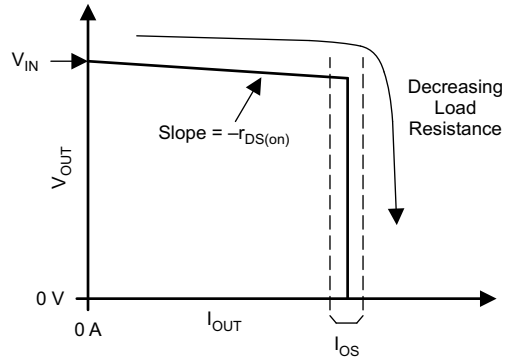
**Figure 2. Response Time to Short Circuit Waveform**



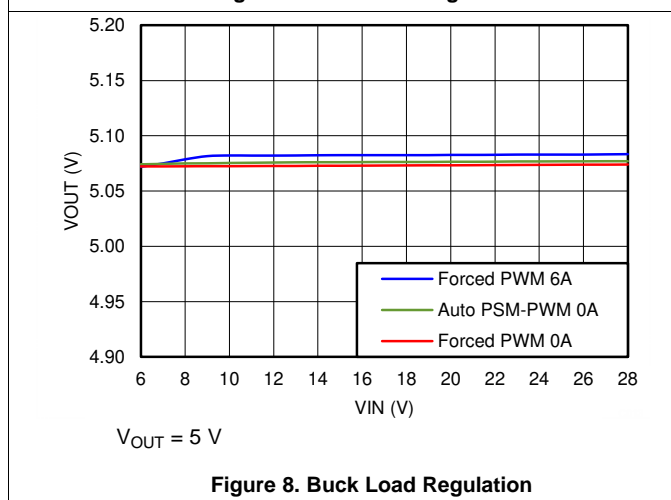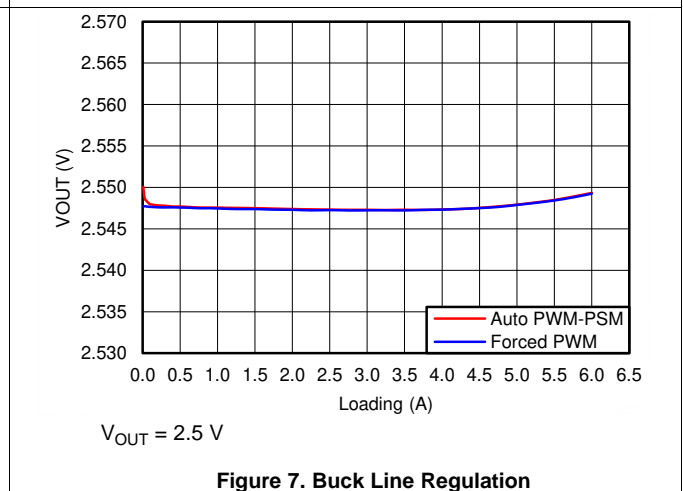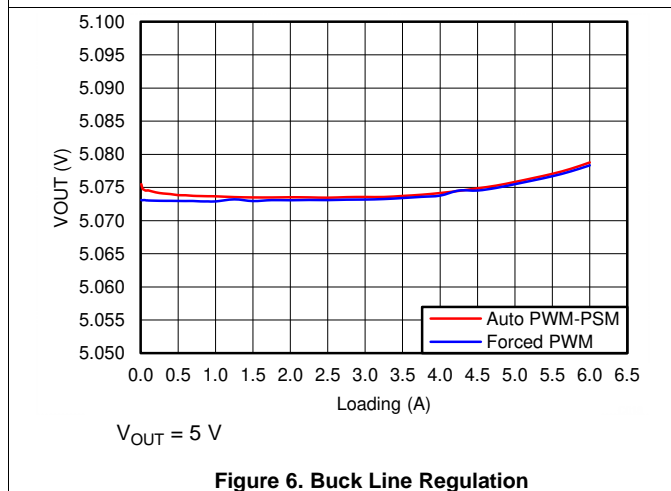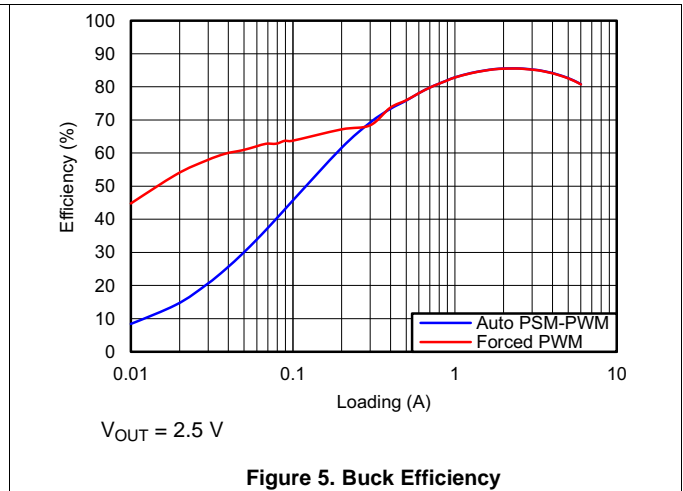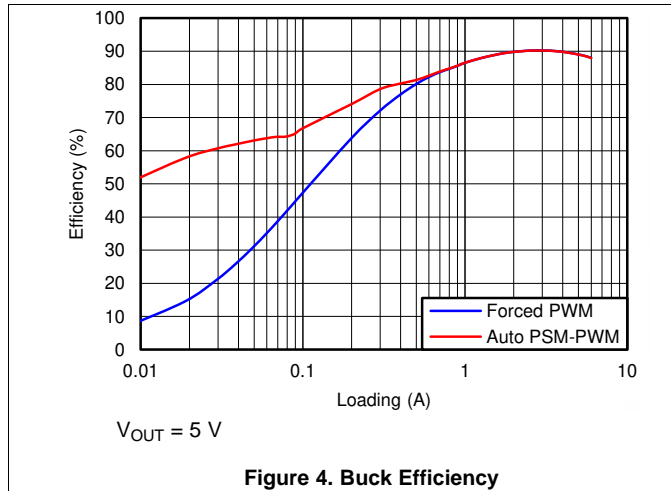**Figure 3. Output Voltage vs Current Limit Threshold**

## 6.6 Typical Characteristics

$T_A$ = 25°C, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz, $R_{nFAULT}$ = 100 kΩ (unless otherwise noted)
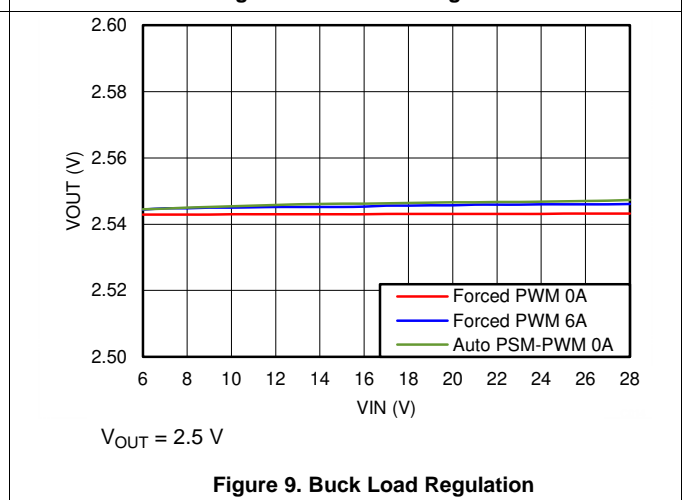
$V_{OUT}$ = 5 V

**Figure 4. Buck Efficiency**

$V_{OUT}$ = 2.5 V

**Figure 5. Buck Efficiency**

$V_{OUT}$ = 5 V

**Figure 6. Buck Line Regulation**

$V_{OUT}$ = 2.5 V

**Figure 7. Buck Line Regulation**

$V_{OUT}$ = 5 V

**Figure 8. Buck Load Regulation**

$V_{OUT}$ = 2.5 V

**Figure 9. Buck Load Regulation**

## Typical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz, $R_{nFAULT}$ = 100 kΩ (unless otherwise noted)
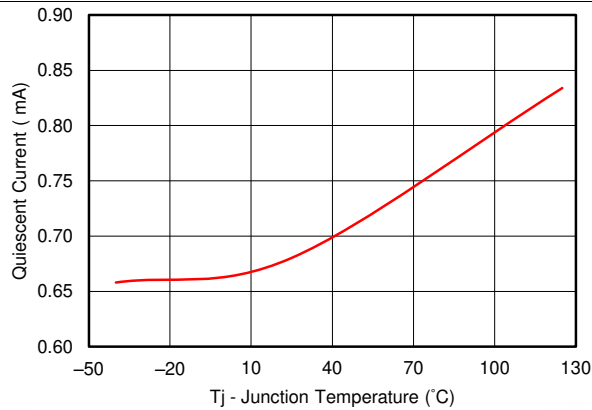
**Figure 10. $I_{IN}$ (Without Switching) vs Temperature**
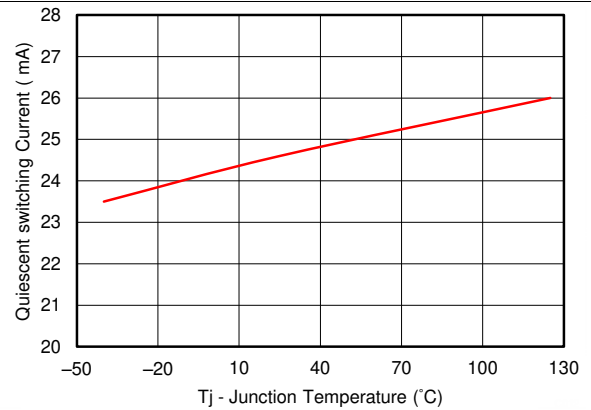
**Figure 11. $I_{IN}$ (With Buck Switching) vs Temperature**
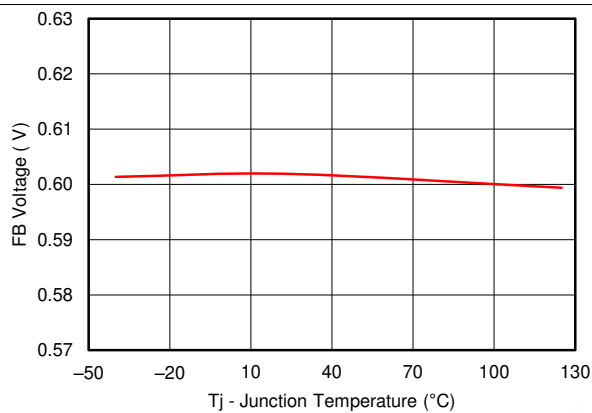
**Figure 12. Reference Voltage vs Temperature**
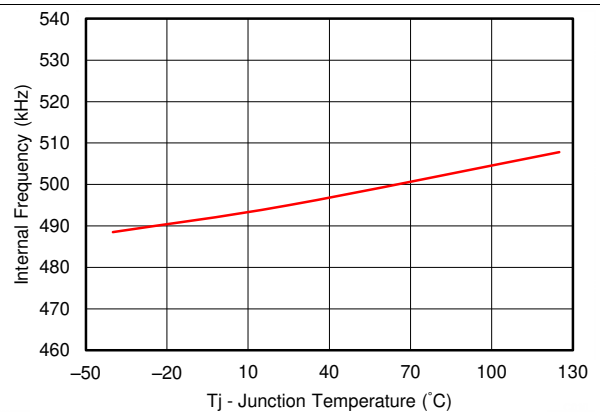
**Figure 13. Oscillator Frequency vs Temperature**
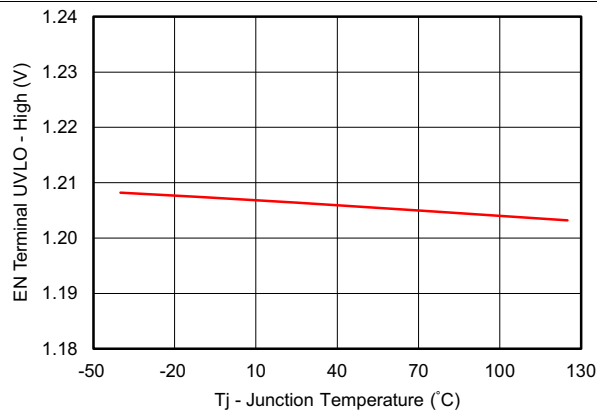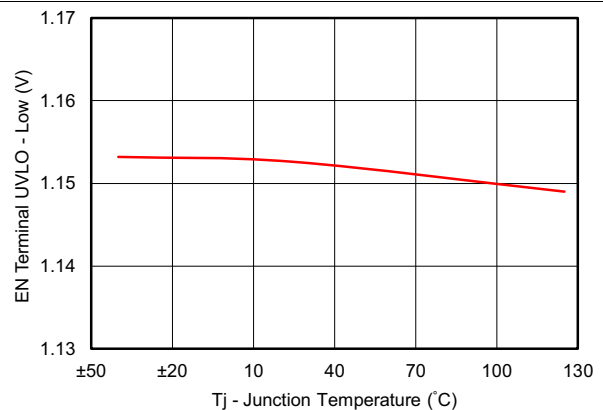
**Figure 14. EN UVLO Start vs Temperature**

**Figure 15. EN UVLO Stop vs Temperature**

## Typical Characteristics (continued)

$T_A$ = 25°C, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz, $R_{nFAULT}$ = 100 kΩ (unless otherwise noted)
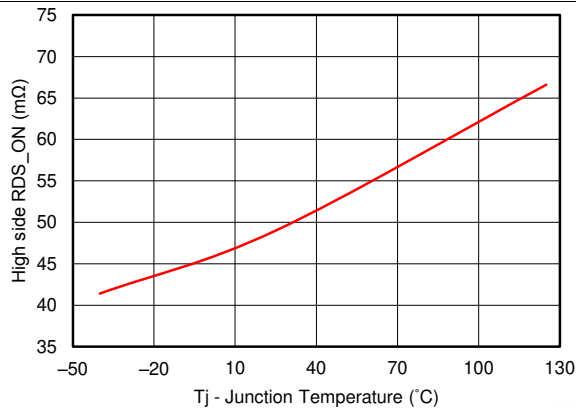


Figure 16. High-Side $R_{DS\_ON}$ vs Temperature
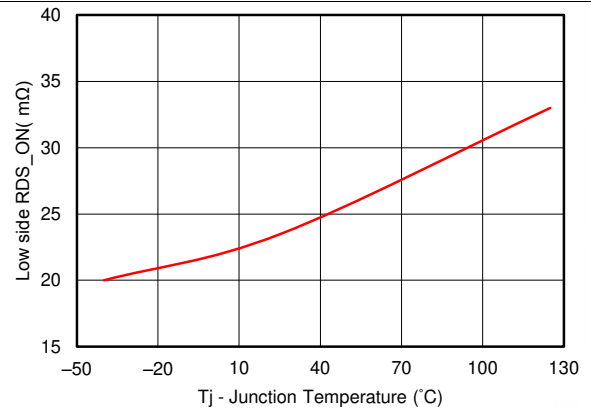


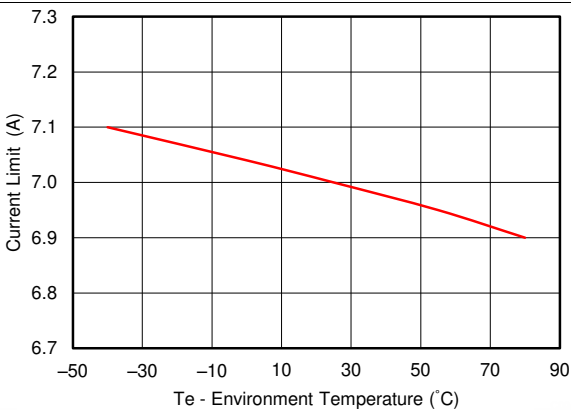Figure 17. Low-Side $R_{DS\_ON}$ vs Temperature



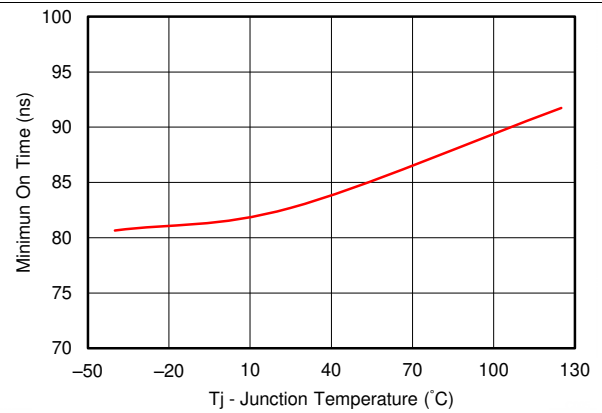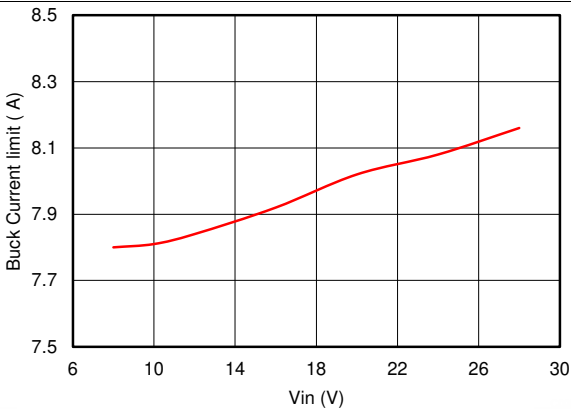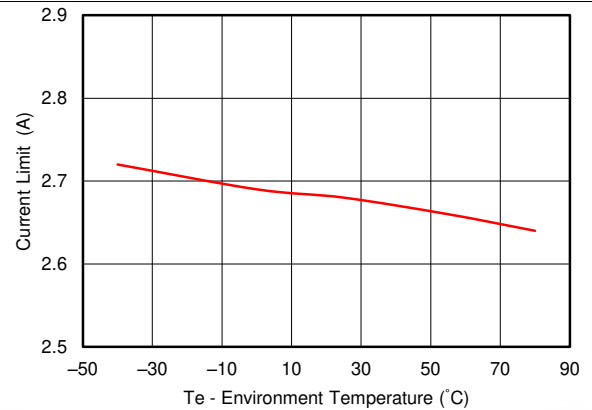Figure 18. Buck DC Max $I_{OUT}$ vs Temperature



Figure 19. Minimum On Time vs Temperature



RLIMIT = 120 kΩ

Figure 20. Buck Current Limit vs $V_{IN}$



RSET = 9.1 kΩ

Figure 21. Power Switch Current Limit vs Temperature

# 7 Detailed Description

## 7.1 Overview

The TPS65286 PMIC integrates two independent current-limited, power distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide precision current limit protection and fast protection response to over current. Additional device features include over temperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate driver circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from the input voltage of power switches as low as 2.5 V. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS65286 device limits output current to a safe level when output load exceeds the current limit threshold. After deglitching time, the device latches off when the load exceeds the current limit threshold. The device asserts the nFAULT1/2 signal during over current or reverse voltage faulty condition.

The TPS65286 PMIC also integrates a synchronous step-down converter with regulated 0.6 V ±1% feedback reference voltage. The synchronous buck converter incorporates 55-mΩ high side power MOSFET and 30-mΩ low side power MOSFETs to achieve high efficiency power conversion. The converter supports an input voltage range from 4.5 V to 28 V. The converter operates in continuous conduction mode (CCM) with peak current mode control for simplified loop compensation. The peak inductor current limit threshold is adjustable to up to 8 A. The switching clock frequency is a fixed 500 kHz. The soft-start time can be adjusted by connecting an external capacitor at the SS terminal or fixed at 1 ms with the SS terminal open.

## 7.2 Functional Block Diagram
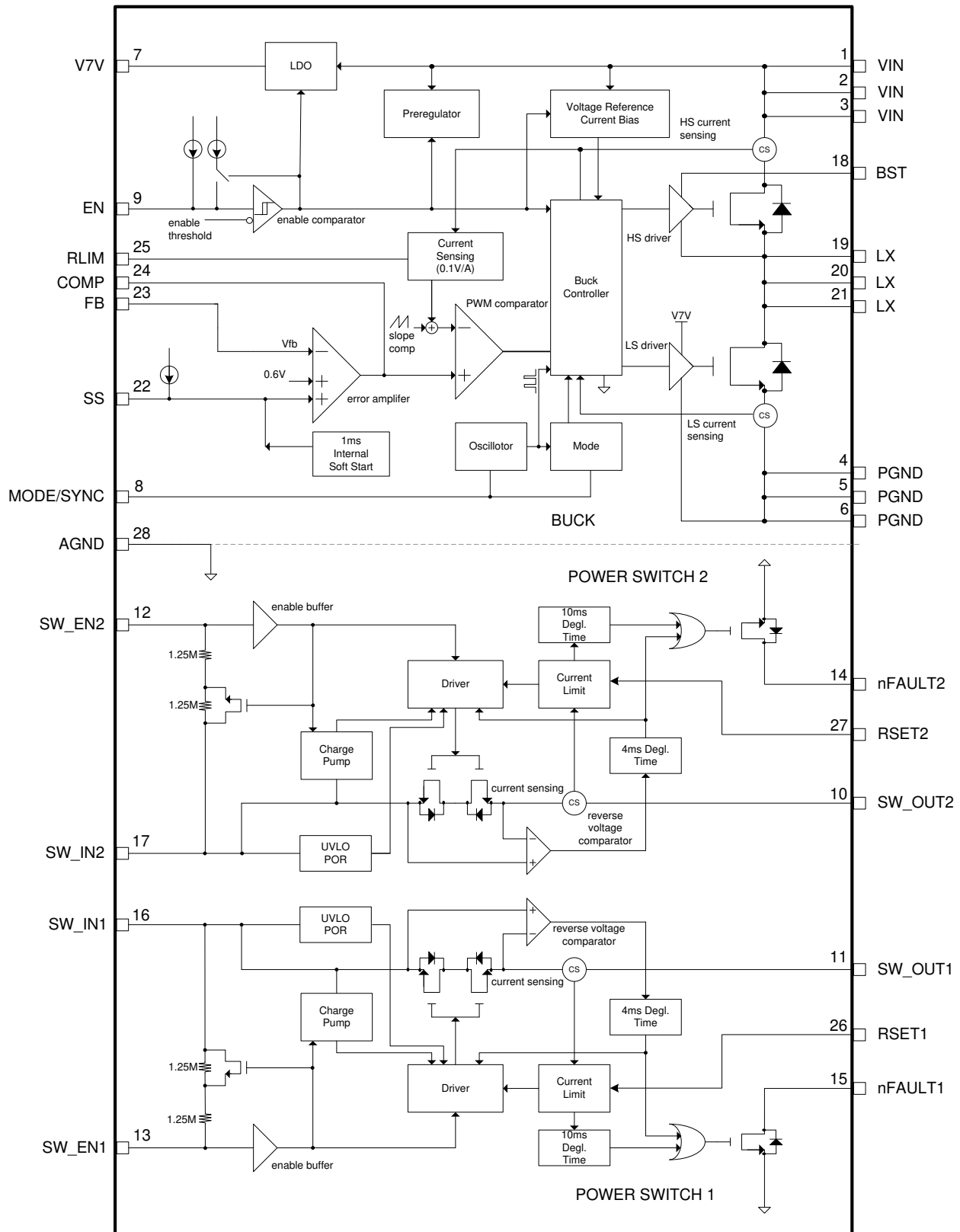
## 7.3 Feature Description

### 7.3.1 Power Switch

#### 7.3.1.1 Over Current Condition

The TPS65286 responds to over-current conditions on power switches by limiting the output currents to the $I_{OS}$ level, which is set by an external resistor. During normal operation the N-channel MOSFET is fully enhanced, and $V_{SW\_OUT} = V_{SW\_IN}$ - ($I_{SW\_OUT}$ x $R_{DSON\_SW}$). The voltage drop across the MOSFET is relatively small compared to $V_{SW\_IN}$, and $V_{SW\_OUT} \approx V_{SW\_IN}$. When an over current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. During current-limit operation, the N-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{SW\_IN} \neq V_{SW\_OUT}$) and $V_{SW\_OUT}$ decreases. The amount that $V_{SW\_OUT}$ decreases is proportional to the magnitude of the overload condition. The expected $V_{SW\_OUT}$ can be calculated by $I_{OS} \times R_{LOAD}$, where $I_{OS}$ is the current-limit threshold and $R_{LOAD}$ is the magnitude of the overload condition.

Three possible overload conditions can occur as summarized in Table 1.

**Table 1. Overload Conditions**

| CONDITIONS | BEHAVIORS |
|---|---|
| Short circuit or partial short circuit present when the device is powered up or enabled. | The output voltage is held near zero potential with respect to ground and the TPS65286 ramps output current to $I_{OS}$. The device limits the current to $I_{OS}$ until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled. |
| Gradually increasing load (< 100 A/s) from normal operating current to $I_{OS}$. | The current rises up to the current limit. Once the threshold has been reached, the device switches into its current limiting at $I_{OS}$. The device limits the current to $I_{OS}$ until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled. |
| Short circuit, partial short circuit or fast transient overload occurs while the device is enabled and powered on. | The device responds to the over-current condition within time $t_{IOS}$. The current sensing amplifier is overdriven during this time and needs time for loop response. Once $t_{IOS}$ has passed, the current sensing amplifier recovers and limits the current to $I_{OS}$. The device limits the current to $I_{OS}$ until the overload condition is removed or the internal deglitch time (10 ms typical) is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled. |

#### 7.3.1.2 Reverse Current and Voltage Protection

A power switch in the TPS65286 incorporates dual back-to-back N-channel power MOSFETs so as to prevent the reverse current flowing back the input through body diode of MOSFET when the power switches are off.

The reverse-voltage protection turns off the N-channel MOSFETs whenever the output voltage exceeds the input voltage by 135 mV (typical) for 4 ms (typical). This prevents damaging devices by blocking significant current reverse injection into the input capacitance of power switch or buck output capacitance. The TPS65286 keeps the power switch turned off even if the reverse-voltage condition is removed and does not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the nFAULT1/2 output (active-low) after 4 ms.

#### 7.3.1.3 nFAULT1/2 Response

The nFAULT1/nFAULT2 open-drain output is asserted (active low) during an over current, over temperature or reverse-voltage condition and remains asserted while the part is latched-off. The nFAULT signal is de-asserted once the device power is cycled or the enable is toggled and the device resumes normal operation. The TPS65286 is designed to eliminate false nFAULT reporting by using an internal delay deglitch circuit for over current (10 ms typical) and reverse-voltage (4 ms typical) conditions without the need for external circuitry. This ensures that nFAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Deglitching circuitry delays entering and leaving fault conditions. Over temperature conditions are not deglitched and assert the FAULT signal immediately. Figure 22 shows the over current operation of USB switch.
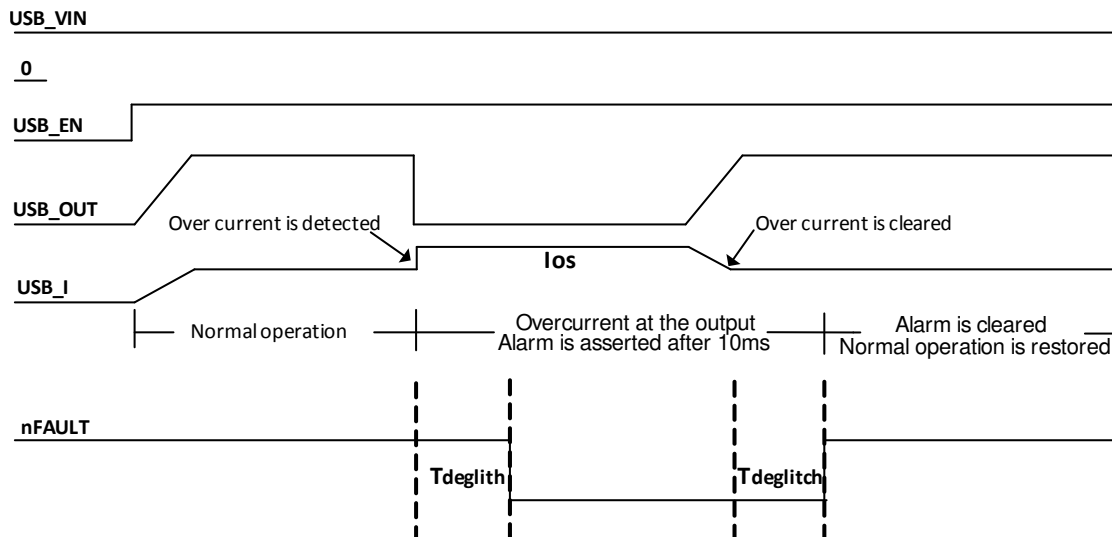
**Figure 22. USB Switch Over Current Operation**

### 7.3.1.4 Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

### 7.3.1.5 Enable and Output Discharge

The logic enable EN_SW1/EN_SW2 controls the power switch, bias for the charge pump, driver, and other circuits. The supply current from power switch driver is reduced to less than 1 µA when a logic low is present on EN_SW1/2. A logic high input on EN_SW1/EN_SW2 enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

When enable is de-asserted, the discharge function is active. The output capacitor of power switch is discharged through an internal NMOS with a 104-Ω resistance. The time taken for discharging is dependent on the RC time constant of the resistance and the output capacitor.

### 7.3.1.6 Power Switch Input and Output Capacitance

Input and output capacitors improve the performance of the device. The actual capacitance should be optimized for the particular application. The output capacitor in buck converter is recommended to place between SW_IN and AGND as close to the device as possible for local noise de-coupling. Additional capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the input of power switches in the evaluation board to the bench power-supply. Placing a high-value electrolytic capacitor on the output terminal is recommended when large transient currents are expected on the output.

### 7.3.1.7 Programming the Current-Limit Threshold

The over-current threshold is user programmable via an external resistor. The TPS65286 uses an internal regulation loop to provide a regulated voltage reference on the RLIM terminal. The current-limit threshold is proportional to the current sourced out of the RSET terminal. A resistor with 1% accuracy is used between 10 kΩ ≤ RSET ≤ 232 kΩ to ensure stability of the internal regulation loop. Equation 1 and Figure 23 can be used to calculate current limiting threshold for a given external resistor value.

Current-limit threshold equation ($I_{OS}$):

$$I_{OS} = 27.465 \times (R_{SET})^{-1.04}$$ (1)
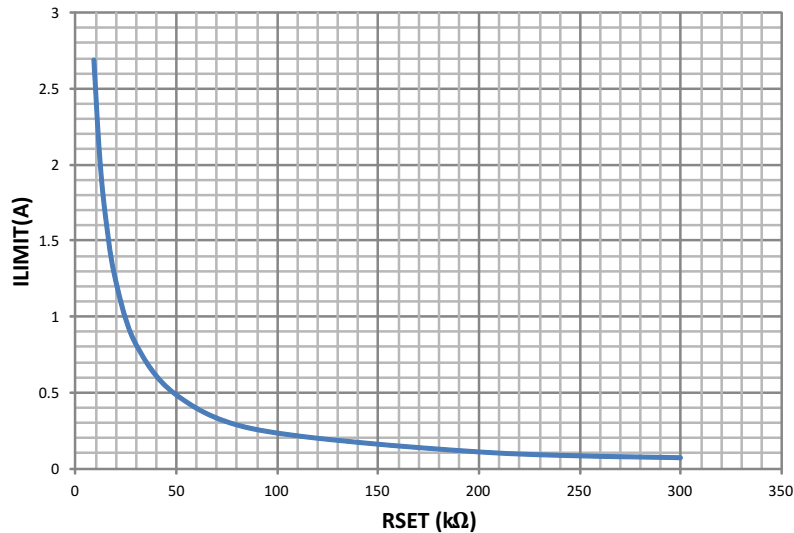
**Figure 23. Current-Limit Threshold $I_{OS}$ vs RLIM**

### 7.3.2 Buck DCDC Converter

#### 7.3.2.1 Output Voltage

The TPS65286 regulate output voltage set by a feedback resistor divider to 0.6-V reference voltage with feedback resistor divider. It is recommended to use 1% tolerance or better divider resistors. Great care should be taken to route the FB line away from noise sources, such as the inductor or the LX switching node line. Start with 39 kΩ for the R1 resistor and use Equation 2 to calculate R2.

$$R_2 = R_1 \cdot \left( \frac{0.6V}{V_{OUT} - 0.6V} \right)$$

(2)
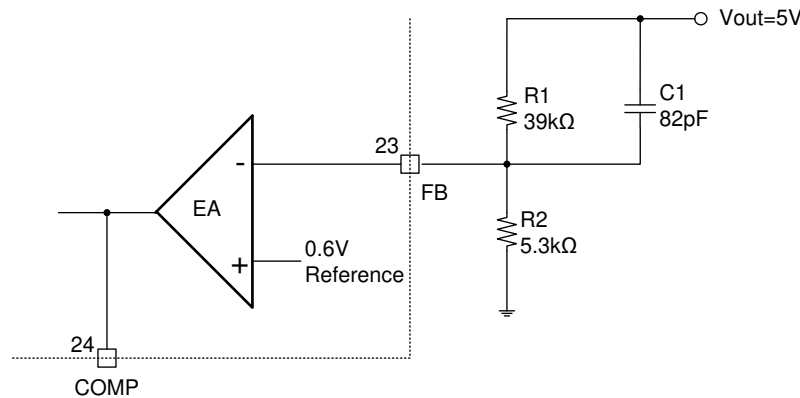


**Figure 24. Buck Feedback Resistor Divider**

#### 7.3.2.2 Clock Synchronization

An internal phase locked loop (PLL) has been implemented to allow an external clock with frequency between 200 kHz and 1600 kHz to be synchronized to the internal clock. To implement the synchronization feature, connect a clock signal to the MODE/SYNC terminal with minimum pulse width larger than 80 ns and low/high voltage threshold at 0.4 V/2V. When an external clock is applied to MODE/SYNC terminal, the internal oscillator will force the rising edge of clock signal to be synchronized with the falling edge of the external clock.
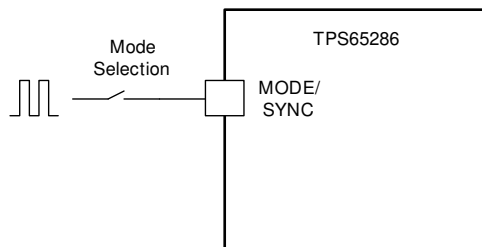
**Figure 25. Clock Synchronization Mode**

### 7.3.2.3 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the SS terminal voltage or the internal 0.6-V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP terminal and ground.

### 7.3.2.4 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The slope rate of slope compensation remains constant over the full duty cycle range.

### 7.3.2.5 Enable and Adjusting Under-Voltage Lockout

The EN terminal provides electrical on/off control of the device. Once the EN terminal voltage exceeds the threshold voltage, the device starts operation. If the EN terminal voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. The EN terminal has an internal pull-up current source, allowing the user to float the EN terminal for enabling the device. If an application requires controlling the EN terminal, use open drain or open collector output logic to interface with the terminal. The device implements internal UVLO circuitry on the VIN terminal. The device is disabled when the VIN terminal voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV. If an application requires either a higher UVLO threshold on the VIN terminal or a secondary UVLO on the PVIN in split rail applications, then the EN terminal can be configured as shown in Figure 26. When using the external UVLO function, it is recommended to set the hysteresis to be greater than 500 mV.

The EN terminal has an internal pull-up current source, allowing the user to float the EN terminal for enabling the device. If an application requires controlling the EN terminal, use open drain or open collector output logic to interface with the terminal. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by $I_h$ once the EN terminal crosses the enable threshold. The UVLO thresholds can be calculated using Equation 3 and Equation 4.
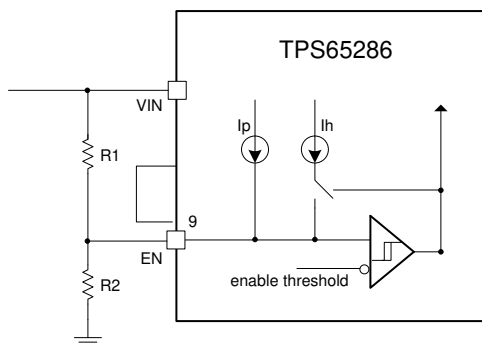


**Figure 26. Adjustable VIN Under Voltage Lock Out**

$$R_1 = \frac{V_{START}(\frac{V_{ENFALLING}}{V_{ENRISING}}) - V_{STOP}}{I_P(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}) + I_h}$$

(3)

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_h + I_p)}$$

(4)

Where $I_h$ = 1 µA, $I_p$ = 2 µA, $V_{ENRISING}$ = 1.21 V, and $V_{ENFALLING}$ = 1.17 V.

### 7.3.2.6  Soft-Start Time

During startup, the output voltage follows up the voltage at the SS terminal to prevent inrush current. When the SS terminal voltage is less than the internal 0.6-V reference, the TPS65286 regulates the feedback voltage to the SS terminal voltage. The SS terminal can be used to program an external soft-start function or to allow output of the buck to track another supply during start-up. An internal pull-up current source of 5.5 µA charges an external soft-start capacitor to provide a ramping voltage at SS terminal. The TPS65286 will regulate the feedback voltage to the SS terminal voltage and VOUT rises smoothly from 0 V to its final regulated voltage. The soft-start time can be calculated by Equation 5:

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(uA)}$$

(5)

With a floating SS terminal, there is default 1-ms (typical) soft-start time built in the chip.

### 7.3.2.7  Internal V7V Regulator

The TPS65286 features an internal low dropout linear regulator (LDO) from VIN to V7V. The LDO regulates V7V to 6.3-V over drive voltage on power MOSFET for the best efficiency performance. the LDO also provides supply bias for internal analog controller and power for low-side MOSFET for the best efficiency performance. The current limit of LDO is 50 mA and connecting a minimum 1-µF ceramic capacitor to the V7V terminal is recommended. Directly placing the capacitor close to the V7V and PGND terminals is highly recommended for high transient current required by the MOSFET gate drivers.

### 7.3.2.8  Hard Short Circuit Protection

The peak inductor current limit trip of buck converter is set by an external resistor at the RLIM terminal. The peak inductor current threshold for over current protection can be calculated by Equation 6.

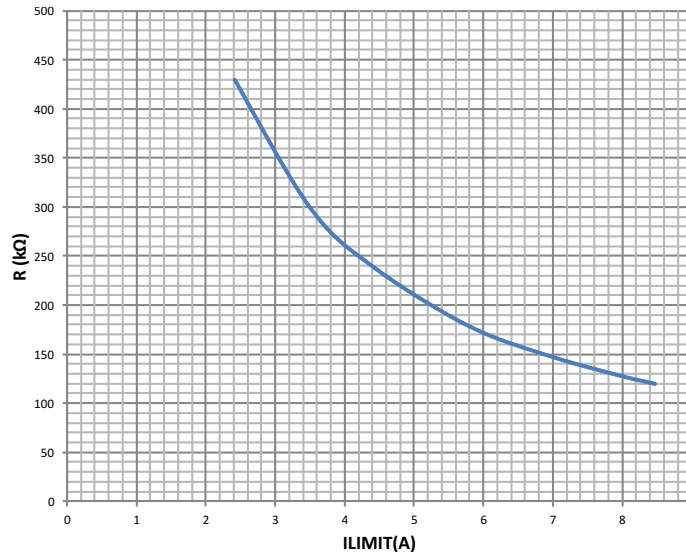$$I_{LIMIT} = 926.78 \times (R_{LIM})^{-0.979} \tag{6}$$



**Figure 27.  Current-Limit Threshold vs RLIM**

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-side MOSFET over current protection:

The device implements current mode control which uses the COMP terminal voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP terminal voltage are compared, the peak switch current intersects the current reference and the high-side switch is turned off.

Low-side MOSFET over current protection:

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally sourcing current limit threshold. If the low-side sourcing current is exceeded, the high-side MOSFET is turned off and the low-side MOSFET is forced on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit threshold at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the next cycle. Furthermore, if an output overload condition (as measured by the COMP terminal voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles, the device will shut down and recover after the hiccup time of 8192 cycles. The hiccup mode helps to reduce the device power dissipation under over current conditions.
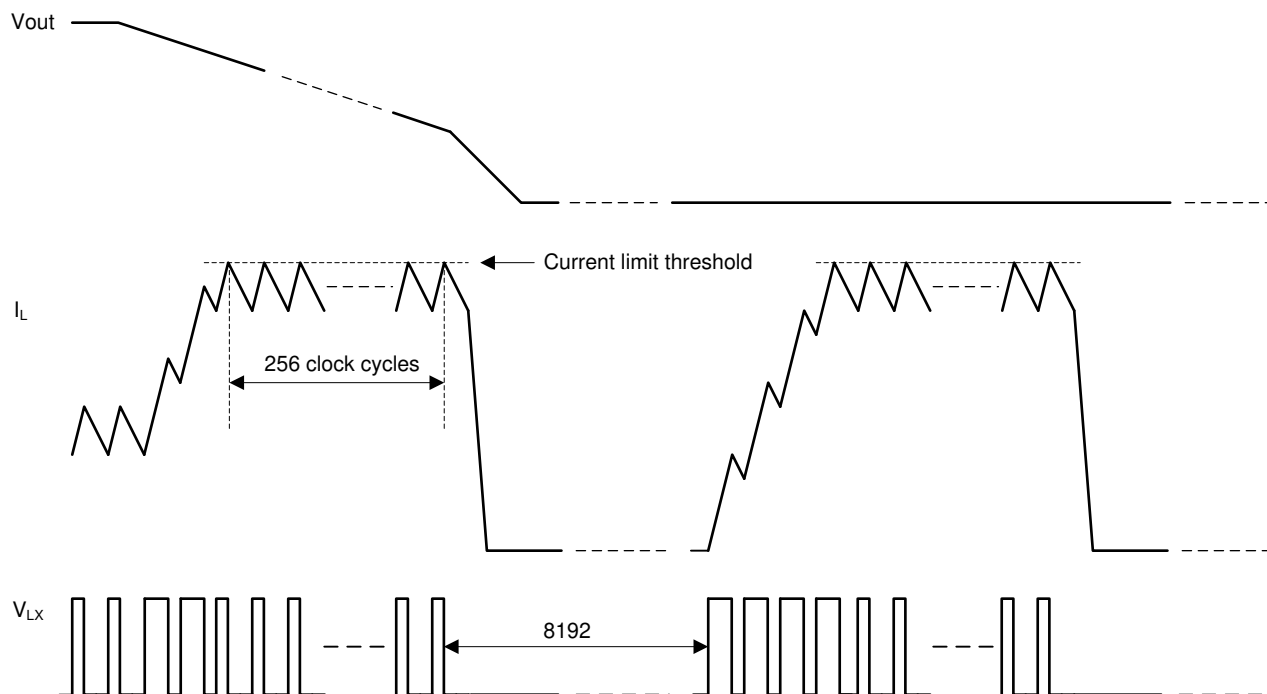
**Figure 28. DCDC Over-Current Protection**

### 7.3.2.9 Bootstrap Voltage (BST) and Low Dropout Operation

The device has an integrated bootstrap regulator and requires a small ceramic capacitor between the BST and LX terminals to provide the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is charged when the BST terminal voltage is less than VIN and BST-LX voltage is below regulation. The value of this ceramic capacitor is recommended 0.047 μF or less. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BST to LX terminal voltage is greater than the BST-LX UVLO threshold which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

### 7.3.2.10 Thermal Performance

The device implements an internal thermal overloading sensor to protect the chip with stopping buck converter switching if the junction temperature exceeds 160°C. Once the die temperature decreases below 140°C, the device automatically reinitiates the power up sequence.

### 7.3.2.11  Loop Compensation

The integrated buck DCDC converter in TPS65286 incorporates a peak current mode. The error amplifier is a trans-conductance amplifier with a gain of 1000 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. $C_b$ adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow these steps:

1. Select switching frequency, $f_{SW}$, that is appropriate for application depending on L and C sizes, output ripple, and EMI. Switching frequency between 500 kHz to 1 MHz gives the best trade off between performance and cost. To optimize efficiency, lower switching frequency is desired.

2. Set up cross over frequency, $f_c$, which is typically between 1/5 and 1/20 of $f_{SW}$.

3. $R_C$ can be determined by:

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$$

(7)

   where $g_M$ is the error amplifier gain (1000 µA/V), $gm_{ps}$ is the power stage voltage to current conversion gain (10 A/V).

4. Calculate $C_C$ by placing a compensation zero at or before the dominant pole (fp = 1 / $C_O$ x $R_L$ x 2π).

$$C_C = \frac{R_L \cdot Co}{R_C}$$

(8)

5. Optional $C_b$ can be used to cancel the zero from the ESR associated with $C_O$.

$$C_b = \frac{Resr \cdot Co}{R_C}$$

(9)

6. Type III compensation can be implemented with the addition of one capacitor, C1. This allows for slightly higher loop bandwidths and higher phase margins. If used, C1 is calculated from Equation 10.
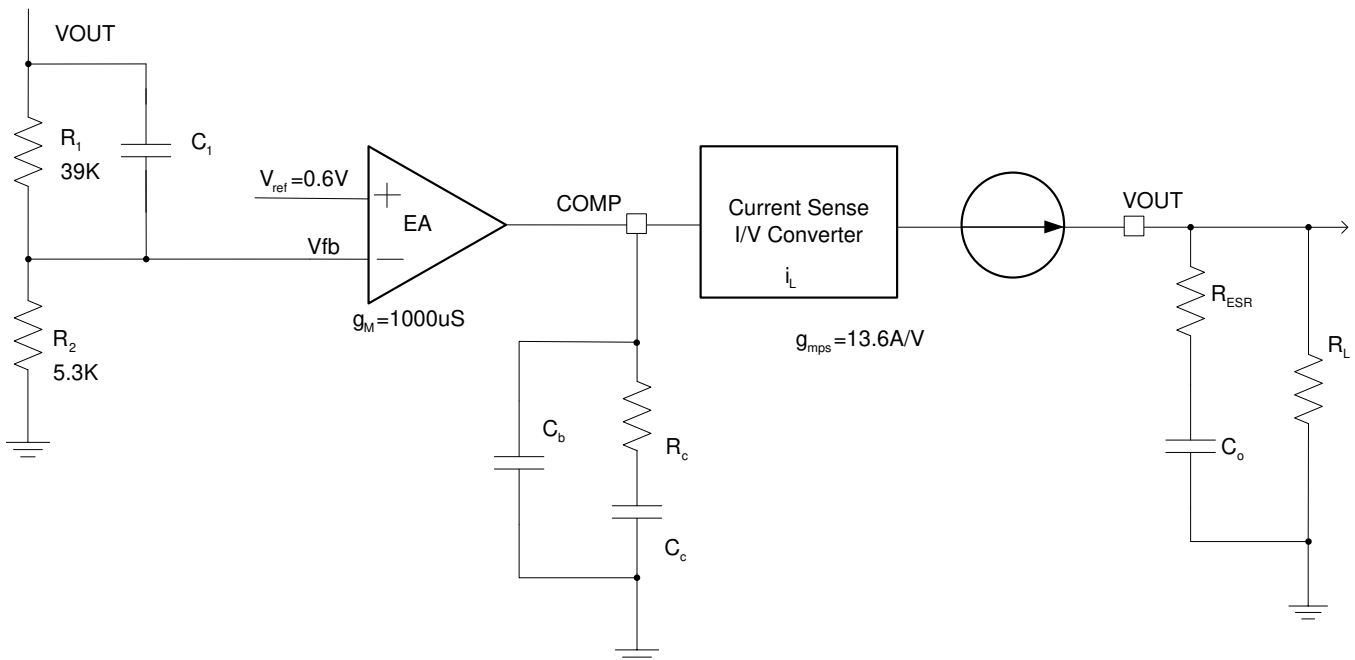
$$C_1 = \frac{1}{2\pi \cdot R_1 \cdot f_C}$$

(10)



**Figure 29.  DCDC Loop Compensation**

## 7.4 Device Functional Modes

### 7.4.1 Pulse Skipping Mode Operation

When a synchronous buck converter operates at light load condition, TPS65286 operates with pulse skipping mode (PSM) to reduce the switching loss by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. The output voltage, load and inductor current diagrams are shown in Figure 30. When the VCOMP falls lower than VGS, the COMP terminal voltage is clamped to VGS internally, typical 350 mV, the device enters pulse skipping mode and high side MOSFET stops switching, then the output falls and the VCOMP rises. When the VCOMP rises larger than VGS, the high side MOSFET starts switching, then the output rises and the VCOMP falls. When the VCOMP falls lower than VGS, the high side MOSFET stops switching again. If the peak inductor current rise above typical 600 mA (V$_{IN}$ = 24 V, V$_{OUT}$ = 5 V) and the COMP terminal voltage to rise above VGS, the converter exits pulse skipping mode. Since converter detects the peak inductor current for pulse skip mode, the average load current entering pulse skipping mode varies with the applications and external output filters.
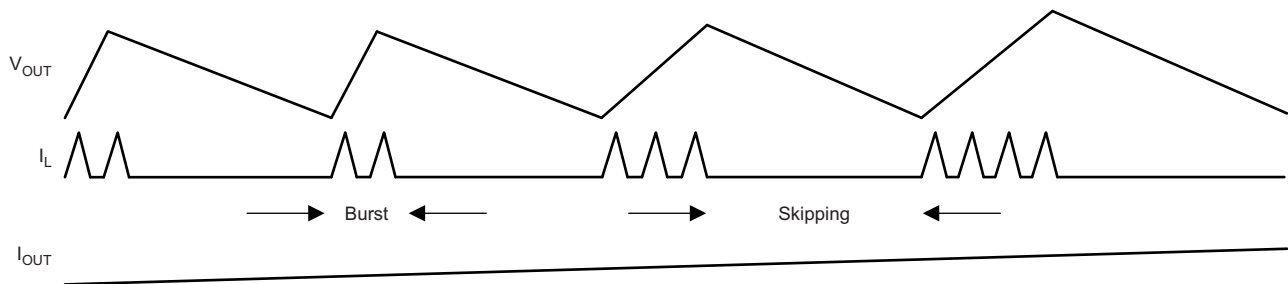


**Figure 30. Pulse Skipping Mode**

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS65286 is a step down dc/dc converter. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 6 A. The following design procedure can be used to select component values for the TPS65286.

Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

## 8.2 Typical Applications

The application schematic of Figure 31 was developed to meet the requirements above. This circuit is available as the TPS65286EVM evaluation module. The design procedure is given in this section.
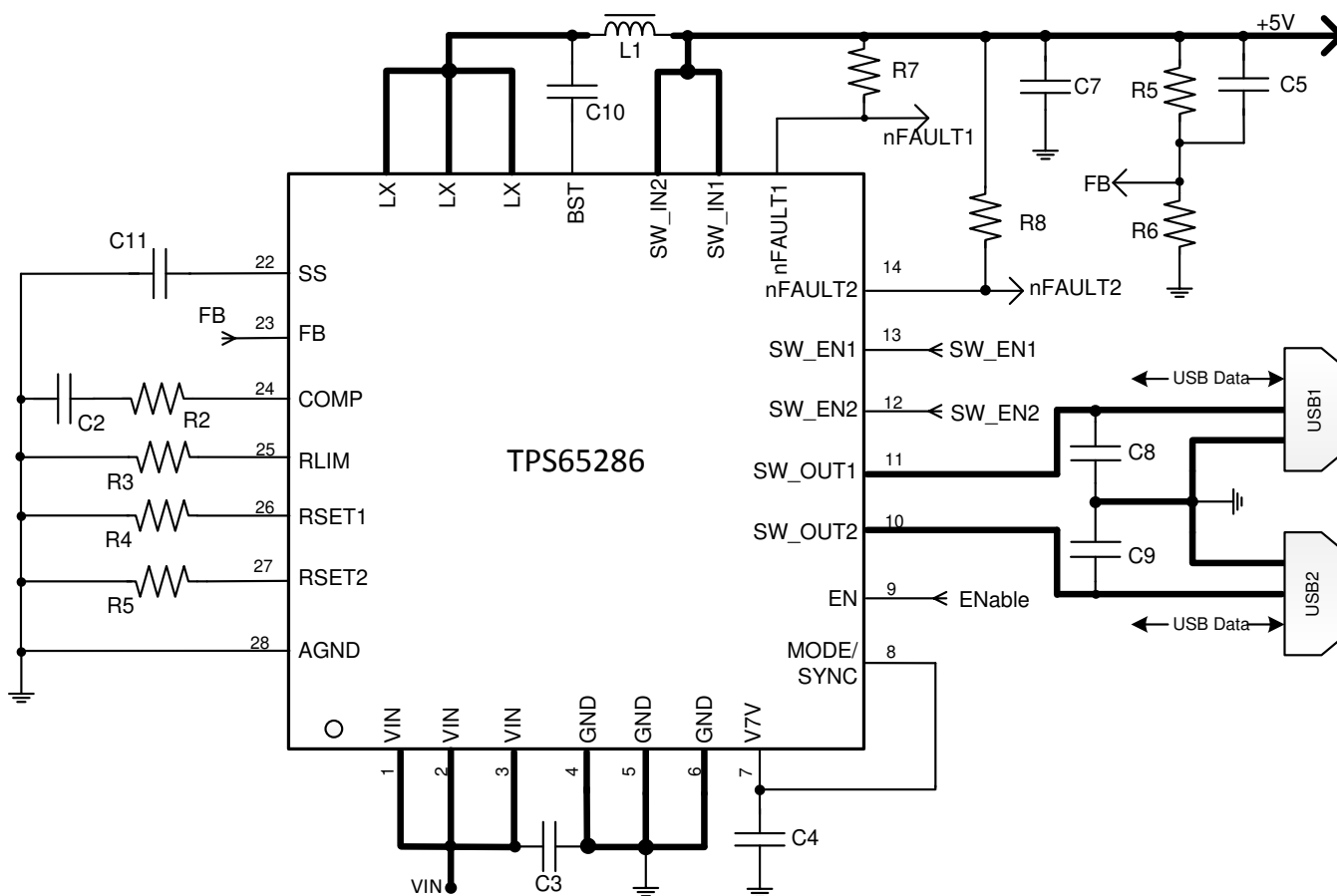


**Figure 31. Typical Application Schematic**

## Typical Applications (continued)

### 8.2.1   Design Requirements

For this design example, use the following as the input parameters.

**Table 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 4.5 V - 28 V |
| Output voltage | 5 V |
| Transient response, 1.5-A load step | $\Delta V_{OUT}$ = ±5% |
| Input ripple voltage | 400 mV |
| Output ripple voltage | 30 mV |
| Output current rating | 6 A |
| Operating frequency | 500 kHz |

### 8.2.2   Detailed Design Procedure

#### 8.2.2.1   Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:
- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

#### 8.2.2.2   Related Parts

| PART NO. | DESCRIPTION | COMMENTS |
|---|---|---|
| TPS65280 | One buck converter and two USB switches | $0.3 \leq f_{SW} \leq 1.4$ MHz, $4.5$ V $\leq V_{IN} \leq 18$ V, $V_{OUT}$ fixed 5 V, maximum DC current 4 A, $2.5$ V $\leq V_{SW\_IN} \leq 6$ V, USB current limit fixed 1.2 A, with manufacture trim option. |
| TPS65281, TPS65281-1 | One buck converter and one USB switch | $0.3 \leq f_{SW} \leq 1.4$ MHz, $4.5$ V $\leq V_{IN} \leq 18$ V, $V_{OUT}$ adjustable, maximum DC current 4 A, $2.5$ V $\leq V_{SW\_IN} \leq 6$ V, USB current limit adjustable form 75 mA to 2.7 A. |
| TPS65282 | One buck converter and two USB switches | $0.3 \leq f_{SW} \leq 1.4$ MHz, $4.5$ V $\leq V_{IN} \leq 18$ V, $V_{OUT}$ adjustable, maximum DC current 4 A, $2.5$ V $\leq V_{SW\_IN} \leq 6$ V, USB current limit adjustable form 75 mA to 2.7 A. |
| TPS65287 | Three buck converters and one USB switch | $0.3 \leq f_{SW} \leq 2.2$ MHz, $4.5$ V $\leq V_{IN} \leq 18$ V, $V_{OUT}$ adjustable, maximum DC current 3/2/2 A, $2.5$ V $\leq V_{SW\_IN} \leq 6$ V, USB current limit adjustable form 75 mA to 2.7 A. |
| TPS65288 | Three buck converters and two USB switches | $0.3 \leq f_{SW} \leq 2.2$ MHz, $4.5$ V $\leq V_{IN} \leq 18$ V, $V_{OUT}$ adjustable, maximum DC current 3/2/2 A, $2.5$ V $\leq V_{SW\_IN} \leq 6$ V, USB current limit fixed 1.2 A, with manufacture trim option. |

#### 8.2.2.3   Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current $i_L$ decreases with higher inductance or higher frequency and increases with higher input voltage $V_{IN}$. Accepting larger values of $i_L$ allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

To calculate the value of the output inductor, use Equation 11. LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. LIR is suggested to choose to 0.1 ~ 0.3 for most applications.

Actual core loss of inductor is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from Equation 13 and Equation 14.

$$L = \frac{V_{in} - V_{out}}{I_O \cdot LIR} \cdot \frac{V_{out}}{V_{in} \cdot fsw}$$
(11)

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{out}}{V_{in} \cdot fsw}$$
(12)

$$i_{Lrms} = \sqrt{I_O^2 + \frac{(\frac{V_{out} \cdot (V_{inmax} - V_{out})}{V_{inmax} \cdot L \cdot fsw})^2}{12}}$$
(13)

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2}$$
(14)

For this design example, use LIR = 0.3 and the inductor is calculated to be 4.40 µH with $V_{IN}$ = 24 V. Choose 4.7 µH value of the standard inductor, the peak to peak inductor ripple is about 28.1% of 6-A DC load current.

### 8.2.2.4  *Output Capacitor Selection*

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. Equation 15 gives the minimum output capacitance to meet the transient specification. For this example, Lo = 4.7 µH, $\Delta I_{OUT}$ = 3 A − 0 A = 3 A and $\Delta V_{OUT}$ = 250 mV (5% of regulated 5 V). Using these numbers gives a minimum capacitance of 34 µF. A standard 4 x 22 µF ceramic is chose in the design.

$$Co > \frac{\Delta I_{OUT}^2 \cdot L}{V_{out} \cdot \Delta V_{out}}$$
(15)

The selection of $C_{OUT}$ is driven by the effective series resistance (ESR). Equation 16 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where $f_{SW}$ is the switching frequency, $\Delta V_{OUT}$ is the maximum allowable output voltage ripple, and $\Delta i_L$ is the inductor ripple current. In this case, the maximum output voltage ripple is 40 mV (1% of regulated 5 V). From Equation 16, the output current ripple is 1.7 A and the minimum output capacitance meeting the output voltage ripple requirement is 12.2 µF with 3-mΩ ESR resistance.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{\Delta V_{out}}{\Delta i_L} - esr}$$
(16)

After considering both requirements, for this example, four 22-µF 6.3-V X7R ceramic capacitors with 3-mΩ of ESR will be used. Equation 17 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 17 indicates the ESR should be less than 23.5 mΩ. In this case, the ceramic capacitors' ESR is much smaller than 23.5 mΩ.

$$\frac{Voripple}{Iripple} \le Re\,sr$$
(17)

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, a 47-µF 6.3-V X5R ceramic capacitor with 3-mΩ of ESR is be used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 18 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 18 yields 486 mA.

$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot f_{SW}}$$

(18)

### 8.2.2.5 Input Capacitor Selection

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input terminals of the converters as they handle the RMS ripple current shown in Equation 19. For this example, $I_{out}$ = 6 A, $V_{out}$ = 5 V, minimum $V_{in\_min}$ = 24 V. The input capacitors must support a ripple current of 2.4-A RMS.

$$I_{inrms} = I_{out} \cdot \sqrt{\frac{V_{out}}{V_{inmin}} \cdot \frac{(V_{inmin} - V_{out})}{V_{inmin}}}$$

(19)

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 20. Using the design example values, $I_{out\_max}$ = 6 A, $C_{in}$ = 22 µF, $f_{sw}$ = 500 kHz, yields an input voltage ripple of 136 mV.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{sw}}$$

(20)

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

### 8.2.2.6 Soft-Start Capacitor Selection

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS65286 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using Equation 21. The soft-start circuit requires 1 nF per around 0.109 ms to be connected at the SS terminal. For the example circuit, the output capacitor value is 47 nF and the soft-start time is 5.1 ms. In TPS65286, Iss is 5.5 µA and Vref is 0.6 V.

$$Tss = Css \cdot \left( \frac{0.6V}{5.5\mu A} \right)$$

(21)

### 8.2.2.7 Minimum Output Voltage

Due to the internal design of the TPS65286, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 22.

$$Voutmin = Ontime_{min} \cdot Fsmax(Vinmax + Ioutmin(RDS2min - RDS1min)) - Ioutmin(RL + RDS2min)$$

(22)

where:

    Voutmin = minimum achievable output voltage

    Ontime$_{min}$ = minimum controllable on-time (120 ns maximum)

    Fsmax = maximum switching frequency including tolerance

    Vinmax = maximum input voltage

    Ioutmin = minimum load current

    RDS1min = minimum high side MOSFET on resistance (52 mΩ typical)

    RDS2min = minimum low side MOSFET on resistance (27 mΩ typical)

    RL = series resistance of output inductor

    For the example circuit, Vin = 24V, Fs = 500 kHz, when Iout = 0 A, the minimum output voltage is 1.44 V

### 8.2.2.8  Compensation Component Selection

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. The method presented here ignores the effects of the slope compensation that is internal to the TPS65286. Since the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use SwitcherPro software for a more accurate design.

First, the modulator pole, fpmod, and the esr zero, fzmod must be calculated using Equation 23 and Equation 24. For Cout, use a derated value of 22.4 µF. Use Equation 25 and Equation 26 to estimate a starting point for the closed loop crossover frequency fco. Then the required compensation components may be derived. For this design example, fpmod is 12.9 kHz and fzmod is 2730 kHz. Equation 23 is the geometric mean of the modulator pole and the ESR zero and Equation 24 is the geometric mean of the modulator pole and one half the switching frequency. Use a frequency near the lower of these two values as the intended crossover frequency fco. In this case, Equation 23 yields 175 kHz and Equation 24 yields 55.7 kHz. The lower value is 55.7 kHz. A slightly higher frequency of 60.5 kHz is chosen as the intended crossover frequency.

$$fpmod = \frac{Iout}{2 \cdot \pi \cdot Vout \cdot Cout} \tag{23}$$

$$fzmod = \frac{Iout}{2 \cdot \pi \cdot RESR \cdot Cout} \tag{24}$$

$$fco = \sqrt{fpmod \cdot fzmod} \tag{25}$$

$$fco = \sqrt{fpmod \cdot \frac{fSW}{2}} \tag{26}$$

Now the compensation components can be calculated. First calculate the value for Rc which sets the gain of the compensated network at the crossover frequency. Use Equation 27 to determine the value of $R_C$.

$$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}} \tag{27}$$

Next calculate the value of $C_C$. Together with $R_C$, $C_C$ places a compensation zero at the modulator pole frequency. Equation 28 to determine the value of C3.

$$C_C = \frac{R_L \cdot Co}{R_C} \tag{28}$$

An additional high frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R4 and C4. The pole frequency can be placed at the ESR zero frequency of the output capacitor as given by Equation 24. Use Equation 29 to calculate the required capacitor value for $C_b$.

$$C_b = \frac{Resr \cdot Co}{R_C} \tag{29}$$

### 8.2.2.9  Auto-Retry Functionality of USB Switches

Some applications require that an over-current condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with external resistors and capacitor shown in Figure 32. During a fault condition, nFAULT pulls low disabling the part. The part is disabled when EN is pulled low, and nFAULT goes high impedance allowing CRETRY1/2 to be charged. The part re-enables when the voltage on EN_SW reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.
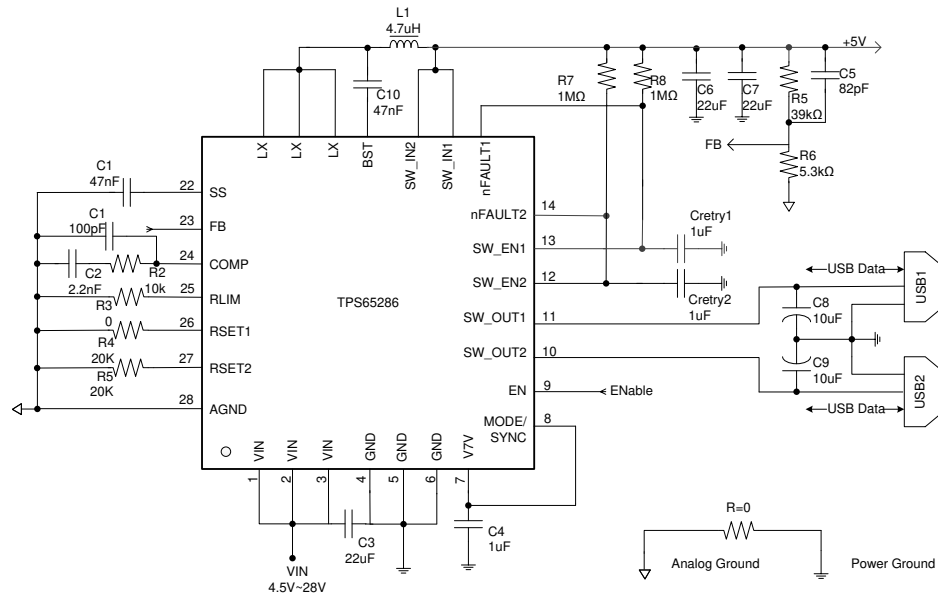
**Figure 32.  Auto Retry Functionality**

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 33 shows how an external logic signal can drive EN_SW through RFAULT and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.
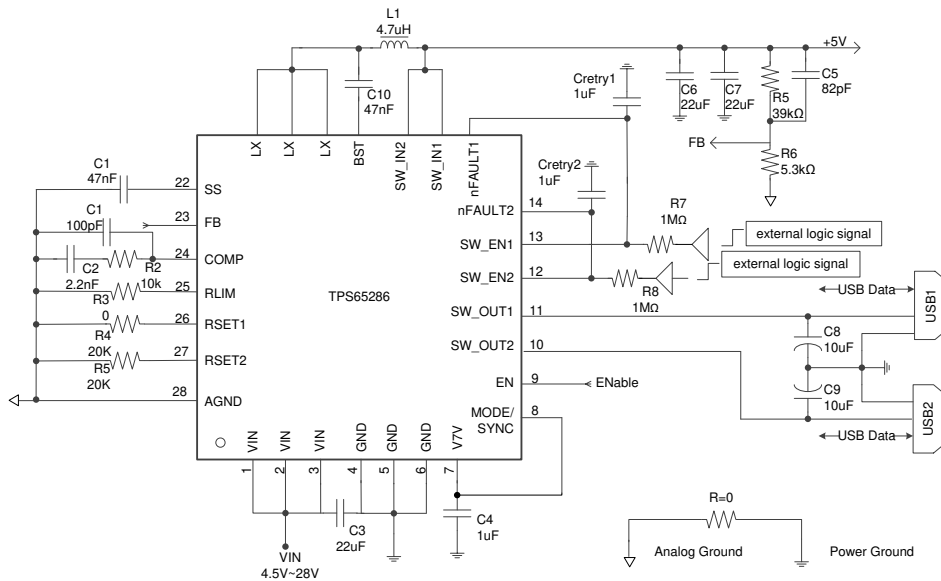


**Figure 33.  Auto Retry Functionality With External Enable Signal**

## 8.2.3 Application Performance Plots

$T_A$ = 25°C, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz, $R_{nFAULT}$ = 100 kΩ (unless otherwise noted)



**Figure 34. Buck Start Up by EN Terminal With an External 47-nF SS Capacitor**
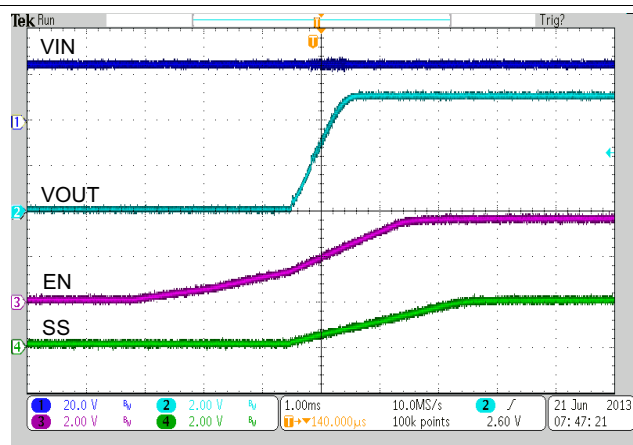


**Figure 35. Buck Start Up by EN Terminal With Internal Soft-Start (SS terminal Open)**
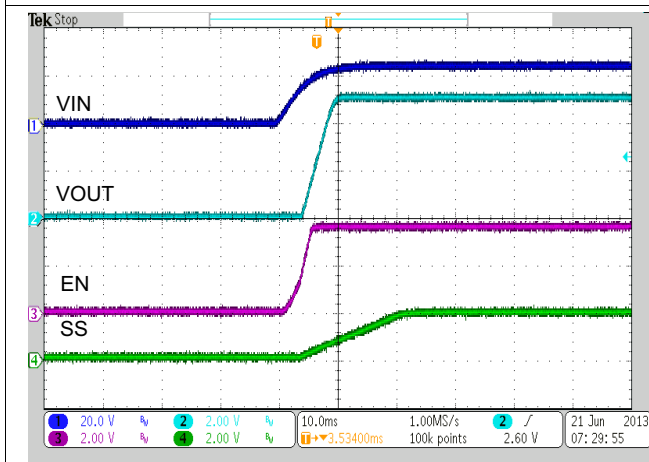


**Figure 36. Ramp $V_{IN}$ to Start Up Buck With an External 22-nF SS Capacitor**
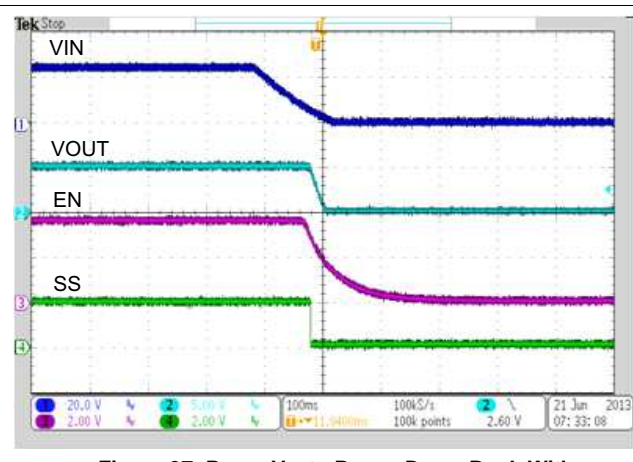


**Figure 37. Ramp $V_{IN}$ to Power Down Buck With an External 22-nF SS Capacitor**
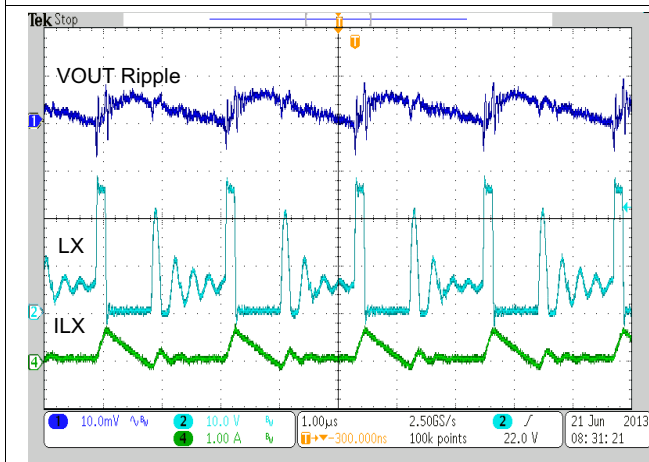


**Figure 38. Buck Output Voltage Ripple, $I_{OUT}$ = 0.1-A PSM Mode**
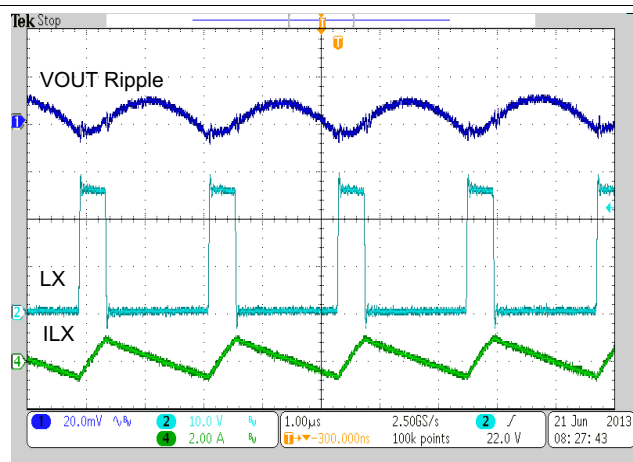


**Figure 39. Buck Output Voltage Ripple, $I_{OUT}$ = 0-A PWM Mode**

$T_A = 25°C$, $V_{IN} = 24$ V, $V_{OUT} = 5$ V, $f_{SW} = 500$ kHz, $R_{nFAULT} = 100$ kΩ (unless otherwise noted)



**Figure 40. Buck Output Voltage Ripple, $I_{OUT}$ = 4 A**
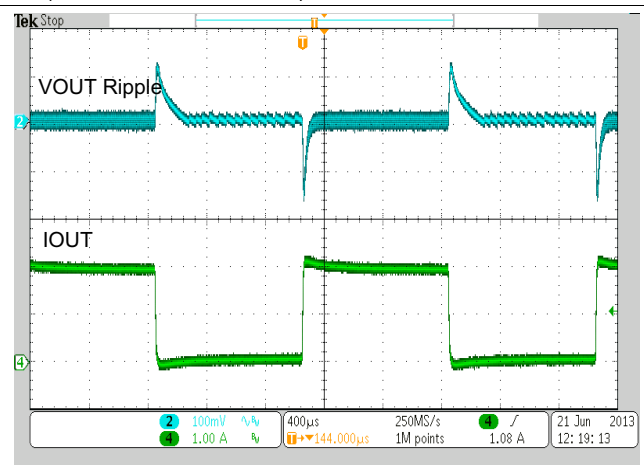


**Figure 41. Buck Output Load Transient in PSM Mode, $I_{OUT}$ = 0 - 2 A**
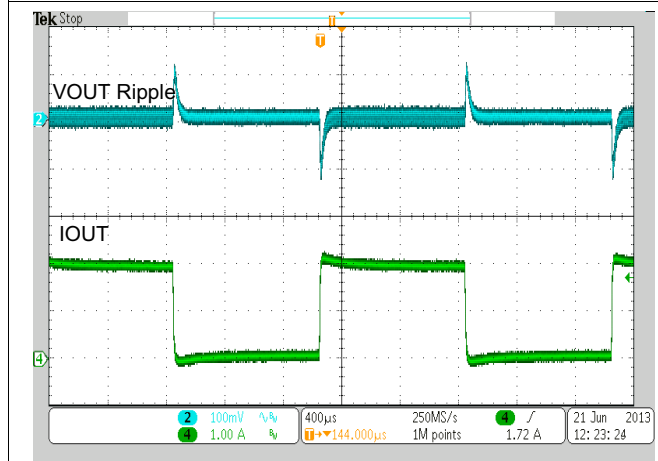


**Figure 42. Buck Output Load Transient in PWM Mode, $I_{OUT}$ = 0 - 2 A**
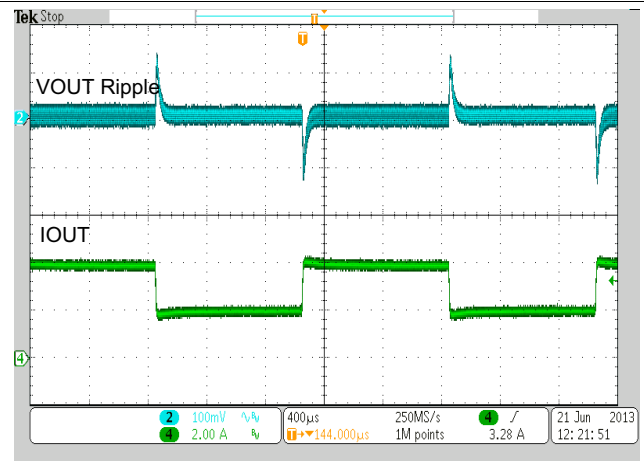


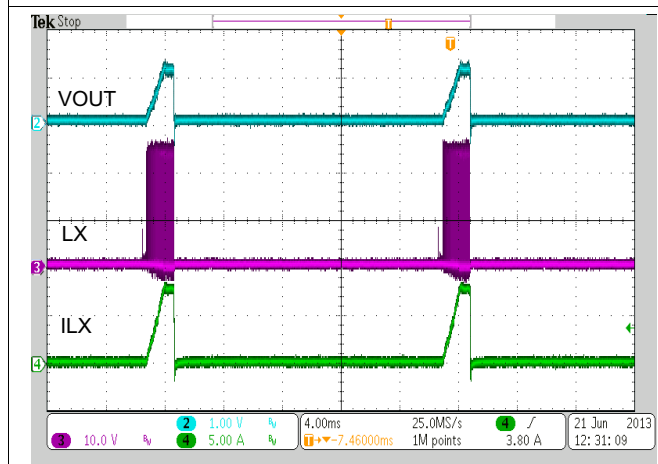**Figure 43. Buck Output Load Transient in PWM Mode, $I_{OUT}$ = 2 - 4 A**
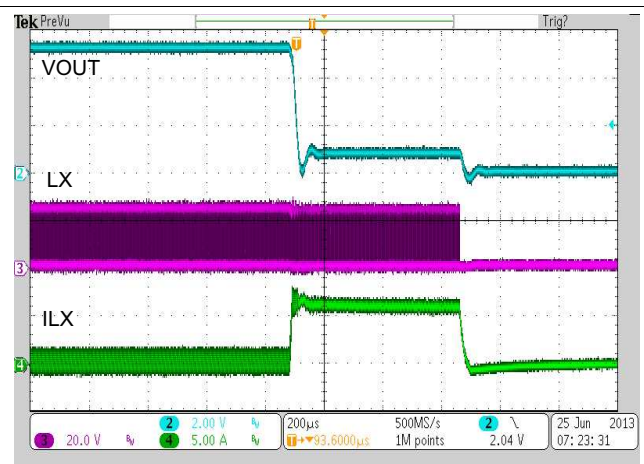


**Figure 44. Buck Hiccup Response to Hard Short Circuit**



**Figure 45. Buck Output Hard Short Response (Zoom In)**

$T_A$ = 25°C, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V, $f_{SW}$ = 500 kHz, $R_{nFAULT}$ = 100 kΩ (unless otherwise noted)



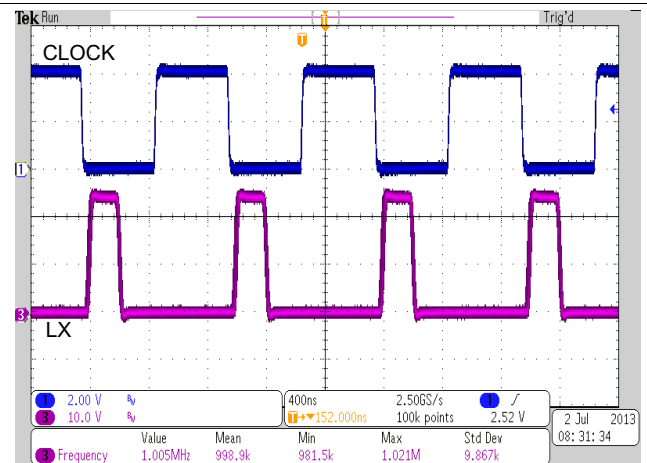**Figure 46. Clock Synchronization Operation**



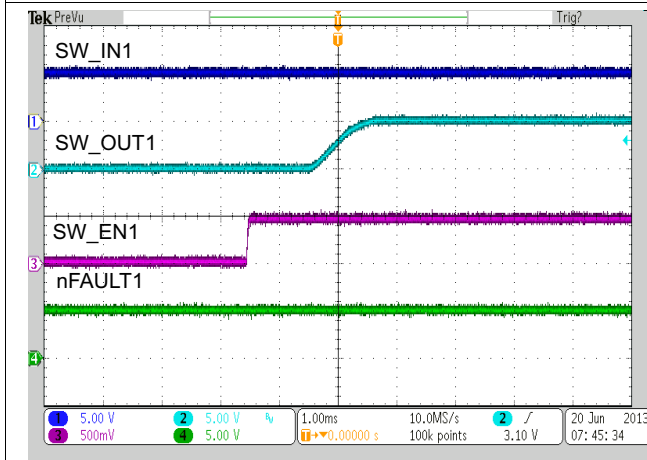**Figure 47. Clock Synchronization at 1 MHz**



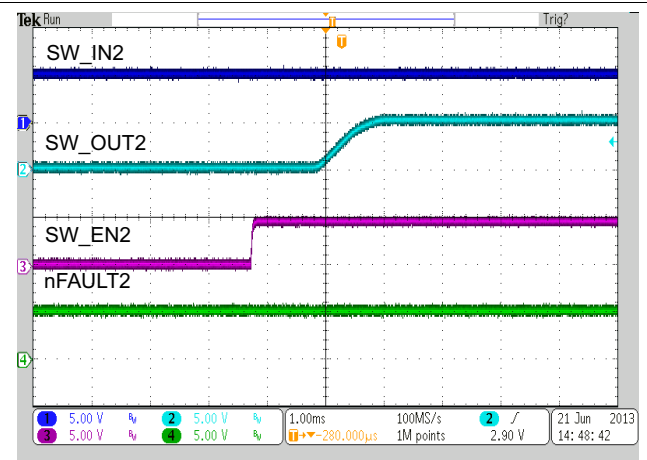**Figure 48. Power Switch1 Turn on Delay and Rise Time**



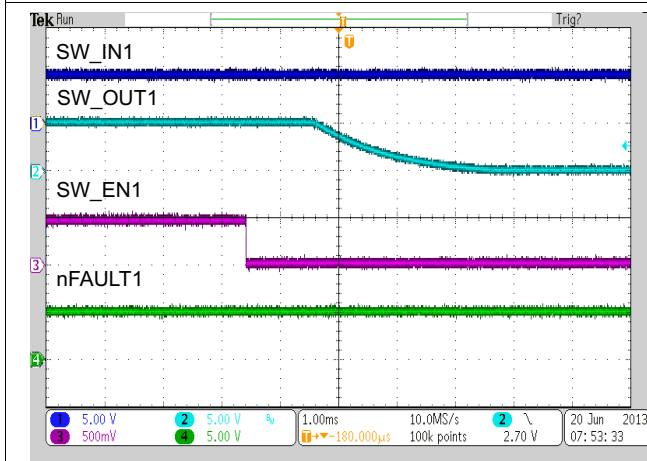**Figure 49. Power Switch2 Turn on Delay and Rise Time**



**Figure 50. Power Switch1 Turn off Delay and Fall Time, $R_{OUT}$ = 50 Ω, $C_{OUT}$ = 10 µF**



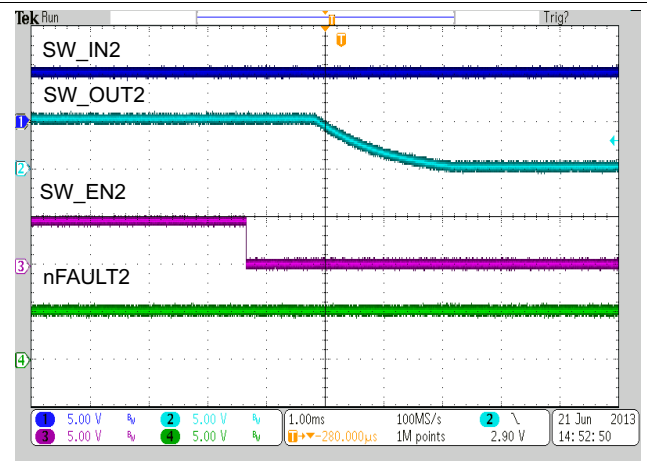**Figure 51. Power Switch2 Turn off Delay and Fall Time, $R_{OUT}$ = 50 Ω, $C_{OUT}$ = 10 µF**

$T_A = 25°C, V_{IN} = 24\ V, V_{OUT} = 5\ V, f_{SW} = 500\ kHz, R_{nFAULT} = 100\ k\Omega$ (unless otherwise noted)
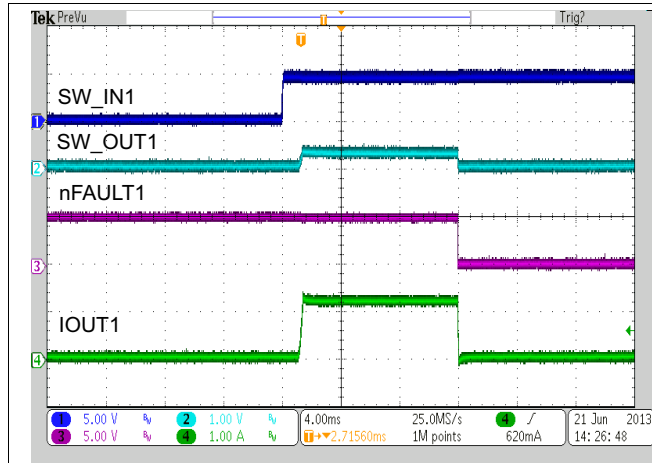


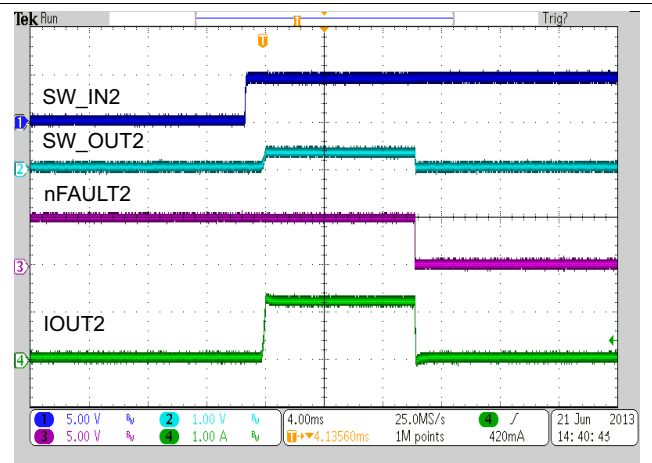**Figure 52. Power Switch1 Enable into Short Circuit**



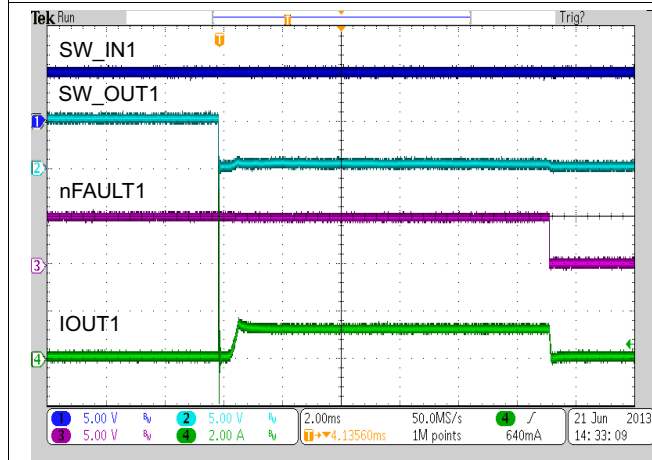**Figure 53. Power Switch2 Enable into Short Circuit**



**Figure 54. Power Switch1 Current Limit Operation**
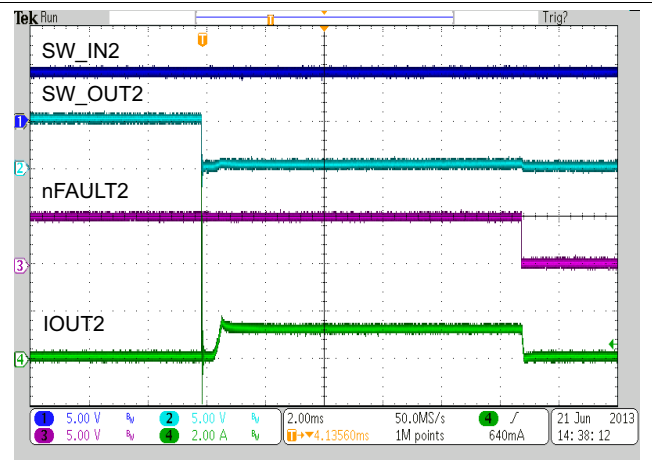


**Figure 55. Power Switch2 Current Limit Operation**
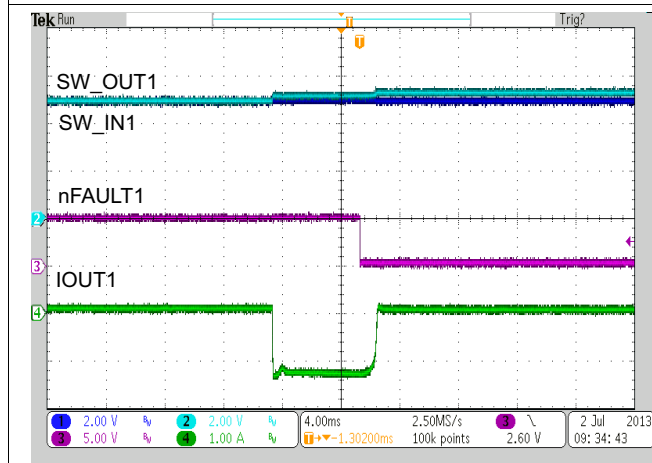


**Figure 56. Power Switch1 Reverse Voltage Protection Response**
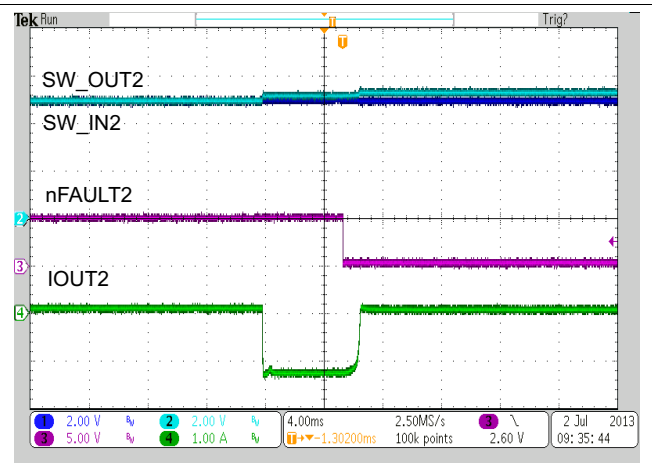


**Figure 57. Power Switch2 Reverse Voltage Protection Response**

# 9 Power Supply Recommendations

The total power dissipation inside TPS65286 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package ($\theta_{JA}$) and ambient temperature. The analysis below gives an approximation in calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

To calculate the temperature inside the device under continuous load, use the following procedure.
1. Define the total continuous current through buck converter (including the load current through power switches). Make sure the continuous current does not exceed maximum load current requirement.
2. From the graphs below, determine the expected losses (Y axis) in watts for buck converter inside the device. The loss $P_{D\_BUCK}$ depends on the input supply and the selected switching frequency.
3. Determine the load current $I_{OUT1}$ and $I_{OUT2}$ through the power switches. Read $R_{DS(on)1/2}$ of power switch from the typical characteristics graph.
4. The power loss through power switches can be calculated by $P_{D\_PW} = R_{DS1(on)} \times I_{OUT1} + R_{DS2(on)} \times I_{OUT2}$.
5. The Dissipating Rating Table provides the thermal resistance $\theta_{JA}$ for specific packages and board layouts.
6. To calculate the maximum temperature inside the IC, use the following formula.

$$T_J = (P_{D\_BUCK} + P_{D\_PW}) \times \theta_{JA} + T_A \tag{30}$$

where:

$T_A$ = Ambient temperature (°C)

$\theta_{JA}$ = Thermal resistance (°C/W)

$P_{D\_BUCK}$ = Total power dissipation in buck converter (W)

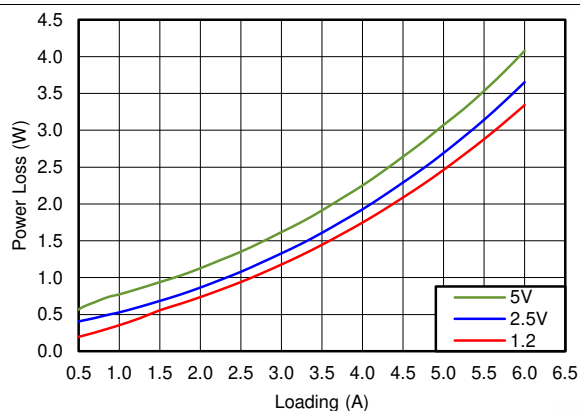$P_{D\_PW}$ = Total power dissipation in power switches (W)



**Figure 58. Power Dissipation of TPS65286, $V_{IN}$ = 24 V**
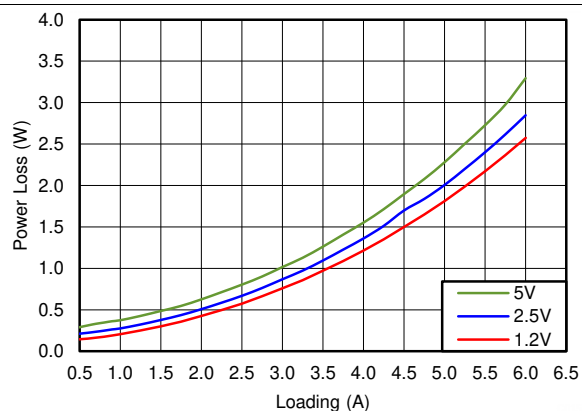


**Figure 59. Power Dissipation of TPS65286, $V_{IN}$ = 12 V**

**Figure 60. Thermal Signature of TPS65286EVM,**
$T_A$ = Room Temperature, $V_{IN}$ = 24 V,
$V_{OUT}$ to $V_{SW\_in}$ = 5 V/0 A, $I_{SW\_OUT1/2}$ = 1.2 A
**EVM Board: 4-Layer PCB, 1.6 mm Thickness, 2 oz. Copper Thickness, 65-mm x 65-mm Size, 25 Vias at Thermal Pad**



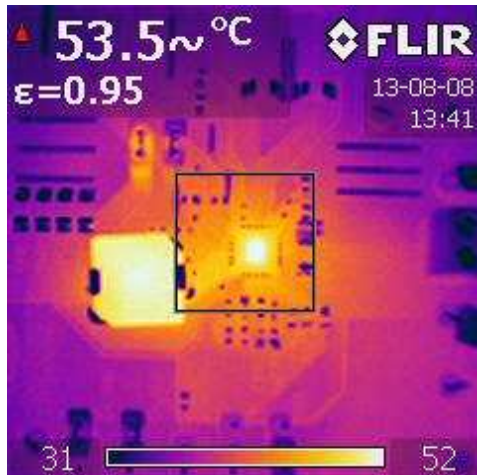**Figure 61. Thermal Signature of TPS65286EVM,**
$T_A$ = Room Temperature, $V_{IN}$ = 24 V, $V_{OUT}$ = 5 V/5 A,
$I_{SW\_OUT1/2}$ = 0 A
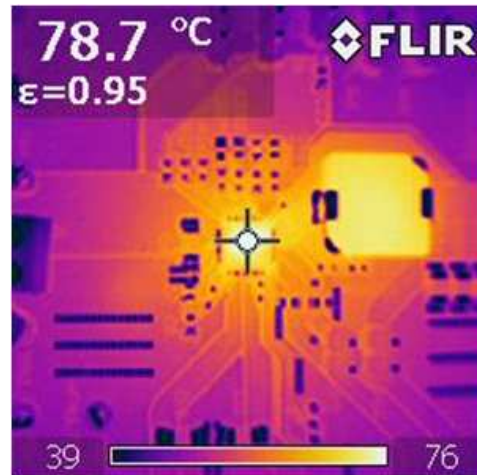**EVM Board: 4-Layer PCB, 1.6 mm Thickness, 2 oz. Copper Thickness, 65-mm x 65-mm Size, 25 Vias at Thermal Pad**

# 10 Layout

## 10.1 Layout Guidelines

When laying out the printed circuit board, the following guideline should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 62.

- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN terminal should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. This capacitor provides the AC current into the internal power MOSFETs. Connect the (+) terminal of the input capacitor as close as possible to the VIN terminal, and Connect the (-) terminal of the input capacitor as close as possible to the PGND terminal. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN terminals, and the power ground PGND connections.

- Since the LX connection is the switching node, the output inductor should be located close to the LX terminal, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. Keep the switching node, LX, away from all sensitive small-signal nodes.

- Connect V7V decoupling capacitor connected close to the IC, between the V7V and the power ground PGND terminal. This capacitor carries the MOSFET drivers' current peaks.

- Place the output filter capacitor of buck converter close to SW_IN terminals. Try to minimize the ground conductor length while maintaining adequate width.

- AGND terminal should be separately routed to the (-) terminal of V7V bypass capacitor to avoid switching grounding path. A ground plane is recommended connecting to this ground path.

- The compensation should be as close as possible to the COMP terminals. The COMP and ROSC terminals are sensitive to noise so the components associated to these terminals should be located as close as possible to the IC and routed with minimal lengths of trace. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to PGND, AGND, VIN or any other DC rail in your system.

- There is no electric signal internal connected to thermal pad in the device. Nevertheless connect exposed pad beneath the IC to ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation.
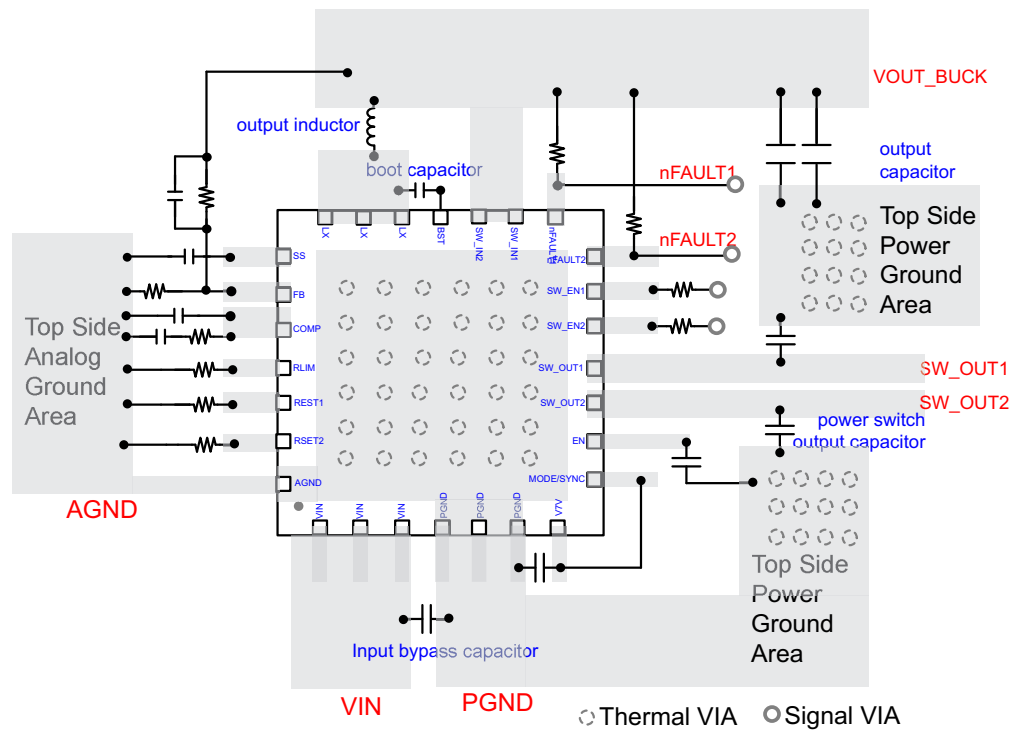
## 10.2 Layout Example



**Figure 62. 4-Layers PCB Layout Recommendation Diagram**

# 11 デバイスおよびドキュメントのサポート

## 11.1 デバイス・サポート

### 11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

## 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 商標

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 11.6 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

# 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS65286RHDR | Active | Production | VQFN (RHD) \| 28 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | TPS 65286 |
| TPS65286RHDT | Active | Production | VQFN (RHD) \| 28 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | TPS 65286 |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



Cavity

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65286RHDR | VQFN | RHD | 28 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65286RHDT | VQFN | RHD | 28 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65286RHDR | VQFN | RHD | 28 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS65286RHDT | VQFN | RHD | 28 | 250 | 210.0 | 185.0 | 35.0 |

Images above are just a representation of the package family, actual package may vary.
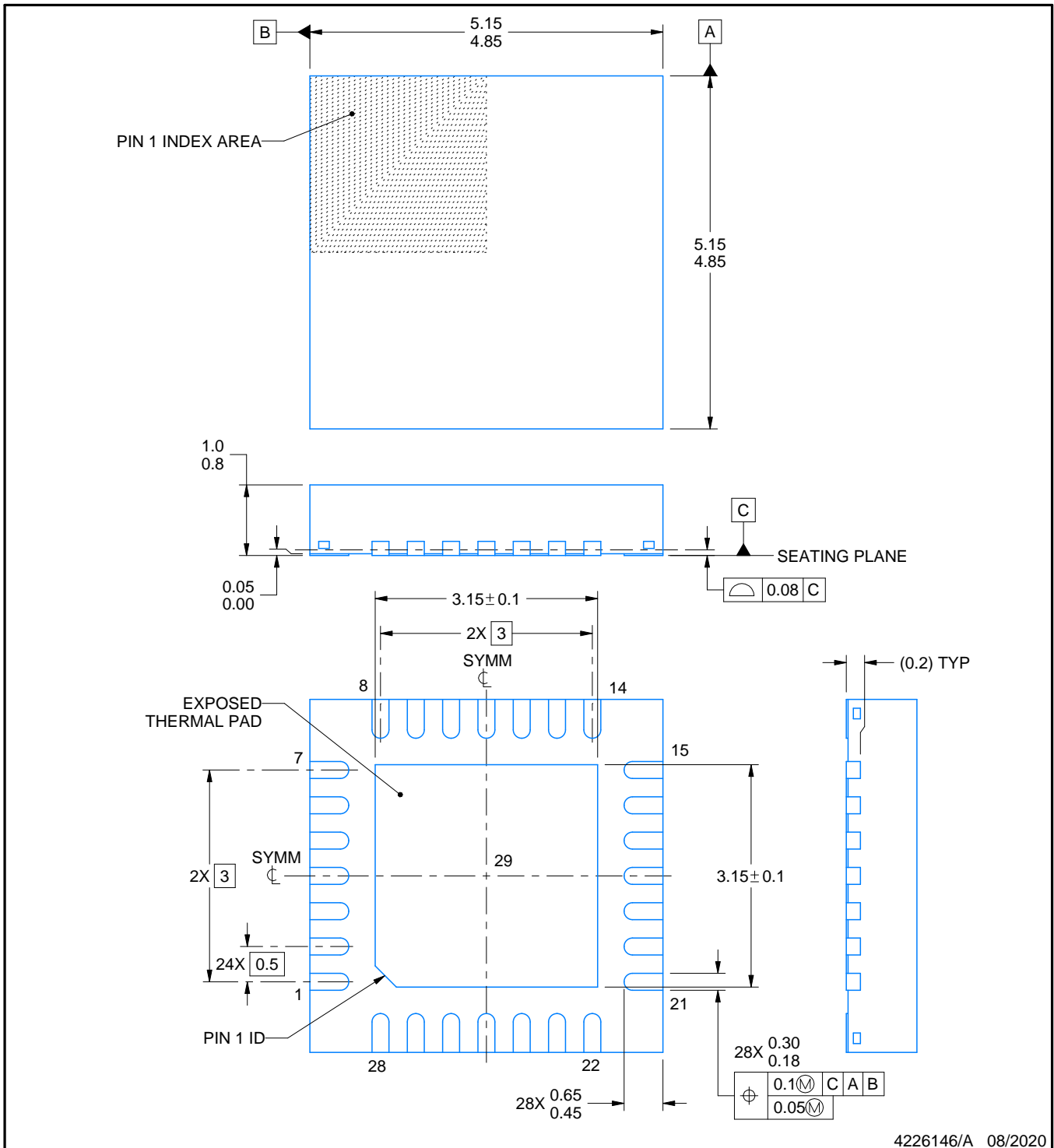Refer to the product data sheet for package details.

4204400/G

**RHD0028B**

B | 5.15 / 4.85 | A

PIN 1 INDEX AREA

5.15 / 4.85

1.0 / 0.8

C

SEATING PLANE

0.08 C

0.05 / 0.00

3.15 ± 0.1

2X 3

SYMM

8    14

EXPOSED THERMAL PAD

7    15

SYMM

2X 3

29    3.15 ± 0.1

24X 0.5

1    21

PIN 1 ID

28    22

28X 0.65 / 0.45

(0.2) TYP

28X 0.30 / 0.18

0.1 (M) C A B
0.05 (M)

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

## RHD0028B

(□ 3.15)

SYMM
¢

28

22

SEE SOLDER MASK
DETAIL

28X (0.75)

28X (0.24)

1

24X (0.5)

29

21

SYMM
¢

(4.65)

(1.325)

(R0.05) TYP

7

15

(Ø 0.2) TYP
VIA

8

14

(1.325)

(4.65)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

0.07 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## RHD0028B

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

(0.785) TYP

28X (0.75)

28X (0.24)

24X (0.5)

SYMM ℄

(R0.05) TYP

29

(0.785) TYP

(4.65)

4X (1.37)

4X (1.37)

SYMM
℄

(4.65)
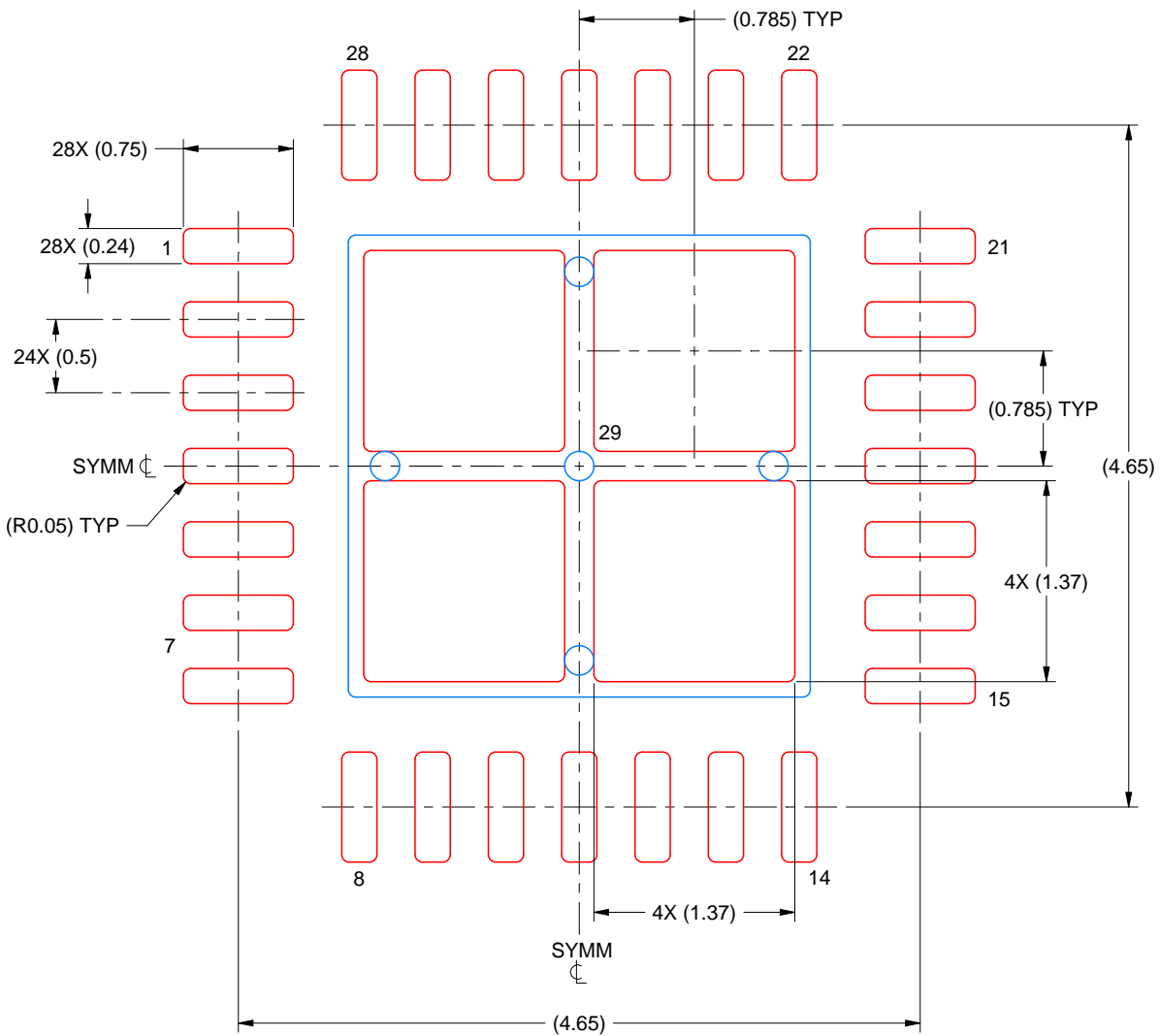
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.