

# MSP430AFE222 Device Erratasheet

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## 1 Functional Errata Revision History

Errata impacting device's operation, function or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
<a href="#">BCL12</a>	✓
<a href="#">FLASH24</a>	✓
<a href="#">FLASH27</a>	✓
<a href="#">FLASH36</a>	✓
<a href="#">TA12</a>	✓
<a href="#">TA16</a>	✓
<a href="#">TA18</a>	✓
<a href="#">TA21</a>	✓
<a href="#">TAB22</a>	✓
<a href="#">US15</a>	✓

## 2 Preprogrammed Software Errata Revision History

Errata impacting pre-programmed software into the silicon by Texas Instruments.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Software in ROM errata.

## 3 Debug only Errata Revision History

Errata only impacting debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
<a href="#">EEM20</a>	✓

## 4 Fixed by Compiler Errata Revision History

Errata completely resolved by compiler workaround. Refer to specific erratum for IDE and compiler versions with workaround.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
<a href="#">CPU4</a>	✓

Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

**TI MSP430 Compiler Tools (Code Composer Studio IDE)**

- [MSP430 Optimizing C/C++ Compiler](#): Check the --silicon\_errata option
- [MSP430 Assembly Language Tools](#)

**MSP430 GNU Compiler (MSP430-GCC)**

- [MSP430 GCC Options](#): Check -msilicon-errata= and -msilicon-errata-warn= options
- [MSP430 GCC User's Guide](#)

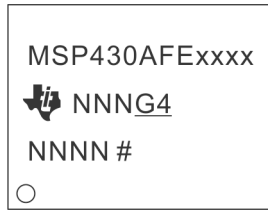
**IAR Embedded Workbench**

- [IAR workarounds for msp430 hardware issues](#)

## 5 Package Markings

**PW24**

**TSSOP (PW), 24 Pin**



# = Die revision  
○ = Pin 1 location  
N = Lot trace code

## 6 Detailed Bug Description

### BCL12 *BCS Module*

**Category** Functional

**Function** Switching RSELx or modifying DCOCTL can cause DCO dead time or a complete DCO stop

**Description** After switching RSELx bits (located in register BCCTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 us. In some instances, the DCO may completely stop, requiring a power cycle.

Furthermore, if all of the RSELx bits in the BCCTL1 register are set, modifying the DCOCTL register to change the DCOx or the MODx bits could also result in DCO dead time or DCO hang up.

**Workaround** - When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

Current RSEL	Target RSEL	Recommended Transition Sequence
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

AND

- When switching RSEL from <12 to >13 it's recommended to set RSEL to its default value first (RSEL = 7) before switching to the desired target frequency.

AND

- In case RSEL is at 15 (highest setting) it's recommended to set RSEL to its default value first (RSEL = 7) before accessing DCOCTL to modify the DCOx and MODx bits. After the DCOCTL register modification the RSEL bits can be manipulated in an additional step.

In the majority of cases switching directly to intermediate RSEL steps as described above will prevent the occurrence of BCL12. However, a more reliable method can be implemented by changing the RSEL bits step by step in order to guarantee safe function without any dead time of the DCO.

Note that the 3-step clock startup sequence consisting of clearing DCOCTL, loading the BCCTL1 target value, and finally loading the DCOCTL target value as suggested in the in the "TLV Structure" chapter of the [MSP430x2xx Family User's Guide](#) is not affected by BCL12 if (and only if) it is executed after a device reset (PUC) prior to any other modifications being made to BCCTL1 since in this case RSEL still is at its default value of 7. However any further changes to the DCOx and MODx bits will require the consideration of the workaround outlined above.

### CPU4 *CPU Module*

**Category** Compiler-Fixed

**Function** PUSH #4, PUSH #8CPU4 - Bug

**Description** The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8.

The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

**Workaround**

Refer to the table below for compiler-specific fix implementation information.

IDE/Compiler	Version Number	Notes
IAR Embedded Workbench	IAR EW430 v2.x until v6.20	User is required to add the compiler flag option below. --hw_workaround=CPU4
IAR Embedded Workbench	IAR EW430 v6.20 or later	Workaround is automatically enabled
TI MSP430 Compiler Tools (Code Composer Studio)	v1.1 or later	
MSP430 GNU Compiler (MSP430-GCC)	MSP430-GCC 4.9 build 167 or later	

**EEM20**
***EEM Module***


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**Category**

Debug

**Function**

Debugger might clear interrupt flags

**Description**

During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

**Workaround**

None.

**FLASH24**
***FLASH Module***


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**Category**

Functional

**Function**

Write or erase emergency exit can cause failures

**Description**

When a flash write or erase is abruptly terminated, the following flash accesses by the CPU may be unreliable resulting in erroneous code execution. The abrupt termination can be the result of one the following events:

1) The flash controller clock is configured to be sourced by an external crystal. An oscillator fault occurs thus stopping this clock abruptly.

or

2) The Emergency Exit bit (EMEX in FCTL3) when set forces a write or an erase operation to be terminated before normal completion.

or

3) The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1) when set with GIE=1 can lead to an interrupt causing an emergency exit during a Flash operation.

**Workaround**

1) Use the internal DCO as the flash controller clock provided from MCLK or SMCLK.

or

2) After setting EMEX = 1, wait for a sufficient amount of time before Flash is accessed again.

or

3) No Workaround. Do not use EEIEX bit.

**FLASH27**
***FLASH Module***


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**Category**

Functional

**Function**

EEl feature can disrupt segment erase

**Description**

When a flash segment erase operation is active with EEl feature selected (EEI=1 in FLCTL1) and GIE=0, the following can occur:

An interrupt event causes the flash erase to be stopped, and the flash controller expects an RETI to resume the erase. Because GIE=0, interrupts are not serviced and RETI will never happen.

**Workaround**

1) Do not set bit EEI=1 when GIE = 0.

or,

2) Force an RETI instruction during the erase operation during the check for BUSY=1 (FCTL3).

Sample code:

```
MOV R5, 0(R5) ; Dummy write, erase segment
```

```
LOOP: BIT #BUSY, &FCTL3 ; test busy bit
```

```
JMP SUB_RETI ; Force RETI instruction
```

```
JNZ LOOP ; loop while BUSY=1
```

```
SUB_RETI: PUSH SR
```

```
RETI
```

**FLASH36**
***FLASH Module***


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**Category**

Functional

**Function**

Flash content may degrade due to aborted page erases

**Description**

If a page erase is aborted by EEIEX, the flash page containing the last instruction before erase operation will start to degrade. This effect is incremental and, after repetitions, may lead to corrupted flash content.

**Workaround**

- Use the EEl (interrupted erasing) feature instead of EEIEX (abort erasing).

or

- A PSA checksum can be calculated over affected flash page using the marginal read mode (marginal 0). If PSA sum differs from expected PSA value the affected flash page has to be reprogrammed.

or

- Start flash erasing from RAM and limit system frequency to <1MHz (to ensure 6-us delay after EEIEX). If the last instruction before erasing is located in RAM, flash cell degradation does not occur.

**TA12**
***TIMER\_A Module***


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**Category**

Functional

<b>Function</b>	Interrupt is lost (slow ACLK)
<b>Description</b>	Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.
<b>Workaround</b>	Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

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**TA16** *TIMER\_A Module*


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<b>Category</b>	Functional
<b>Function</b>	First increment of TAR erroneous when IDx > 00
<b>Description</b>	The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.
<b>Workaround</b>	None

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**TA18** *TIMER\_A Module*


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<b>Category</b>	Functional
<b>Function</b>	MOV to TACTL may clear TAR
<b>Description</b>	When TACTL is modified with a MOV instruction, the contents of TAR may be cleared, even when TACLR is not set.
<b>Workaround</b>	Use BIS or BIC instructions to modify TACTL.

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**NOTE:** A DMA transfer must not occur while these BIS and BIC instructions execute. This can be prevented by disabling the DMA prior to these instructions, or by using the DMAONFETCH bit to align DMA transfers to instruction fetch boundaries.

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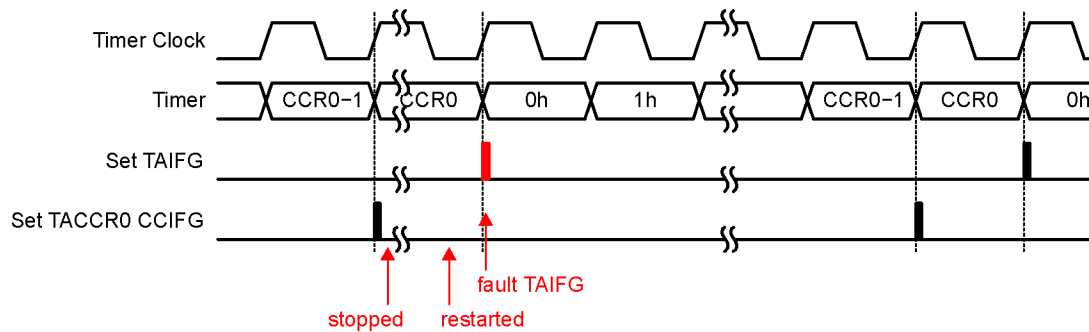


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**TA21** *TIMER\_A Module*


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<b>Category</b>	Functional
<b>Function</b>	TAIFG Flag is erroneously set after Timer A restarts in Up Mode
<b>Description</b>	In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



**Workaround** None.

## TAB22 *TIMER\_A/TIMER\_B Module*

**Category** Functional

**Function** Timer\_A/Timer\_B register modification after Watchdog Timer PUC

**Description** Unwanted modification of the Timer\_A/Timer\_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer\_A/Timer\_B counter register TACCRx/TBCCRx is incremented/decremented (Timer\_A/Timer\_B does not need to be running).

**Workaround** Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

## US15 *USART Module*

**Category** Functional

**Function** UART receive with two stop bits

**Description** USART hardware does not detect a missing second stop bit when SPB = 1.

The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

**Workaround** None (Configure USART for a single stop bit, SPB = 0)



## 7 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Errata BCL12 was added
2. Errata BSL3 was added
3. Errata BSL4 was added
4. Errata EEM20 was added
5. Errata FLASH36 was added
6. Errata SDA7 was added
7. Errata TA22 was renamed to TAB22
8. Description for TAB22 was updated
9. Workaround for CPU4 was updated

Changes from device specific erratasheet to document Revision A.

1. Errata BSL3 was removed from the errata documentation.
2. Errata BSL4 was removed from the errata documentation.

Changes from document Revision A to Revision B.

1. BCL12 Workaround was updated.

Changes from document Revision B to Revision C.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision C to Revision D.

1. TA18 Workaround was updated.

Changes from document Revision D to Revision E.

1. Errata SDA7 was removed from the errata documentation.
2. Package Markings section was updated.

Changes from document Revision E to Revision F.

1. TA21 Description was updated.

Changes from document Revision F to Revision G.

1. Function for CPU4 was updated.
2. Workaround for CPU4 was updated.

Changes from document Revision G to Revision H.

1. Erratasheet format update.
2. Added errata category field to "Detailed bug description" section

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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