2N7001T 単一ビット、デュアル電源のバッファ付き電圧信号コンバータ

1 特長

- 1.65V～3.6Vの昇圧および降圧変換
- 動作温度範囲: -40℃～+125℃
- 最大静止電流(I_{CCA} + I_{CCB}): 14µA (最大125℃)
- 電源電圧の全範囲にわたって最高100Mbpsをサポート
- V_{CC}絶縁機能
  - いずれかのV_{CC}入力が100mVより低下した場合、出力は高インピーダンスに変化
- I_{off}により部分的パワーダウン・モードをサポート
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
  - 2000V、人体モデル
  - 1000V、デバイス帯電モデル

2 アプリケーション

- MCU/FPGA/プロセッサのGPIO変換
- 通信モジュールからプロセッサへの変換
- プッシュプルI/Oのバッファ

3 概要

2N7001Tは単一ビットのバッファ付き電圧信号コンバータで、2つの独立した設定可能な電源レールを使用して、単方向の信号を昇圧または降圧変換します。このデバイスは、V_{CCA}とV_{CCB}電源の両方が最低1.65V、最高3.60Vの範囲で動作します。V_{CCA}は、A入力の入力スレッショルド電圧を定義します。V_{CCB}は、B出力の出力駆動電圧を定義します。

このデバイスは、I_{off}電流を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}保護回路により、電源切断時に入力、出力、複合I/Oは指定の電圧にバイアスされ、それらとの間に過剰な電流が流れることはありません。

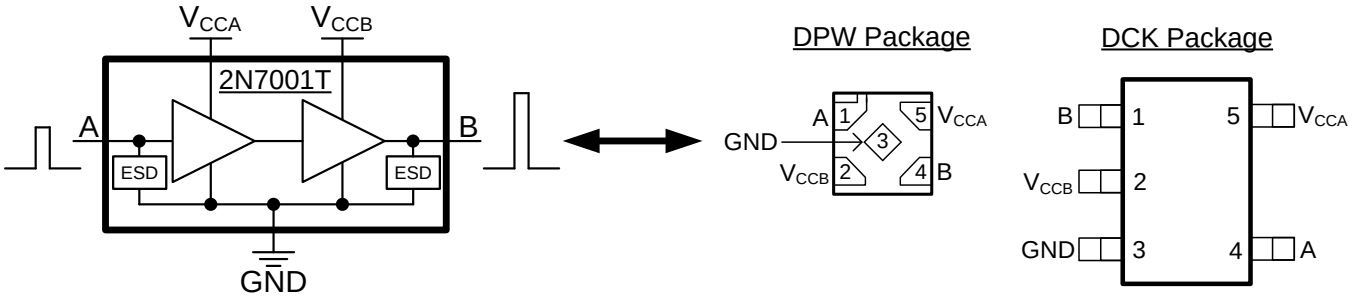
V_{CC}絶縁機能により、V_{CCA}とV_{CCB}のいずれかが100mVよりも低下した場合、出力ポート(B)は高インピーダンス状態に移行します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
2N7001TDCK	SC70 (5)	2.00mm×1.25mm
2N7001TDPW	X2SON (5)	0.80mm×0.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック図とピン配置



目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 6
6.7 Operating Characteristics ... 6
6.8 Typical Characteristics ... 7
7 **Parameter Measurement Information** ... 8
7.1 Load Circuit and Voltage Waveforms ... 8
8 **Detailed Description** ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 10
9 **Application and Implementation** ... 11
9.1 Application Information ... 11
9.2 Typical Applications ... 11
10 **Power Supply Recommendations** ... 13
11 **Layout** ... 13
11.1 Layout Guidelines ... 13
11.2 Layout Example ... 13
12 デバイスおよびドキュメントのサポート ... 14
12.1 ドキュメントのサポート ... 14
12.2 ドキュメントの更新通知を受け取る方法 ... 14
12.3 コミュニティ・リソース ... 14
12.4 商標 ... 14
12.5 静電気放電に関する注意事項 ... 14
12.6 Glossary ... 14
13 メカニカル、パッケージ、および注文情報 ... 14

4 改訂履歴

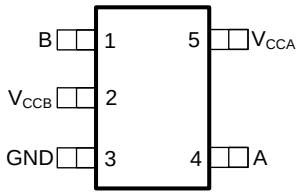
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年5月発行のものから更新 **Page**

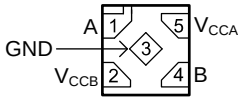
- 事前情報から量産データに 変更 ... 1

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



DPW Package
5-Pin X2SON
Transparent Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DCK	DPW		
A	4	1	I	Data Input. This pin is referenced to V_{CCA}.
B	1	4	O	Data Output. This pin is referenced to V_{CCB}.
V_{CCA}	5	5	—	Input Supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6 V.
V_{CCB}	2	2	—	Output Supply voltage. 1.65V ≤ V_{CCB} ≤ 3.6 V.
GND	3	3	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A Port		–0.5	4.2	V
V_{CCB}	Supply voltage, B Port		–0.5	4.2	V
V_I	Input voltage(2)		–0.5	4.2	V
V_O	Voltage applied to the output in the high-impedance or power-off state(2)		–0.5	4.2	V
V_O	Voltage applied to the output in the high or low state(2)(3)		–0.5	V_{CCB} + 0.2	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
I_O	Continuous current through V_{CCB} or GND		–50	50	mA
I_O	Continuous current through V_{CCA}		–10	10	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under the *Absolute Maximum Ratings* table may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, V_{CCA}		1.65	3.6	V
V_{CCB}	Supply voltage, V_{CCB}		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 1.65 V - 1.95 V	V_{CCA} × 0.65		V
		V_{CCA} = 2.30 V - 2.70 V	1.60		
		V_{CCA} = 3.00 V - 3.60 V	2.00		
V_{IL}	Low-level input voltage	V_{CCA} = 1.65 V - 1.95 V		V_{CCA} × 0.65	V
		V_{CCA} = 2.30 V - 2.70 V		0.70	
		V_{CCA} = 3.00 V - 3.60 V		0.80	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CCB}	V
		Tri-state	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate			100	ns/V
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		2N7001T		UNIT
		DCK (SC70)	DPW (X2SON)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.5	462.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	162.6	227.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	140.6	326.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	69.8	33.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	139.7	325.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V	V_{CCB} - 0.1			V
			I_{OH} = –8 mA	1.65 V	1.65 V	1.2			
			I_{OH} = –9 mA	2.3 V	2.3 V	1.75			
			I_{OH} = –12 mA	3 V	3 V	2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V			0.1	V
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7	
I_{off}	Partial power down current	V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–8		8	µA
		V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	–8		8	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCA}$ or GND, I_O = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.6 V	–8			
				3.6 V	0 V			8	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.6 V			8	
				3.6 V	0 V	–8			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			14	µA
C_I	Input capacitance	V_I = 1.65 V DC + 1MHz -16 dBm sine wave		3.3 V	0 V		2		pF
C_O	Output capacitance	V_I = 1.65 V DC + 1MHz -16 dBm sine wave		0 V	3.3 V		4		pF

(1) All typical values are for T_A = 25°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{pd}	Propagation Delay	V_{CCA}= 1.80 ± 0.15 V	V_{CCB} = 1.80 ± 0.15 V	0.5	20	ns
			V_{CCB} = 2.50 ± 0.20 V	0.5	17	
			V_{CCB} = 3.30 ± 0.30 V	0.5	14	
		V_{CCA}= 2.50 ± 0.20 V	V_{CCB} = 1.80 ± 0.15 V	0.5	18	
			V_{CCB} = 2.50 ± 0.20 V	0.5	15	
			V_{CCB} = 3.30 ± 0.30 V	0.5	12	
		V_{CCA} = 3.30 ± 0.30 V	V_{CCB} = 1.80 ± 0.15 V	0.5	16	
			V_{CCB} = 2.50 ± 0.20 V	0.5	13	
			V_{CCB} = 3.30 ± 0.30 V	0.5	10	

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power dissipation capacitance - Port A	I_O = 0 mA C_L = 0 pF, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V		1		pF
			V_{CCA} = V_{CCB} = 2.5 V		1.3		
			V_{CCA} = V_{CCB} = 3.3 V		1.8		
C_{pdB}	Power dissipation capacitance - B Port	I_O = 0 mA C_L = 0 pF, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V		12		pF
			V_{CCA} = V_{CCB} = 2.5 V		15		
			V_{CCA} = V_{CCB} = 3.3 V		18		

6.8 Typical Characteristics

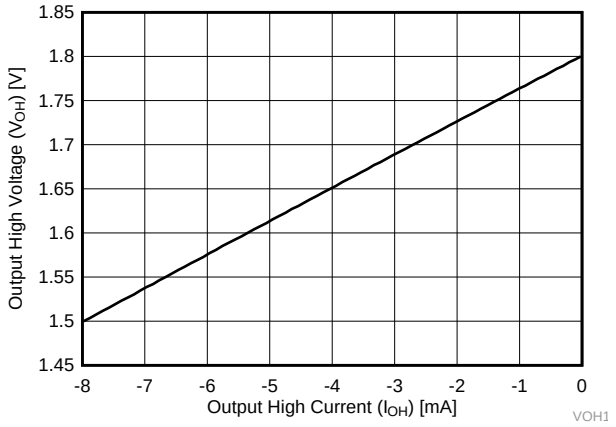


図 1. V_{OH} vs I_{OH}, 1.8 V

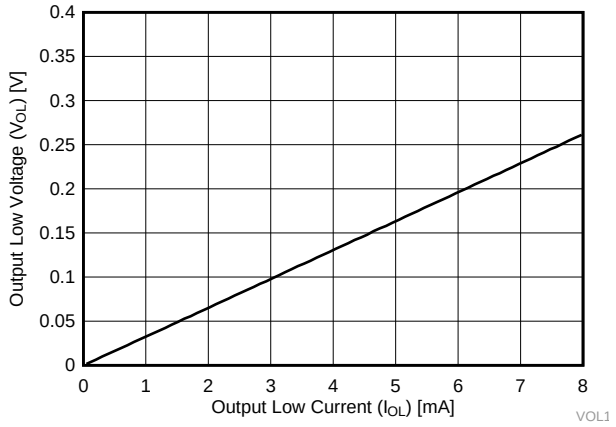


図 2. V_{OL} vs I_{OL}, 1.8 V

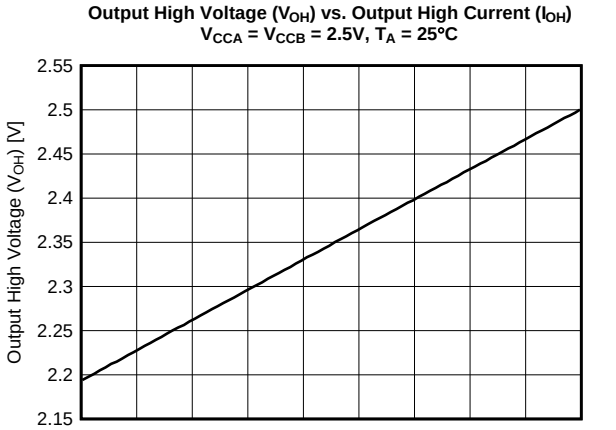


図 3. V_{OH} vs I_{OH}, 2.5 V

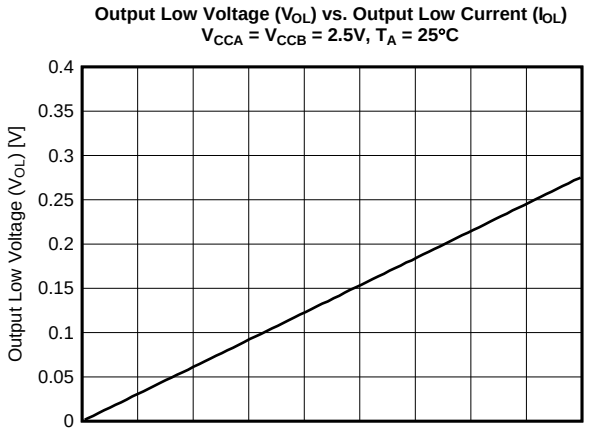


図 4. V_{OL} vs I_{OL}, 2.5 V

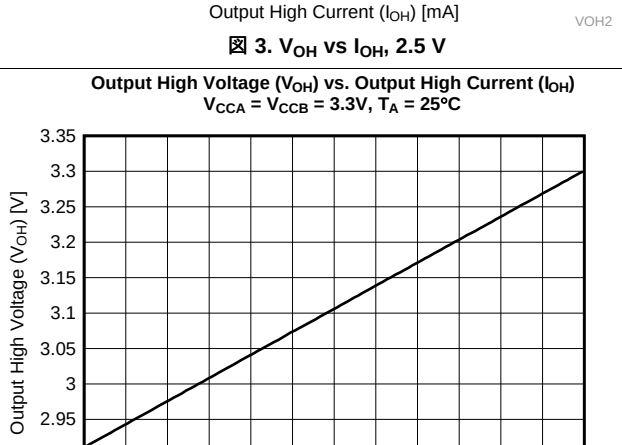


図 5. V_{OH} vs I_{OH}, 3.3 V

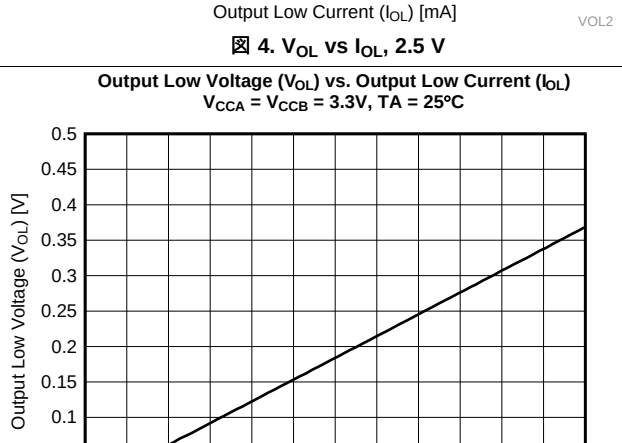


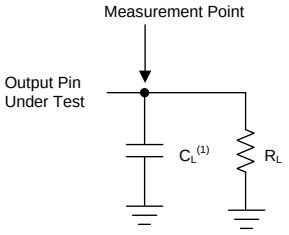
図 6. V_{OL} vs I_{OL}, 3.3 V

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

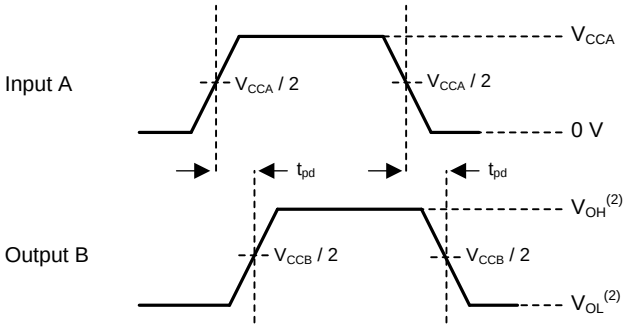


(1) C_L includes probe and jig capacitance.

図 7. Load Circuit

表 1. Load Circuit Conditions

Parameter		V_{CC}	R_L	C_L
t_{pd}	Propagation (delay) time	1.65 V – 3.6 V	2 kΩ	15 pF



(1) V_{CCI} is the supply pin associated with the input port.

(2) V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L and C_L.

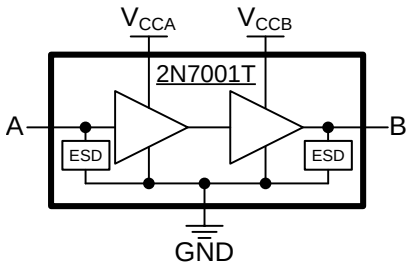
図 8. Propagation Delay

8 Detailed Description

8.1 Overview

The 2N7001T is a single-bit dual-supply buffered voltage signal converter that can be used to up or down-translate a single unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65 V and up to 3.60 V. V_{CCA} defines the input threshold voltage on the A input while V_{CCB} defines the output voltage on the B output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Up-Translation or Down-Translation from 1.65 V to 3.60 V

The V_{CCA} and V_{CCB} pins can both be supplied by a voltage range from 1.65 V to 3.6 V. This voltage range makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, and 3.3 V).

8.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Raings* must be followed at all times.

8.3.3 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance shown in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, shown in the *Absolute Maximum Ratings*, and the maximum input leakage current, shown in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.4 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in 図 9.

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

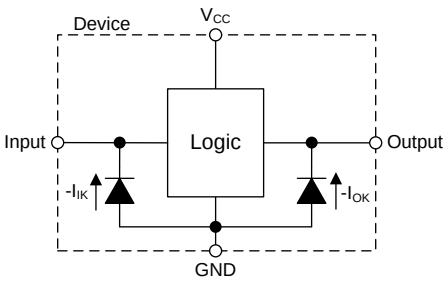


図 9. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.5 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input pin or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.6 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the input supply voltage (V_{CCA}), as long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.4 Device Functional Modes

表 2 lists the functional modes of the 2N7001T device.

表 2. Function Table

INPUT	OUTPUT
L (Referenced to V_{CCA})	L (Referenced to V_{CCB})
H (Referenced to V_{CCA})	H (Referenced to V_{CCB})

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The 2N7001T device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages.

9.2 Typical Applications

9.2.1 Processor Error Up Translation

図 10 shows an example of the 2N7001T being used in a unidirectional logic level-shifting application.

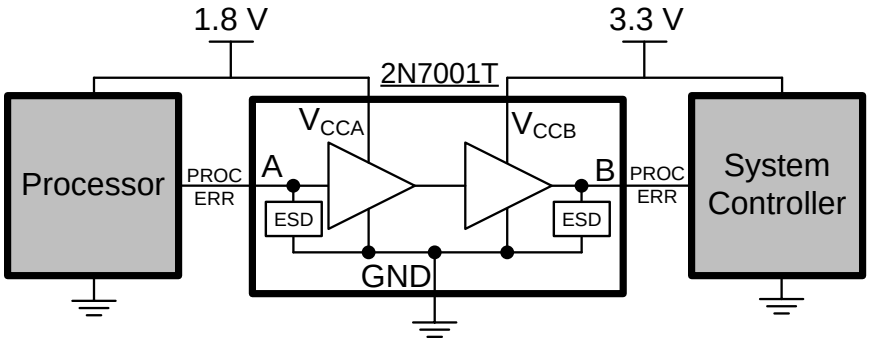


図 10. Processor Error Up Translation Application

9.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 3.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage supply	1.8 V
Output voltage supply	3.3 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - The supply voltage of the upstream device (device that is driving input pin A) will determine the appropriate input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - The supply voltage of the downstream device (device that output pin B is driving) will determine the appropriate output voltage range.

9.2.1.3 Application Curve

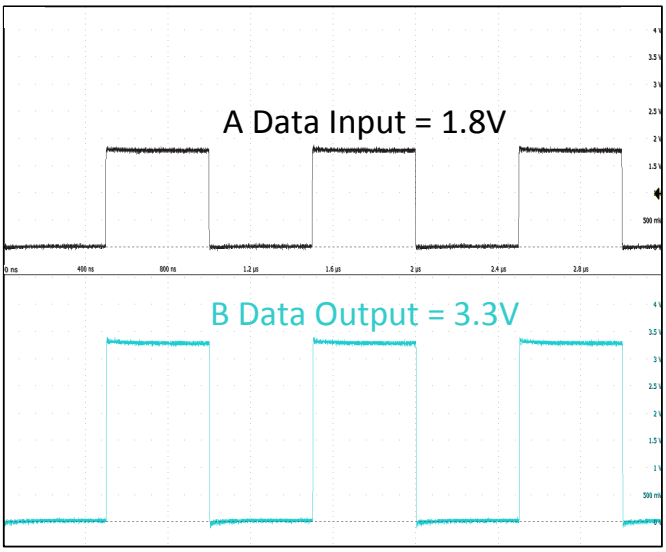


図 11. Up Translation (1.8 V to 3.3 V) at 1 MHz

9.2.2 Discrete FET Translation Replacement

The 2N7001T device is an excellent option for replacing discrete translators, as shown in 図 12, and has the following benefits regarding discrete translation implementations:

- A single device vs a four component solution
- Minimized implementation size
- Lower power consumption
- V_{CC} isolation feature
- Higher data rates
- Integrated ESD protection
- Improved glitch performance

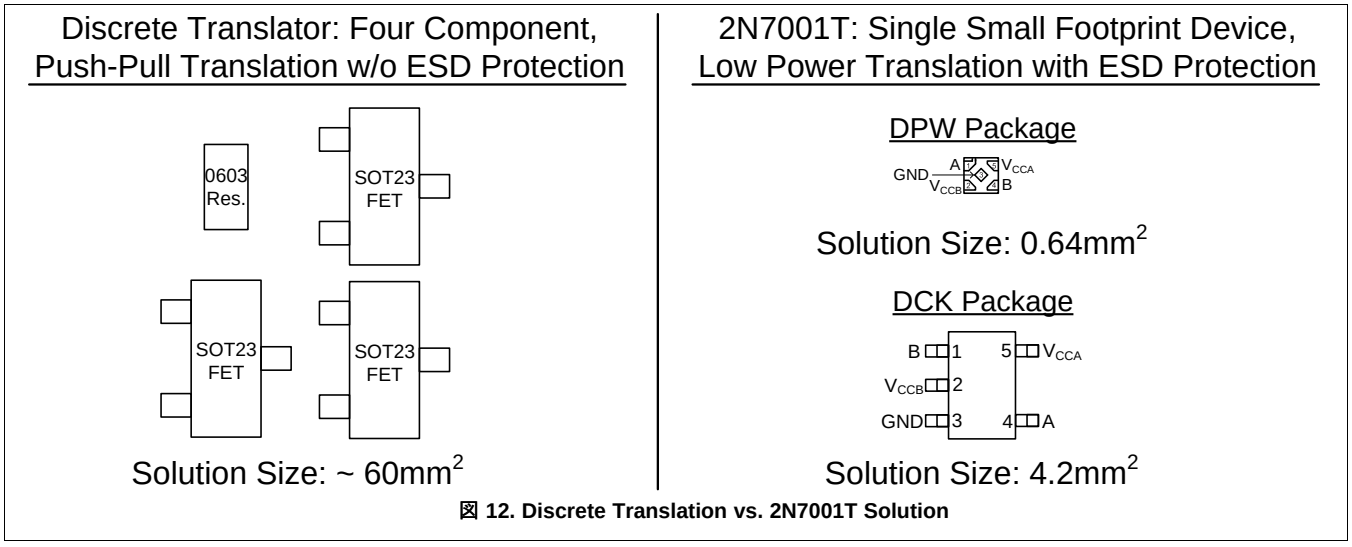


図 12. Discrete Translation vs. 2N7001T Solution

10 Power Supply Recommendations

The 2N7001T device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. The V_{CCA} and V_{CCB} power-supply rails accept any supply voltage that range from 1.65 V to 3.6 V. The A input and B output are referenced to V_{CCA} and V_{CCB} respectively allowing up or down translation among the 1.8-V, 2.5-V, and 3.3-V voltage nodes. A 0.1 µF bypass capacitor is recommended on all V_{CC} pins.

Always apply a ground reference to the GND pin first. However, there are no additional requirement for power supply sequencing.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, follow the common printed-circuit board layout guidelines listed below:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.

An example layout is given in 図 13 for the DPW (X2SON-5) package. This example layout includes two 0402 (metric) capacitors, and uses the measurements that are in the package outline drawing appended to the end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or the via can be left out of the layout.

11.2 Layout Example

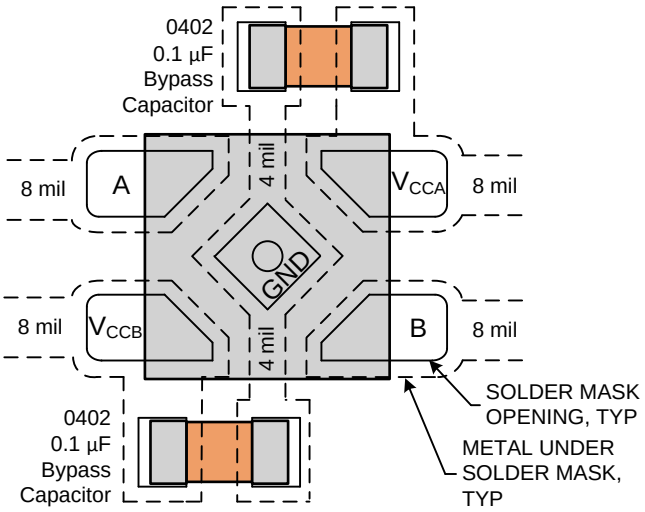


図 13. Example Layout for the DPW (X2SON-5) Package

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『低速またはフローティングCMOS入力の影響』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『TIのX2SONパッケージによる設計と製造』*アプリケーション・レポート

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つ**E2E**フォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.4 商標

E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2N7001TDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(DQ, DQL)	Samples
2N7001TDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(D, DP)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF 2N7001T :

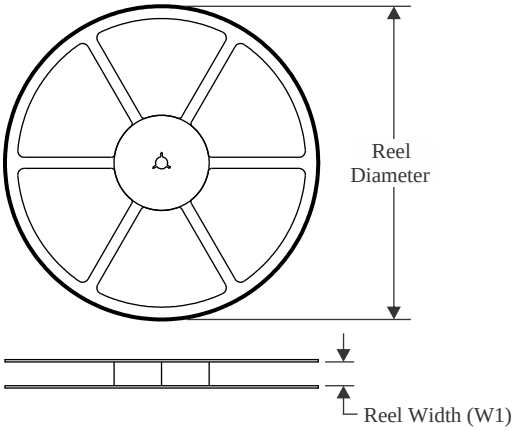
- Automotive : 2N7001T-Q1

NOTE: Qualified Version Definitions:

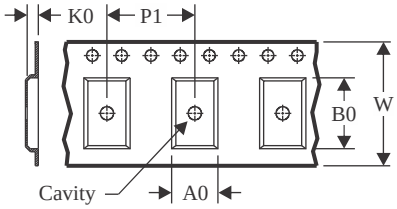
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

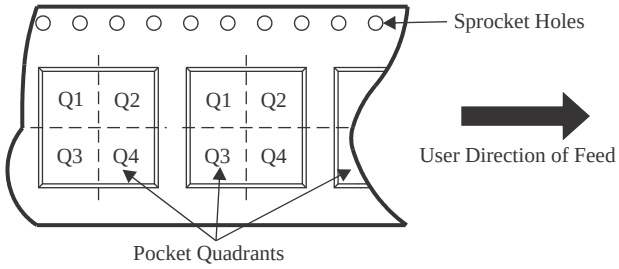


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

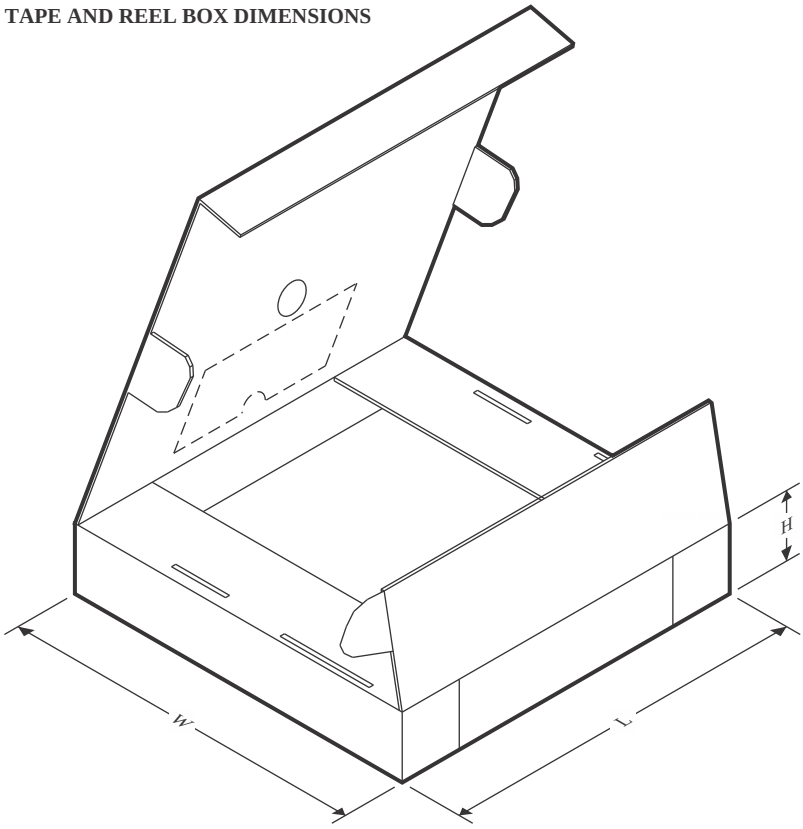
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2N7001TDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
2N7001TDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2N7001TDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
2N7001TDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

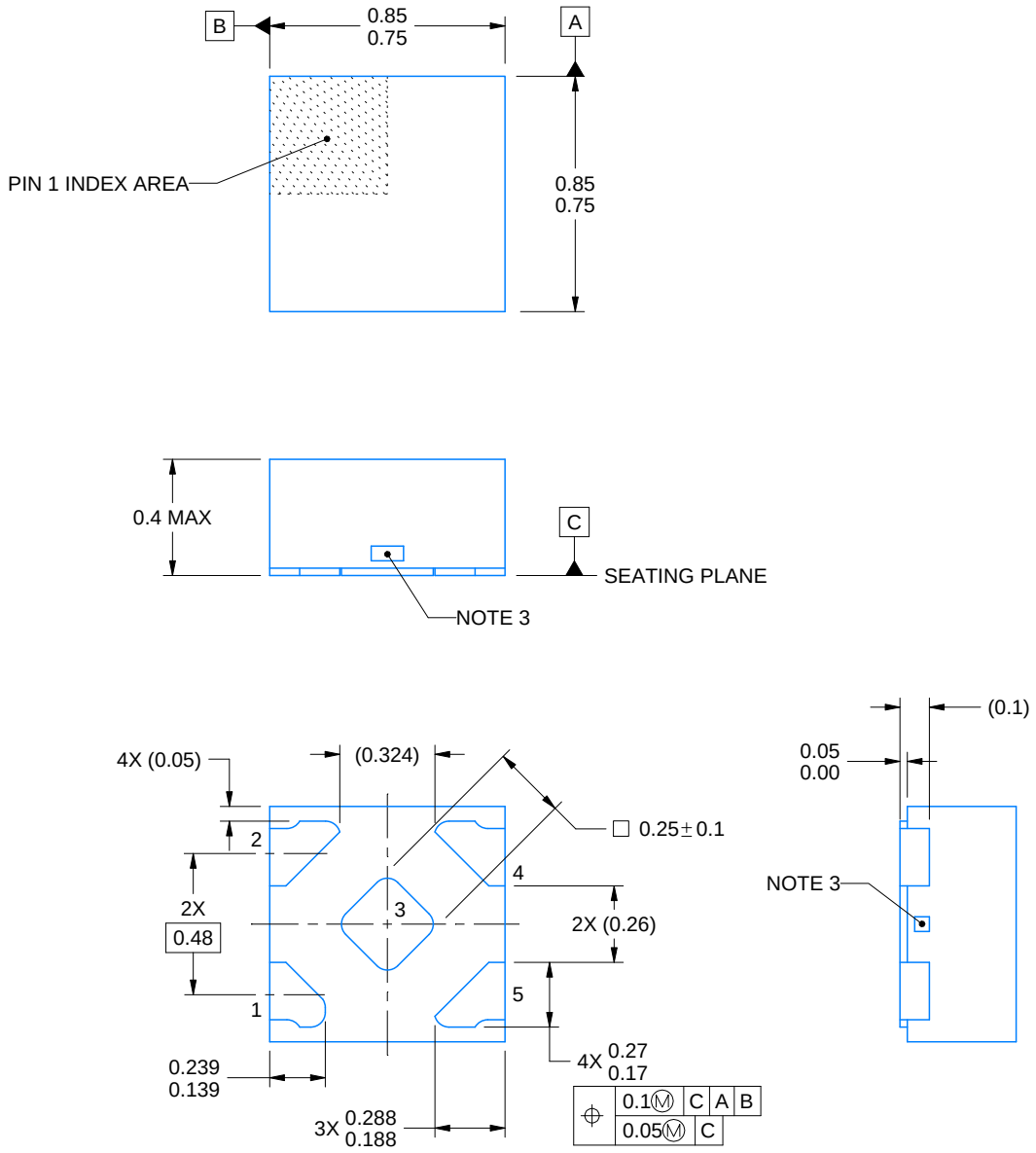
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

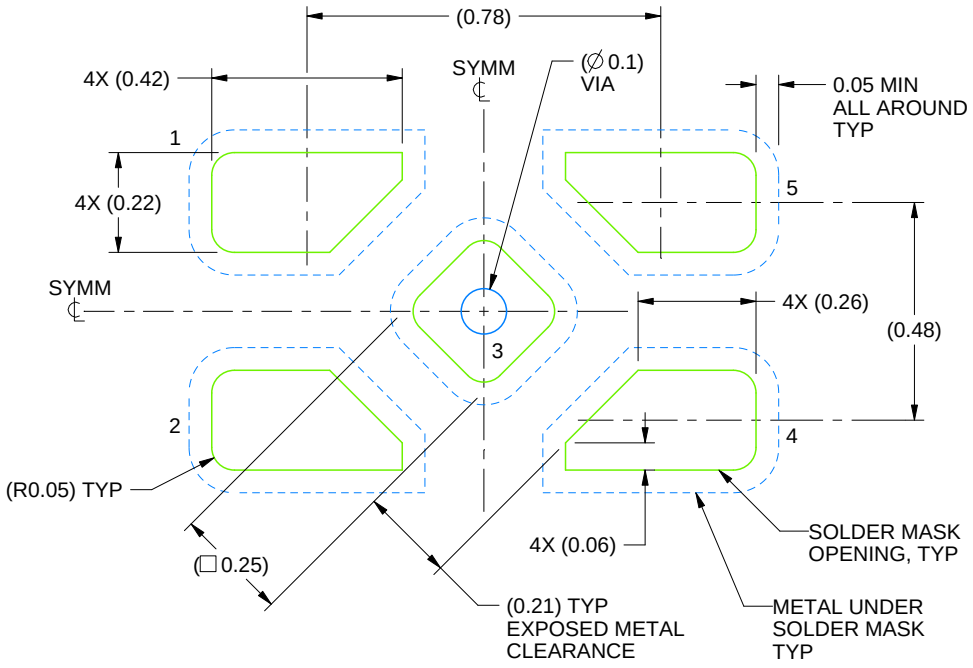
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

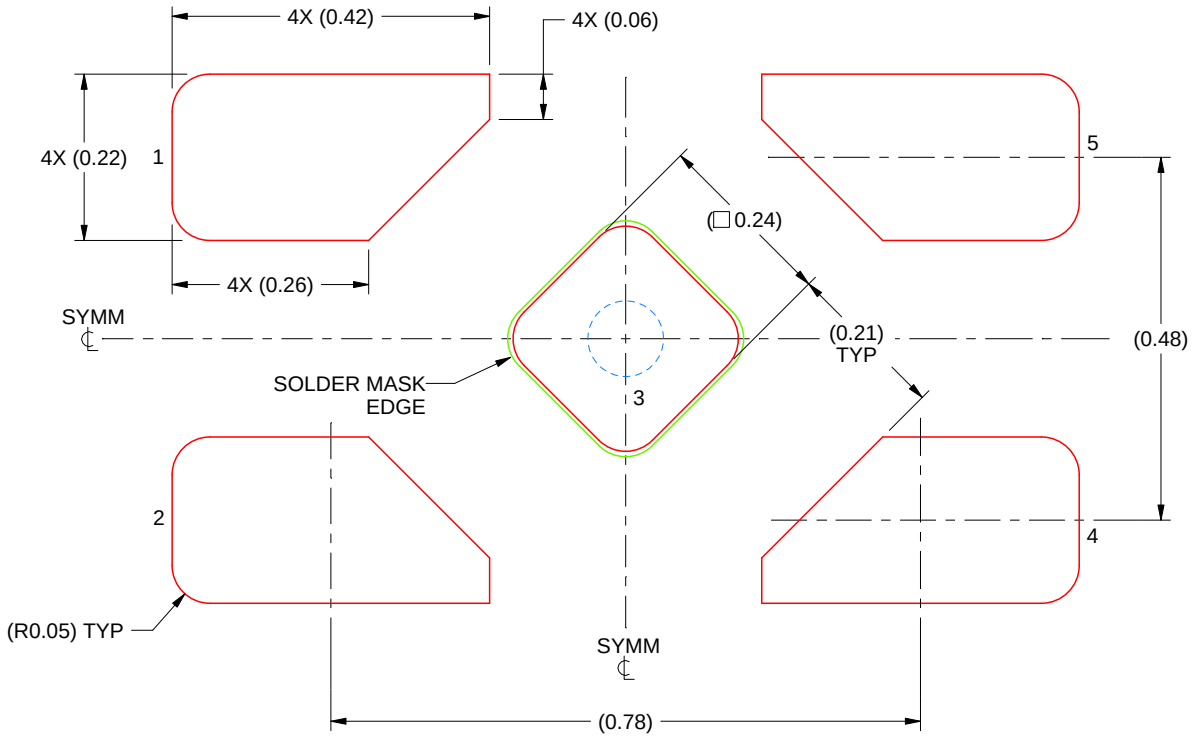
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

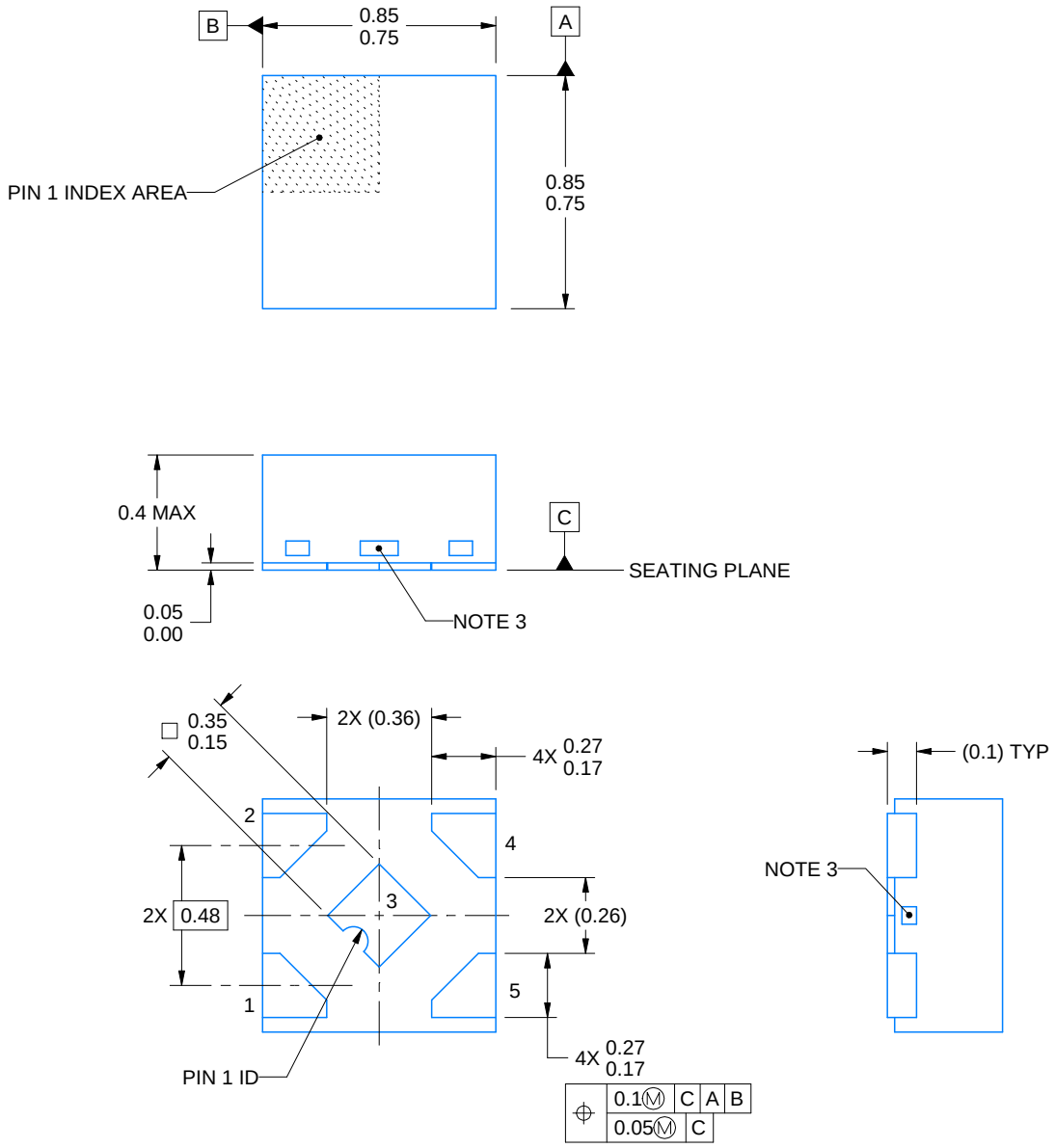
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DPW0005B

X2SON - 0.4 mm max height

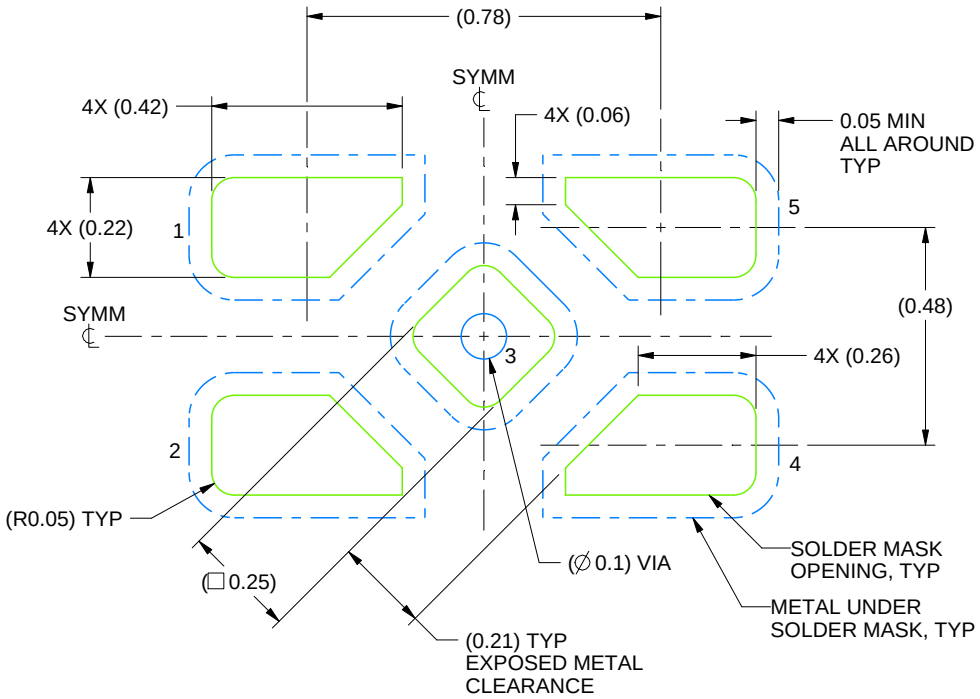
PLASTIC SMALL OUTLINE - NO LEAD



4228233/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

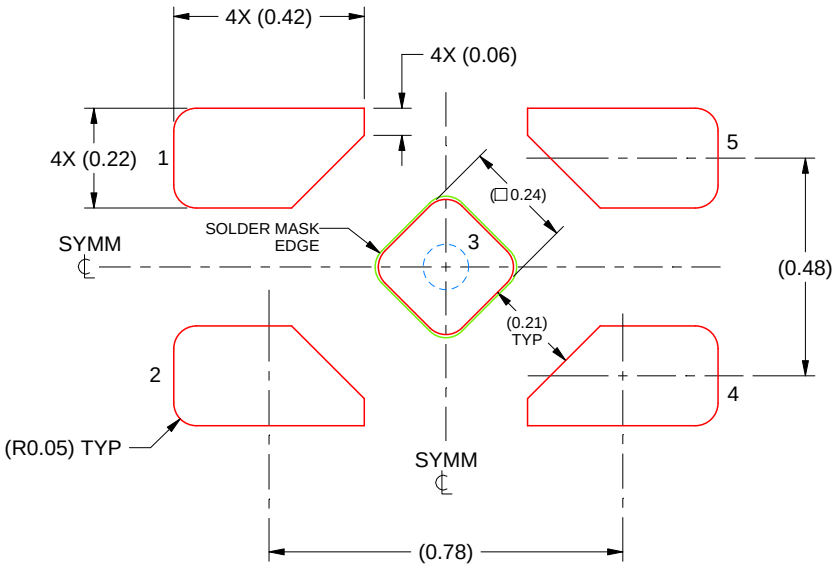


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

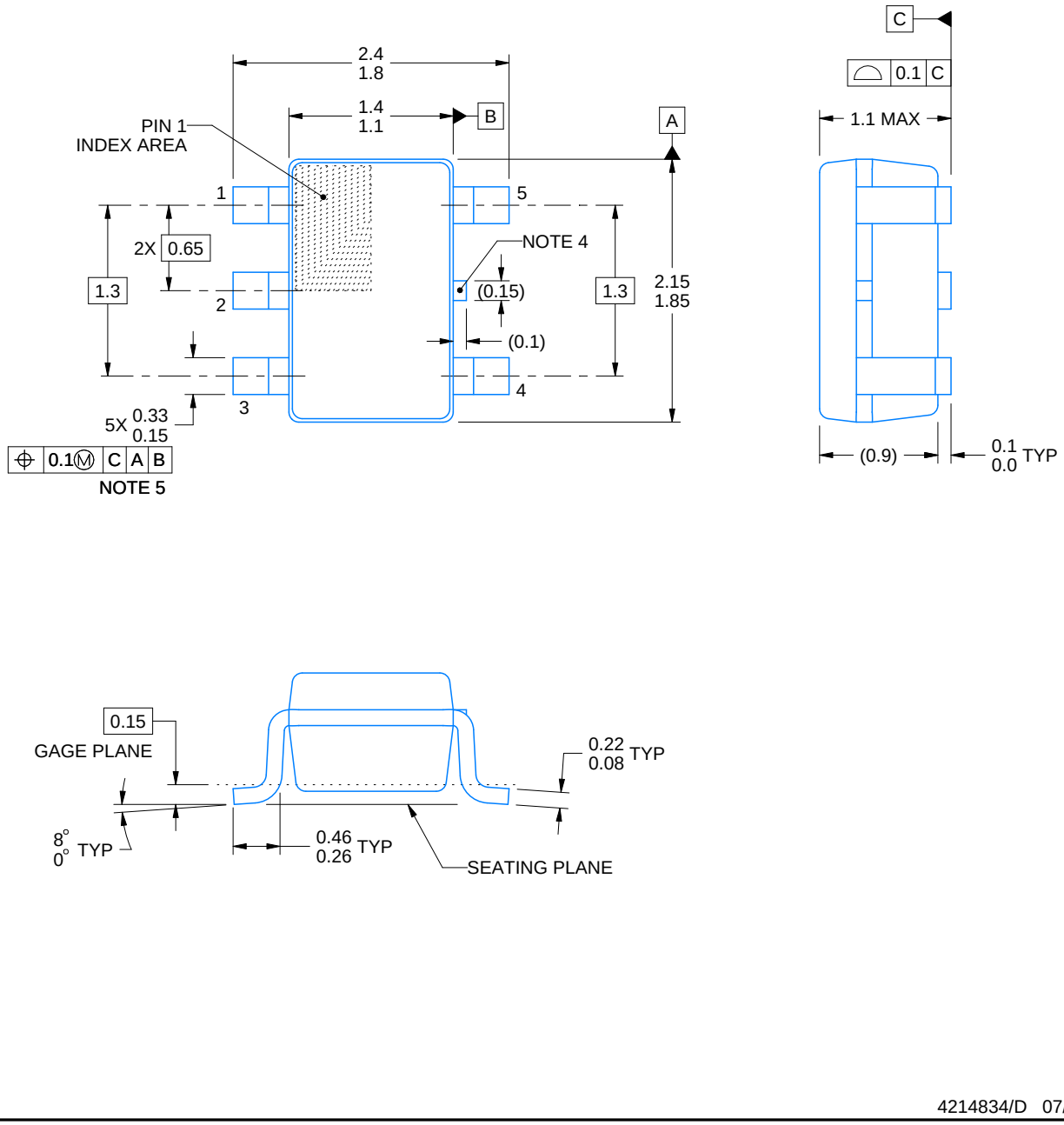
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

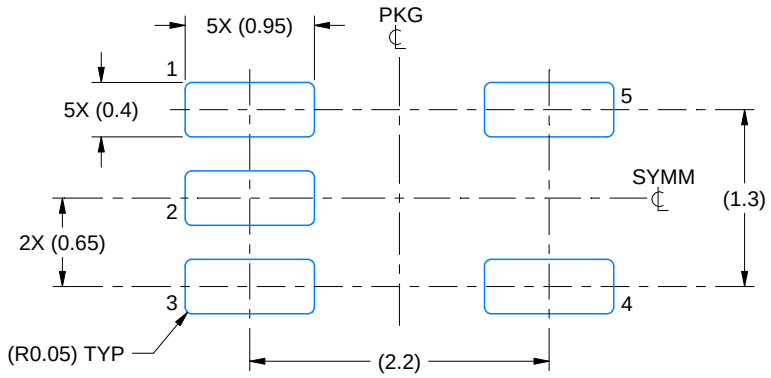
SMALL OUTLINE TRANSISTOR



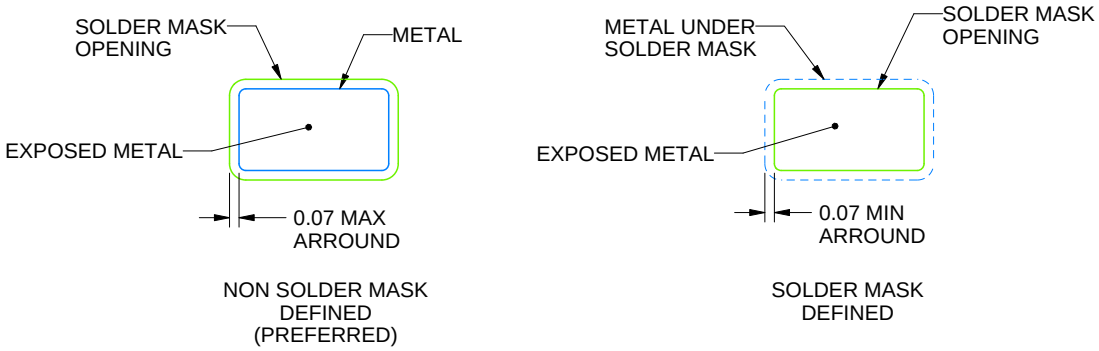
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

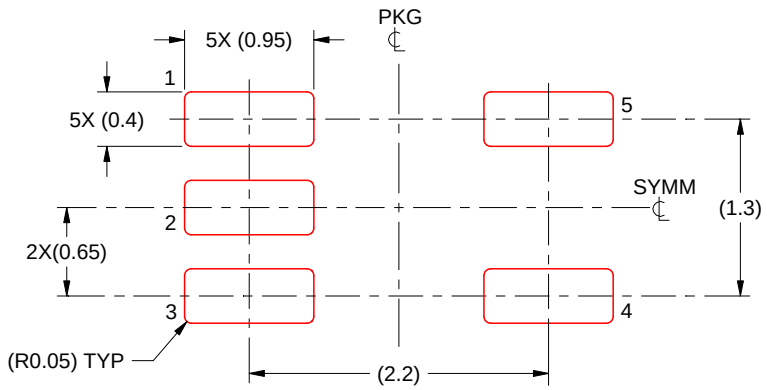


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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