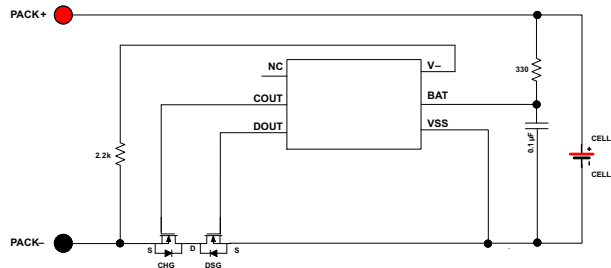


BQ297xx シングル・セルのリチウムイオンおよびリチウムポリマー・バッテリー用のコスト効率の優れた電圧および電流保護 IC

1 特長

- 入力電圧範囲 (pack+): (VSS – 0.3V) ~ 12V
- FET ドライブ:
 - CHG および DSG FET ドライブ出力
- 過電流保護 (OCP) 用の外部 FET 両端の電圧センシングは $\pm 5\text{mV}$ 以内 (標準値)
- 故障検出
 - 過充電検出 (OVP)
 - 過放電検出 (UVP)
 - 充電過電流検出 (OCC)
 - 放電過電流検出 (OCD)
 - 負荷短絡検出 (SCP)
- 消耗したバッテリー用のゼロ電圧充電
- フォルト保護のスレッシュホールドを出荷時プログラム
 - フォルト検出電圧スレッシュホールド
 - フォルト・トリガ・タイマ
 - フォルト回復タイマ
- バッテリー充電器を有効にしない動作モード
 - 通常モード $I_{CC} = 4\mu\text{A}$
 - シャットダウン時 $I_q = 100\text{nA}$
- 動作温度範囲: $T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$
- パッケージ:
 - 6 ピン DSE (1.50mm × 1.50mm × 0.75mm)



概略回路図

2 アプリケーション

- タブレット PC
- モバイル・ハンドセット
- ハンドヘルド・データ端末

3 概要

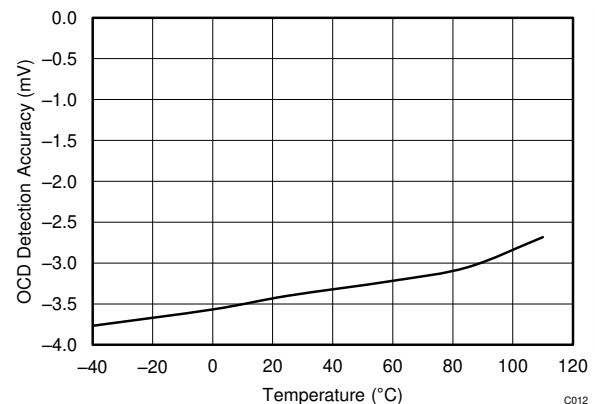
BQ2970 バッテリー・セル保護デバイスは、大電流の放電 / 充電動作やバッテリーの過充電状況において、過電流保護のスレッシュホールドを正確に監視およびトリガします。

BQ2970 デバイスは、リチウムイオン / リチウムポリマー・セル用の保護機能を実装しており、複数の外部パワー FET を監視し、大きな充電または放電電流に対する保護を行います。さらに、過充電と消耗したバッテリーの監視と保護も行います。これらの機能は、通常モード動作時に消費電流を少なくする方法で実装されています。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | 本体サイズ (公称) |
|--------------------------------|----------------------|-----------------|
| BQ2970, BQ2971, BQ2972, BQ2973 | WSO (6) | 1.50mm × 1.50mm |

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



OCD 検出精度と温度との関係



Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 特長 | 1 | 9 Detailed Description | 14 |
| 2 アプリケーション | 1 | 9.1 Overview..... | 14 |
| 3 概要 | 1 | 9.2 Functional Block Diagram..... | 15 |
| 4 Revision History | 2 | 9.3 Feature Description..... | 15 |
| 5 Device Comparison Table | 3 | 9.4 Device Functional Modes..... | 15 |
| 6 Pin Configuration and Functions | 3 | 10 Application and Implementation | 19 |
| 6.1 Pin Descriptions..... | 4 | 10.1 Application Information..... | 19 |
| 7 Specifications | 4 | 10.2 Typical Application..... | 19 |
| 7.1 Absolute Maximum Ratings..... | 4 | 11 Power Supply Recommendations | 22 |
| 7.2 ESD Ratings..... | 4 | 12 Layout | 22 |
| 7.3 Recommended Operating Conditions..... | 5 | 12.1 Layout Guidelines..... | 22 |
| 7.4 Thermal Information..... | 5 | 12.2 Layout Example..... | 22 |
| 7.5 DC Characteristics..... | 5 | 13 Device and Documentation Support | 23 |
| 7.6 Programmable Fault Detection Thresholds..... | 6 | 13.1 Related Documentation..... | 23 |
| 7.7 Programmable Fault Detection Timer Ranges..... | 6 | 13.2 サポート・リソース..... | 23 |
| 7.8 Typical Characteristics..... | 7 | 13.3 Trademarks..... | 23 |
| 8 Parameter Measurement Information | 10 | 13.4 Electrostatic Discharge Caution..... | 23 |
| 8.1 Timing Charts..... | 10 | 13.5 Glossary..... | 23 |
| 8.2 Test Circuits..... | 12 | 14 Mechanical, Packaging, and Orderable Information | 23 |
| 8.3 Test Circuit Diagrams..... | 14 | | |

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| | |
|---|-------------|
| Changes from Revision G (December 2018) to Revision H (June 2021) | Page |
| • Changed the BQ29728 and BQ29737 devices to Production Data..... | 3 |
| Changes from Revision F (December 2018) to Revision G (January 2020) | Page |
| • Changed the <i>Device Comparison Table</i> | 3 |

5 Device Comparison Table

| PART NUMBER ⁽¹⁾ | OVP (V) | OVP DELAY (s) | UVP (V) | UVP DELAY (ms) | OCC (V) | OCC DELAY (ms) | OCD (V) | OCD DELAY (ms) | SCD (V) | SCD DELAY (μs) |
|----------------------------|----------|--------------------|---------|------------------|------------------|----------------|-------------|----------------|--------------------|----------------|
| BQ29700 | 4.275 | 1.25 | 2.800 | 144 | −0.100 | 8 | 0.100 | 20 | 0.5 | 250 |
| BQ29701 | 4.280 | 1.25 | 2.300 | 144 | −0.100 | 8 | 0.125 | 8 | 0.5 | 250 |
| BQ29702 | 4.350 | 1 | 2.800 | 96 | −0.155 | 8 | 0.160 | 16 | 0.3 | 250 |
| BQ29703 | 4.425 | 1.25 | 2.300 | 20 | −0.100 | 8 | 0.160 | 8 | 0.5 | 250 |
| BQ29704 | 4.425 | 1.25 | 2.500 | 20 | −0.100 | 8 | 0.125 | 8 | 0.5 | 250 |
| BQ29705 | 4.425 | 1.25 | 2.500 | 20 | −0.100 | 8 | 0.150 | 8 | 0.5 | 250 |
| BQ29706 | 3.850 | 1.25 | 2.500 | 144 | −0.150 | 8 | 0.200 | 8 | 0.6 | 250 |
| BQ29707 | 4.280 | 1 | 2.800 | 96 | −0.090 | 6 | 0.090 | 16 | 0.3 | 250 |
| BQ29716 | 4.425 | 1.25 | 2.300 | 20 | −0.100 | 8 | 0.165 | 8 | 0.5 | 250 |
| BQ29717 | 4.425 | 1.25 | 2.500 | 20 | −0.100 | 8 | 0.130 | 8 | 0.5 | 250 |
| BQ29718 | 4.425 | 1.25 | 2.500 | 20 | −0.100 | 8 | 0.100 | 8 | 0.5 | 250 |
| BQ29723 | 4.425 | 1 | 2.500 | 96 | −0.060 | 4 | 0.100 | 8 | 0.3 | 250 |
| BQ29728 | 4.280 | 1.25 | 2.800 | 144 | −0.100 | 8 | 0.150 | 8 | 0.5 | 250 |
| BQ29729 | 4.275 | 1.25 | 2.300 | 20 | −0.100 | 8 | 0.130 | 8 | 0.5 | 250 |
| BQ29732 | 4.280 | 1.25 | 2.500 | 144 | −0.100 | 8 | 0.190 | 8 | 0.5 | 250 |
| BQ29733 | 4.400 | 1.25 | 2.800 | 20 | −0.100 | 8 | 0.120 | 8 | 0.3 | 250 |
| BQ29737 | 4.250 | 1 | 2.800 | 96 | −0.050 | 16 | 0.100 | 16 | 0.3 | 250 |
| BQ297xy | 3.85–4.6 | 0.25, 1, 1.25, 4.5 | 2.0–2.8 | 20, 96, 125, 144 | −0.045 to −0.155 | 4, 6, 8, 16 | 0.090–0.200 | 8, 16, 20, 48 | 0.3, 0.4, 0.5, 0.6 | 250 |

- (1) All of the protections have a recovery delay time. The recovery timer starts as soon as the fault is triggered. The device starts to check for a recovery condition only when the recovery timer expires. This is NOT a delay time between recovery condition to FETs recovery. OVP recovery delay = 12 ms; UVP/OCC/OCD recovery delay = 8 ms.

6 Pin Configuration and Functions

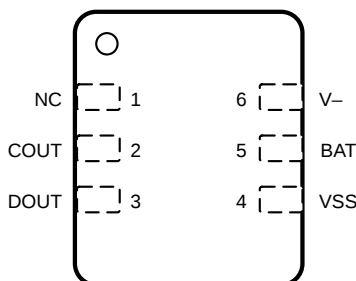


图 6-1. DSE Package 6-PIN WSON Top View

表 6-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|------|-----|------|--|
| NAME | NO. | | |
| BAT | 5 | P | VDD pin |
| COUT | 2 | O | Gate Drive Output for Charge FET |
| DOUT | 3 | O | Gate Drive Output for Discharge FET |
| NC | 1 | NC | No Connection (electrically open, do <i>not</i> connect to BAT or VSS) |
| VSS | 4 | P | Ground pin |
| V− | 6 | I/O | Input pin for charger negative voltage |

6.1 Pin Descriptions

6.1.1 Supply Input: BAT

This pin is the input supply for the device and is connected to the positive terminal of the battery pack. A 0.1- μ F input capacitor is connected to ground for filtering noise.

6.1.2 Cell Negative Connection: VSS

This pin is an input to the device for cell negative ground reference. Internal circuits associated with cell voltage measurements and overcurrent protection input to differential amplifier for either Vds sensing or external sense resistor sensing will be referenced to this node.

6.1.3 Voltage Sense Node: V–

This is a sense node used for measuring several fault detection conditions, such as overcurrent charging or overcurrent discharging configured as Vds sensing for protection. This input, in conjunction with VSS, forms the differential measurement for the stated fault detection conditions. A 2.2-k Ω resistor is connected between this input pin and Pack– terminal of the system in the application.

6.1.4 Discharge FET Gate Drive Output: DOUT

This pin is an output to control the discharge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the DSG FET to turn OFF. A 5-M Ω high impedance resistor is connected from DOUT to VSS for gate capacitance discharge when the FET is turned OFF.

6.1.5 Charge FET Gate Drive Output: COUT

This pin is an output to control the charge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the CHG FET to turn OFF. A 5-M Ω high impedance resistor is connected from COUT to Pack– for gate capacitance discharge when FET is turned OFF.

7 Specifications

7.1 Absolute Maximum Ratings

| | | MIN ⁽¹⁾ | MAX | UNIT |
|---------------------------------------|--|--------------------|-----------|------|
| Supply control and input | Input voltage: BAT | –0.3 | 12 | V |
| | V– pin(pack–) | BAT – 28 | BAT + 0.3 | V |
| FET drive and protection | DOUT (Discharge FET Output), GDSD (Discharge FET Gate Drive) | VSS – 0.3 | BAT + 0.3 | V |
| | COUT (Charge FET Output), GCHG (Charge FET Gate Drive) | BAT – 28 | BAT + 0.3 | V |
| | Operating temperature: T _{FUNC} | –40 | 85 | °C |
| Storage temperature, T _{stg} | | –55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|---------------------------------|-------------------------|--|-------|------|
| V _{ESD} ⁽¹⁾ | Electrostatic Discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS–001, all pins ⁽²⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽³⁾ | ±500 | |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 1000 V can have higher performance.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V can have higher performance.

7.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|--------------------------|---|----------|-----|------|
| Supply control and input | Positive input voltage: BAT | –0.3 | 8 | V |
| | Negative input voltage: V– | BAT – 25 | BAT | V |
| FET drive and protection | Discharge FET control: DOUT | VSS | BAT | V |
| | Charge FET control: COUT | BAT – 25 | BAT | V |
| Temperature Ratings | Operating temperature: T _{Amb} | –40 | 85 | °C |
| | Storage temperature: T _S | –55 | 150 | °C |
| | Lead temperature (soldering 10 s) | | 300 | °C |
| | Thermal resistance junction to ambient, θ_{JA} | | 250 | °C/W |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | BQ297xx | UNIT |
|-------------------------------|--|-----------|------|
| | | DSE (WSN) | |
| | | 12 PINS | |
| R _{θJA} , High K | Junction-to-ambient thermal resistance | 190.5 | °C/W |
| R _{θJC(top)} | Junction-to-case(top) thermal resistance | 94.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 149.3 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 6.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 152.8 | °C/W |
| R _{θJC(bottom)} | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 DC Characteristics

Typical Values stated where T_A = 25°C and BAT = 3.6 V. Min/Max values stated where T_A = –40°C to 85°C, and BAT = 3 V to 4.2 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|------------------------|-----|------|
| Current consumption | | | | | |
| V _{BAT} Device operating range | BAT – VSS | 1.5 | | 8 | V |
| | BAT – V– | 1.5 | | 28 | |
| I _{NORMAL} Current consumption in NORMAL mode | BAT = 3.8 V, V– = 0 V | | 4 | 5.5 | μA |
| I _{Power_down} Current consumption in power down mode | BAT = V– = 1.5 V | | | 0.1 | μA |
| FET Output, DOUT and COUT | | | | | |
| V _{OL} Charge FET low output | I _{OL} = 30 μA, BAT = 3.8 V | | 0.4 | 0.5 | V |
| V _{OH} Charge FET high output | I _{OH} = –30 μA, BAT = 3.8 V | 3.4 | 3.7 | | V |
| V _{OL} Discharge FET low output | I _{OL} = 30 μA, BAT = 2 V | | 0.2 | 0.5 | V |
| V _{OH} Discharge FET high output | I _{OH} = –30 μA, BAT = 3.8 V | 3.4 | 3.7 | | V |
| Pullup Internal Resistance on V– | | | | | |
| R _{V–D} Resistance between V– and VBAT | V _{BAT} = 1.8 V, V– = 0 V | 100 | 300 | 550 | kΩ |
| Current sink on V– | | | | | |
| I _{V–S} Current sink on V– to VSS | V _{BAT} = 3.8 V | 8 | | 24 | μA |
| Load short detection on V– | | | | | |
| V _{short} Short detection voltage | V _{BAT} = 3.8 V and R _{PackN} = 2.2 kΩ | | V _{BAT} – 1 V | | V |
| 0-V battery charge function | | | | | |
| V _{0CHG} 0-V battery charging start voltage | 0-V battery charging function allowed | 1.7 | | | V |

7.5 DC Characteristics (continued)

Typical Values stated where $T_A = 25^\circ\text{C}$ and $BAT = 3.6\text{ V}$. Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C , and $BAT = 3\text{ V}$ to 4.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----|-----|------|------|
| 0-V battery charge inhibit function | | | | | | |
| V_{0INH} | 0-V battery charging inhibit voltage threshold | 0-V battery charging function disallowed | | | 0.75 | V |

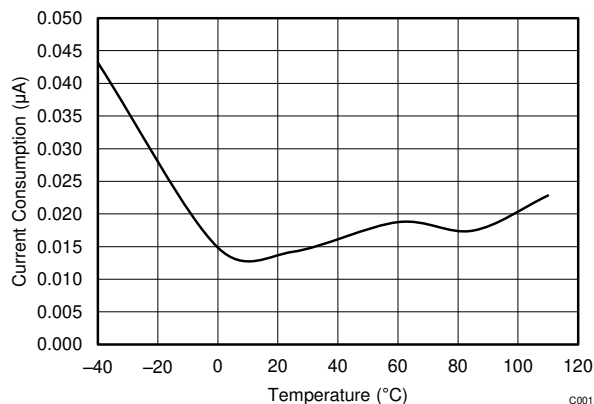
7.6 Programmable Fault Detection Thresholds

| PARAMETER | | CONDITION | MIN | TYP | MAX | UNIT |
|----------------------|--|---|---|------|-----|------|
| V_{OVP} | Overcharge detection voltage | Factory Device Configuration: 3.85 V to 4.60 V in 50-mV steps | $T_A = 25^\circ\text{C}$ | | 10 | mV |
| | | | $T_A = 0^\circ\text{C}$ to 60°C | | 20 | mV |
| $V_{OVP-Hys}$ | Overcharge release hysteresis voltage | 100 mV and $(V_{SS} - V_-) > OCC$ (min) for release, $T_A = 25^\circ\text{C}$ | -20 | | 20 | mV |
| V_{UVP} | Over-discharge detection voltage | Factory Device Configuration: 2.00 V to 2.80 V in 50-mV steps, $T_A = 25^\circ\text{C}$ | -50 | | 50 | mV |
| $V_{UVP-Hys}$ | Over-discharge release hysteresis voltage | 100 mV and $(BAT - V_-) > 1\text{ V}$ for release, $T_A = 25^\circ\text{C}$ | -50 | | 50 | mV |
| V_{OCD} | Discharging overcurrent detection voltage | Factory Device Configuration: 90 mV to 200 mV in 5-mV steps | $T_A = 25^\circ\text{C}$ | | 10 | mV |
| | | | $T_A = -40^\circ\text{C}$ to 85°C | | 15 | mV |
| Release of V_{OCD} | Release of discharging overcurrent detection voltage | Release when $BAT - V_- > 1\text{ V}$ | | 1 | | V |
| V_{OCC} | Charging overcurrent detection voltage | Factory Device Configuration: -45 mV to -155 mV in 5-mV steps | $T_A = 25^\circ\text{C}$ | | 10 | mV |
| | | | $T_A = -40^\circ\text{C}$ to 85°C | | 15 | mV |
| Release of V_{OCC} | Release of overcurrent detection voltage | Release when $V_{SS} - V_- \geq OCC$ (min) | | 40 | | mV |
| V_{SCC} | Short Circuit detection voltage | Factory Device Configuration: 300 mV, 400 mV, 500 mV, 600 mV | $T_A = 25^\circ\text{C}$ | -100 | 100 | mV |
| V_{SCCR} | Release of Short Circuit detection voltage | Release when $BAT - V_- \geq 1\text{ V}$ | | 1 | | V |

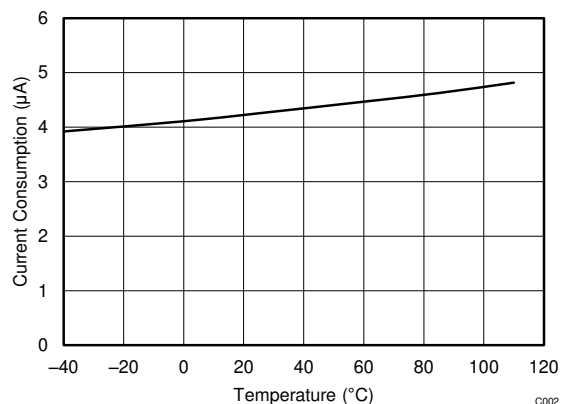
7.7 Programmable Fault Detection Timer Ranges

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|------------|--|--|------|-----|---------------|
| t_{OVPD} | Overcharge detection delay time | Factory Device Configuration: 0.25 s, 1 s, 1.25 s, 4.5 s | -20% | 20% | s |
| t_{UVPD} | Over-discharge detection delay time | Factory Device Configuration: 20 ms, 96 ms, 125 ms, 144 ms | -20% | 20% | ms |
| t_{OCDD} | Discharging overcurrent detection delay time | Factory Device Configuration: 8 ms, 16 ms, 20 ms, 48 ms | -20% | 20% | ms |
| t_{OCCD} | Charging overcurrent detection delay time | Factory Device Configuration: 4 ms, 6 ms, 8 ms, 16 ms | -20% | 20% | ms |
| t_{SCCD} | Short Circuit detection delay time | 250 μs (fixed) | -50% | 50% | μs |

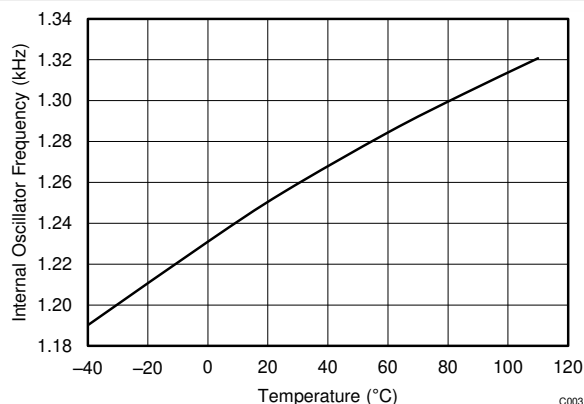
7.8 Typical Characteristics



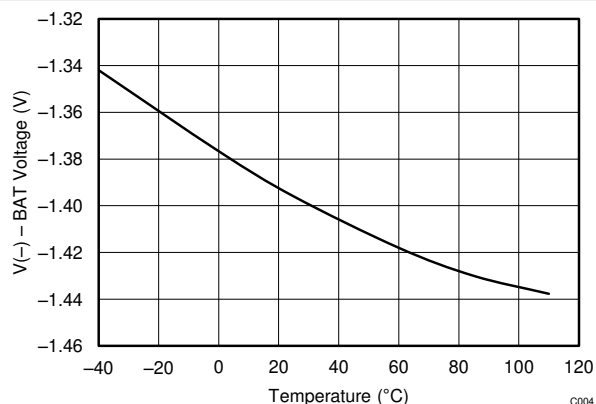
7-1. 1.5-V I_{BAT} Versus Temperature



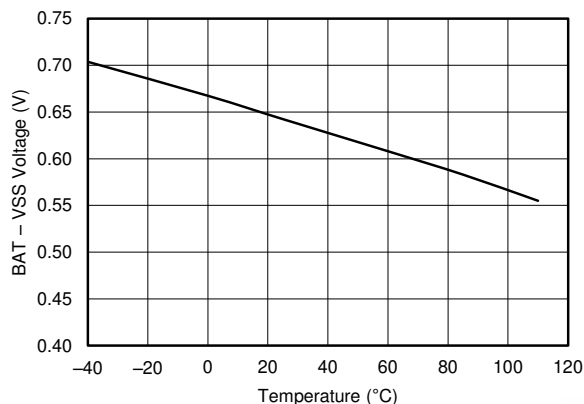
7-2. 3.9-V I_{BAT} Versus Temperature



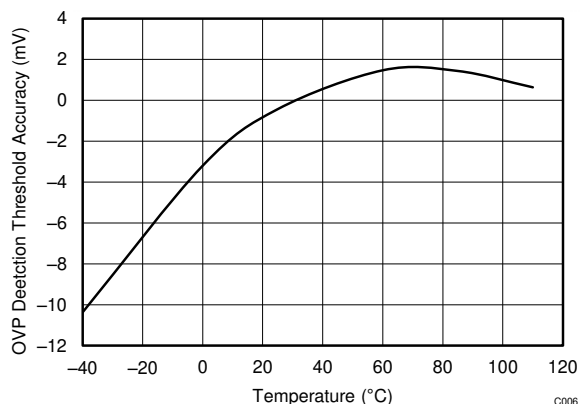
7-3. Internal Oscillator Frequency Versus Temperature



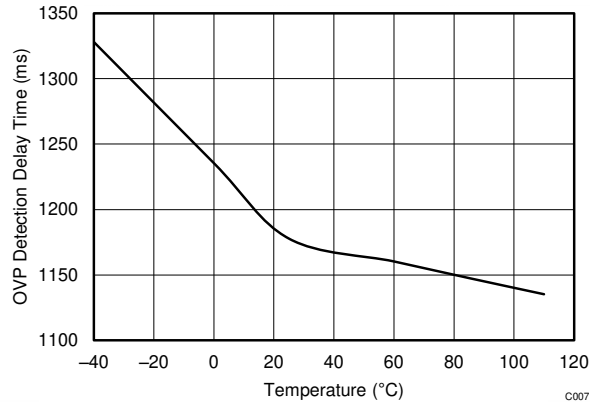
7-4. 0-V Charging Allowed Versus Temperature



7-5. 0-V Charging Disallowed Versus Temperature

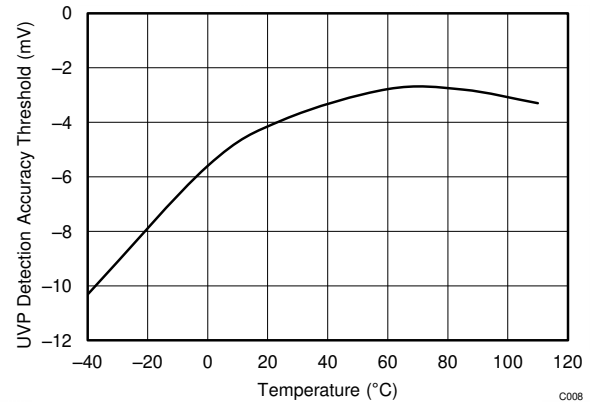


7-6. OVP Detection Accuracy Versus Temperature



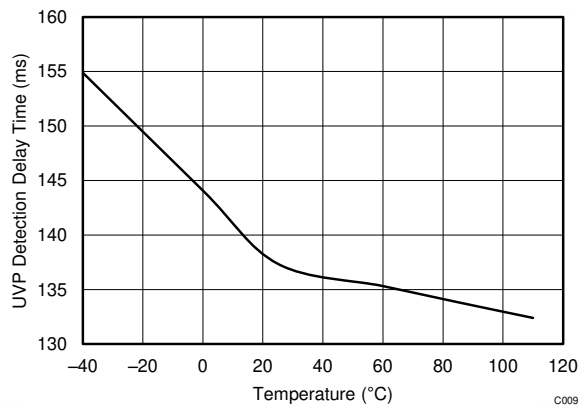
t_{OVPD} , Setting = 1.25 s

FIG 7-7. OVP Detection Delay Time Versus Temperature



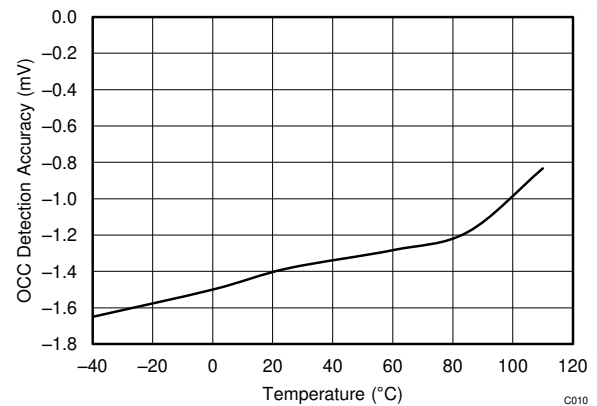
UVP, Setting = 2.800 V

FIG 7-8. UVP Detection Accuracy Versus Temperature



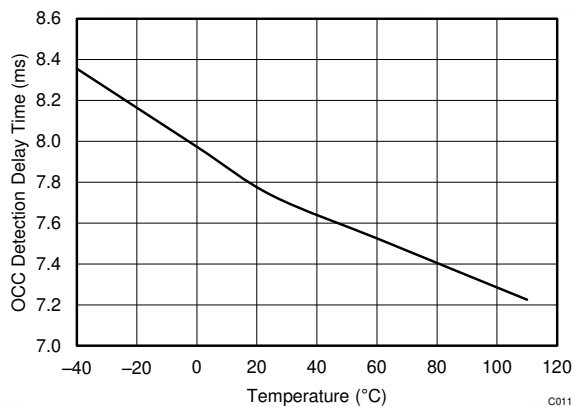
t_{UVPD} , Setting = 144 ms

FIG 7-9. UVP Detection Delay Time Versus Temperature



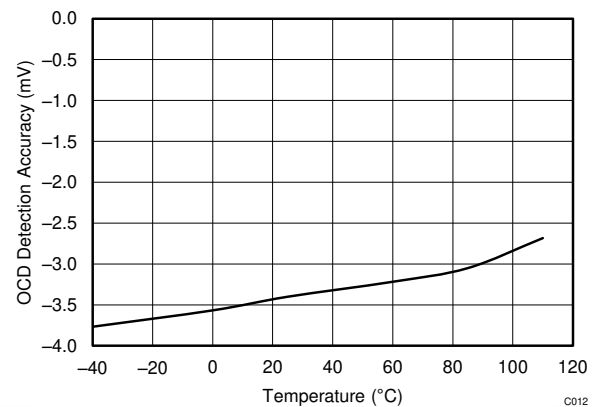
V_{OCC} , Setting = -100 mV

FIG 7-10. OCC Detection Accuracy Versus Temperature



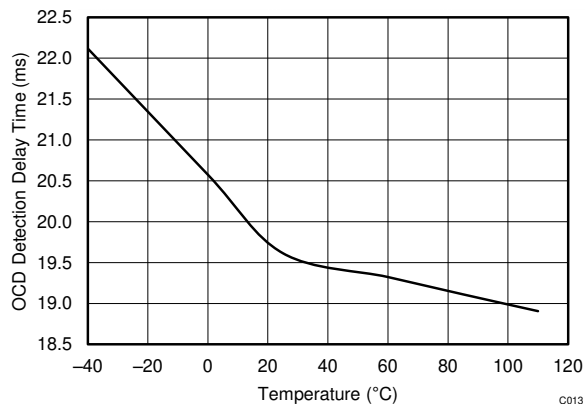
t_{OCCD} , Setting = 8 ms

FIG 7-11. OCC Detection Delay Time Versus Temperature



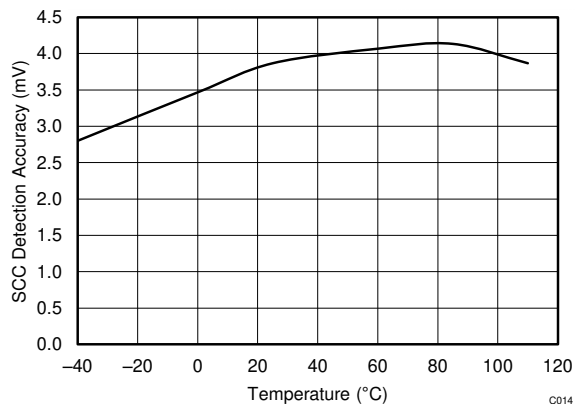
V_{OCD} , Setting = 100 mV

FIG 7-12. OCD Detection Accuracy Versus Temperature



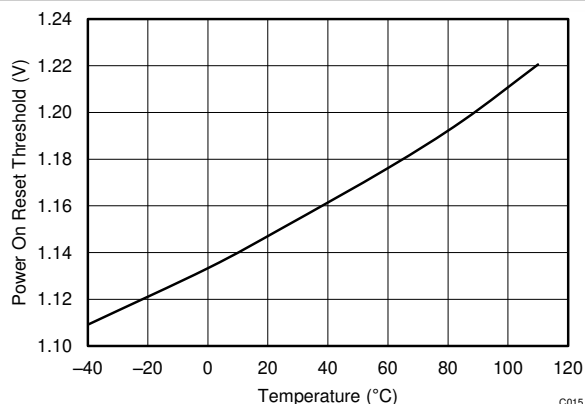
t_{UVPD} , Setting = 20 ms

7-13. OCD Detection Delay Time Versus Temperature

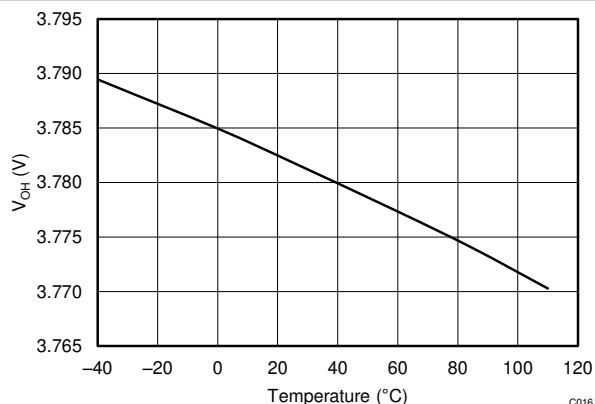


V_{SCC} , Setting = 500 mV

7-14. SCC Detection Accuracy Versus Temperature

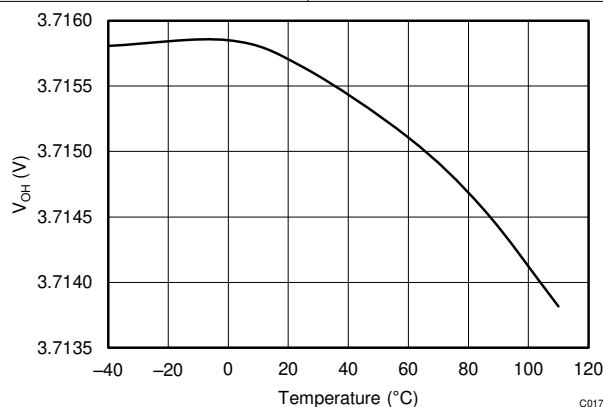


7-15. Power On Reset Versus Temperature



V_{BAT} , Setting = 3.9 V

7-16. COUT Versus Temperature with $I_{OH} = -30 \mu A$

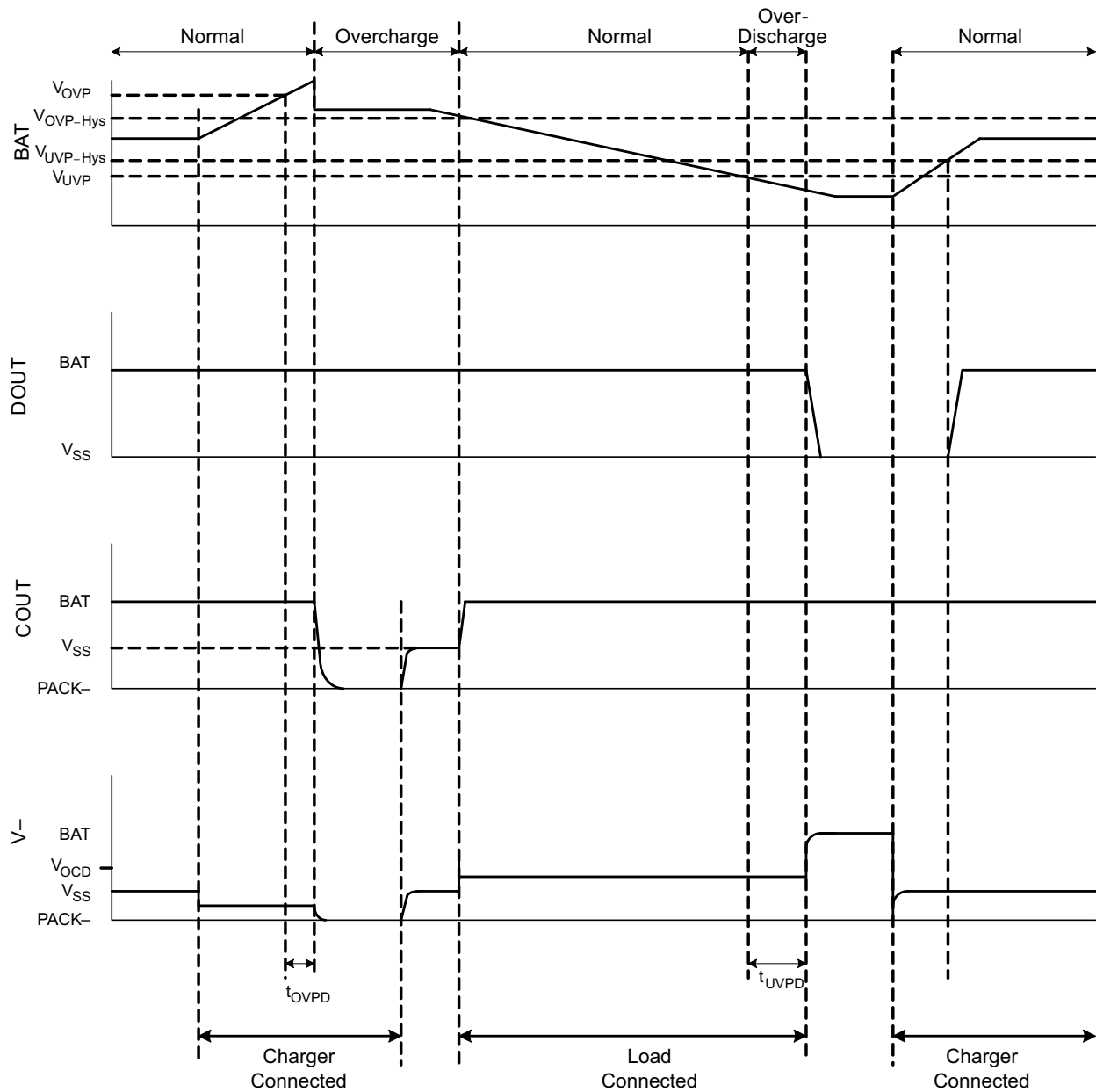


V_{BAT} , Setting = 3.9 V

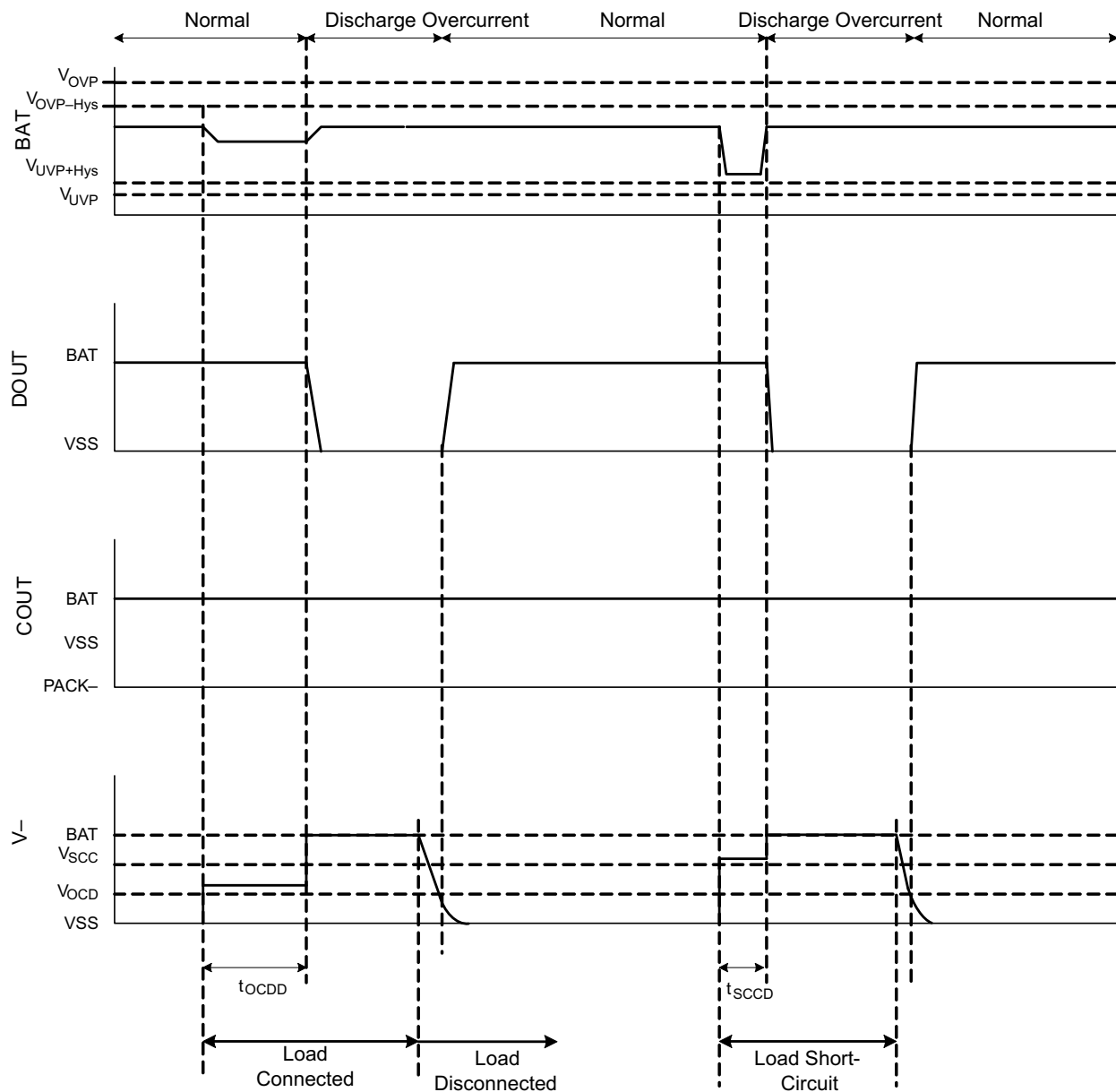
7-17. DOUT Versus Temperature with $I_{OH} = -30 \mu A$

8 Parameter Measurement Information

8.1 Timing Charts



8-1. Overcharge Detection, Over-Discharge Detection



8-2. Discharge Overcurrent Detection

8.2 Test Circuits

The following tests are referenced as follows: The COUT and DOUT outputs are “H,” which are higher than the threshold voltage of the external logic level FETs and regarded as ON state. “L” is less than the turn ON threshold for external NMOS FETs and regarded as OFF state. The COUT pin is with respect to V–, and the DOUT pin is with respect to VSS.

1. **Overcharge detection voltage and overcharge release voltage (Test Circuit 1):**

The overcharge detection voltage (V_{OVP}) is measured between the BAT and VSS pins, respectively. Once V1 is increased, the over-detection is triggered, and the delay timer expires. Then, COUT transitions from a high to low state and reduces the V1 voltage to check for the overcharge hysteresis parameter ($V_{OVP-Hys}$). The delta voltage between overcharge detection voltages (V_{OVP}) and the overcharge release occurs when the CHG FET drive output goes from low to high.

2. **Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):**

Over-discharge detection (V_{UVP}) is defined as the voltage between BAT and VSS at which the DSG drive output goes from high to low by reducing the V1 voltage. V1 is set to 3.5 V and gradually reduced while V2 is set to 0 V. The over-discharge release voltage is defined as the voltage between BAT and VSS at which the DOUT drive output transition from low to high when V1 voltage is gradually increased from a V_{UVP} condition. The overcharge hysteresis voltage is defined as the delta voltage between V_{UVP} and the instance at which the DOUT output drive goes from low to high.

3. **Discharge overcurrent detection voltage (Test Circuit 2):**

The discharge overcurrent detection voltage (V_{OCD}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{OCD} threshold with respect to VSS. This delta voltage once satisfied will trigger an internal timer t_{OCD} before the DOUT output drive transitions from high to low.

4. **Load short circuit detection voltage (Test Circuit 2):**

Load short-circuit detection voltage (V_{SCC}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{SCC} threshold with respect to VSS within 10 μ s. This delta voltage, once satisfied, triggers an internal timer t_{SCC} before the DOUT output drive transitions from high to low.

5. **Charge overcurrent detection voltage (Test Circuit 2):**

The charge overcurrent detection voltage (V_{OCC}) is measured between VSS and V– pins and triggered when the V2 voltage is increased above V_{OCC} threshold with respect to V–. This delta voltage, once satisfied, triggers an internal timer t_{OCC} before the COUT output drive transitions from high to low.

6. **Operating current consumption (Test Circuit 2):**

The operating current consumption $I_{BNORMAL}$ is the current measured going into the BAT pin under the following conditions: V1 = 3.9 V and V2 = 0 V.

7. **Power down current consumption (Test Circuit 2):**

The operating current consumption I_{Power_down} is the current measured going into the BAT pin under the following conditions: V1 = 1.5 V and V2 = 1.5 V.

8. **Resistance between V– and BAT pin (Test Circuit 3):**

Measure the resistance (R_{V_D}) between V– and BAT pins by setting the following conditions: V1 = 1.8 V and V2 = 0 V.

9. **Current sink between V– and VSS (Test Circuit 3):**

Measure the current sink I_{V_S} between V– and VSS pins by setting the following condition: V1 = 4 V.

10. **COUT current source when activated High (Test Circuit 4):**

Measure I_{COUT} current source on the COUT pin by setting the following conditions: V1 = 3.9 V, V2 = 0 V, and V3 = 3.4 V.

11. **COUT current sink when activated Low (Test Circuit 4):**

Measure I_{COUT} current sink on COUT pin by setting the following conditions: V1 = 4.5 V, V2 = 0 V, and V3 = 0.5 V.

12. **DOUT current source when activated High (Test Circuit 4):**

Measure I_{DOUT} current source on DOUT pin by setting the following conditions: $V_1 = 3.9\text{ V}$, $V_2 = 0\text{ V}$, and $V_3 = 3.4\text{ V}$.

13. DOUT current sink when activated Low (Test Circuit 4):

Measure I_{DOUT} current sink on DOUT pin by setting the following conditions: $V_1 = 2.0\text{ V}$, $V_2 = 0\text{ V}$, and $V_3 = 0.4\text{ V}$.

14. Overcharge detection delay (Test Circuit 5):

The overcharge detection delay time t_{OVPD} is the time delay before the COUT drive output transitions from high to low once the voltage on V_1 exceeds the V_{OVP} threshold. Set $V_2 = 0\text{ V}$ and then increase V_1 until BAT input exceeds the V_{OVP} threshold, then check the time for when COUT goes from high to low.

15. Over-discharge detection delay (Test Circuit 5):

The over-discharge detection delay time t_{UVPD} is the time delay before the DOUT drive output transitions from high to low once the voltage on V_1 decreases to V_{UVP} threshold. Set $V_2 = 0\text{ V}$ and then decrease V_1 until BAT input reduces to the V_{UVP} threshold, then check the time of when DOUT goes from high to low.

16. Discharge overcurrent detection delay (Test Circuit 5):

The discharge overcurrent detection delay time t_{OCDD} is the time for DOUT drive output to transition from high to low after the voltage on V_2 is increased from 0 V to 0.35 V . $V_1 = 3.5\text{ V}$ and V_2 starts from 0 V and increases to trigger threshold.

17. Load short circuit detection delay (Test Circuit 5):

The load short-circuit detection delay time t_{SCCD} is the time for DOUT drive output to transition from high to low after the voltage on V_2 is increased from 0 V to $V_1 - 1\text{ V}$. $V_1 = 3.5\text{ V}$ and V_2 starts from 0 V and increases to trigger threshold.

18. Charge overcurrent detection delay (Test Circuit 5):

The charge overcurrent detection delay time t_{OCCD} is the time for COUT drive output to transition from high to low after the voltage on V_2 is decreased from 0 V to -0.3 V . $V_1 = 3.5\text{ V}$ and V_2 starts from 0 V and decreases to trigger threshold.

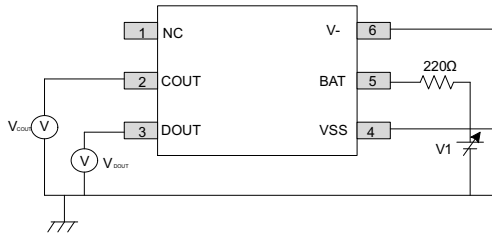
19. 0-V battery charge starting charger voltage (Test Circuit 2):

The 0-V charge for start charging voltage V_{0CHA} is defined as the voltage between BAT and V_- pins at which COUT goes high when voltage on V_2 is gradually decreased from a condition of $V_1 = V_2 = 0\text{ V}$.

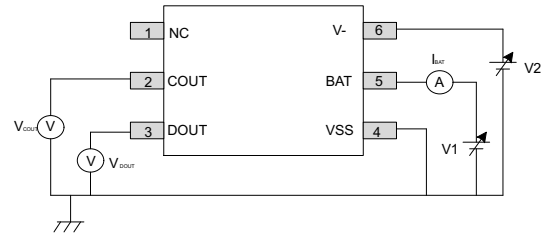
20. 0-V battery charge inhibition battery voltage (Test Circuit 2):

The 0-V charge inhibit for charger voltage V_{0INH} is defined as the voltage between BAT and VSS pins at which COUT should go low as V_1 is gradually decreased from $V_1 = 2\text{ V}$ and $V_2 = -4\text{ V}$.

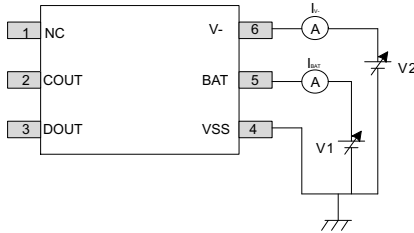
8.3 Test Circuit Diagrams



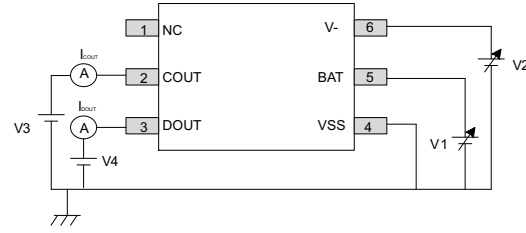
8-3. Test Circuit 1



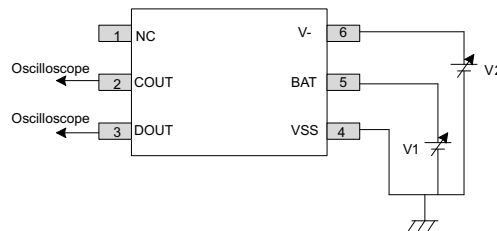
8-4. Test Circuit 2



8-5. Test Circuit 3



8-6. Test Circuit 4



8-7. Test Circuit 5

9 Detailed Description

9.1 Overview

This BQ2970 device is a primary protector for a single-cell Li-ion/Li-polymer battery pack. The device uses a minimum number of external components to protect for overcurrent conditions due to high discharge/charge currents in the application. In addition, it monitors and helps to protect against battery pack overcharging or depletion of energy in the pack. The BQ2970 device is capable of having an input voltage of 8 V from a charging adapter and can tolerate a voltage of BAT – 25 V across the two input pins. In the condition when a fault is triggered, there are timer delays before the appropriate action is taken to turn OFF either the CHG or DSG FETs. The recovery period also has a timer delay once the threshold for recovery condition is satisfied. These parameters are fixed once they are programmed. There is also a feature called zero voltage charging that enables depleted cells to be charged to an acceptable level before the battery pack can be used for normal operation. Zero voltage charging is allowed if the charger voltage is above 1.7 V. For Factory Programmable Options, see 表 9-1.

表 9-1. Factory Programmable Options

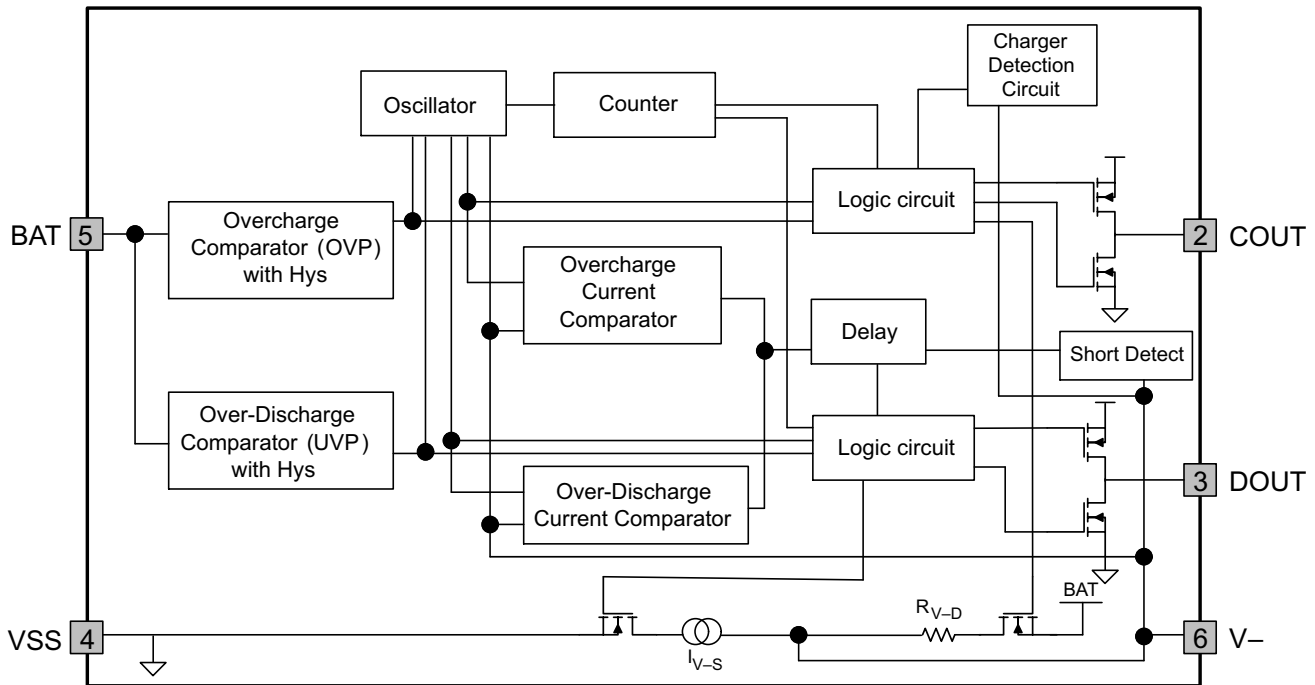
| PARAMETER | | FACTORY DEVICE CONFIGURATION |
|-------------------|---|---------------------------------|
| V _{OVP} | Overcharge detection voltage | 3.85 V to 4.60 V in 50-mV steps |
| V _{UVP} | Over-discharge detection voltage | 2.00 V to 2.80 V in 50-mV steps |
| V _{OCD} | Discharging overcurrent detection voltage | 90 mV to 200 mV in 5-mV steps |
| V _{OCC} | Charging overcurrent detection voltage | –45 mV to –155 mV in 5-mV steps |
| V _{SCC} | Short Circuit detection voltage | 300 mV, 400 mV, 500 mV, 600 mV |
| t _{OVPD} | Overcharge detection delay time | 0.25 s, 1.00 s, 1.25 s, 4.50 s |
| t _{UVPD} | Over-discharge detection delay time | 20 ms, 96 ms, 125 ms, 144 ms |

表 9-1. Factory Programmable Options (continued)

| PARAMETER | | FACTORY DEVICE CONFIGURATION |
|------------|--|------------------------------|
| t_{OCDD} | Discharging overcurrent detection delay time | 8 ms, 16 ms, 20 ms, 48 ms |
| t_{OCCD} | Charging overcurrent detection delay time | 4 ms, 6 ms, 8 ms, 16 ms |
| t_{SCD} | Short Circuit detection delay time | 250 μ s (fixed) |

For available released devices, see the [Released Device Configurations](#) table.

9.2 Functional Block Diagram



9.3 Feature Description

The BQ2970 family of devices measures voltage drops across several input pins for monitoring and detection of the following faults: OCC, OCD, OVP, and UVP. An internal oscillator initiates a timer to the fixed delays associated with each parameter once the fault is triggered. Once the timer expires due to a fault condition, the appropriate FET drive output (COUT or DOUT) is activated to turn OFF the external FET. The same method is applicable for the recovery feature once the system fault is removed and the recovery parameter is satisfied, then the recovery timer is initiated. If there are no reoccurrences of this fault during this period, the appropriate gate drive is activated to turn ON the appropriate external FET.

9.4 Device Functional Modes

9.4.1 Normal Operation

This device monitors the voltage of the battery connected between BAT pin and VSS pin and the differential voltage between V- pin and VSS pin to control charging and discharging. The system is operating in NORMAL mode when the battery voltage range is between the over-discharge detection threshold (V_{UVP}) and the overcharge detection threshold (V_{OVP}), and the V- pin voltage is within the range for charge overcurrent threshold (V_{OCC}) to over-discharge current threshold (V_{OCD}) when measured with respect to VSS. If these conditions are satisfied, the device turns ON the drive for COUT and DOUT FET control.

CAUTION

When the battery is connected for the first time, the discharging circuit might not be enabled. In this case, short the V– pin to the VSS pin.

Alternatively, connect the charger between the Pack+ and Pack– terminals in the system.

9.4.2 Overcharge Status

This mode is detected when the battery voltage measured is higher than the overcharge detection threshold (V_{OVP}) during charging. If this condition exists for a period greater than the overcharge detection delay (t_{OVPD}) or longer, the COUT output signal is driven low to turn OFF the charging FET to prevent any further charging of the battery.

The overcharge condition is released if one of the following conditions occurs:

- If the V– pin is higher than the overcharge detection voltage (V_{OCC_Min}), the device releases the overcharge status when the battery voltage drops below the overcharge release voltage ($V_{OVP-Hys}$).
- If the V– pin is higher than or equal to the over-discharge detection voltage (V_{OCD}), the device releases the overcharge status when the battery voltage drops below the overcharge detection voltage (V_{OVP}).

The discharge is initiated by connecting a load after the overcharge detection. The V– pin rises to a voltage greater than VSS due to the parasitic diode of the charge FET conducting to support the load. If the V– pin voltage is higher than or equal to the discharge overcurrent detection threshold (V_{OCD}), the overcurrent condition status is released only if the battery voltage drops lower than or equal to the overcharge detection voltage (V_{OVP}).

CAUTION

1. If the battery is overcharged to a level greater than overcharge detection (V_{OVP}) and the battery voltage does *not* drop below the overcharge detection voltage (V_{OVP}) with a heavy load connected, the discharge overcurrent and load short-circuit detection features do *not* function until the battery voltage drops below the overcharge detection voltage (V_{OVP}). The internal impedance of a battery is in the order of tens of mΩ, so application of a heavy load on the output should allow the battery voltage to drop immediately, enabling discharge overcurrent detection and load short-circuit detection features after an overcharge release delay.
2. When a charger is connected after an overcharge detection, the overcharge status does *not* release even if the battery voltage drops below the overcharge release threshold. The overcharge status is released when the V– pin voltage exceeds the overcurrent detection voltage (V_{OCD}) by removing the charger.

9.4.3 Over-Discharge Status

If the battery voltage drops below the over-discharge detection voltage (V_{UVP}) for a time greater than (t_{UVPD}) the discharge control output, DOUT is switched to a low state and the discharge FET is turned OFF to prevent further discharging of the battery. This is referred to as an over-discharge detection status. In this condition, the V– pin is internally pulled up to BAT by the resistor R_{V-D} . When this occurs, the voltage difference between V– and BAT pins is 1.3 V or lower, and the current consumption of the device is reduced to power-down level $I_{STANDBY}$. The current sink I_{V-S} is not active in power-down state or over-discharge state. The power-down state is released when a charger is connected and the voltage delta between V– and BAT pins is greater than 1.3 V.

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is lower than – 0.7 V, the device releases the over-discharge state and allows the DOUT pin to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection voltage (V_{UVP}).

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is higher than – 0.7 V, the device releases the over-discharge state and allows the DOUT pin to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection release hysteresis voltage ($V_{UVP+Hys}$).

9.4.4 Discharge Overcurrent Status (Discharge Overcurrent, Load Short-Circuit)

When a battery is in normal operation and the V₋ pin is equal to or higher than the discharge overcurrent threshold for a time greater than the discharge overcurrent detection delay, the DOUT pin is pulled low to turn OFF the discharge FET and prevent further discharge of the battery. This is known as the discharge overcurrent status. In the discharge overcurrent status, the V₋ and VSS pins are connected by a constant current sink I_{V-S}. When this occurs and a load is connected, the V₋ pin is at BAT potential. If the load is disconnected, the V₋ pin goes to VSS (BAT/2) potential.

This device detects the status when the impedance between Pack+ and Pack- (see [Figure 26](#)) increases and is equal to the impedance that enables the voltage at the V₋ pin to return to BAT – 1 V or lower. The discharge overcurrent status is restored to the normal status.

Alternatively, by connecting the charger to the system, the device returns to normal status from discharge overcurrent detection status, because the voltage at the V₋ pin drops to BAT – 1 V or lower.

The resistance R_{V-D} between V₋ and BAT is not connected in the discharge overcurrent detection status.

9.4.5 Charge Overcurrent Status

When a battery is in normal operation status and the voltage at V₋ pin is lower than the charge overcurrent detection due to high charge current for a time greater than charge overcurrent detection delay, the COUT pin is pulled low to turn OFF the charge FET and prevent further charging to continue. This is known as charge overcurrent status.

The device is restored to normal status from charge overcurrent status when the voltage at the V₋ pin returns to charge overcurrent detection voltage or higher by removing the charger from the system.

The charge overcurrent detection feature does *not* work in the over-discharge status.

The resistance R_{V-D} between V₋ and BAT and the current sink I_{V-S} is not connected in the charge overcurrent status.

9.4.6 0-V Charging Function Enabled

This feature enables recharging a connected battery that has very low voltage due to self-discharge. When the charger applies a voltage greater than or equal to V_{0CHG} to Pack+ and Pack- connections, the COUT pin gate drive is fixed by the BAT pin voltage.

Once the voltage between the gate and the source of the charging FET becomes equal to or greater than the turn ON voltage due to the charger voltage, the charging FET is ON and the battery is charged with current flow through the charging FET and the internal parasitic diode of the discharging FET. Once the battery voltage is equal to or higher than the over-discharge release voltage, the device enters normal status.

CAUTION

1. Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the 0-V battery charger function.
2. The 0-V battery charge feature has a higher priority than the charge overcurrent detection function. In this case, the 0-V charging will be allowed and the battery charges forcibly, which results in charge overcurrent detection being disabled if the battery voltage is lower than the over-discharge detection voltage.

9.4.7 0-V Charging Inhibit Function

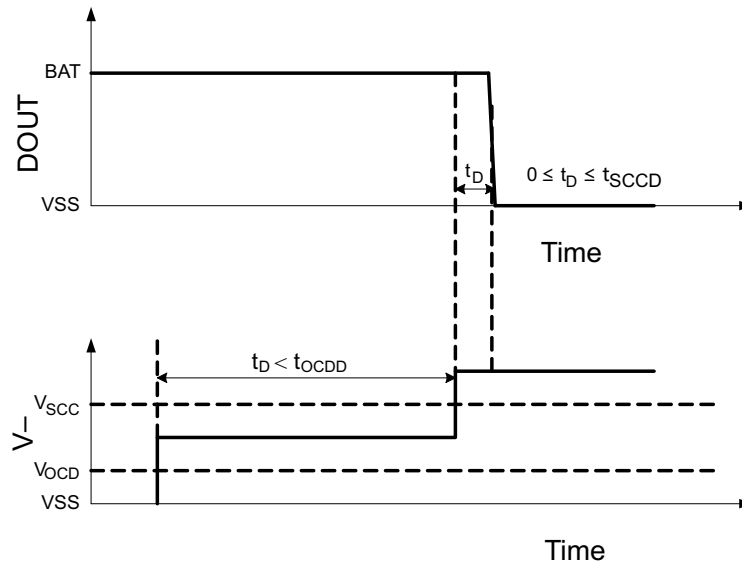
This feature inhibits recharging a battery that has an internal short circuit of a 0-V battery. If the battery voltage is below the charge inhibit voltage V_{0INH} or lower, the charge FET control gate is fixed to the Pack- voltage to inhibit charging. When the battery is equal to V_{0INH} or higher, charging can be performed. The 0-V charge inhibit function is available in all configurations of the BQ297xx device.

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to enable or inhibit the 0-V battery charger function.

9.4.8 Delay Circuit

The detection delay timers are based from an internal clock with a frequency of 10 kHz.



9-1. Delay Circuit

If the over-discharge current is detected, but remains below the over-discharge short circuit detection threshold, the over-discharge detection conditions must be valid for a time greater than or equal to over-discharge current delay t_{OCDD} time before the **DOUT** goes low to turn OFF the discharge FET. However, during any time the discharge overcurrent detection exceeds the short circuit detection threshold for a time greater than or equal to load circuit detection delay t_{SCCD} , the **DOUT** pin goes low in a faster delay for protection.

10 Application and Implementation

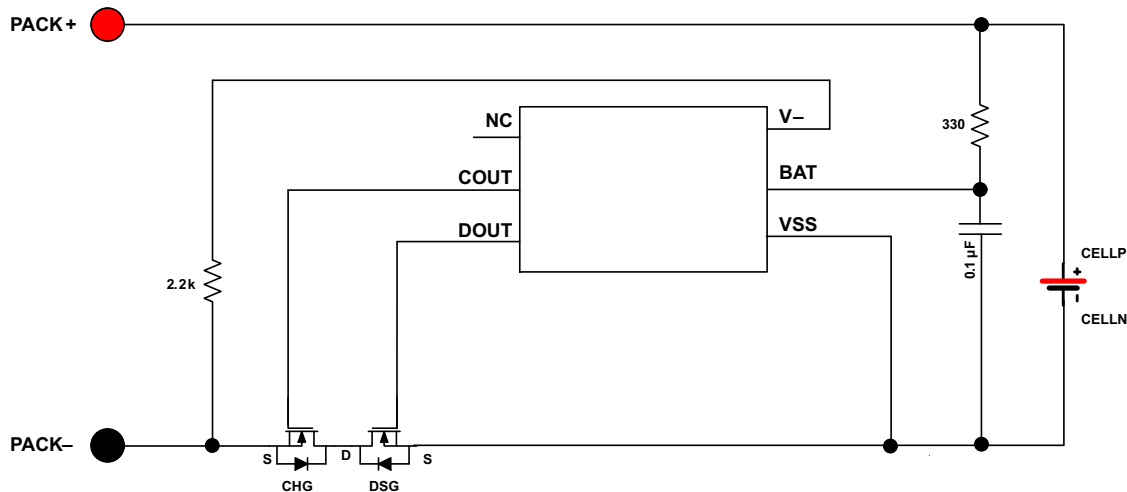
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The BQ2970 devices are a family of primary protectors used for protection of the battery pack in the application. The application drives two low-side NMOS FETs that are controlled to provide energy to the system loads or interrupt the power in the event of a fault condition.

10.2 Typical Application



The 5-M resistor for an external gate-source is optional.

Figure 10-1. Typical Application Schematic, BQ2970

10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 10-1](#).

Table 10-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE at T _A = 25°C |
|---|--|
| Input voltage range | 4.5 V to 7 V |
| Maximum operating discharge current | 7 A |
| Maximum Charge Current for battery pack | 4.5 A |
| Overvoltage Protection (OVP) | 4.275 V |
| Overvoltage detection delay timer | 1.2 s |
| Overvoltage Protection (OVP) release voltage | 4.175 V |
| Undervoltage Protection (UVP) | 2.8 V |
| Undervoltage detection delay timer | 150 ms |
| Undervoltage Protection (UVP) release voltage | 2.9 V |
| Charge Overcurrent detection (OCC) voltage | -70 mV |
| Charge Overcurrent Detection (OCC) delay timer | 9 ms |
| Discharge Overcurrent Detection (OCD) voltage | 100 mV |
| Discharge Overcurrent Detection (OCD) delay timer | 18 ms |

表 10-1. Design Parameters (continued)

| DESIGN PARAMETER | EXAMPLE VALUE at T _A = 25°C |
|---|--|
| Load Short Circuit Detection (SCC) voltage, BAT to –V ≤ threshold | 500 mV |
| Load Short Circuit Detection (SCC) delay timer | 250 μs |
| Load Short Circuit release voltage, BAT to –V ≥ Threshold | 1 V |

10.2.2 Detailed Design Procedure

Note

The external FET selection is important to ensure the battery pack protection is sufficient and complies to the requirements of the system.

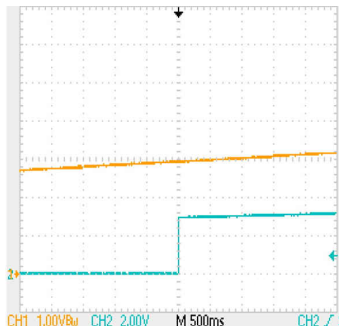
- FET Selection: Because the maximum desired discharge current is 7 A, ensure that the Discharge Overcurrent circuit does *not* trigger until the discharge current is above this value.
- The total resistance tolerated across the two external FETs (CHG + DSG) should be 100 mV/7 A = 14.3 mΩ.
- Based on the information of the total ON resistance of the two switches, determine what would be the Charge Overcurrent Detection threshold, 14.3 mΩ × 4.5 A = 65 mV. Selecting a device with a 70-mV trigger threshold for Charge Overcurrent trigger is acceptable.
- The total R_{ds} ON should factor in any worst-case parameter based on the FET ON resistance, de-rating due to temperature effects and minimum required operation, and the associated gate drive (V_{gs}). Therefore, the FET choice should meet the following criteria:

$$V_{dss} = 25 \text{ V}$$

$$\text{Each FET } R_{ds} \text{ ON} = 7.5 \text{ m}\Omega \text{ at } T_j = 25^\circ\text{C and } V_{gs} = 3.5 \text{ V}$$

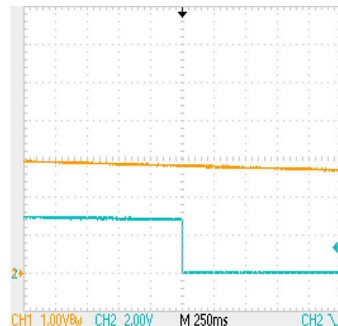
- I_{max} > 50 A to allow for short Circuit Current condition for 350 μs (max delay timer). The only limiting factor during this condition is Pack Voltage/(Cell Resistance + (2 × FET_R_{ds}ON) + Trace Resistance).
- Use the CSD16406Q3 FET for the application.
- An RC filter is required on the BAT for noise, and enables the device to operate during sharp negative transients. The 330-Ω resistor also limits the current during a reverse connection on the system.
- TI recommends placing a high impedance 5-MΩ across the gate source of each external FET to deplete any charge on the gate-source capacitance.

10.2.3 Application Performance Plots



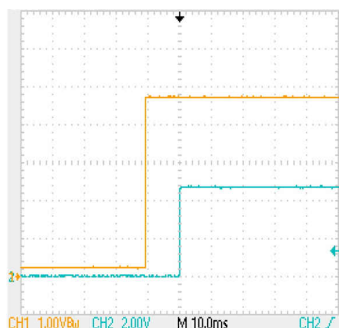
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = DOUT Gate Drive Output
DOUT goes from low to high when UVP Recovery = UVP Set Threshold + 100 mV

10-2. UVP Recovery



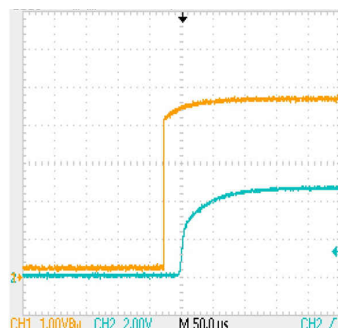
Orange Line (Channel 1) = Power Down Ramp on BAT Pin
Turquoise Line (Channel 2) = DOUT Gate Drive Output
DOUT goes from high to low when UVP threshold = UVP set Threshold + set delay time

10-3. UVP Set Condition



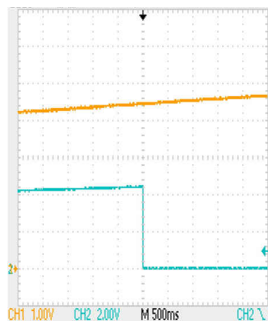
Orange Line (Channel 1) = Power Up Ramp on BAT pin
Turquoise Line (Channel 2) = DOUT Gate Drive Output

10-4. Initial Power Up, DOUT



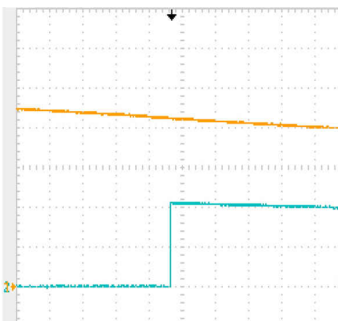
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output

10-5. Initial Power Up, COUT



Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from high to low when OVP threshold = OVP set Threshold + set delay time

10-6. OVP Set Condition



Orange Line (Channel 1) = Decrease Voltage on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from low to high when OVP Recovery = OVP Set Threshold - 100 mV

10-7. OVP Recovery Condition

11 Power Supply Recommendations

The recommended power supply for this device is a maximum 8-V operation on the BAT input pin.

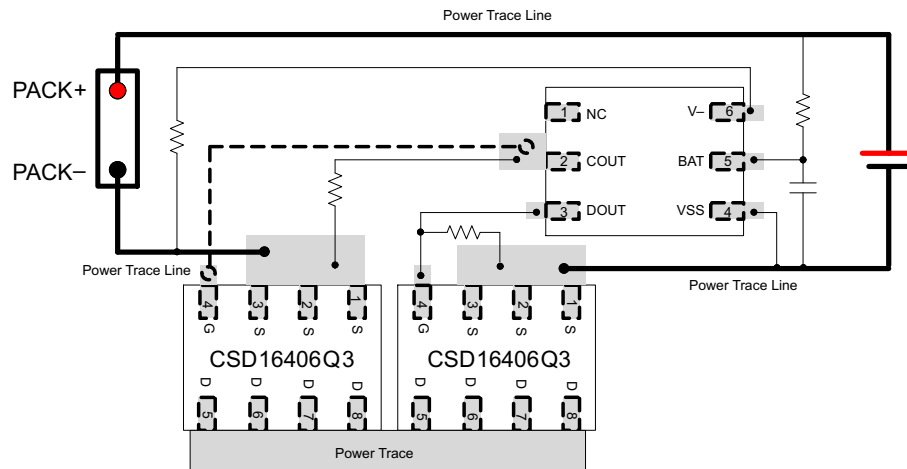
12 Layout

12.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the external power FETs are adequately compensated for heat dissipation with sufficient thermal heat spreader based on worst-case power delivery.
2. The connection between the two external power FETs should be very close to ensure there is not an additional drop for fault sensing.
3. The input RC filter on the BAT pin should be close to the terminal of the IC.

12.2 Layout Example



↻ Via connects between two layers

12-1. BQ2970 Board Layout

13 Device and Documentation Support

13.1 Related Documentation

[BQ29700 Single-Cell Li-Ion Protector EVM User's Guide \(SLUUAZ3\)](#)

13.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ29700DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FA | Samples |
| BQ29700DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FA | Samples |
| BQ29701DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FY | Samples |
| BQ29701DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FY | Samples |
| BQ29702DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FZ | Samples |
| BQ29702DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FZ | Samples |
| BQ29703DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F1 | Samples |
| BQ29703DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F1 | Samples |
| BQ29704DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2 | Samples |
| BQ29704DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2 | Samples |
| BQ29705DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F3 | Samples |
| BQ29705DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F3 | Samples |
| BQ29706DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F4 | Samples |
| BQ29706DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F4 | Samples |
| BQ29707DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F5 | Samples |
| BQ29707DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F5 | Samples |
| BQ29716DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3P | Samples |
| BQ29716DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3P | Samples |
| BQ29717DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3Q | Samples |
| BQ29717DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3Q | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ29718DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3R | Samples |
| BQ29718DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3R | Samples |
| BQ29723DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3S | Samples |
| BQ29723DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3S | Samples |
| BQ29728DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EJ | Samples |
| BQ29728DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EJ | Samples |
| BQ29729DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3T | Samples |
| BQ29729DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3T | Samples |
| BQ29732DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3U | Samples |
| BQ29732DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3U | Samples |
| BQ29733DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4Q | Samples |
| BQ29733DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 4Q | Samples |
| BQ29737DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EI | Samples |
| BQ29737DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

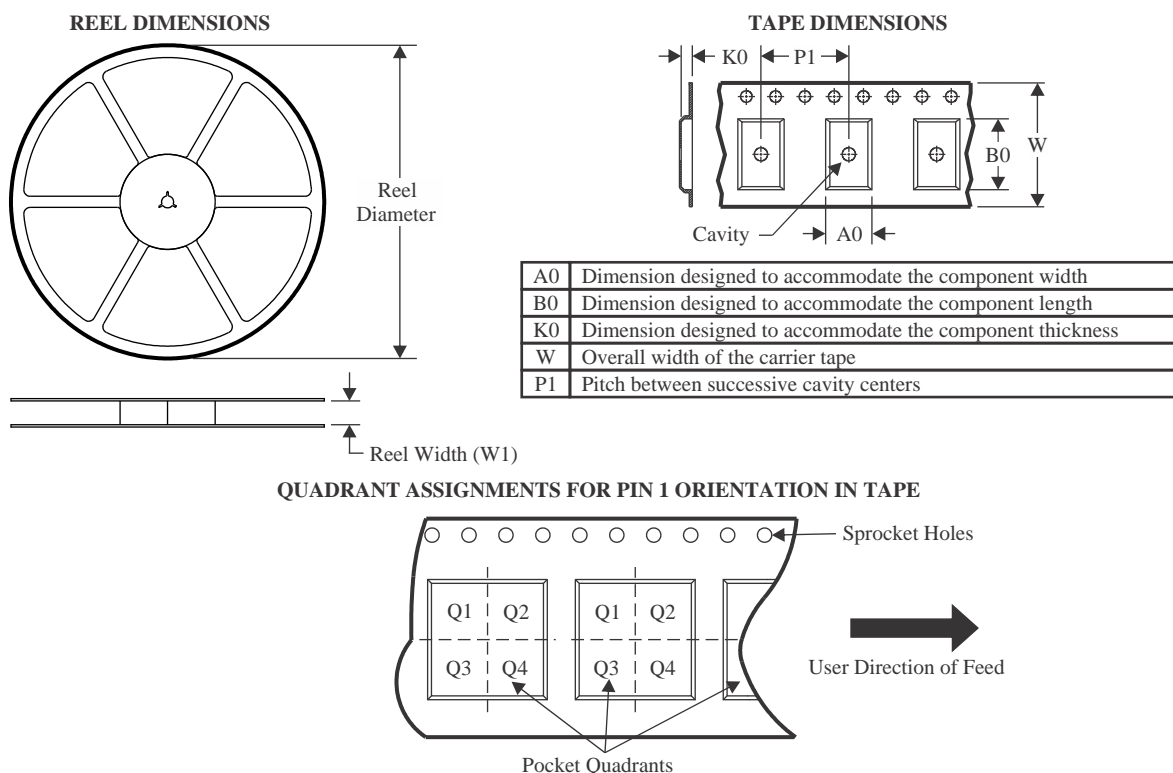
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ29700DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29700DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29700DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29701DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29701DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29701DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29701DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29702DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29702DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29703DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29703DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29704DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29704DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29705DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29705DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29706DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ29706DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29707DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29707DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29707DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29707DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29716DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29716DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29717DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29717DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29717DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29717DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29718DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29718DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29718DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29718DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29723DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29723DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29723DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29723DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29728DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29728DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29729DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29729DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29729DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29729DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29732DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29732DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29733DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29733DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29737DSER | WSO | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| BQ29737DSET | WSO | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

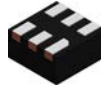


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ29700DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29700DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29700DSET | WSN | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29701DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29701DSER | WSN | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29701DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29701DSET | WSN | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29702DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29702DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29703DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29703DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29704DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29704DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29705DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29705DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29706DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29706DSET | WSN | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29707DSER | WSN | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |

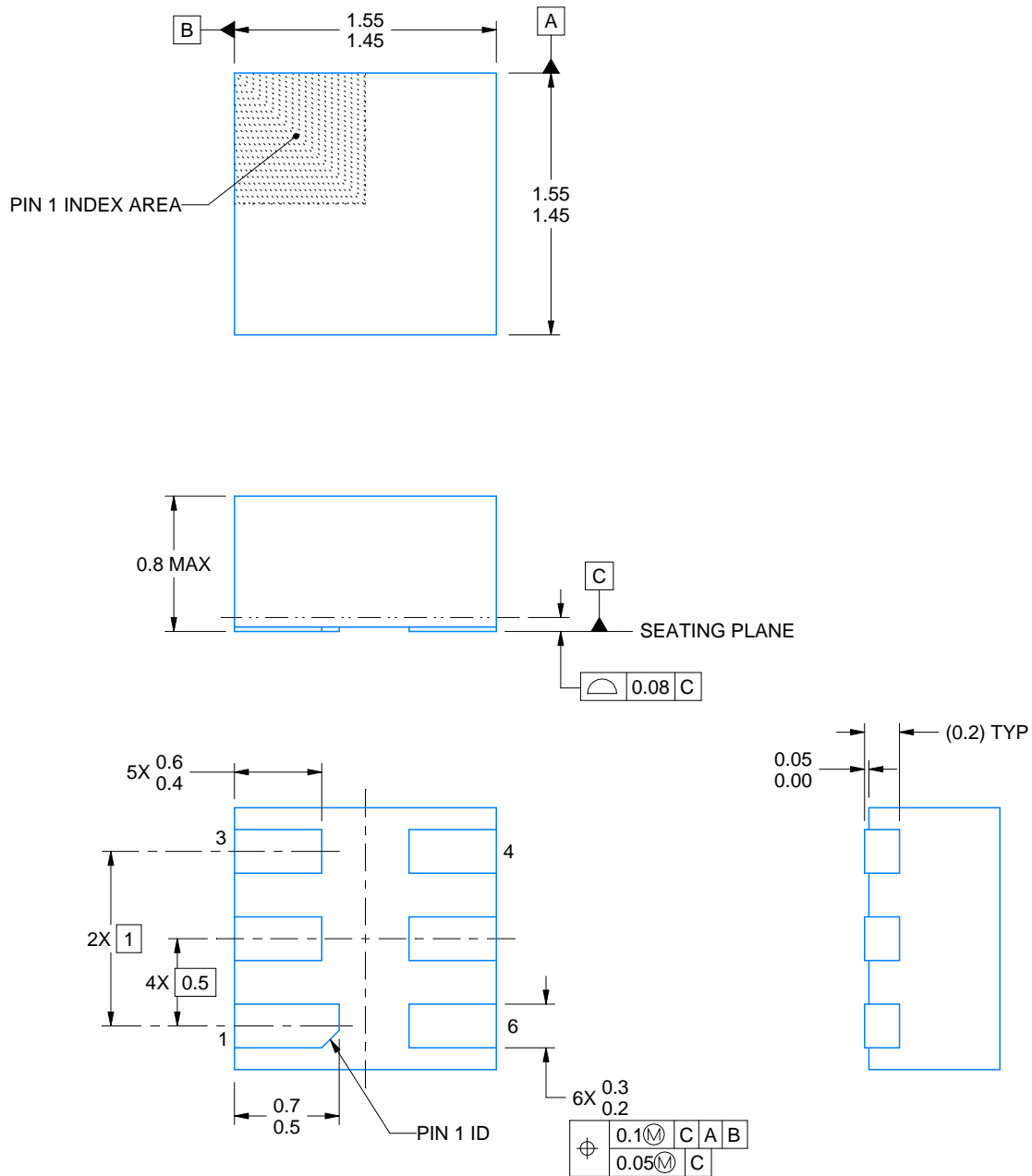
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ29707DSER | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29707DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29707DSET | WSON | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29716DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29716DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29717DSER | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29717DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29717DSET | WSON | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29717DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29718DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29718DSER | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29718DSET | WSON | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29718DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29723DSER | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29723DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29723DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29723DSET | WSON | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29728DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29728DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29729DSER | WSON | DSE | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ29729DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29729DSET | WSON | DSE | 6 | 250 | 210.0 | 185.0 | 35.0 |
| BQ29729DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29732DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29732DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29733DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29733DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| BQ29737DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| BQ29737DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |

DSE0006A



PACKAGE OUTLINE
WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

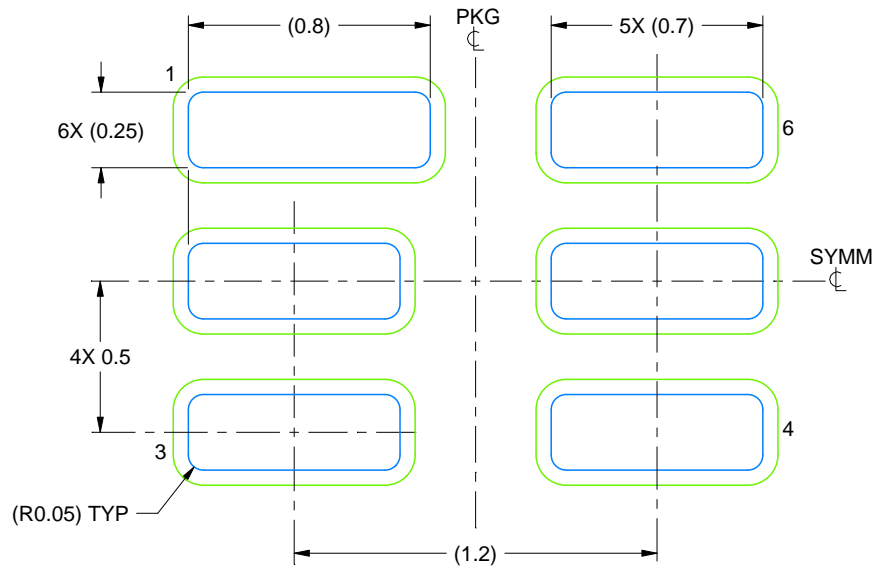
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

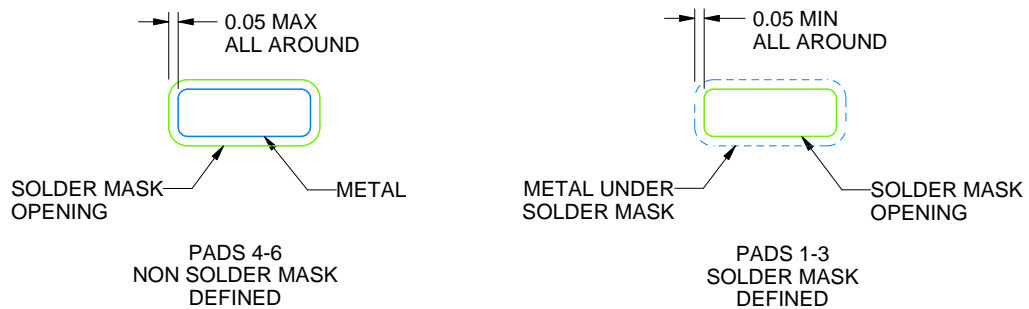
DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

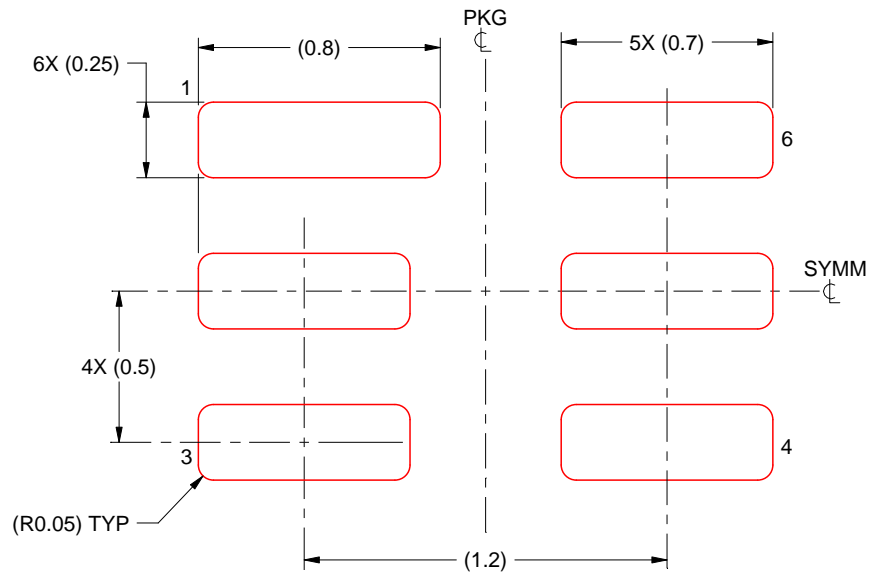
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated