

CDx4HC4075 トリプル 3 入力 OR ゲート

1 特長

- バッファ付き入力
- 広い動作電圧範囲: 2V~6V
- 広い動作温度範囲: -55°C~+125°C
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

2 アプリケーション

- 少ない入力によりエラー信号を監視
- アクティブ Low のイネーブル信号の結合

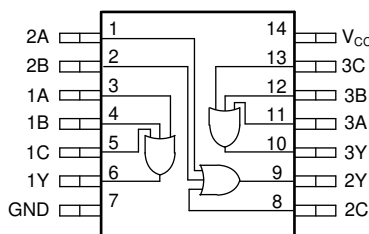
3 概要

このデバイスには、3 つの独立した 3 入力 OR ゲートが内蔵されています。各ゲートはブール関数 $Y = A + B + C$ を正論理で実行します。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
CD74HC4075M	SOIC (14)	8.70mm × 3.90mm
CD74HC4075E	PDIP (14)	19.30mm × 6.40mm
CD74HC4075NS	SO (14)	10.20mm × 5.30mm
CD74HC4075PW	TSSOP (14)	5.00mm × 4.40mm
CD54HC4075F	CDIP (14)	21.30mm × 7.60mm
CD54HC4075FK	LCCC (20)	8.90mm × 8.90mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能とピン配置



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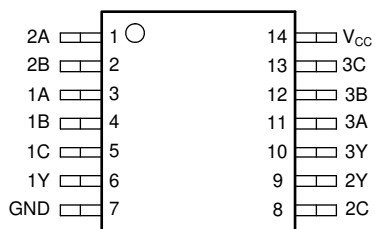
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4 Revision History

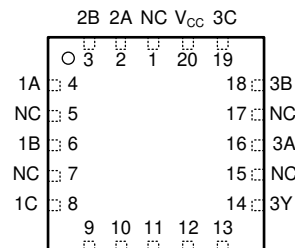
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (June 2006) to Revision H (June 2021)	Page
• 新しいデータシート標準に更新.....	1
• HCT デバイスをスタンドアロンのデータシート (SCHS408) へ移動.....	1
• R _{θJA} increased for the D (86 to 133.6 °C/W), PW (133 to 151.7 °C/W), and NS (76 to 122.6 °C/W) packages and decreased for the N package (80 to 61.3 °C/W).....	5

5 Pin Configuration and Functions



D, N, NS, PW, or J Package
14-Pin SOIC, PDIP, SO, TSSOP, or CDIP
Top View



FK Package
20-Pin LCCC
Top View

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, N, NS, PW, or J	FK		
2A	1	2	Input	Channel 2, Input A
2B	2	3	Input	Channel 2, Input B
1A	3	4	Input	Channel 1, Input A
1B	4	6	Input	Channel 1, Input B
1C	5	8	Input	Channel 1, Input C
1Y	6	9	Output	Channel 1, Output Y
GND	7	10	—	Ground
2C	8	12	Input	Channel 2, Input C
2Y	9	13	Output	Channel 2, Output Y
3Y	10	14	Output	Channel 3, Output Y
3A	11	16	Input	Channel 3, Input A
3B	12	18	Input	Channel 3, Input B
3C	13	19	Input	Channel 3, Input C
V _{CC}	14	20	—	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		±20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature ⁽³⁾	Plastic package		150	°C
		Hermetic package or die		175	°C
	Lead temperature (soldering 10s)	SOIC - lead tips only		300	°C
T_{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
CD74HC4075 IN D (SOIC) AND N (PDIP) PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 6\text{ V}$	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 6\text{ V}$			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition time	$V_{CC} = 2\text{ V}$			1000	ns
		$V_{CC} = 4.5\text{ V}$			500	
		$V_{CC} = 6\text{ V}$			400	
T_A	Operating free-air temperature	CD74HC4075	−55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD74HC4075				UNIT
		PW (TSSOP)	N (PDIP)	D (SOIC)	NS (SOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	61.3	133.6	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	49.0	89.0	81.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	41.0	89.5	83.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	28.7	45.5	45.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	40.8	89.1	83.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

Operating free-air temperature (T _A)														UNIT	
PARAMETER		TEST CONDITIONS		V _{CC}	25°C			–40°C to 85°C			–55°C to 125°C				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V _{OH}	High-level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	2 V	1.9			1.9			1.9			V	
				4.5 V	4.4			4.4			4.4				
				6 V	5.9			5.9			5.9				
			I _{OH} = –4 mA	4.5 V	3.98			3.84			3.7				
				I _{OH} = –5.2 mA	6 V	5.48			5.34			5.2			
V _{OL}	Low-level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V				0.1			0.1			V	
				4.5 V				0.1			0.1				
				6 V				0.1			0.1				
			I _{OL} = 4 mA	4.5 V				0.26			0.33				0.4
				I _{OL} = 5.2 mA	6 V				0.26			0.33			
I _I	Input leakage current	V _I = V _{CC} or 0		6 V				±0.1			±1			μA	
I _{CC}	Supply current	V _I = V _{CC} or 0	I _O = 0	6 V				2			20			μA	
C _i	Input capacitance			5 V				10			10			pF	

6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		FROM	TO	TEST CONDITIO NS	V _{CC}	Operating free-air temperature (T _A)									UNIT
						25°C			–40°C to 85°C			–55°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	Propagation delay	A, B, or C	Y	C _L = 50 pF	2 V	100			125			150			ns
					4.5 V	20			25			30			
					6 V	17			21			26			
		A, B, or C	Y	C _L = 15 pF	5 V	8									

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		FROM	TO	TEST CONDITIO NS	V _{CC}	Operating free-air temperature (T _A)									UNIT
						25°C			−40°C to 85°C			−55°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _t	Transition-time		Y	C _L = 50 pF	2 V	75			95			110			ns
					4.5 V	15			19			22			
					6 V	13			16			19			

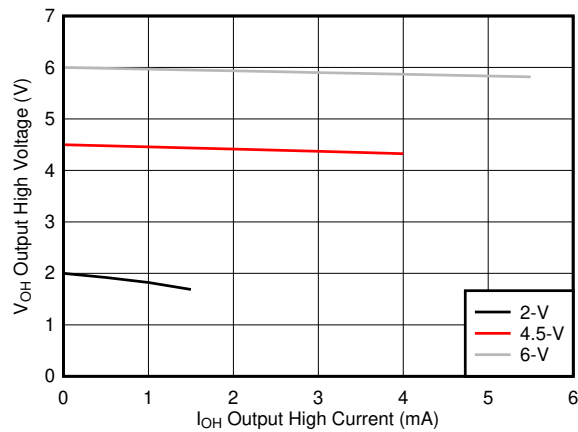
6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

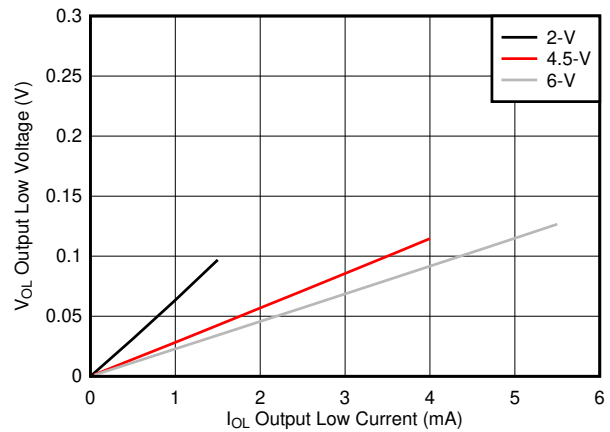
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		26		pF

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$



6-1. Typical output voltage in the high state (V_{OH})



6-2. Typical output voltage in the low state (V_{OL})

7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.



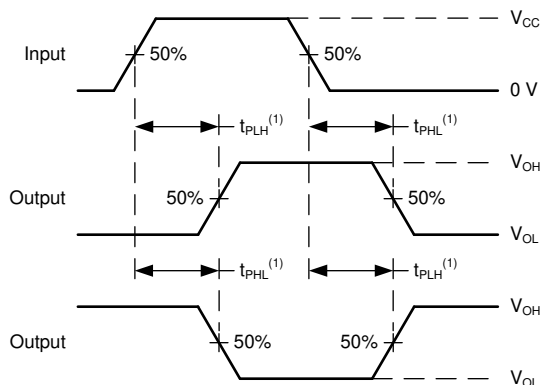
A. $C_L = 50 \text{ pF}$ and includes probe and jig capacitance.

FIG 7-1. Load Circuit



A. t_t is the greater of t_r and t_f .

FIG 7-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

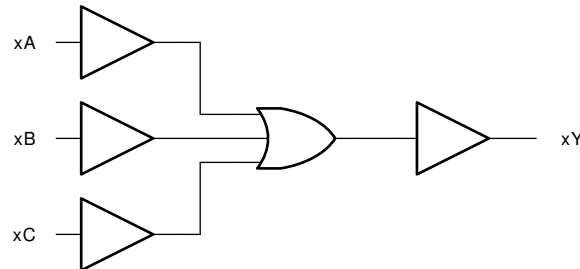
FIG 7-3. Voltage Waveforms Propagation Delays

8 Detailed Description

8.1 Overview

This device contains three independent 3-input OR gates. Each gate performs the Boolean function $Y = A + B + C$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [セクション 6.1](#) must be followed at all times.

The CD74HC4075 can drive a load with a total capacitance less than or equal to the maximum load listed in the [セクション 6.6](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [セクション 6.1](#).

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [セクション 6.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [セクション 6.1](#), and the maximum input leakage current, given in the [セクション 6.5](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [セクション 6.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [図 8-1](#).

注意

Voltages beyond the values specified in the [セクション 6.1](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証テストすることで、システムの機能を確認する必要があります。

9.1 Application Information

In this application, one 3-input OR gates is used to combine overhear signals to control a fan as shown in [図 9-1](#). The other two gates can be used for another application in the system, or the inputs can be grounded and the channels left unused.

This device is used to directly control the Enable pin of a fan driver. The fan driver requires only one input signal to be HIGH before being enabled, and should be disabled in the event that all signals go LOW. The 4-input OR gate function combines the four individual overhear signals into a single active-high enable signal.

9.2 Typical Application

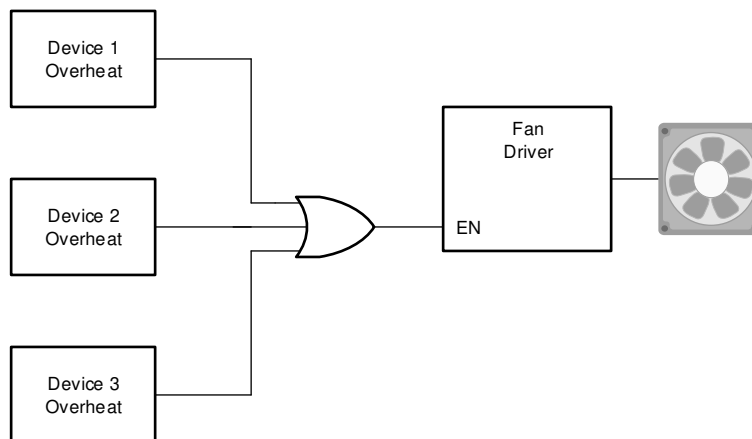


図 9-1. Typical application schematic

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [セクション 6.3](#). The supply voltage sets the device's electrical characteristics as described in the [セクション 6.5](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC4075 plus the maximum supply current, I_{CC} , listed in the [セクション 6.5](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [セクション 6.1](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

注意

The maximum junction temperature, $T_J(\text{max})$ listed in the [セクション 6.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [セクション 6.1](#). These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC4075, as specified in the [セクション 6.5](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The CD74HC4075 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [セクション 6.3](#).

Refer to the [セクション 8.3](#) for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [セクション 6.5](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [セクション 6.5](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [セクション 8.3](#) for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [セクション 11](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC4075 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(\text{max})}) \Omega$. This will ensure that the maximum output current from the [セクション 6.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

9.2.3 Application Curves

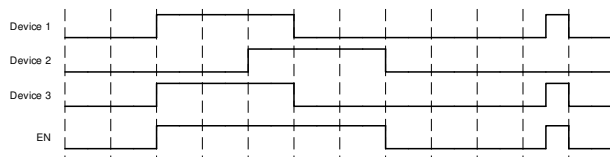


図 9-2. Typical application timing diagram

10 Power Supply Recommendations

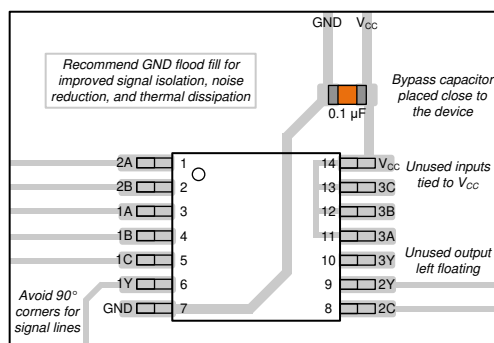
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 6.3](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [図 11-1](#).

11.1 Layout Guidelines

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example



11-1. Example layout for the CD74HC4075

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87722012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87722012A CD54HC 4075FK	Samples
5962-8772201CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772201CA CD54HC4075F3A	Samples
CD54HC4075F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8772201CA CD54HC4075F3A	Samples
CD54HC4075FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87722012A CD54HC 4075FK	Samples
CD74HC4075E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4075E	Samples
CD74HC4075EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4075E	Samples
CD74HC4075M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4075M	Samples
CD74HC4075NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4075M	Samples
CD74HC4075PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HJ4075	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC4075, CD74HC4075 :

- Catalog : [CD74HC4075](#)
- Military : [CD54HC4075](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4075M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4075NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD74HC4075PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4075M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC4075NSR	SO	NS	14	2000	356.0	356.0	35.0
CD74HC4075PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87722012A	FK	LCCC	20	55	506.98	12.06	2030	NA
CD54HC4075FK	FK	LCCC	20	55	506.98	12.06	2030	NA
CD74HC4075E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4075EE4	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

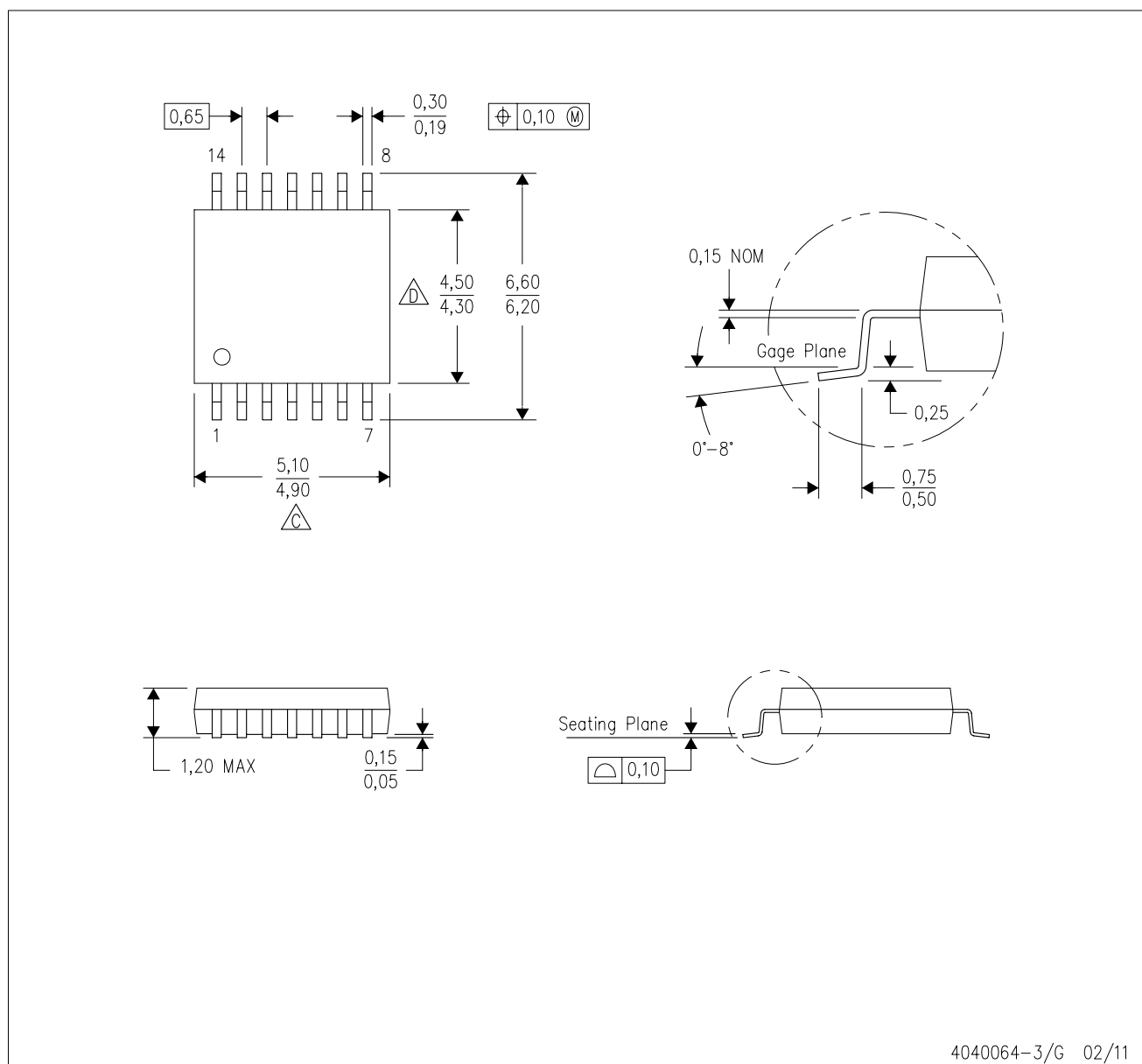


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

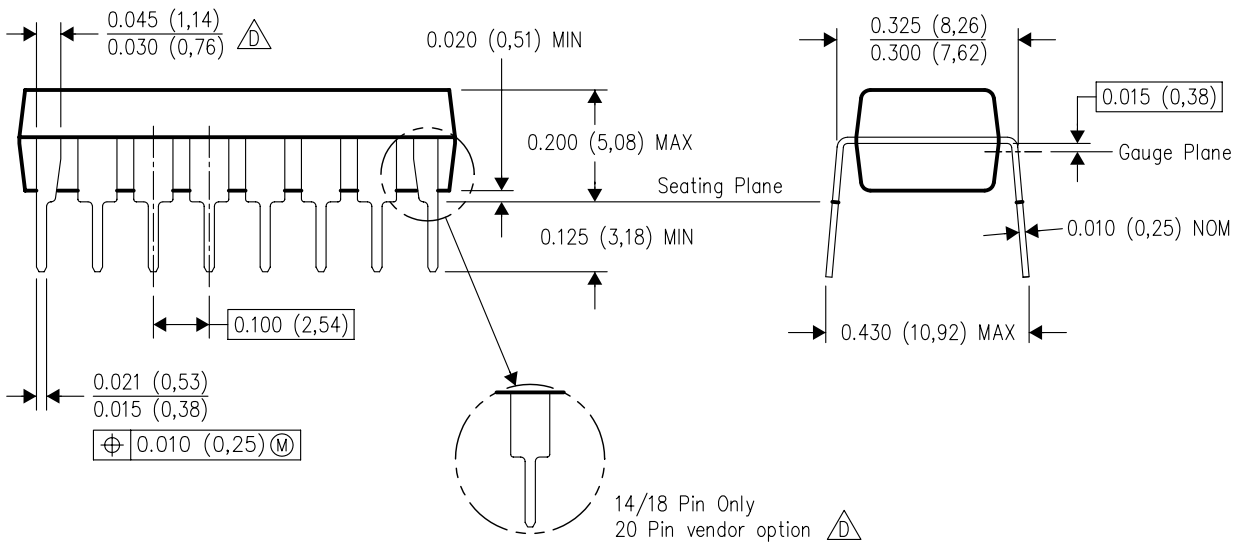
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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