参考資料



# DLP650LE 0.65 WXGA D デジタル・マイクロミラー・デバイス

## 1 特長

- 対角 0.65 インチのマイクロミラー・アレイ
  - WXGA (1280 × 800) アレイ、100 万超のマイクロミラー付き
  - マイクロミラー・ピッチ:10.8µm
  - マイクロミラー傾斜角:±12° (フラット状態に対して)
  - コーナー・イルミネーション (対角照射) 対応
- 2 つの LVDS 入力データ・バス
- DLP650LE チップセットの構成部品:
  - DLP470TE DMD
  - DLPC4430 コントローラ
  - DLPA100 コントローラ・パワー・マネージメントおよびモーター・ドライバ IC
  - DLPA200 DMD パワー・マネージメント IC

## 2 アプリケーション

- スマート照明
- ビジネス・プロジェクタ
- 教育用プロジェクタ

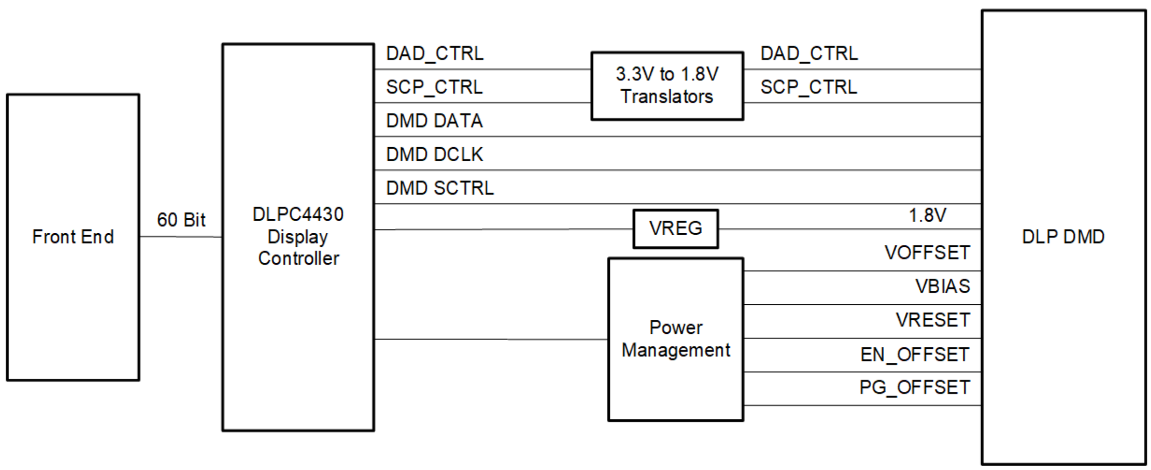
## 3 概要

テキサス・インスツルメンツ DLP® DLP650LE デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御型の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかな WXGA ディスプレイ・ソリューションを低コストで実現します。DLP650LE DMD—は、DLPC4430 ディスプレイ・コントローラ、DLPA100 電源およびモーター・ドライバ、DLPA200 DMD マイクロミラー・ドライバー—と組み合わせて使用すると、高性能システムを実現できます。16:10 の広いアスペクト比、高輝度、システムの簡素化を必要とするディスプレイ・アプリケーションに最適です。

**製品情報**

| 部品番号 | パッケージ(1) | 本体サイズ (公称) |
|---|---|---|
| DLP650LE | FYL (149) | 32.20mm × 22.30mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**DLP650LE のアプリケーション概略図**

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## 4 Revision History

| Changes from Revision * (November 2017) to Revision A (February 2023) | Page |
|---|---|
| • ドキュメントのステータスを「事前情報」から「量産データ」に変更 | 1 |
| • 文書全体にわたって表、図、相互参照の採番方法を更新。コントローラを DLPC4430 に更新。チップセット・コンポーネントへのリンクを更新。。 | 1 |
| • コントローラを DLPC4430 に更新 | 1 |
| • Updated controller to DLPC4430 | 20 |
| • Updated controller to DLPC4430 | 21 |
| • Added a table for legacy part numbers and listed the mechanical ICD | 27 |
| • Updated controller to DLPC4430 | 27 |
| • Updated controller to DLPC4430 | 28 |
| • Updated controller to DLPC4430 | 28 |
| • Updated controller to DLPC4430, updated the links | 32 |

# 5 Pin Configuration and Functions

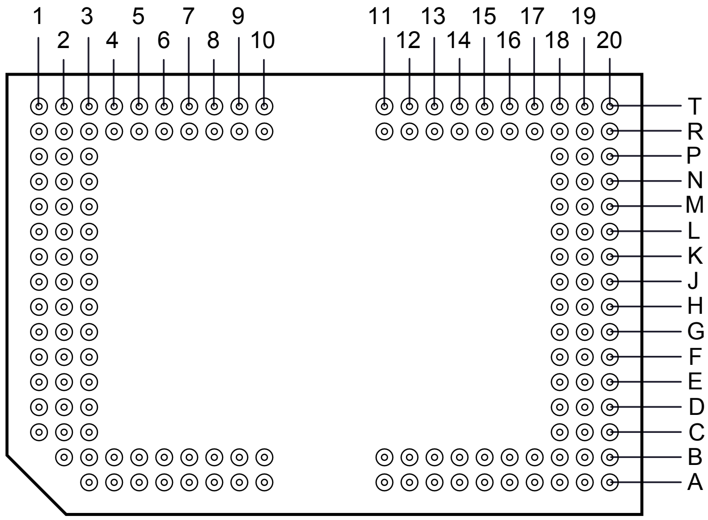



図 5-1. FYL Package 149-Pin CLGA Bottom View

表 5-1. Pin Functions

| PIN | | NET LENGTH (mils) | SIGNAL | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **DATA INPUTS** | | | | | |
| D_AN(1) | G20 | 711.64 | LVDS | I | LVDS pair for Data Bus A |
| D_AN(3) | H19 | 711.60 | | | |
| D_AN(5) | F18 | 711.60 | | | |
| D_AN(7) | E18 | 711.60 | | | |
| D_AN(9) | C20 | 711.60 | | | |
| D_AN(11) | B18 | 711.60 | | | |
| D_AN(13) | A20 | 711.60 | | | |
| D_AN(15) | B19 | 711.58 | | | |
| D_AP(1) | H20 | 711.66 | | | |
| D_AP(3) | G19 | 711.61 | | | |
| D_AP(5) | G18 | 711.59 | | | |
| D_AP(7) | D18 | 711.60 | | | |
| D_AP(9) | D20 | 711.59 | | | |
| D_AP(11) | A18 | 711.58 | | | |
| D_AP(13) | B20 | 711.59 | | | |
| D_AP(15) | A19 | 711.59 | | | |

表 5-1. Pin Functions (continued)

| PIN | | NET LENGTH (mils) | SIGNAL | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| D_BN(1) | K20 | 711.61 | LVDS | I | LVDS pair for Data Bus B |
| D_BN(3) | J19 | 711.59 | | | |
| D_BN(5) | L18 | 711.59 | | | |
| D_BN(7) | M18 | 711.6 | | | |
| D_BN(9) | P20 | 711.6 | | | |
| D_BN(11) | R18 | 711.59 | | | |
| D_BN(13) | T20 | 711.59 | | | |
| D_BN(15) | R19 | 711.59 | | | |
| D_BP(1) | J20 | 711.61 | | | |
| D_BP(3) | K19 | 711.6 | | | |
| D_BP(5) | K18 | 711.58 | | | |
| D_BP(7) | N18 | 711.58 | | | |
| D_BP(9) | N20 | 711.6 | | | |
| D_BP(11) | T18 | 711.61 | | | |
| D_BP(13) | R20 | 711.59 | | | |
| D_BP(15) | T19 | 711.6 | | | |
| DCLK_AN | D19 | 711.59 | | I | LVDS pair for Data Clock A |
| DCLK_AP | E19 | 711.59 | | | |
| DCLK_BN | N19 | 711.6 | | I | LVDS pair for Data Clock B |
| DCLK_BP | M19 | 711.61 | | | |
| **DATA CONTROL INPUTS** | | | | | |
| SCTRL_AN | F20 | 711.62 | | I | LVDS pair for Serial Control (Sync) A |
| SCTRL_AP | E20 | 711.6 | | | |
| SCTRL_BN | L20 | 711.59 | | I | LVDS pair for Serial Control (Sync) B |
| SCTRL_BP | M20 | 711.59 | | | |

表 5-1. Pin Functions (continued)

| PIN | | NET LENGTH (mils) | SIGNAL | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **MICROMIRROR BIAS RESET INPUTS** | | | | | |
| MBRST(0) | C3 | 507.20 | | I | Nonlogic compatible Micromirror Bias Reset signals. Connected directly to the array of pixel micromirrors. Used to hold or release the micromirrors. Bond Pads connect to an internal pulldown resistor. |
| MBRST(1) | D2 | 576.83 | | | |
| MBRST(2) | D3 | 545.78 | | | |
| MBRST(3) | E2 | 636.33 | | | |
| MBRST(4) | G3 | 618.42 | | | |
| MBRST(5) | E1 | 738.25 | | | |
| MBRST(6) | G2 | 718.82 | | | |
| MBRST(7) | G1 | 777.04 | | | |
| MBRST(8) | N3 | 543.29 | | | |
| MBRST(9) | M2 | 612.93 | | | |
| MBRST(10) | M3 | 580.97 | | | |
| MBRST(11) | L2 | 672.43 | | | |
| MBRST(12) | J3 | 653.61 | | | |
| MBRST(13) | L1 | 764.00 | | | |
| MBRST(14) | J2 | 764.37 | | | |
| MBRST(15) | J1 | 813.14 | | | |
| **SCP CONTROL** | | | | | |
| SCPCLK | A8 | | | I | Serial Communications Port Clock. Bond Pad connects to an internal pulldown circuit. |
| SCPDI | A5 | | | I | Serial Communications Port Data. Bond Pad connects to an internal pulldown circuit. |
| SCPENZ | B7 | | | I | Active low serial communications port enable. Bond pad connects to an internal pulldown circuit. |
| SCPDO | A9 | | | O | Serial communications port output |
| **OTHER SIGNALS** | | | | | |
| EVCC | A3 | | | P | Do not connect on the DLP system board. |
| MODE_A | A4 | 415.1 | | I | Data Bandwidth Mode Select. Bond Pad connects to an internal pulldown circuit. Refer to Table 4 for DLP system board connection information. |
| PWRDNZ | B9 | 110.38 | | I | Active Low Device Reset. Bond Pad connects to an internal pulldown circuit. |
| **POWER** | | | | | |
| $V_{CC}$ [(2)] | B11, B12, B13, B16, R12, R13, R16, R17 | | | P | Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes |
| $V_{CCI}$ [(2)] | A12, A14, A16, T12, T14, T16 | | | P | Power supply for low voltage CMOS LVDS interface |
| $V_{OFFSET}$ [(2)] | C1, D1, M1, N1 | | | P | Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes |

**表 5-1. Pin Functions (continued)**

| PIN | | NET LENGTH (mils) | SIGNAL | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| $V_{SS}$ (Ground)[(3)] | A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17 | | | P | Common Return for all power |
| **RESERVED SIGNALS** | | | | | |
| RESERVED_FC | R7 | 40.64 | | I | Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit. |
| RESERVED_FD | R8 | 94.37 | | I | Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit. |
| RESERVED_PFE | T8 | 50.74 | | I | Connect to ground on the DLP system board. Bond Pad connects to an internal pulldown circuit. |
| RESERVED_STM | B6 | | | I | Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit. |
| RESERVED_TP0 | R10 | 93.3 | | I | Do not connect on the DLP system board. |
| RESERVED_TP1 | T11 | 263.74 | | I | Do not connect on the DLP system board. |
| RESERVED_TP2 | R11 | 281.47 | | I | Do not connect on the DLP system board. |
| RESERVED_BA | T10 | 148.85 | | O | Do not connect on the DLP system board. |
| RESERVED_BB | A10 | 105.28 | | O | Do not connect on the DLP system board. |
| RESERVED_RA1 | T9 | | | O | Do not connect on the DLP system board. |
| RESERVED_RB1 | A7 | | | O | Do not connect on the DLP system board. |
| RESERVED_TS | B10 | 145.42 | | O | Do not connect on the DLP system board. |
| RESERVED_A(0) | T2 | | | NC | Do not connect on the DLP system board. |
| RESERVED_A(1) | T3 | | | | |
| RESERVED_A(2) | R3 | | | | |
| RESERVED_A(3) | T4 | | | | |
| RESERVED_M(0) | R2 | | | NC | Do not connect on the DLP system board. |
| RESERVED_M(1) | P1 | | | NC | Do not connect on the DLP system board. |
| RESERVED_S(0) | T1 | | | NC | Do not connect on the DLP system board. |
| RESERVED_S(1) | R1 | | | NC | Do not connect on the DLP system board. |
| RESERVED_IRQZ | T6 | | | NC | Do not connect on the DLP system board. |
| RESERVED_OEZ | R5 | | | NC | Do not connect on the DLP system board. |
| RESERVED_RSTZ | R6 | | | NC | Do not connect on the DLP system board. |
| RESERVED_STR | T5 | | | NC | Do not connect on the DLP system board. |
| RESERVED_STR | T5 | | | NC | Do not connect on the DLP system board. |

**表 5-1. Pin Functions (continued)**

| PIN | | NET LENGTH (mils) | SIGNAL | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| RESERVED_VB | E3, F3, K3, L3 | | | NC | Do not connect on the DLP system board. |
| RESERVED_VR | B2, B3, P2, P3 | | | NC | Do not connect on the DLP system board. |

(1) I = Input, O = Output, G = Ground, A = Analog, P = Power, NC = No Connect.
(2) Power supply pins required for all DMD operating modes are $V_{SS}$, $V_{BIAS}$, $V_{CC}$, $V_{CCI}$, $V_{OFFSET}$, and $V_{RESET}$.
(3) $V_{SS}$ must be connected for proper DMD operation.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[(1)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **SUPPLY VOLTAGES** | | | | |
| $V_{CC}$ | Supply voltage for LVCMOS core logic[(2)] | –0.5 | 4 | V |
| $V_{CCI}$ | Supply voltage for LVDS Interface[(2)] | –0.5 | 4 | V |
| $V_{OFFSET}$ | Micromirror Electrode and HVCMOS voltage[(2) (3)] | –0.5 | 9 | V |
| $V_{MBRST}$ | Input voltage for MBRST(15:0)[(2)] | –28 | 28 | V |
| $\lvert V_{CCI} – V_{CC}\rvert$ | Supply voltage delta (absolute value)[(4)] | | 0.3 | V |
| **INPUT VOLTAGES** | | | | |
| | Input voltage for all other input pins[(2)] | –0.5 | $V_{CC}$ + 0.3 | V |
| $\lvert V_{ID}\rvert$ | Input differential voltage (absolute value)[(5)] | | 700 | mV |
| **CLOCKS** | | | | |
| $f_{CLOCK}$ | Clock frequency for LVDS interface, DCLK_A | | 400 | MHz |
| $f_{CLOCK}$ | Clock frequency for LVDS interface, DCLK_B | | 400 | MHz |
| **ENVIRONMENTAL** | | | | |
| $T_{ARRAY}$ and $T_{WINDOW}$ | Temperature, operating[(6)] | 0 | 90 | °C |
| | Temperature, non–operating[(6)] | –40 | 90 | °C |
| $\lvert T_{DELTA}\rvert$ | Absolute Temperature delta between any point on the window edge and the ceramic test point TP1[(7)] | | 30 | °C |
| $T_{DP}$ | Dew point temperature, operating and non–operating (noncondensing) | | 81 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground $V_{SS}$. $V_{BIAS}$, $V_{CC}$, $V_{CCI}$, $V_{OFFSET}$, and $V_{RESET}$ power supplies are all required for all DMD operating modes.
(3) $V_{OFFSET}$ supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between $V_{CC}$ and $V_{CCI}$ may result in excessive current draw.
(5) The maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(6) The highest temperature of the active array (as calculated using セクション 7.6) or of any point along the window edge as defined in 図 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, then that point should be used.
(7) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, then that point should be used.
(8) $V_{OFFSET}$ supply transients must fall within specified voltages.
(9) Excludes micromirror Bias Reset inputs MBRST(15:0).

## 6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{DMD}$ | DMD storage temperature | –40 | 80 | °C |
| $T_{DP\text{-}AVG}$ | Average dew point temperature (non-condensing)(1) | | 28 | °C |
| $T_{DP\text{-}ELR}$ | Elevated dew point temperature range (non-condensing)(2) | 28 | 36 | °C |
| $CT_{ELR}$ | Cumulative time in elevated dew point temperature range | | 24 | Months |

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of $CT_{ELR}$.

## 6.3 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except MBRST(15:0) | ±2000 | V |
| | | | Pins MBRST(15:0) | < 250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | |
| $V_{CC}$ | Supply voltage for LVCMOS core logic(1) | 3.0 | 3.3 | 3.6 | V |
| $V_{CCI}$ | Supply voltage for LVDS interface(1) | 3.0 | 3.3 | 3.6 | V |
| $V_{OFFSET}$ | Micromirror electrode and HVCMOS voltage(1) (2) | 8.25 | 8.5 | 8.75 | V |
| $V_{MBRST}$ | Micromirror bias / reset voltage(1) | –27 | | 26.5 | V |
| $\|V_{CC} – V_{CCI}\|$ | Supply voltage delta (absolute value)(3) | | 0 | 0.3 | V |
| **LVCMOS INTERFACE** | | | | | |
| $V_{IH}$ | Input high voltage | 1.7 | 2.5 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input low voltage | –0.3 | | 0.7 | V |
| $I_{OH}$ | High level output current | | | –20 | mA |
| $I_{OL}$ | Low level output current | | | 15 | mA |
| $t_{PWRDNZ}$ | PWRDNZ pulse width(4) | 10 | | | ns |
| **SCP INTERFACE** | | | | | |
| $f_{SCPCLK}$ | SCP clock frequency(5) | 50 | | 500 | kHz |
| $t_{SCP\_PD}$ | Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO(6) | 0 | | 900 | ns |
| $t_{SCP\_DS}$ | SCPDI clock setup time (before SCPCLK falling-edge)(6) | 800 | | | ns |
| $t_{SCP\_DH}$ | SCPDI hold time (after SCPCLK falling-edge)(6) | 900 | | | ns |
| $t_{SCP\_NEG\_ENZ}$ | Time between falling-edge of SCPENZ and the rising-edge of SCPCLK.(5) | 1 | | | us |
| SCP_POS_ENZ | Time between falling-edge of SCPCLK and the rising-edge of SCPENZ | 1 | | | us |
| $t_{SCP\_OUT\_EN}$ | Time required for SCP output buffer to recover after SCPENZ (from tristate) | | | $192/f_{DCLK}$ | s |
| $t_{SCP\_PW\_ENZ}$ | SCPENZ inactive pulse width (high level) | 1 | | | $1/f_{scpclk}$ |
| $t_r$ | Rise Time (20% to 80%). See (6). | | | 200 | ns |

## 6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_f$ | Fall time (80% to 20%). See [6]. | | | 200 | ns |
| **LVDS INTERFACE** | | | | | |
| $f_{CLOCK}$ | Clock frequency for LVDS interface (all channels), DCLK[7] | | 320 | 330 | MHz |
| $\|V_{ID}\|$ | Input differential voltage (absolute value)[8] | 100 | 400 | 600 | mV |
| $V_{CM}$ | Common mode voltage[8] | | 1200 | | mV |
| $V_{LVDS}$ | LVDS voltage[8] | 0 | | 2000 | mV |
| $t_{LVDS\_RSTZ}$ | Time required for LVDS receivers to recover from PWRDNZ | | | 10 | ns |
| $Z_{IN}$ | Internal differential termination resistance | 95 | | 105 | Ω |
| $Z_{LINE}$ | Line differential impedance (PWB/trace) | 85 | 90 | 95 | Ω |
| **ENVIRONMENTAL** | | | | | |
| $T_{ARRAY}$ | Array temperature, long-term operational[9] [10] [11] | 10 | | 40 to 70[12] | °C |
| | Array temperature, short-term operational[10] [13] | 0 | | 10 | °C |
| $T_{WINDOW}$ | Window temperature (all part numbers except *1280-6434B)[14] [15] | 10 | | 90 | °C |
| | Window temperature (part number 1280-6434B)[14] | 10 | | 85 | |
| $T_{\|DELTA\|}$ | Absolute temperature delta between any point on the window edge and the ceramic test point TP1[16] | | | 26 | °C |
| $T_{DP\text{-}AVG}$ | Average dew point average temperature (non-condensing)[17] | | | 28 | °C |
| $T_{DP\text{-}ELR}$ | Elevated dew point temperature range (non-condensing)[18] | 28 | | 36 | °C |
| $CT_{ELR}$ | Cumulative time in elevated dew point temperature range | | | 24 | Months |
| $ILL_{UV}$ | Illumination Wavelengths < 395 nm[9] | | 0.68 | 2.00 | $mW/cm^2$ |
| $ILL_{VIS}$ | Illumination Wavelengths between 395 nm and 800 nm | | Thermally limited | | $mW/cm^2$ |
| $ILL_{IR}$ | Illumination Wavelengths > 800 nm | | | 10 | $mW/cm^2$ |

(1) All voltages are referenced to common ground $V_{SS}$. $V_{BIAS}$, $V_{CC}$, $V_{CCI}$, $V_{OFFSET}$, and $V_{RESET}$ power supplies are all required for proper DMD operation. $V_{SS}$ must also be connected.
(2) $V_{OFFSET}$ supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit. See セクション 9, 図 9-1, and 表 9-2.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See 図 6-2.
(7) See LVDS Timing Requirements in セクション 6.8 and 図 6-6.
(8) See 図 6-5 LVDS Waveform Requirements.
(9) Simultaneous exposure of the DMD to the maximum セクション 6.4 for temperature and UV illumination will reduce device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-1 and the package *thermal resistance* using セクション 7.6.
(11) Long-term is defined as the usable life of the device.
(12) Per 図 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See セクション 7.7 for a definition of micromirror landed duty cycle.
(13) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(14) The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(15) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(17) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(18) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of $CT_{ELR}$.

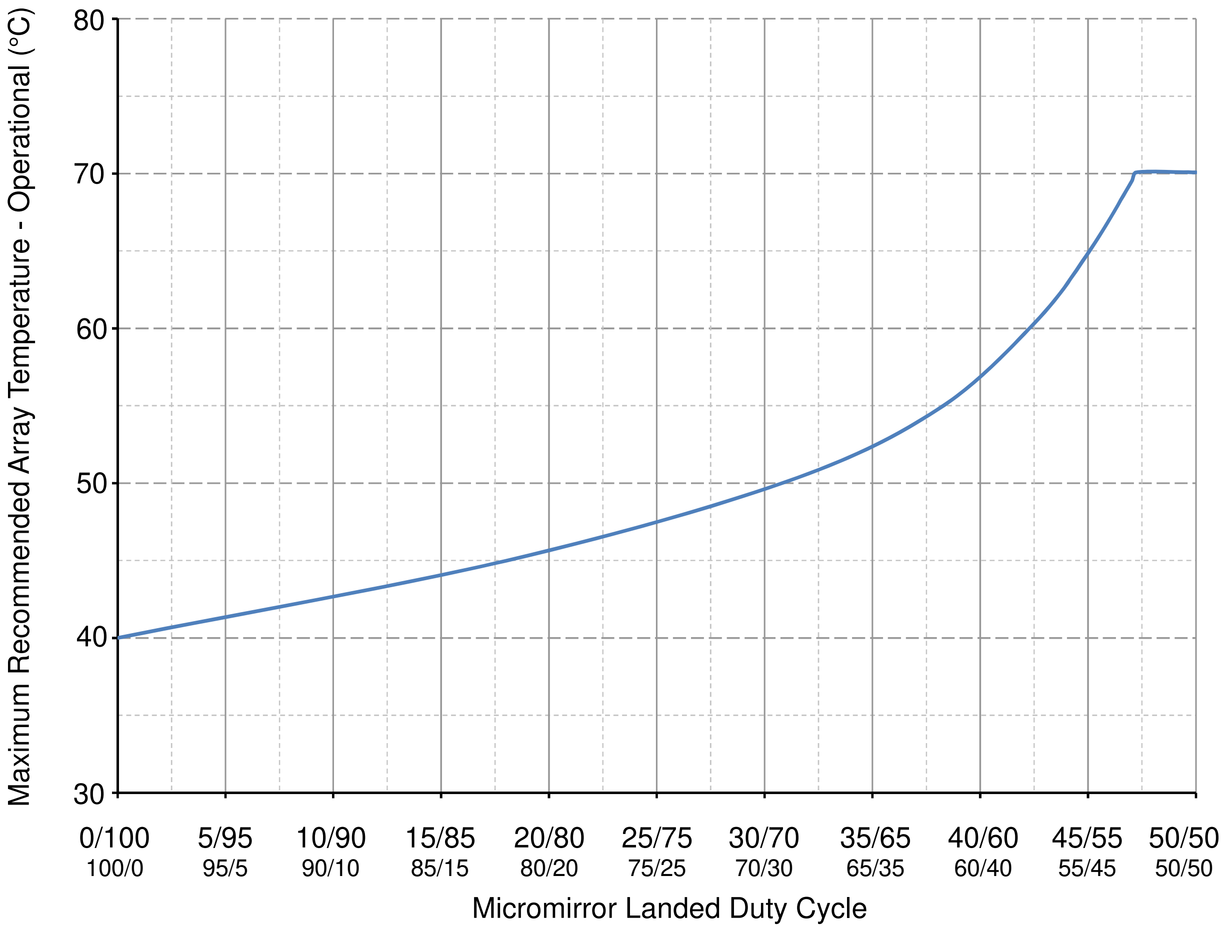



**図 6-1. Maximum Recommended Array Temperature—Derating Curve**

## 6.5 Thermal Information

| THERMAL METRIC | DLP650LE FYL Package 149 PINS | UNIT |
|---|---|---|
| Thermal resistance, active area to test point 1 (TP1)(1) | 0.50 | °C/W |

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the セクション 6.4.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

## 6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 3 V, $I_{OH}$ = –20 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 3.6 V, $I_{OL}$ = 15 mA | | | 0.4 | V |
| $I_{OZ}$ | High-impedance output current | $V_{CC}$ = 3.6 V | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 3.6 V, VI = 0 | | | –60 | µA |
| $I_{IH}$ | High-level input current (1) | $V_{CC}$ = 3.6 V, VI = $V_{CC}$ | | | 200 | µA |
| $I_{CC}$ | Supply current VCC (2) | $V_{CC}$ = 3.6 V | | | 479 | mA |
| $I_{CCI}$ | Supply current VCCI (2) | $V_{CCI}$ = 3.6 V | | | 309 | mA |
| $I_{OFFSET}$ | Supply current VOFFSET (3) | $V_{OFFSET}$ = 8.75 V | | | 25 | mA |
| | Supply input power total | f = 1 MHz | | | 3060 | mW |

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit in セクション 6.4.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit in セクション 6.4.

## 6.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range, $f$ = 1 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $C_I$ | Input capacitance | | | 10 | pF |
| $C_O$ | Output capacitance | | | 10 | pF |
| $C_{IM}$ | MBRST(15:0) input capacitance | 1280 × 800 array all inputs interconnected | 230 | 290 | pF |

### 6.8 Timing Requirements

Over セクション 6.4 (unless otherwise noted).

| PARAMETER DESCRIPTION | | SIGNAL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS** (1) | | | | | | |
| $t_C$ | Clock cycle duration for DCLK_A | LVDS | 3.03 | | | ns |
| $t_C$ | Clock cycle duration for DCLK_B | LVDS | 3.03 | | | ns |
| $t_W$ | Pulse duration for DCLK_A | LVDS | 1.36 | 1.52 | | ns |
| $t_W$ | Pulse duration for DCLK_B | LVDS | 1.36 | 1.52 | | ns |
| $t_{SU}$ | Setup time for D_A(15:0) before DCLK_A | LVDS | 0.35 | | | ns |
| $t_{SU}$ | Setup time for D_A(15:0) before DCLK_B | LVDS | 0.35 | | | ns |
| $t_{SU}$ | Setup time for SCTRL_A before DCLK_A | LVDS | 0.35 | | | ns |
| $t_{SU}$ | Setup time for SCTRL_B before DCLK_B | LVDS | 0.35 | | | ns |
| $t_H$ | Hold time for D_A(15:0) after DCLK_A | LVDS | 0.35 | | | ns |
| $t_H$ | Hold time for D_B(15:0) after DCLK_B | LVDS | 0.35 | | | ns |
| $t_H$ | Setup time for SCTRL_A after DCLK_A | LVDS | 0.35 | | | ns |
| $t_H$ | Setup time for SCTRL_B after DCLK_B | LVDS | 0.35 | | | ns |
| $t_{SKEW}$ | Channel B relative to Channel A (2) (3) | LVDS | –1.51 | | 1.51 | ns |

(1) See 図 6-6 for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).

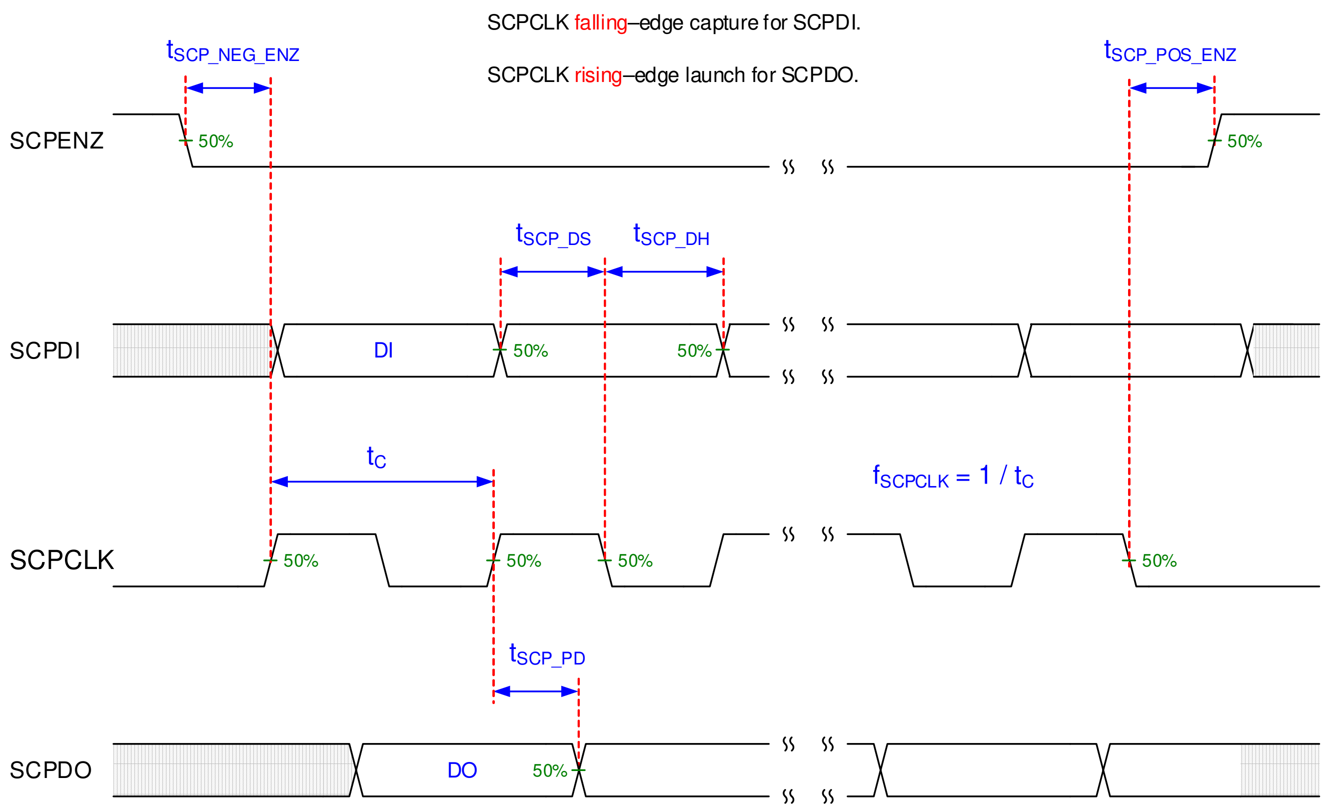
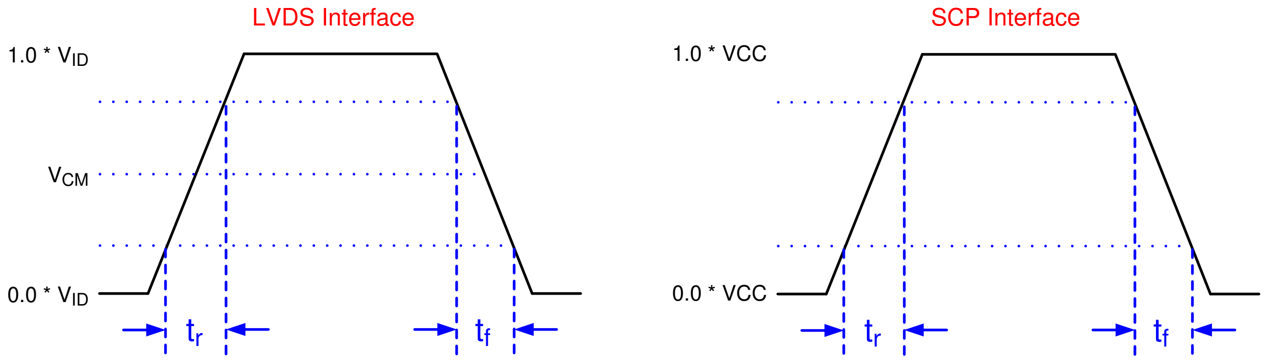



**図 6-2. SCP Timing Requirements**

See セクション 6.4 for $f_{SCPCLK}$, $t_{SCP\_DS}$, $t_{SCP\_DH}$, and $t_{SCP\_PD}$ specifications.

See セクション 6.4 for $t_r$ and $t_f$ specifications and conditions.




Not to scale.

Refer to the セクション 6.8.

Refer to セクション 5 for list of LVDS pins and SCP pins.

**図 6-3. Rise Time and Fall Time**

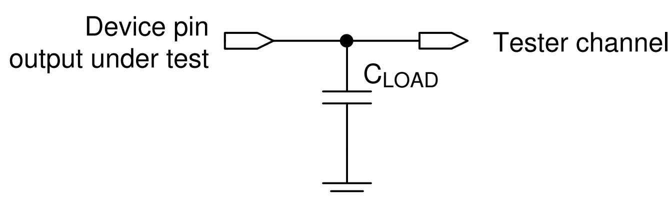



**図 6-4. Test Load Circuit for Output Propagation Measurement**

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. See 図 6-4.

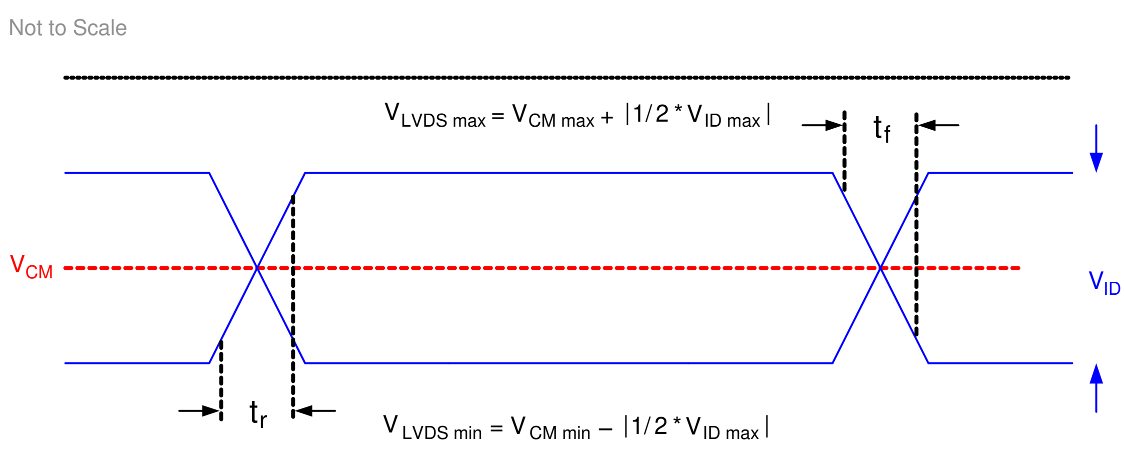



**図 6-5. LVDS Waveform Requirements**

See セクション 6.4 for $V_{CM}$, $V_{ID}$, and $V_{LVDS}$ specifications and conditions.

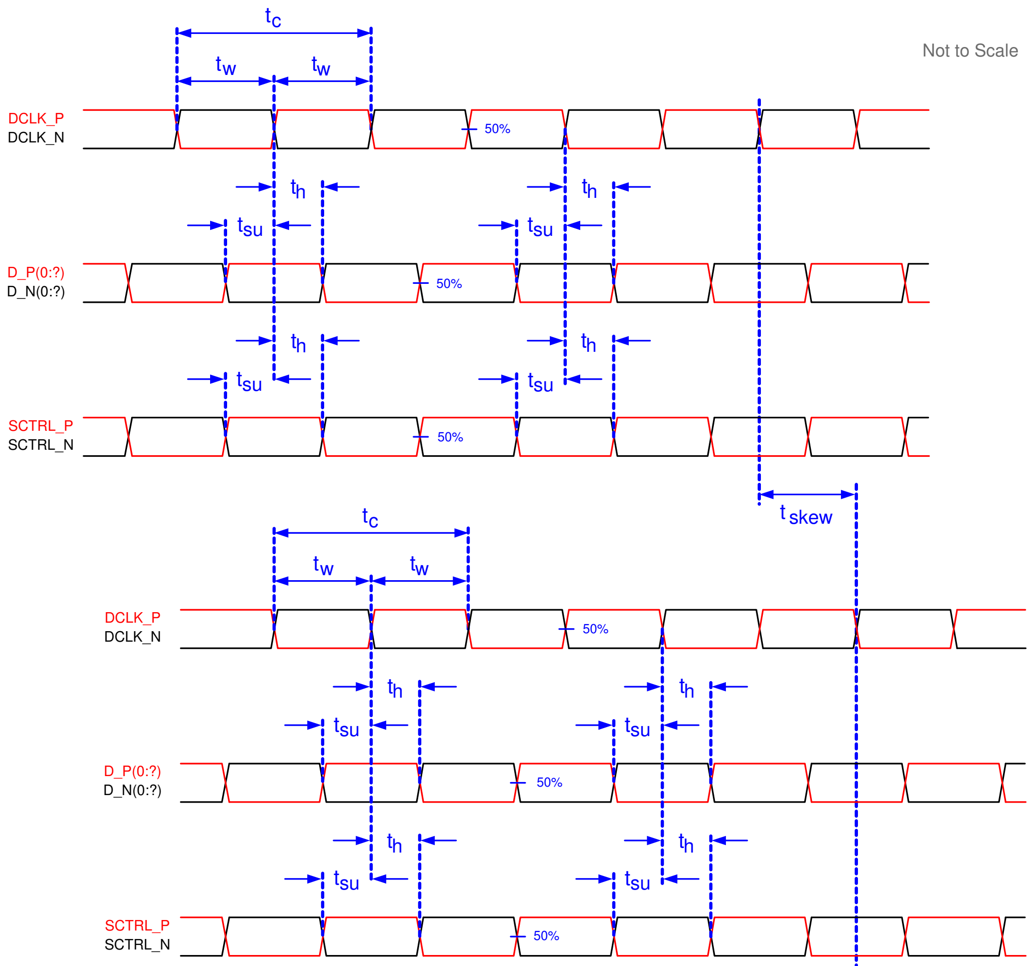



**図 6-6. Timing Requirements**

See セクション 6.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(0:x) and D_N(0:x).

## 6.9 Window Characteristics

**表 6-1. DMD Window Characteristics**

| PARAMETER | MIN | NOM |
|---|---|---|
| Window material | | Corning Eagle XG |
| Window Refractive Index at 546.1 nm | | 1.5119 |
| Window Transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0°–30° AOI. (1) (2) | 97% | |
| Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30°–45° AOI. (1) (2) | 97% | |

(1) Single-pass through both surfaces and glass
(2) AOI—Angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

## 6.10 System Mounting Interface Loads

**表 6-2. System Mounting Interface Loads**

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Condition 1: | | | | |
| Thermal Interface area(1) | | | 11.3 | kg |
| Electrical Interface area(1) | | | 11.3 | kg |
| Condition 2: | | | | |
| Thermal Interface area(1) | | | 0 | kg |
| Electrical Interface area(1) | | | 22.6 | kg |

(1) Uniformly distributed within area shown in 図 6-7

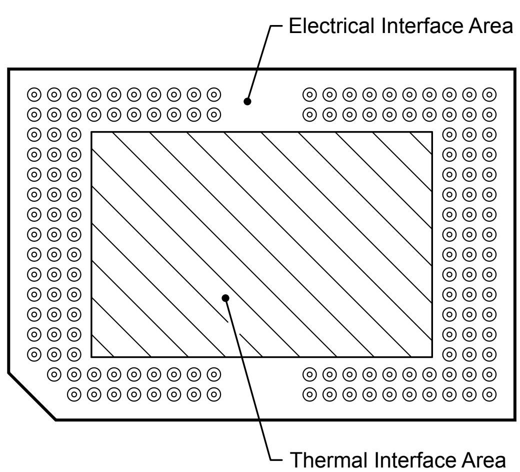



**図 6-7. System Mounting Interface Loads**

## 6.11 Micromirror Array Physical Characteristics

**表 6-3. Micromirror Array Physical Characteristics**

| PARAMETER DESCRIPTION | | VALUE | UNIT |
|---|---|---|---|
| Number of active columns(1) | M | 1280 | micromirrors |
| Number of active rows(1) | N | 800 | |
| Micromirror (pixel) pitch (1) | P | 10.8 | µm |
| Micromirror active array width(1) | Micromirror pitch × number of active columns | 13.824 | mm |
| Micromirror active array height(1) | Micromirror pitch × number of active rows | 8.640 | mm |
| Micromirror active border size(2) | Pond of Micromirror (POM) | 10 | micromirrors / side |

(1) See 図 6-8.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the *Pond Of Mirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

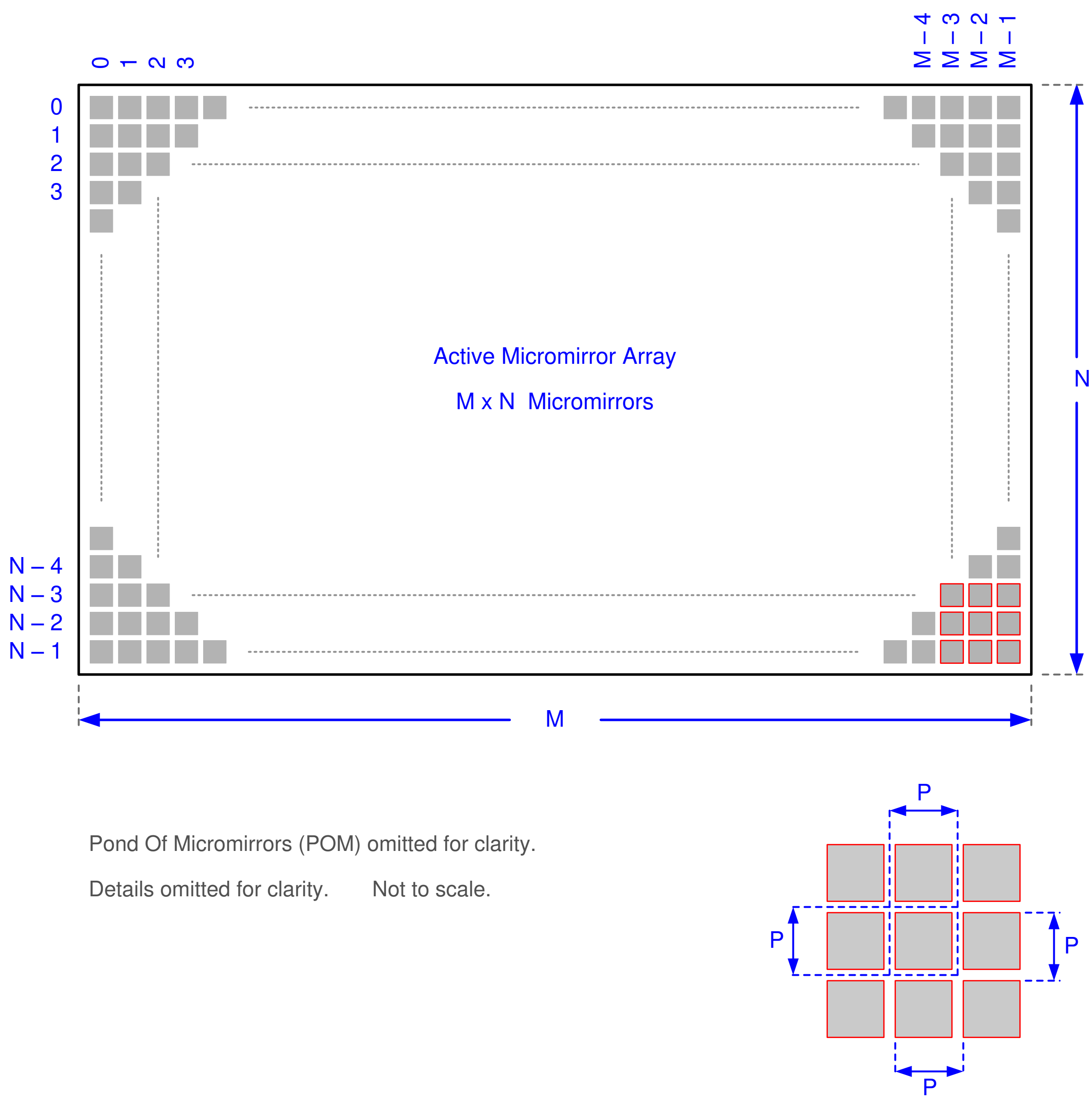



**図 6-8. Micromirror Array Physical Characteristics**

Refer to セクション 6.11 table for M, N, and P specifications.

## 6.12 Micromirror Array Optical Characteristics

**表 6-4. Micromirror Array Optical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Mirror Tilt angle, variation device to device(1) (2) (3) (4) | | 11 | 12 | 13 | degrees |
| Number of out-of-specification micromirrors(5) | Adjacent micromirrors | | | 0 | micromirrors |
| | Non-adjacent micromirrors | | | 10 | |

(1) Measured relative to the plane formed by the overall micromirror array
(2) Variation can occur between any two individual micromirrors located on the same device or located on different devices.
(3) Additional variation exists between the micromirror array and the package datums. See the package drawing.
(4) See 図 6-9.
(5) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states.

注

This number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.

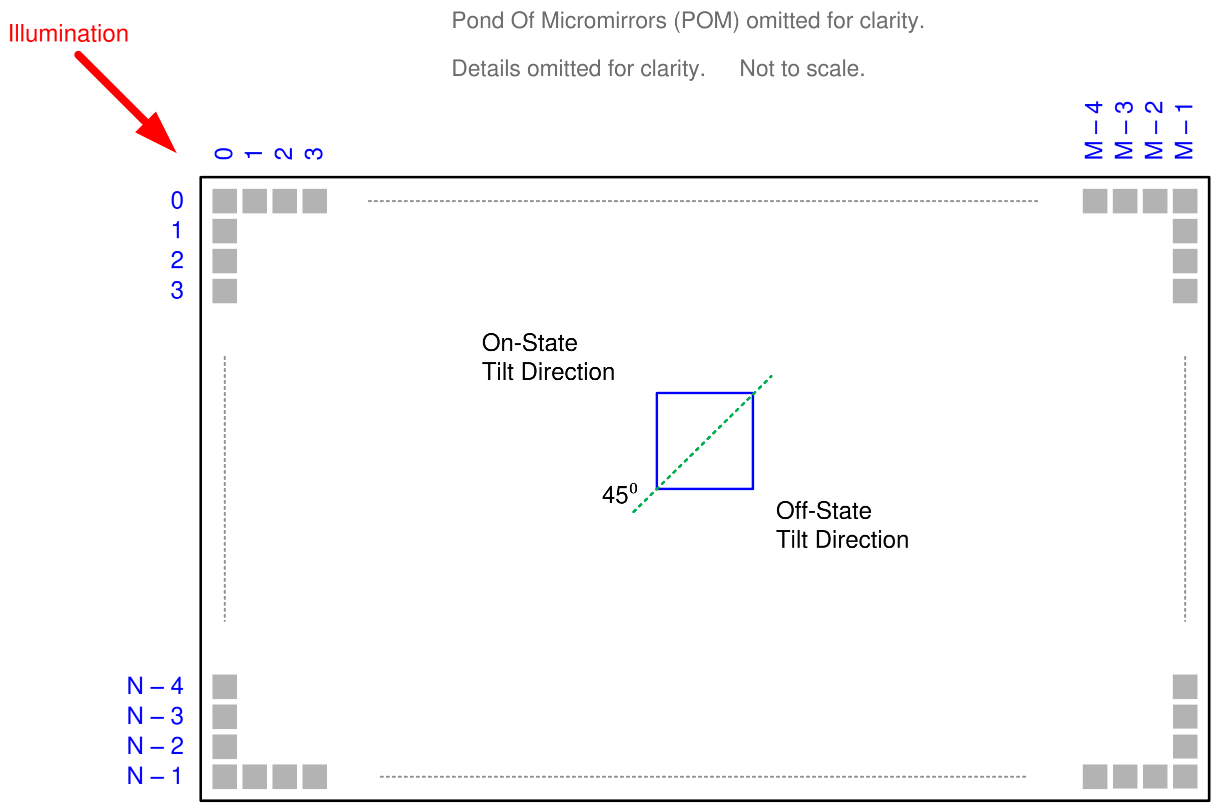



**図 6-9. Micromirror Landed Orientation and Tilt**

Refer to セクション 6.11 table for M, N, and P specifications.

## 6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP650LE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

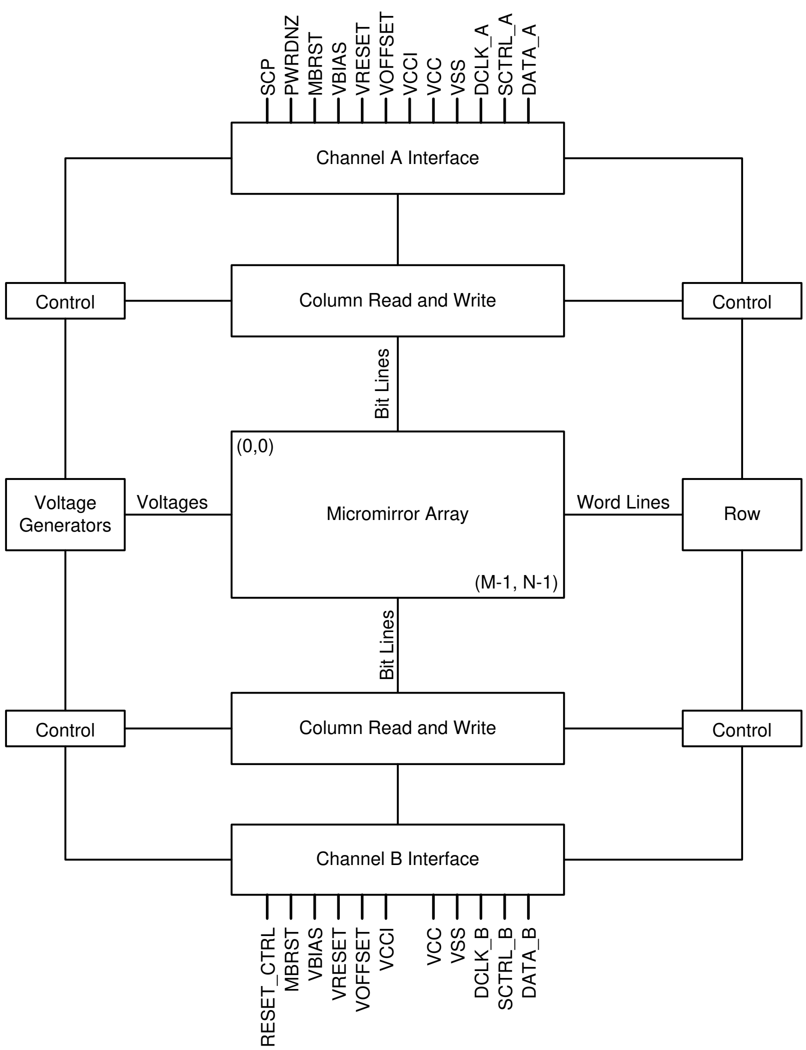
# 7 Detailed Description

## 7.1 Overview

The DMD is a 0.65 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to セクション 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP650LE DMD is part of the chipset comprising of the DLP650LE DMD, the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver. To ensure reliable operation, the DLP650LE DMD must always be used with the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver.

## 7.2 Functional Block Diagram






For pin details on Channels A, B refer to セクション 5 and LVDS Interface section of セクション 6.8.

## 7.3 Feature Description

### 7.3.1 Power Interface

The DMD requires 3 DC voltages: DMD_P3P3V, $V_{OFFSET}$, and MBRST. DMD_P3P3V is created by the DLPA100 power and motor driver and the DLPA200 DMD micromirror driver. Both the DLPA100 and DLPA200 create the main DMD voltages, as well as powering various peripherals (TMP411, $I^2C$, and TI level translators). DMD_P3P3V provides the VCC voltage required by the DMD. $V_{OFFSET}$ (8.5V) and MBRST are made by the DLPA200 and are supplied to the DMD to control the micromirrors.

### 7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4430 display controller. See the DLPC4430 display controller data sheet or contact a TI applications engineer.

## 7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

### 7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation, and objectionable artifacts in the display's border and/or active area could occur.

### 7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

### 7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately

10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

## 7.6 Micromirror Array Temperature Calculation

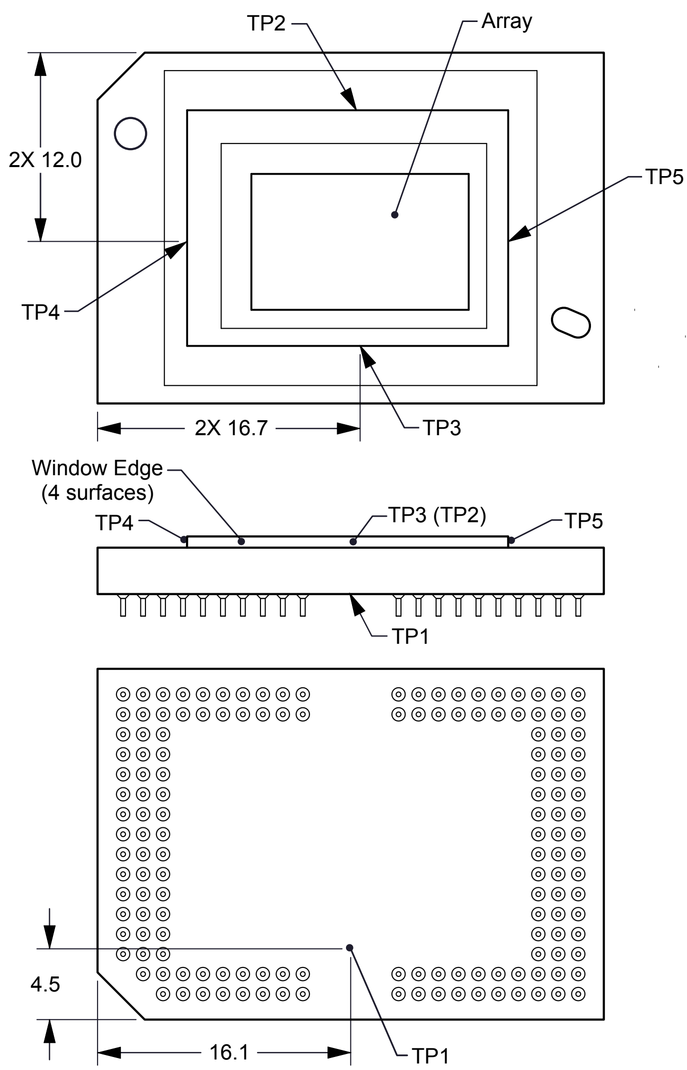



**図 7-1. DMD Thermal Test Points**

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 図 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (1)$$

where

- $T_{ARRAY}$ = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = thermal resistance of package (specified in セクション 6.5) from array to ceramic TP1 (°C/Watt)
- $Q_{ARRAY}$ = Total DMD power (electrical + absorbed) on the array (Watts)
- $Q_{ELECTRICAL}$ = Nominal Electrical Power
- $C_{L2W}$ = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- SL = measured screen Lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.5 Watts. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant $C_{L2W}$ is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/Watt for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture.

Sample Calculations:

$$T_{CERAMIC} = 55.0°C$$

$$SL = 3000 \text{ lm}$$

$$Q_{ELECTRICAL} = 1.5 \text{ W}$$

$$C_{L2W} = 0.00274 \text{ W/lm}$$

$$Q_{ARRAY} = 1.5 \text{ W} + (0.00274 \times 3000 \text{ lm}) = 9.72 \text{ W}$$

$$T_{ARRAY} = 55.0°C + (9.72 \text{ W} \times 0.50°C/W) = 59.9°C$$

## 7.7 Micromirror Landed-On/Landed-Off Duty Cycle

### 7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

### 7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

### 7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD’s usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD’s usable life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature at a given long-term average Landed Duty Cycle.

### 7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

**表 7-1. Grayscale Value and Landed Duty Cycle**

| GRAYSCALE VALUE | LANDED DUTY CYCLE |
|---|---|
| 0% | 0/100 |
| 10% | 10/90 |
| 20% | 20/80 |
| 30% | 30/70 |
| 40% | 40/60 |
| 50% | 50/50 |
| 60% | 60/40 |
| 70% | 70/30 |
| 80% | 80/20 |
| 90% | 90/10 |
| 100% | 100/0 |

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

- Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, and blue color intensities would be as shown in 表 7-2 and 表 7-3.

**表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage**

| RED CYCLE | GREEN CYCLE | BLUE CYCLE |
|---|---|---|
| 50% | 20% | 30% |

表 7-3. Example Landed Duty Cycle for Full-Color

| RED SCALE | GREEN SCALE | BLUE SCALE | LANDED DUTY CYCLE |
|---|---|---|---|
| 0% | 0% | 0% | 0/100 |
| 100% | 0% | 0% | 50/50 |
| 0% | 100% | 0% | 20/80 |
| 0% | 0% | 100% | 30/70 |
| 12% | 0% | 0% | 6/94 |
| 0% | 35% | 0% | 7/93 |
| 0% | 0% | 60% | 18/82 |
| 100% | 100% | 0% | 70/30 |
| 0% | 100% | 100% | 50/50 |
| 100% | 0% | 100% | 80/20 |
| 12% | 35% | 0% | 13/87 |
| 0% | 35% | 60% | 25/75 |
| 12% | 0% | 60% | 24/76 |
| 100% | 100% | 100% | 100/0 |

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

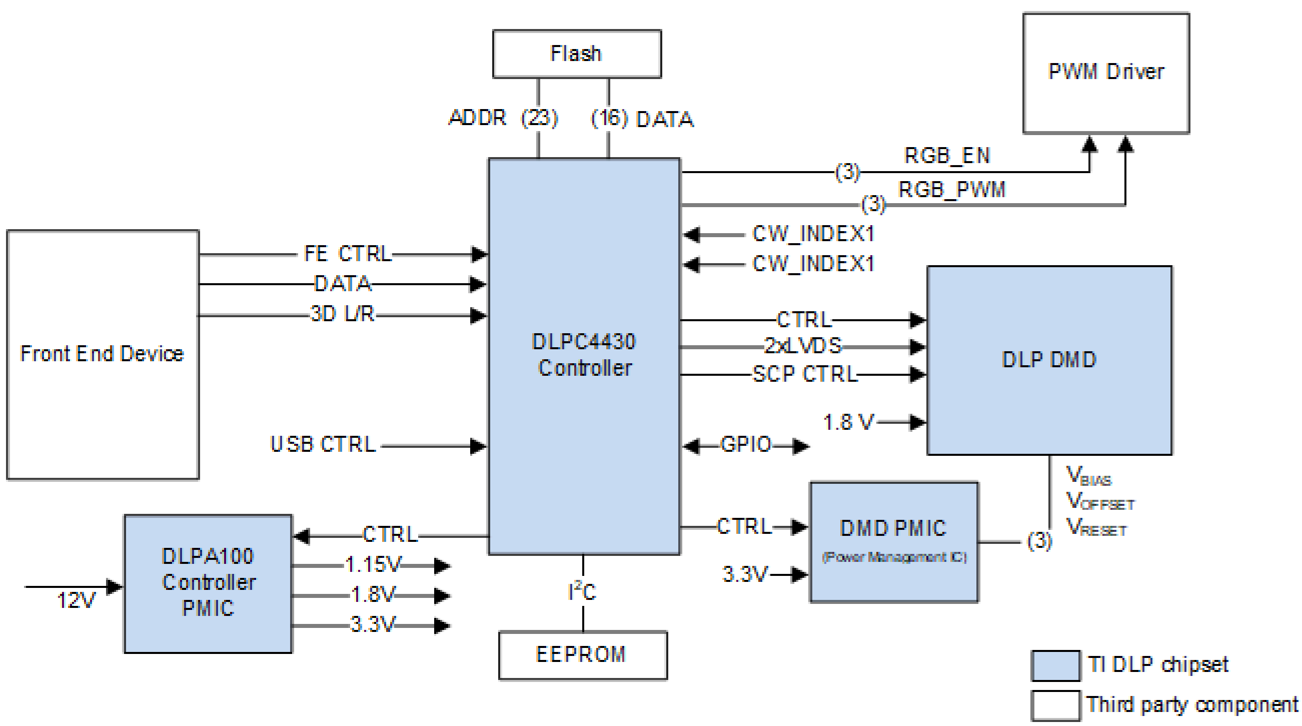
Texas Instruments DLP® technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, either towards the projection optics, or the collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP650LE include smart lighting, education projectors, and business projectors. The following orderables have been replaced by the DLP650LE:

**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) | MECHANICAL ICD |
|---|---|---|---|
| DLP650LET | FYL (149) | 32.20 mm × 22.30 mm | 2512372 |
| 1280-6434B | FYL (149) | 32.20 mm × 22.30 mm | 2512372 |
| 1280-6438B | FYL (149) | 32.20 mm × 22.30 mm | 2512372 |
| 1280-6439B | FYL (149) | 32.20 mm × 22.30 mm | 2512372 |
| 1280-643AB | FYL (149) | 32.20 mm × 22.30 mm | 2512372 |

## 8.2 Typical Application

The DLP650LE DMD combined with a DLPC4430 digital controller, DLPA100 power management device, and DLPA200 micromirror driver provides WXGA resolution for bright, colorful display applications. A typical display system using the DLP650LE and additional system components is shown in 図 8-1.



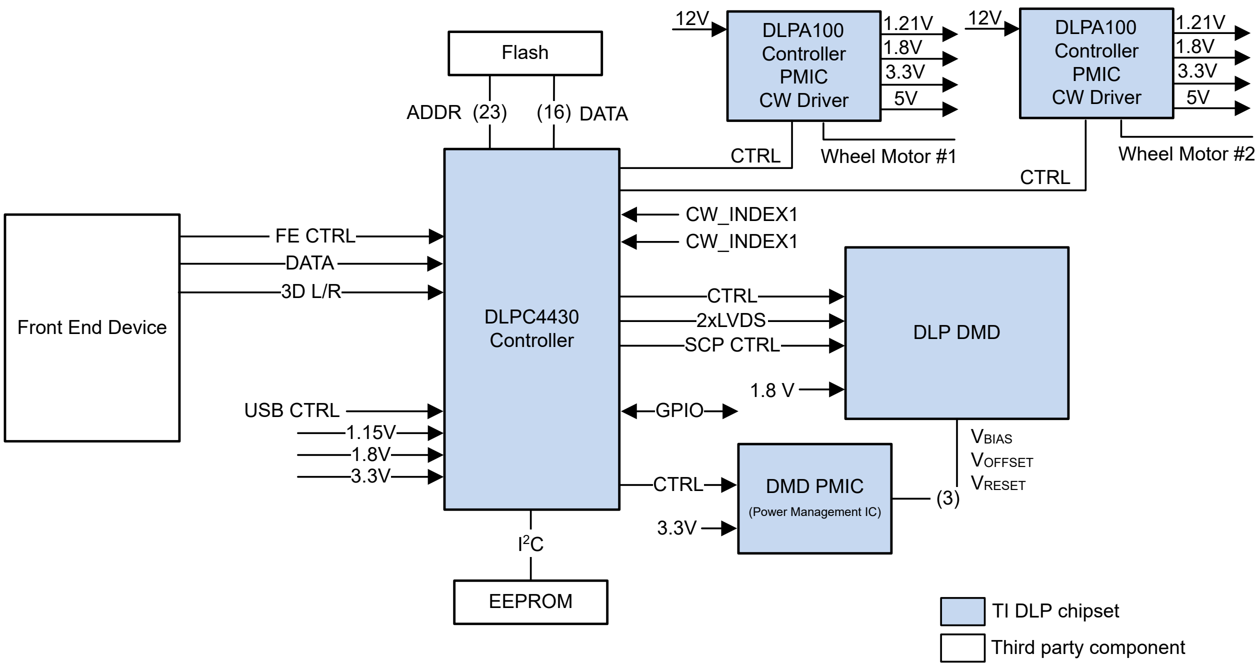



**図 8-1. Typical DLPC4430 Application (LED - top, LPCW - bottom)**

### 8.2.1 Design Requirements

The DLP 0.65 WXGA chipset can be used to create a powerful projection system. This chipset includes the DLP650LE, DLPC4430, DLPA100, and the DLPA200. The DLP650LE is used as the core imaging device in the display system and contains a 0.65-inch array of micromirrors. The DLPC4430 controller is the digital interface between the DMD and the rest of the system. The controller drives the DMD by taking the converted source data from the front end receiver and transmitting it to the DMD over a high speed interface. The DLPA100 power management device provides voltage regulators for the controller and colorwheel motor control. The DLPA200 provides the power and sequencing to drive the DLP650LE. To ensure reliable operation, the DLP650LE DMD must always be used with the DLPC4430 display controller, a DLPA100 PMIC driver, and a DLPA200 DMD micromirror driver.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

### 8.2.2 Detailed Design Procedure

For help connecting the DLPC4430 display controller and the DLP650LE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP650LE DMD, associated illumination sources, optical elements, and necessary mechanical components. The optical module is typically supplied by an optical OMM (optical module manufacturer) who specializes in designing optics for DLP projectors.

### 8.2.3 Application Curve

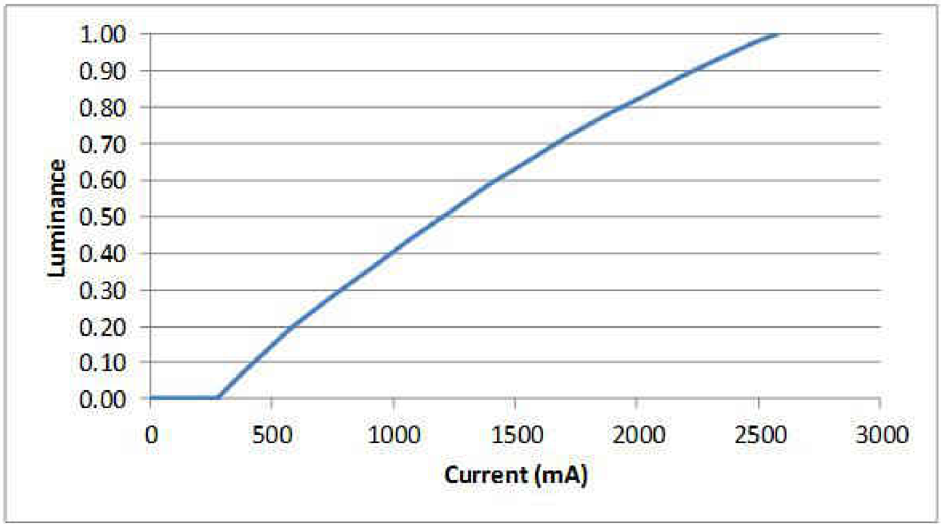



**図 8-2. Luminance vs Current**

# 9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: $V_{SS}$, $V_{BIAS}$, $V_{CC}$, $V_{CCI}$, $V_{OFFSET}$, and $V_{RESET}$. DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

注

CAUTION: For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 図 9-1 - DMD Power Supply Sequencing Requirements.

$V_{BIAS}$, $V_{CC}$, $V_{CCI}$, $V_{OFFSET}$, and $V_{RESET}$ power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Common ground $V_{SS}$ must also be connected.

## 9.1 DMD Power Supply Power-Up Procedure

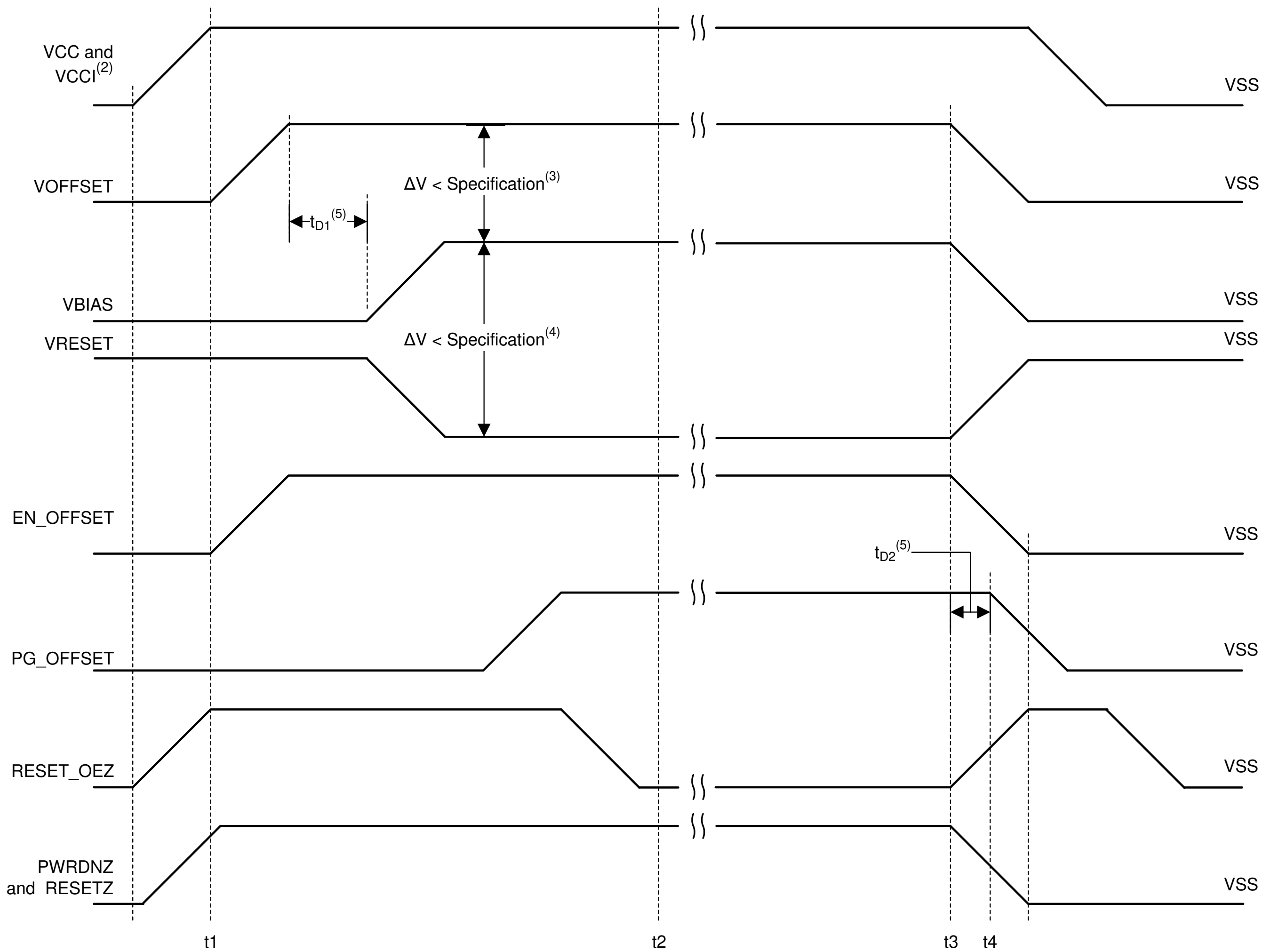
- During power-up, $V_{CC}$ and $V_{CCI}$ must always start and settle before $V_{OFFSET}$ plus the first time delay period ($t_{D1}$) specified in 表 9-2. $V_{BIAS}$, and $V_{RESET}$ voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between $V_{BIAS}$ and $V_{OFFSET}$ must be within the specified limit shown in セクション 6.4.
- During power-up, there is no requirement for the relative timing of $V_{RESET}$ with respect to $V_{BIAS}$.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-up, LVCMOS input pins must not be driven high until after $V_{CC}$ and $V_{CCI}$ have settled at operating voltages listed in セクション 6.4.

## 9.2 DMD Power Supply Power-Down Procedure

- During power-down, $V_{CC}$ and $V_{CCI}$ must be supplied until after $V_{BIAS}$, $V_{RESET}$, and $V_{OFFSET}$ are discharged to within the specified limit of ground. See 表 9-2.
- During power-down, it is a strict requirement that the voltage delta between $V_{BIAS}$ and $V_{OFFSET}$ must be within the specified limit shown in セクション 6.4.
- During power-down, there is no requirement for the relative timing of $V_{RESET}$ with respect to $V_{BIAS}$.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-down, LVCMOS input pins must be less than specified in セクション 6.4.

**表 9-1. DMD Power Supply Transition Points**

| TIME | DESCRIPTION |
|---|---|
| t1 | DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high |
| t1 | PG_OFFSET turns OFF after EN_OFFSET turns OFF per the $t_{D2}$ specification in 表 9-2. |
| t2 | DLP controller software initiates the global $V_{BIAS}$ command. |
| t3 | After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables $V_{BIAS}$, $V_{RESET}$ and $V_{OFFSET}$. |
| t4 | Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal should go high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures. |




1. Not to scale. Some details omitted for clarity. See セクション 6.4 for all specified limits and セクション 5 table for pin descriptions.
2. To prevent excess current, the supply voltage difference $|V_{CCI} – V_{CC}|$ must be less than the specified limit.
3. To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
4. To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
5. See 表 9-2 for delay time descriptions.
6. See 表 9-1 for transition time point descriptions.

**図 9-1. Power Supply Timing(1)**

**表 9-2. Delay Times Requirements**

| DELAY TIME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{D1}$ | Delay time period from $V_{OFFSET}$ settled at recommended operating voltage to $V_{BIAS}$ and $V_{RESET}$ power up. | 1 | 2 | | ms |
| $t_{D2}$ | Delay time period between PG_OFFSET hold time and when EN_OFFSET goes low | 100 | | | ns |

# 10 Device and Documentation Support

## 10.1 サード・パーティ製品に関する免責事項

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## 10.2 Device Support

### 10.2.1 Device Nomenclature

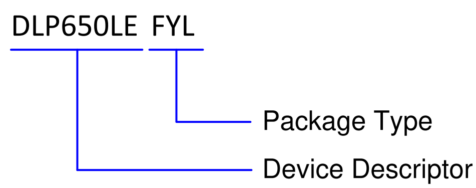


**図 10-1. Part Number Description**

### 10.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *1280-643AB GHXXXXX LLLLLLM

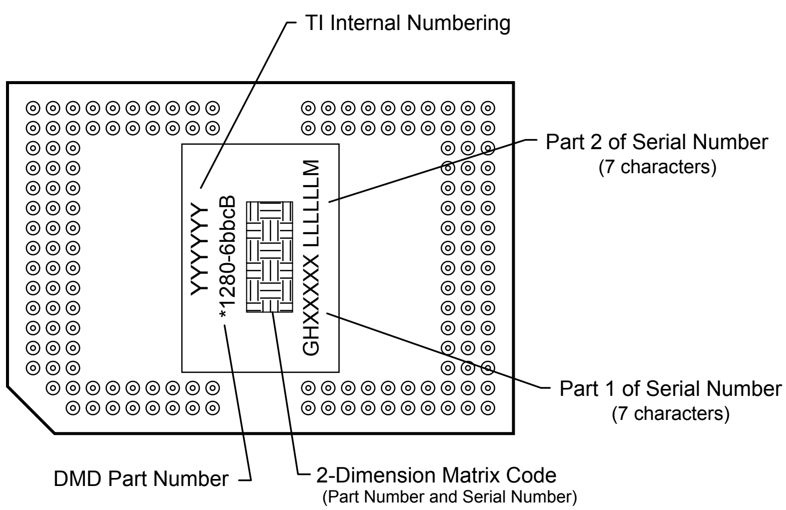


**図 10-2. DMD Marking Locations**

## 10.3 Documentation Support

### 10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP650LE:

- *DLPC4430 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*

- *DLPA200 Micromirror Driver Data Sheet*

### 10.4 ドキュメントの更新通知を受け取る方法

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### 10.5 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.8 用語集

| | |
|---|---|
| テキサス・インスツルメンツ用語集 | この用語集には、用語や略語の一覧および定義が記載されています。 |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DLP650LEFYL | ACTIVE | CLGA | FYL | 149 | 33 | RoHS & Green | NI-AU | N / A for Pkg Type | 0 to 70 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES: UNLESS OTHERWISE SPECIFIED:

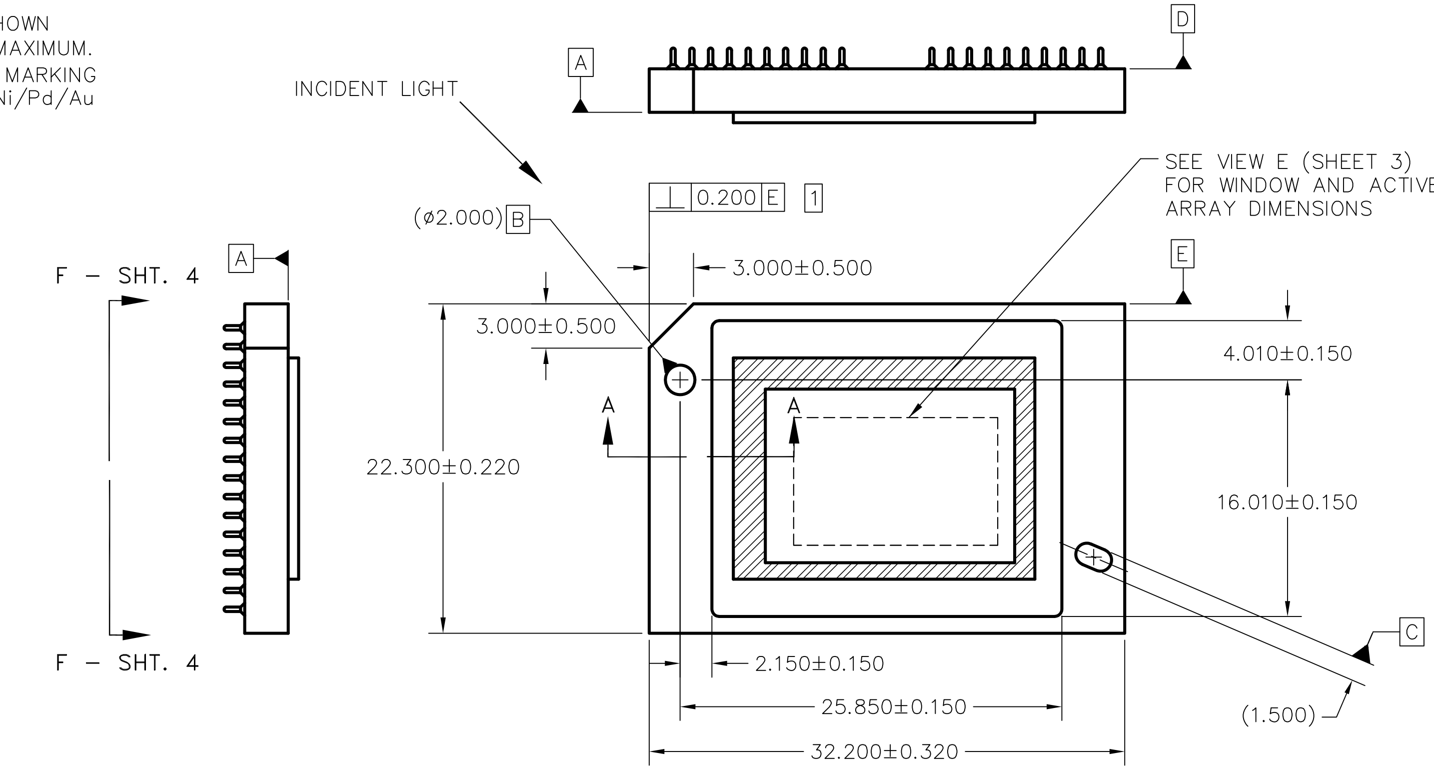
1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

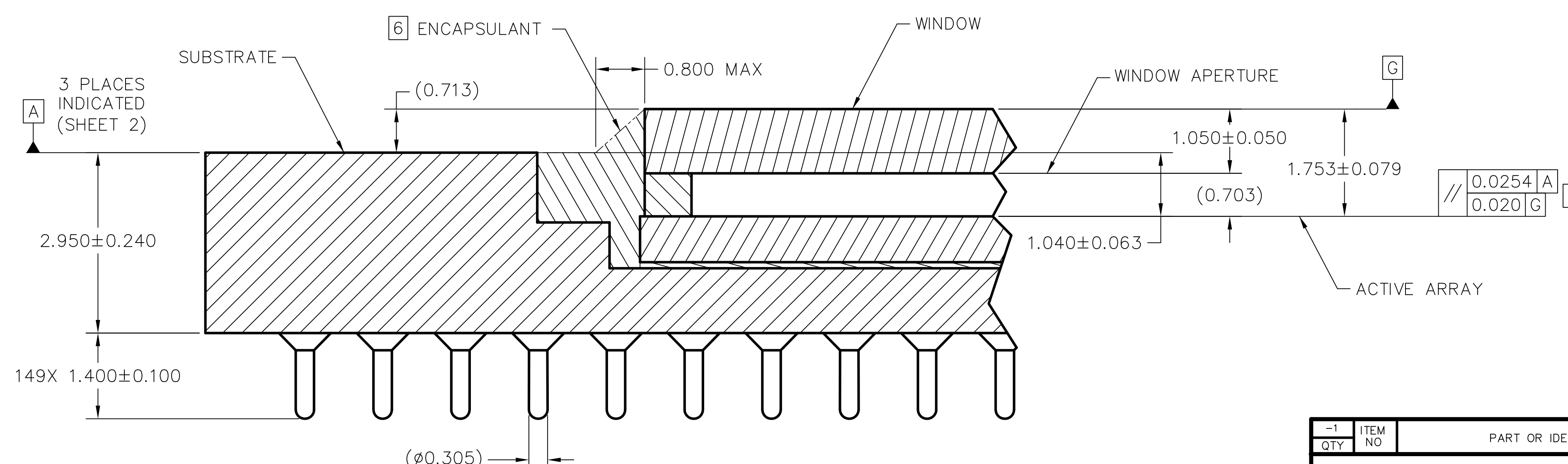


DWG NO 2512372 SH 1

REVISIONS

| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| A | ECO 2022283, INITIAL RELEASE | 02/07/12 | F. ARMSTRONG |
| B | ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD | 03/16/12 | F. ARMSTRONG |
| C | ECO 2135104, ADD NOTE 8 TO SHEETS 1 & 4 | 08/02/13 | F. ARMSTRONG |
| D | ECO 2168423, ADD FYL PACKAGE TO TITLE | 08/17/17 | M. AVERY |




SECTION A–A
SCALE 20/1

| -1 QTY | ITEM NO | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | NOTES |
|---|---|---|---|---|

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

THIRD ANGLE PROJECTION

| NONE | 0314DA |
|---|---|
| NEXT ASSY | USED ON |
| APPLICATION | |

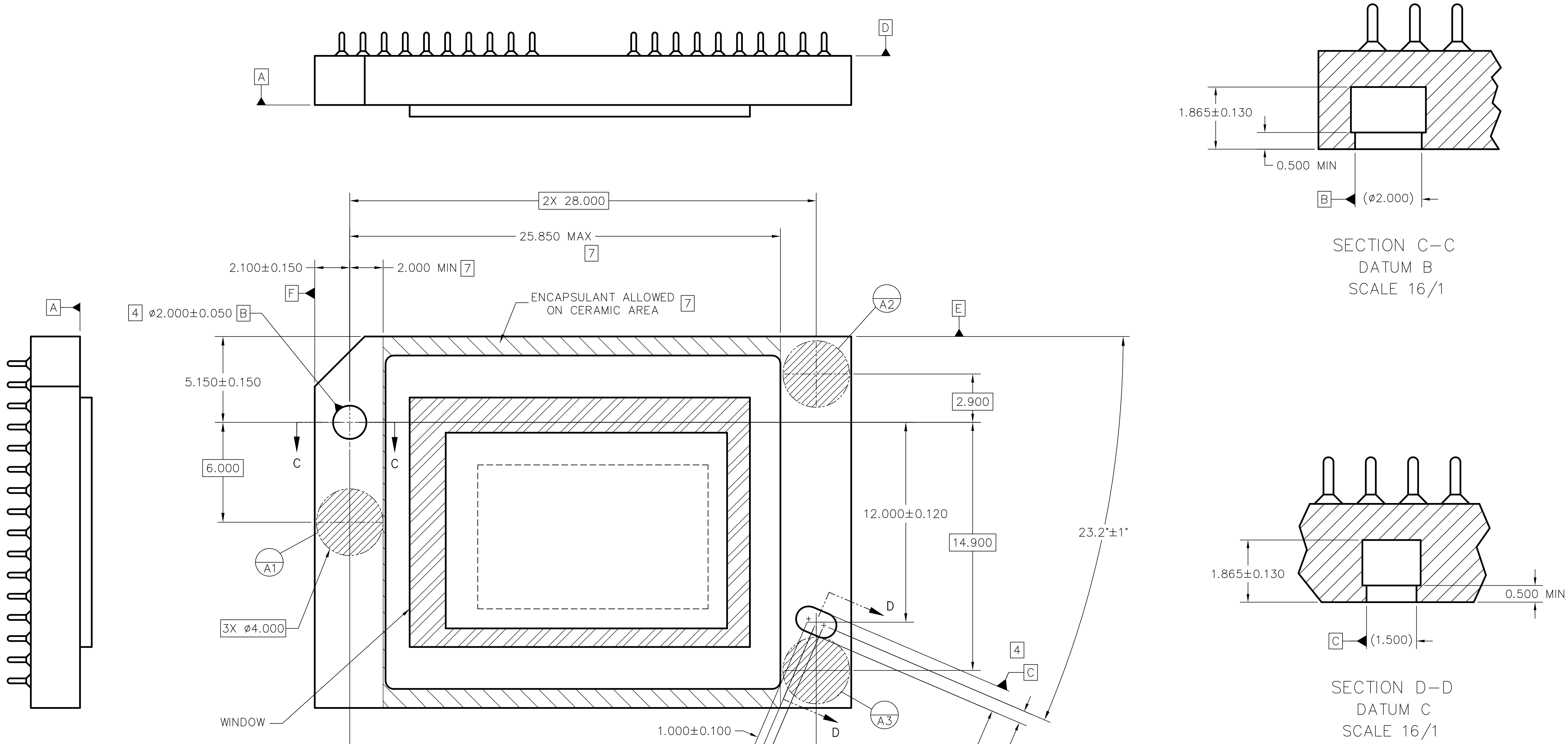
DWN F. ARMSTRONG DATE 02/07/12
ENGR F. ARMSTRONG 02/07/12
QA P. KONRAD
CQE M. DORAK

TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.65 WXGA-800 2xLVDS V2
SERIES 450 (FYL PACKAGE)

SIZE D | DRAWING NO 2512372 | REV D
SCALE 4/1 | SHEET 1 OF 4

ACED1g



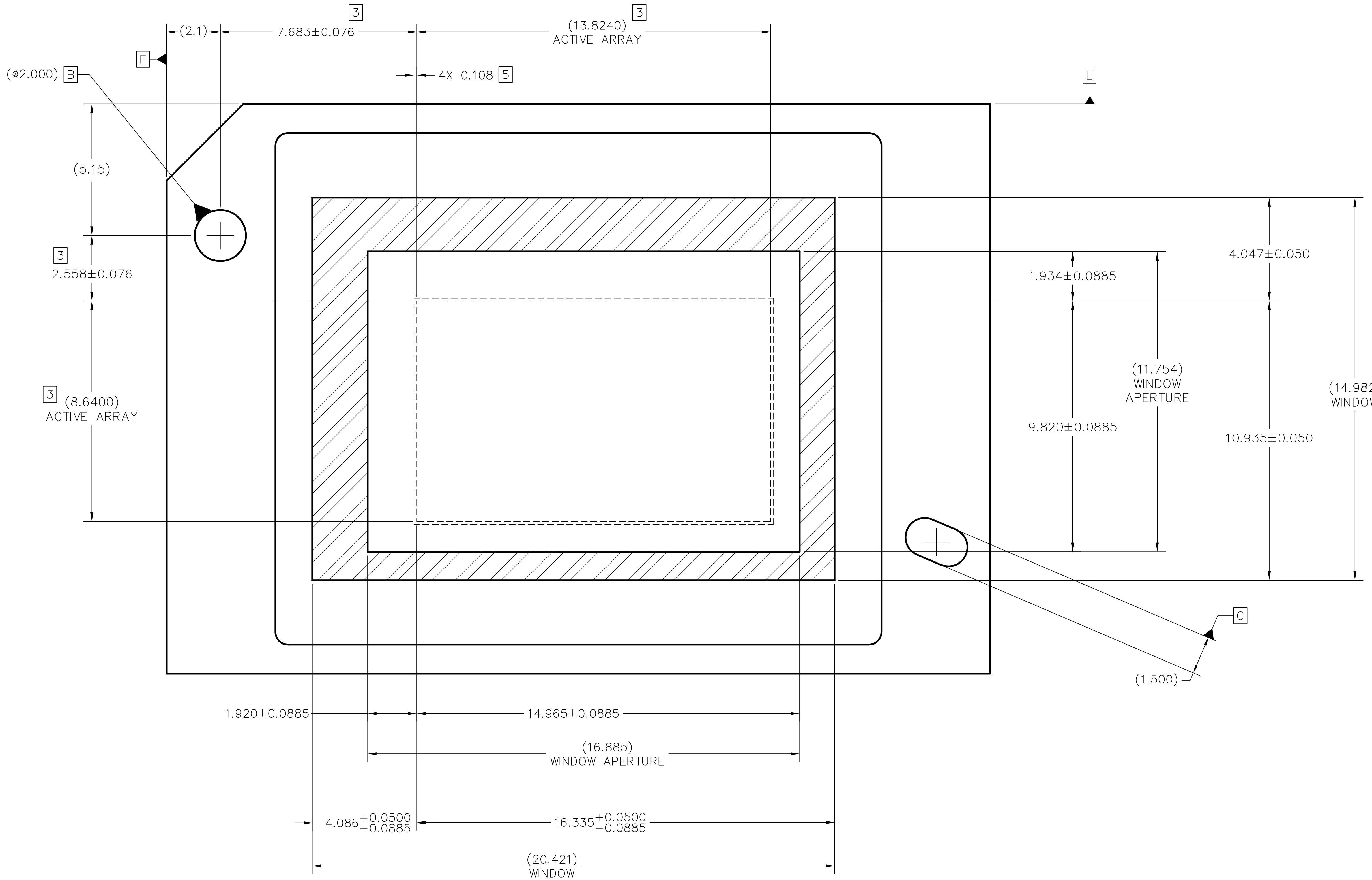

VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1

SECTION C–C
DATUM B
SCALE 16/1

SECTION D–D
DATUM C
SCALE 16/1

| TEXAS INSTRUMENTS Dallas, Texas | DWN | DATE | SIZE D | DRAWING NO 2512372 | REV D |
|---|---|---|---|---|---|
| | ISSUE DATE | | SCALE 4/1 | SHEET 2 | |

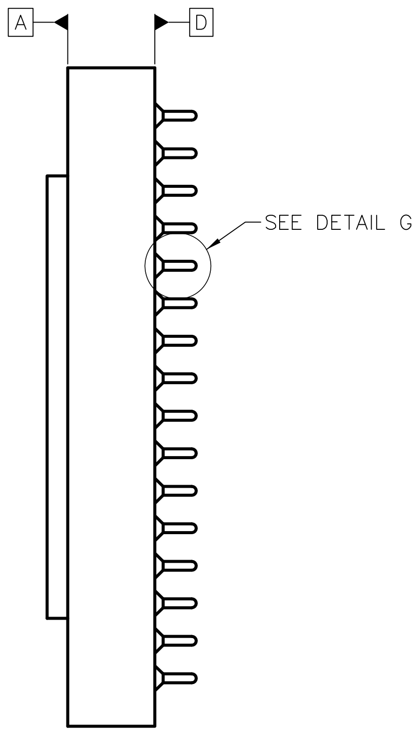
ACED2c

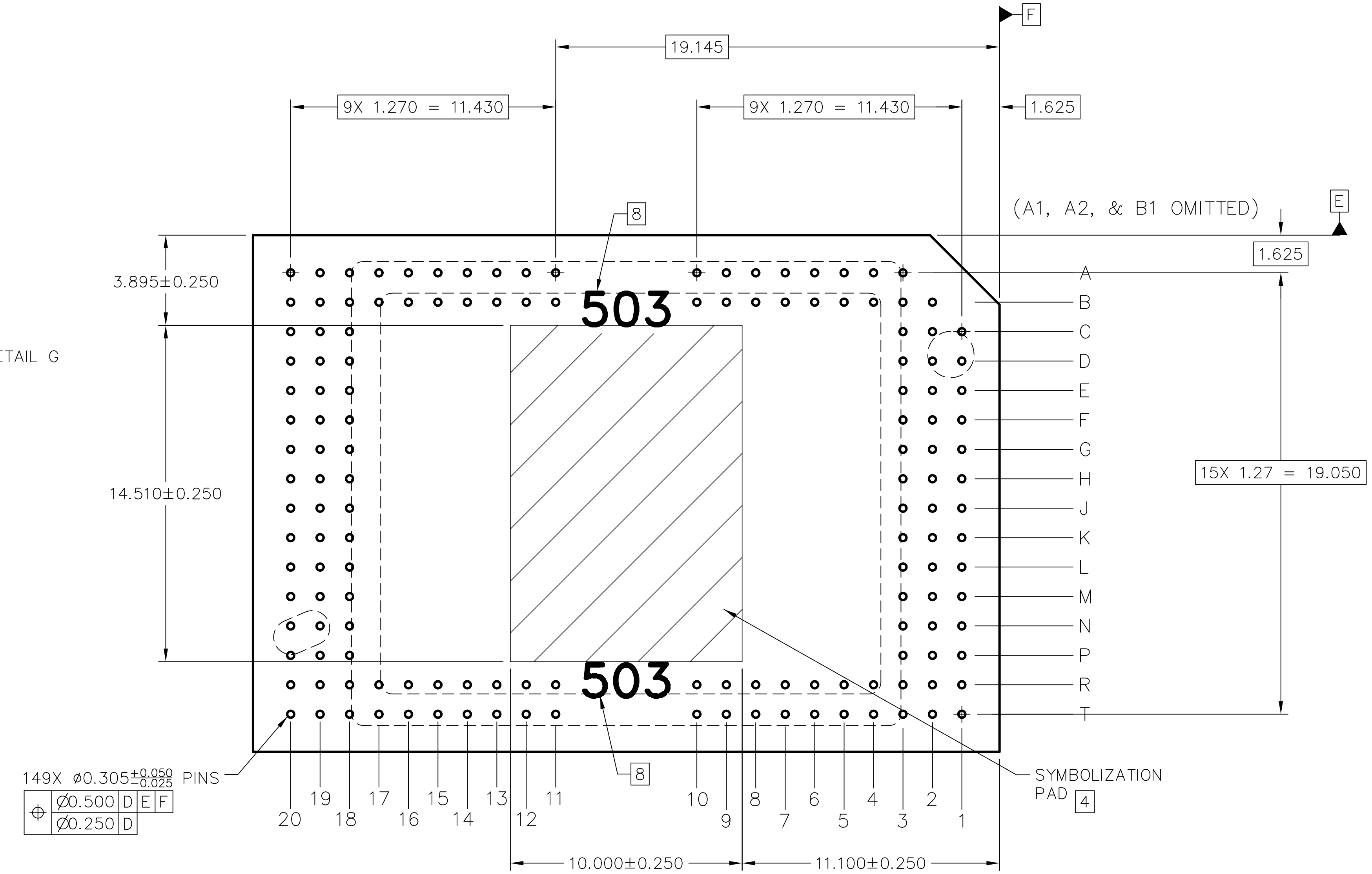



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

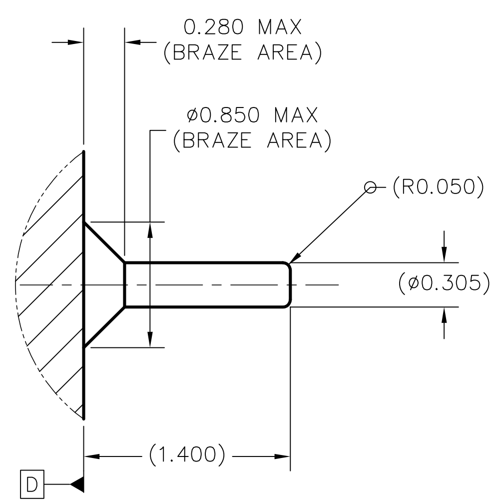
TEXAS INSTRUMENTS
Dallas, Texas

DWN DATE
ISSUE DATE
SIZE D
SCALE 4/1
DRAWING NO 2512372
REV D
SHEET 3




VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1




DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

| | | | | |
|---|---|---|---|---|
| TEXAS INSTRUMENTS Dallas, Texas | DWN / DATE | SIZE D | DRAWING NO 2512372 | REV D |
| | ISSUE DATE | SCALE 4/1 | SHEET 4 | |

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