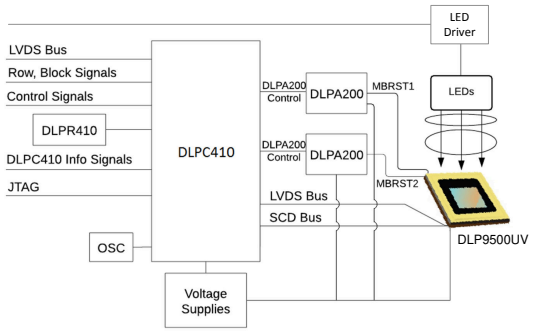
DLP9500UV DLP® 0.95 UV 1080p 2x LVDS Type A DMD

1 特長

- 対角 0.95 インチのマイクロミラー・アレイ
  - 1920 × 1080 のアルミニウム製、マイクロメートル・サイズのミラー (1080p 解像度)
  - マイクロミラー・ピッチ:10.8µm
  - マイクロミラー傾斜角:±12° (フラット状態に対して)
  - コーナー・イルミネーション (対角照射) 対応
- UV 光 で使用するよう設計:(363nm～420nm):
  - ウインドウ透過率 98% (シングル・パス、2 つのウィンドウ表面を通過)(公称値)
  - マイクロミラーの反射率 88%(公称値)
  - アレイの回折効率 85% (公称値)
  - アレイの充填率 94% (公称値)
- 4 つの 16 ビット、低電圧差動信号 (LVDS)、ダブル・データ・レート (DDR) 入力データ・バス
- 最高 400MHz の入力データ・クロック速度
- 42.2mm × 42.2mm × 7mm のパッケージ・フットプリント
- 気密パッケージ

2 アプリケーション

- 産業用:
  - ダイレクト・イメージング・リソグラフィー
  - レーザー・マーキングおよびリペア・システム
  - コンピュータ・トゥ・プレート・プリンタ
  - ラピッド・プロトタイプ・マシン
  - 3D プリンタ
- 医療用:
  - 眼科用
  - 光線療法
  - ハイパースペクトル画像処理



簡略回路図

3 概要

DLP9500UV は、デジタル制御のマイクロ電気機械システム (MEMS) 空間光変調器 (SLM) です。適切な光学系と組み合わせることで、DLP9500UV を使用して受信光の振幅、方向、位相を変調できます。

DLP95000UV チップセットは、DLP® Discovery™ 4100 プラットフォームに追加された新しいデジタル・マイクロミラー・デバイス (DMD) であり、可視スペクトルを超えて UVA スペクトル (363nm～420nm) に到達する高分解能で高性能の空間光変調を実現できます。DLP9500UV DMD には、UV の伝達に最適化された特殊な窓が設けられています。

DLP9500UV は、気密パッケージの 0.95 1080p DMD であり、23000Hz (1 ビット・バイナリ) および 1700Hz (8 ビット・グレー) を超える高いパターン速度を達成するのに必要な 1 つの専用 DLPC410 コントローラ、1 つの DLPR410 (DLP Discovery 4100 構成 PROM)、2 つの DLPA200 (DMD マイクロミラー・ドライバ) とともに販売されています。DLPC410 、DLPA200 、DLPR410 、DLP9500UV の機能ブロック図を参照してください。

DLP9500UV の機能と動作の信頼性を確保するには、チップセットのその他の部品と組み合わせて使用する必要があります。専用のチップセットにより、開発者は、マイクロミラーを高速に独立して制御することに加え、DMD へ簡単にアクセスすることができます。

DLP9500UV は、デジタル制御のマイクロ電気機械システム (MEMS) 空間光変調器 (SLM) です。適切な光学系と組み合わせることで、DLP9500UV を使用して受信光の振幅、方向、位相を変調できます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DLP9500UV	LCCC (355)	42.16mm × 42.16mm x 7.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Revision History.....2
5 概要 (続き).....4
6 Pin Configuration and Functions.....4
Pin Functions.....5
7 Specifications.....14
7.1 Absolute Maximum Ratings.....14
7.2 Storage Conditions.....14
7.3 ESD Ratings.....14
7.4 Recommended Operating Conditions.....15
7.5 Thermal Information.....17
7.6 Electrical Characteristics.....17
7.7 LVDS Timing Requirements.....18
7.8 LVDS Waveform Requirements.....19
7.9 Serial Control Bus Timing Requirements.....20
7.10 Systems Mounting Interface Loads.....21
7.11 Micromirror Array Physical Characteristics.....22
7.12 Micromirror Array Optical Characteristics.....23
7.13 Chipset Component Usage Specification.....24
8 Detailed Description.....25
8.1 Overview.....25
8.2 Functional Block Diagram.....25
8.3 Feature Description.....27
8.4 Device Functional Modes.....34
8.5 Window Characteristics and Optics.....36
8.6 Micromirror Array Temperature Calculation.....37
8.7 Micromirror Landed-On and Landed-Off Duty Cycle.....41
9 Application and Implementation.....43
9.1 Application Information.....43
9.2 Typical Application.....45
10 Power Supply Recommendations.....48
10.1 Power-Up Sequence (Handled by the DLPC410).....48
10.2 DMD Power-Up and Power-Down Procedures.....48
11 Layout.....49
11.1 Layout Guidelines.....49
11.2 Layout Example.....51
12 Device and Documentation Support.....52
12.1 Device Support.....52
12.2 Documentation Support.....53
12.3 Related Links.....53
12.4 サポート・リソース.....53
12.5 Trademarks.....53
12.6 静電気放電に関する注意事項.....53
12.7 用語集.....53
13 Mechanical, Packaging, and Orderable Information.....53

4 Revision History

Changes from Revision C (February 2017) to Revision D (April 2023) **Page**

- Changed Micromirror switching time typical value from 13 µs to 12.5 µs and removed 22 µs Max value. 23

Changes from Revision B (June 2015) to Revision C (February 2017) **Page**

- Changed the name of Micromirror clocking pulse reset in Pin Functions.....5
- Changed $T_{GRADIENT}$ from 5°C to 10°C to accommodate increase in power density from 400 to 420 nm in *セクション 7.1* 14
- Added RH name for relative humidity in *セクション 7.1* 14
- Clarified $T_{GRADIENT}$ footnote in *セクション 7.1* 14
- Changed T_{stg} to T_{DMD} in *セクション 7.2* to conform to current nomenclature.....14
- Changed typical micromirror crossover time to the time required to transition from mirror position to the other in *セクション 7.12* 23
- Added typical micromirror switching time - 13 µs in *セクション 7.12* 23
- Changed "Micromirror switching time" to "Array switching time" for clarity in *セクション 7.12* 23
- Added clarification to Micromirror switching time at 400 MHz with global reset in *セクション 7.12* 23
- Corrected number of banks of DMD mirrors to 15 in *セクション 9.2.1.1* 46
- Removed link to DLP Discovery 4100 chipset datasheet in *セクション 12.2.1* 53
- Added *セクション 12.3* table.....53

Changes from Revision A (June 2015) to Revision B (June 2015) **Page**

- 完全なデータシートをリリースし、デバイスのステータスを量産データに更新。.....1

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- チップセットの一覧の DLPR410 に DLPR4101 拡張 PROM を追加 1
- 「製品情報」の本体サイズに 7.00mm の測定値を追加。 1
- Added environmental parameters to *セクション 7.1* 14
- Moved V_{ESD} to *セクション 7.3* 14
- Added new note to *セクション 7.5* 17
- Replaced 図 7-4 20
- Changed units in *セクション 7.10* from lbs to N. 21
- Added *セクション 7.13* 24
- Corrected 6.33 W to 6.83 W in T_{Array} sample calculation 38
- Updated 図 9-3 47
- Removed *Thermal Considerations* 51

Changes from Revision * (November 2014) to Revision A () Page

- リリースのためにデバイスのステータスを製品プレビューに更新 1
- 最初のページの図を更新 1

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5 概要 (続き)

DLP9500UV は、電気的には 1920 列 × 1080 行の格子状構造の 1 ビット CMOS メモリ・セルの 2 次元配列から成ります。CMOS メモリ・アレイは、4 つの 16 ビット LVDS DDR バスにより行単位でアドレス指定されます。アドレス指定は、シリアル制御バスによって処理されます。特定の CMOS メモリ・アクセス・プロトコルは、DLPC410 デジタル・コントローラによって処理されます。

6 Pin Configuration and Functions

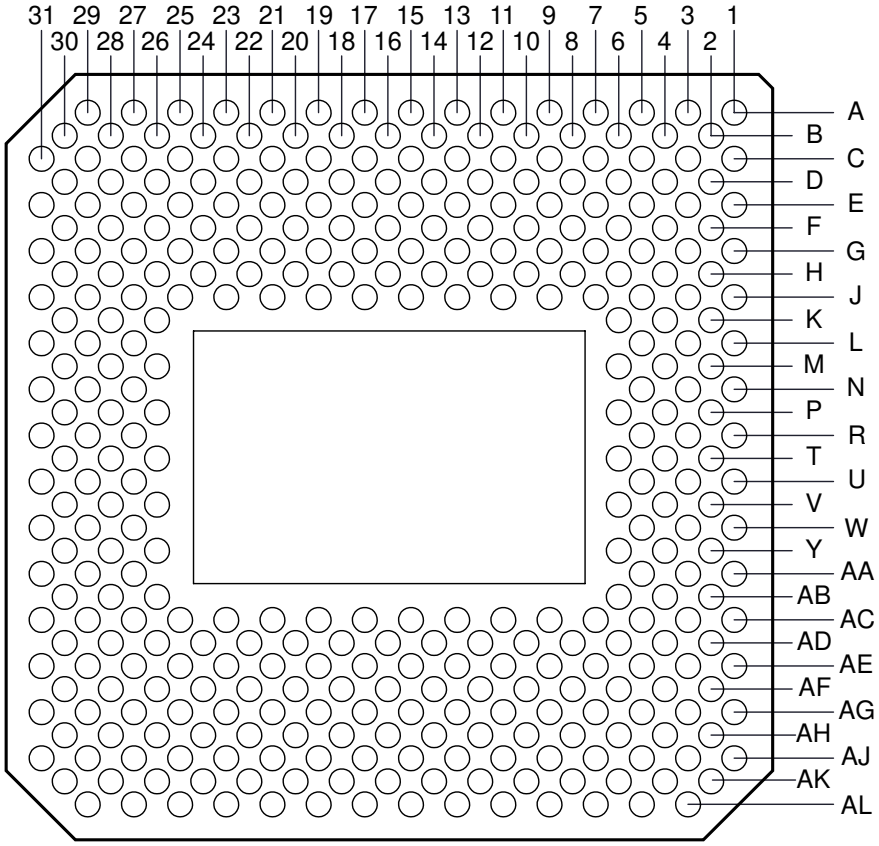


図 6-1. FLN Package 355-Pin LCCC Bottom View

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Pin Functions

PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
DATA BUS A								
D_AN(0)	F2	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A	Input data bus A (2x LVDS)	512.01
D_AN(1)	H8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		158.79
D_AN(2)	E5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		471.24
D_AN(3)	G9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		159.33
D_AN(4)	D2	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		585.41
D_AN(5)	G3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		551.17
D_AN(6)	E11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		229.41
D_AN(7)	F8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		300.54
D_AN(8)	C9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		346.35
D_AN(9)	H2	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		782.27
D_AN(10)	B10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		451.52
D_AN(11)	G15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		74.39
D_AN(12)	D14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		194.26
D_AN(13)	F14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		148.29
D_AN(14)	C17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		244.9
D_AN(15)	H16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		73.39
D_AP(0)	F4	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		509.63
D_AP(1)	H10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		152.59
D_AP(2)	E3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		464.09
D_AP(3)	G11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		152.39
D_AP(4)	D4	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		591.39
D_AP(5)	G5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		532.16
D_AP(6)	E9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		230.78
D_AP(7)	F10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		300.61
D_AP(8)	C11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		338.16
D_AP(9)	H4	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		773.17
D_AP(10)	B8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		449.57
D_AP(11)	H14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A	Input data bus A (2x LVDS)	71.7
D_AP(12)	D16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		198.69
D_AP(13)	F16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		143.72
D_AP(14)	C15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		240.14
D_AP(15)	G17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		74.05

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
DATA BUS B								
D_BN(0)	AH2	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B	Input data bus B (2x LVDS)	525.25
D_BN(1)	AD8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		190.59
D_BN(2)	AJ5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		525.25
D_BN(3)	AE3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		494.91
D_BN(4)	AG9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		222.67
D_BN(5)	AE11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		205.45
D_BN(6)	AH10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		309.05
D_BN(7)	AF10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		285.62
D_BN(8)	AK8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		483.58
D_BN(9)	AG5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		711.58
D_BN(10)	AL11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		462.21
D_BN(11)	AE15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		74.39
D_BN(12)	AH14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		194.26
D_BN(13)	AF14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		156
D_BN(14)	AJ17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		247.9
D_BN(15)	AD16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		111.52
D_BP(0)	AH4	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		525.02
D_BP(1)	AD10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		190.61
D_BP(2)	AJ3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		524.22
D_BP(3)	AE5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		476.07
D_BP(4)	AG11	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		222.8
D_BP(5)	AE9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		219.48
D_BP(6)	AH8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		306.55
D_BP(7)	AF8	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		298.04
D_BP(8)	AK10	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		480.31
D_BP(9)	AG3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B	Input data bus B (2x LVDS)	727.18
D_BP(10)	AL9	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		461.02
D_BP(11)	AD14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		71.35
D_BP(12)	AH16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		197.69
D_BP(13)	AF16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		150.38
D_BP(14)	AJ15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		243.14
D_BP(15)	AE17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		113.36

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
DATA BUS C								
D_CN(0)	B14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C	Input data bus C (2x LVDS)	459.04
D_CN(1)	E15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		342.79
D_CN(2)	A17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		456.22
D_CN(3)	G21	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		68.24
D_CN(4)	B20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		362.61
D_CN(5)	F20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		163.07
D_CN(6)	D22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		204.16
D_CN(7)	G23	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		105.59
D_CN(8)	B26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		450.51
D_CN(9)	F28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		302.04
D_CN(10)	C29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		429.8
D_CN(11)	G27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		317.1
D_CN(12)	D26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		276.76
D_CN(13)	H28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		186.78
D_CN(14)	E29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		311.3
D_CN(15)	J29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		262.62
D_CP(0)	B16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		463.64
D_CP(1)	E17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		347.65
D_CP(2)	A15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		456.45
D_CP(3)	H20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		67.72
D_CP(4)	B22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		362.76
D_CP(5)	F22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		161.69

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_CP(6)	D20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C	Input data bus C (2x LVDS)	195.09
D_CP(7)	H22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		104.86
D_CP(8)	B28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		451.41
D_CP(9)	F26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		294.22
D_CP(10)	C27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		429.68
D_CP(11)	G29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		314.98
D_CP(12)	D28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		276.04
D_CP(13)	H26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		186.25
D_CP(14)	E27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		312.07
D_CP(15)	J27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		262.94
DATA BUS D								
D_DN(0)	AK14	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D	Input data bus D (2x LVDS)	492.53
D_DN(1)	AG15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		342.78
D_DN(2)	AL17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		491.83
D_DN(3)	AE21	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		74.24
D_DN(4)	AK20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		356.23
D_DN(5)	AF20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		163.07
D_DN(6)	AH22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		204.16
D_DN(7)	AE23	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		105.59
D_DN(8)	AK26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		450.51
D_DN(9)	AF28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		302.04
D_DN(10)	AJ29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		429.8
D_DN(11)	AE27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		298.87

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
D_DN(12)	AH26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D	Input data bus D (2x LVDS)	276.76
D_DN(13)	AD28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		186.78
D_DN(14)	AG29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		311.3
D_DN(15)	AC29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		262.62
D_DP(0)	AK16	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		495.13
D_DP(1)	AG17	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		342.47
D_DP(2)	AL15	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		492.06
D_DP(3)	AD20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		67.72
D_DP(4)	AK22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		356.37
D_DP(5)	AF22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		161.98
D_DP(6)	AH20	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		195.09
D_DP(7)	AD22	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		102.86
D_DP(8)	AK28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		451.41
D_DP(9)	AF26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		296.7
D_DP(10)	AJ27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		429.68
D_DP(11)	AE29	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		302.74
D_DP(12)	AH28	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		276.04
D_DP(13)	AD26	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		186.25
D_DP(14)	AG27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		312.07
D_DP(15)	AC27	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		262.94

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
DATA CLOCKS								
DCLK_AN	D10	Input	LVCMOS	—	Differentially terminated – 100 Ω	—	Input data bus A Clock (2x LVDS)	325.8
DCLK_AP	D8	Input	LVCMOS	—	Differentially terminated – 100 Ω	—		319.9
DCLK_BN	AJ11	Input	LVCMOS	—	Differentially terminated – 100 Ω	—	Input data bus B Clock (2x LVDS)	318.92
DCLK_BP	AJ9	Input	LVCMOS	—	Differentially terminated – 100 Ω	—		318.74
DCLK_CN	C23	Input	LVCMOS	—	Differentially terminated – 100 Ω	—	Input data bus C Clock (2x LVDS)	252.01
DCLK_CP	C21	Input	LVCMOS	—	Differentially terminated – 100 Ω	—		241.18
DCLK_DN	AJ23	Input	LVCMOS	—	Differentially terminated – 100 Ω	—	Input data bus D Clock (2x LVDS)	252.01
DCLK_DP	AJ21	Input	LVCMOS	—	Differentially terminated – 100 Ω	—		241.18
DATA CONTROL INPUTS								
SCTRL_AN	J3	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A	Serial control for data bus A (2x LVDS)	608.14
SCTRL_AP	J5	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_A		607.45
SCTRL_BN	AF4	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B	Serial control for data bus B (2x LVDS)	698.12
SCTRL_BP	AF2	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_B		703.8
SCTRL_CN	E23	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C	Serial control for data bus C (2x LVDS)	232.46
SCTRL_CP	E21	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_C		235.21
SCTRL_DN	AG23	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D	Serial control for data bus D (2x LVDS)	235.53
SCTRL_DP	AG21	Input	LVCMOS	DDR	Differentially terminated – 100 Ω	DCLK_D		235.66
SERIAL COMMUNICATION AND CONFIGURATION								
SCPCLK	AE1	Input	LVCMOS	—	pull-down	—	Serial port clock	324.26
SCPDO	AC3	Output	LVCMOS	—	—	SCP_CLK	Serial port output	281.38
SCPDI	AD2	Input	LVCMOS	—	pull-down	SCP_CLK	Serial port input	261.55
$\overline{\text{SCPEN}}$	AD4	Input	LVCMOS	—	pull-down	SCP_CLK	Serial port enable	184.86
$\overline{\text{PWRDN}}$	B4	Input	LVCMOS	—	pull-down	—	Device reset	458.78
MODE_A	J1	Input	LVCMOS	—	pull-down	—	Data bandwidth mode select	471.57
MODE_B	G1	Input	LVCMOS	—	pull-down	—		521.99

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
MICROMIRROR CLOCKING PULSE (BIAS RESET)								
MBRST(0)	L5	Input	Analog	—	—	—	Micromirror clocking pulse reset MBRST signals clock micromirrors into state of LVCMOS memory cell associated with each mirror.	898.97
MBRST(1)	M28	Input	Analog	—	—	—		621.98
MBRST(2)	P4	Input	Analog	—	—	—		846.88
MBRST(3)	P30	Input	Analog	—	—	—		784.18
MBRST(4)	L3	Input	Analog	—	—	—		763.34
MBRST(5)	P28	Input	Analog	—	—	—		749.61
MBRST(6)	P2	Input	Analog	—	—	—		878.25
MBRST(7)	T28	Input	Analog	—	—	—		783.83
MBRST(8)	M4	Input	Analog	—	—	—		969.36
MBRST(9)	L29	Input	Analog	—	—	—		621.24
MBRST(10)	T4	Input	Analog	—	—	—		918.43
MBRST(11)	N29	Input	Analog	—	—	—		685.14
MBRST(12)	N3	Input	Analog	—	—	—		812.31
MBRST(13)	L27	Input	Analog	—	—	—		591.89
MBRST(14)	R3	Input	Analog	—	—	—		878.5
MBRST(15)	V28	Input	Analog	—	—	—		660.15
MBRST(16)	V4	Input	Analog	—	—	—		848.64
MBRST(17)	R29	Input	Analog	—	—	—		796.31
MBRST(18)	Y4	Input	Analog	—	—	—		715
MBRST(19)	AA27	Input	Analog	—	—	—		604.35
MBRST(20)	W3	Input	Analog	—	—	—		832.39
MBRST(21)	W27	Input	Analog	—	—	—		675.21
MBRST(22)	AA3	Input	Analog	—	—	—		861.18
MBRST(23)	W29	Input	Analog	—	—	—		662.66
MBRST(24)	U5	Input	Analog	—	—	—		850.06
MBRST(25)	U29	Input	Analog	—	—	—		726.56
MBRST(26)	Y2	Input	Analog	—	—	—		861.48
MBRST(27)	AA29	Input	Analog	—	—	—		683.83
MBRST(28)	U3	Input	Analog	—	—	—		878.5
MBRST(29)	Y30	Input	Analog	—	—	—		789.2

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
POWER								
VCC	A3, A5, A7, A9, A11, A13, A21, A23, A25, A27, A29, B2, C1, C31, E31, G31, J31, K2, L31, N31, R31, U31, W31, AA31, AC1, AC31, AE31, AG1, AG31, AJ31, AK2, AK30, AL3, AL5, AL7, AL19, AL21, AL23, AL25, AL27	Power	Analog	—	—	—	Power for LVCMOS logic	—
VCCI	H6, H12, H18, H24, M6, M26, P6, P26, T6, T26, V6, V26, Y6, Y26, AD6, AD12, AD18, AD24	Power	Analog	—	—	—	Power supply for LVDS Interface	—
VCC2	L1, N1, R1, U1, W1, AA1	Power	Analog	—	—	—	Power for high voltage CMOS logic	—
VSS	A1, B12, B18, B24, B30, C7, C13, C19, C25, D6, D12, D18, D24, D30, E1, E7, E13, E19, E25, F6, F12, F18, F24, F30, G7, G13, G19, G25, K4, K6, K26, K28, K30, M2, M30, N5, N27, R5, T2, T30, U27, V2, V30, W5, Y28, AB2, AB4, AB6, AB26, AB28, AB30, AD30, AE7, AE13, AE19, AE25, AF6, AF12, AF18, AF24, AF30, AG7, AG13, AG19, AG25, AH6, AH12, AH18, AH24, AH30, AJ1, AJ7, AJ13, AJ19, AJ25, AK6, AK12, AK18, AL29	Power	Analog	—	—	—	Common return for all power inputs	—

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PIN (1)		TYPE (I/O/P)	SIGNAL	DATA RATE (2)	INTERNAL TERM (3)	CLOCK	DESCRIPTION	TRACE (MILS)
NAME	NO.							
RESERVED SIGNALS (NOT FOR USE IN SYSTEM)								
RESERVED_FC	J7	Input	LVCMOS	—	pull-down	—	Pins should be connected to VSS	—
RESERVED_FD	J9	Input	LVCMOS	—	pull-down	—		—
RESERVED_PFE	J11	Input	LVCMOS	—	pull-down	—		—
RESERVED_STM	AC7	Input	LVCMOS	—	pull-down	—		—
RESERVED_AE	C3	Input	LVCMOS	—	pull-down	—		—
NO_CONNECT	A19, B6, C5, H30, J13, J15, J17, J19, J21, J23, J25, R27, AA5, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC5, AC9, AK24, AK4, AL13	—	—	—	—	—	No connection (any connection to these terminals may result in undesirable effects)	—

(1) The following power supplies are required to operate the DMD: VCC, VCC1, VCC2. VSS must also be connected.
(2) DDR = Double Data Rate. SDR = Single Data Rate. Refer to the *セクション 7.7* for specifications and relationships.
(3) Refer to *セクション 7.6* for differential termination specification.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted). (1)

		MIN	MAX	UNIT
ELECTRICAL				
V_{CC}	Voltage applied to V_{CC} (2) (3)	–0.5	4	V
V_{CCI}	Voltage applied to V_{CCI} (2) (3)	–0.5	4	V
V_{CC2}	Voltage applied to V_{VCC2} (2) (3) (4)	–0.5	9	V
V_{MBRST}	Clocking pulse waveform voltage applied to MBRST[29:0] input pins (supplied by DLPA200s)	–28	28	V
$\lvert V_{CC} – V_{CCI} \rvert$	Supply voltage delta (absolute value) (4)		0.3	V
	Voltage applied to all other input terminals (2)	–0.5	V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Maximum differential voltage, damage can occur to internal termination resistor if exceeded, see 図 7-3		700	mV
	Current required from a high-level output, V_{OH} = 2.4 V		–20	mA
	Current required from a low-level output, V_{OL} = 0.4 V		15	mA
ENVIRONMENTAL				
T_{ARRAY}	Array temperature – operational (5)	20	30	°C
	Array temperature – non-operational (5)	–40	80	°C
T_{DELTA}	Absolute temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1 (6)		10	°C
RH	Relative humidity (non-condensing)		95	%

(1) Stresses beyond those listed under *セクション 7.4* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.4*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS} (ground).
(3) Voltages V_{CC}, V_{CCI}, and V_{CC2} are required for proper DMD operation.
(4) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. The difference between V_{CC} and V_{CCI}, $\lvert V_{CC} – V_{CCI} \rvert$, should be less than the specified limit.
(5) The worst-case temperature of any test point shown in *図 8-11*, or the active array as calculated by the *セクション 8.6.2*.
(6) As either measured, predicted, or both between any two points - measured on the exterior of the package, or as predicted at any point inside the micromirror array cavity. Refer to *セクション 8.6.2*.

7.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{DMD}	Storage temperature	–40	80	°C
RH	Storage humidity (non-condensing)		95	%

7.3 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except MBRST[29:0]	±2000	V
			MBRST[29:0] pins	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

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7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT	
ELECTRICAL (2) (3)						
V_{CC}	Supply voltage for LVCMOS core logic	3.0	3.3	3.6	V	
V_{CC1}	Supply voltage for LVDS receivers	3.0	3.3	3.6	V	
V_{CC2}	Mirror electrode and HVCMOS supply voltage	8.25	8.5	8.75	V	
VMBRST	Clocking Pulse Waveform Voltage applied to MBRST[29:0] Input Pins (supplied by DLPA200s)	-27		26.5	V	
|VCCI–VCC|	Supply voltage delta (absolute value) (4)			0.3	V	
ENVIRONMENTAL (5) For Illumination Source Between 420 nm and 700 nm						
T_{ARRAY}	Array temperature, Long–term operational (12) (7) (6) (8)	20	25-45	65 (13)	°C	
	Array temperature, Short–term operational (12) (7) (9)	0		20		
T_{WINDOW}	Window temperature test points TP2 and TP3, Long-term operational(8).	10		70	°C	
$\|T_{DELTA}\|$	Absolute temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1.(11)			10	°C	
ILL_{VIS}	Illumination(10)			Thermally limited	W/cm^2	
ENVIRONMENTAL (5) For Illumination Source Between 400 nm and 420 nm						
T_{ARRAY}	Array temperature, Long–term operational (12) (7) (6) (8)	20		30	°C	
T_{WINDOW}	Window temperature test points TP2 and TP3, Long-term operational(8)			30	°C	
$\|T_{DELTA}\|$	Absolute temperature delta between the window test points (TP2, TP3) and the ceramic test point TP1.(11)			10	°C	

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over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT	
ILL	Illumination(10)			11	W/cm^2
				26.6	W
ENVIRONMENTAL (5) For Illumination Source <400 nm and >700 nm					
T_{ARRAY}	Array temperature, Long–term operational (12) (7) (6) (8)	20		40 (13)	°C
	Array temperature, Short–term operational (12) (7) (9)	0		20	°C
T_{WINDOW}	Window temperature test points TP2 and TP3, Long-term operational(8)	10		70	°C
ILL	Illumination(10)			10	mW/cm^2

(1) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(2) Voltages V_{CC}, V_{CC1}, and V_{CC2} are required for proper DMD operation. V_{SS} must also be connected.
(3) All voltages are referenced to common ground V_{SS}.
(4) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CC1} may result in excess current draw. The difference between VCC and V_{CC1}, $|V_{CC} – V_{CC1}|$, should be less than the specified limit.
(5) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(6) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 8-11 and the package thermal resistance in *セクション 7.5* using Micromirror Array Temperature CalculationMicromirror Array Temperature Calculation.
(8) Long-term is defined as the usable life of the device.
(9) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(10) Total integrated illumination power density on the array in the indicated wavelength range.
(11) The temperature delta is the highest difference between the ceramic test point (TP1) and window test points (TP2) and (TP3) in 図 8-11.
(12) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See Micromirror Array Temperature Calculation for further details.
(13) Per 図 7-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *セクション 8.7* for a definition of micromirror landed duty cycle.

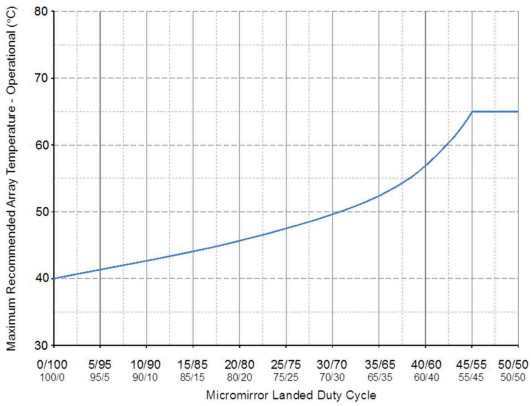


図 7-1. Max Recommended DMD Temperature – Derating Curve

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7.5 Thermal Information

THERMAL METRIC	DLP9500UV FLN (LCCC) 355 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1) (1)	0.5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the セクション 7.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

7.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (1), See 図 8-4	V_{CC} = 3 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage (1), See 図 8-4	V_{CC} = 3.6 V, I_{OH} = 15 mA			0.4	V
V_{MBRST}	Clocking pulse waveform applied to MBRST[29:0] input pins (supplied by DLPA200s)		–27		26.5	V
I_{OZ}	High-impedance output current (1)	V_{CC} = 3.6 V			10	µA
I_{OH}	High-level output current (1)	V_{OH} = 2.4 V, V_{CC} ≥ 3 V			–20	mA
		V_{OH} = 1.7 V, V_{CC} ≥ 2.25 V			–15	
I_{OL}	Low-level output current (1)	V_{OL} = 0.4 V, V_{CC} ≥ 3 V			15	mA
		V_{OL} = 0.4 V, V_{CC} ≥ 2.25 V			14	
V_{IH}	High-level input voltage (1)		1.7		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (1)		–0.3		0.7	V
I_{IL}	Low-level input current (1)	V_{CC} = 3.6 V, V_I = 0 V			–60	µA
I_{IH}	High-level input current (1)	V_{CC} = 3.6 V, V_I = V_{CC}			60	µA
I_{CC}	Current into V_{CC} pin	V_{CC} = 3.6 V,			2990	mA
I_{CCI}	Current into V_{OFFSET} pin (2)	V_{CCI} = 3.6 V			910	mA
I_{CC2}	Current into V_{CC2} pin	V_{CC2} = 8.75 V			25	mA
P_D	Power dissipation			4.4		W
Z_{IN}	Internal differential impedance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB, trace)		90	100	110	Ω
C_I	Input capacitance (1)	f = 1 MHz			10	pF
C_O	Output capacitance (1)	f = 1 MHz			10	pF
C_{IM}	Input capacitance for MBRST[29:0] pins	f = 1 MHz	270		355	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw (See *セクション 7.1* for details).

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7.7 LVDS Timing Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-2

		MIN	NOM	MAX	UNIT
f_{DCLK_x}	DCLK_x clock frequency (where *x* = [A, B, C, or D])	200		400	MHz
t_c	Clock cycle - DLCK_x	2.5			ns
t_w	Pulse duration - DLCK_x		1.25		ns
t_s	Setup time - D_x[15:0] and SCTRL_x before DCLK_x	0.35			ns
t_h	Hold time, D_x[15:0] and SCTRL_x after DCLK_x	0.35			ns
t_{skew}	Skew between any two buses (A ,B, C, and D)	–1.25		1.25	ns

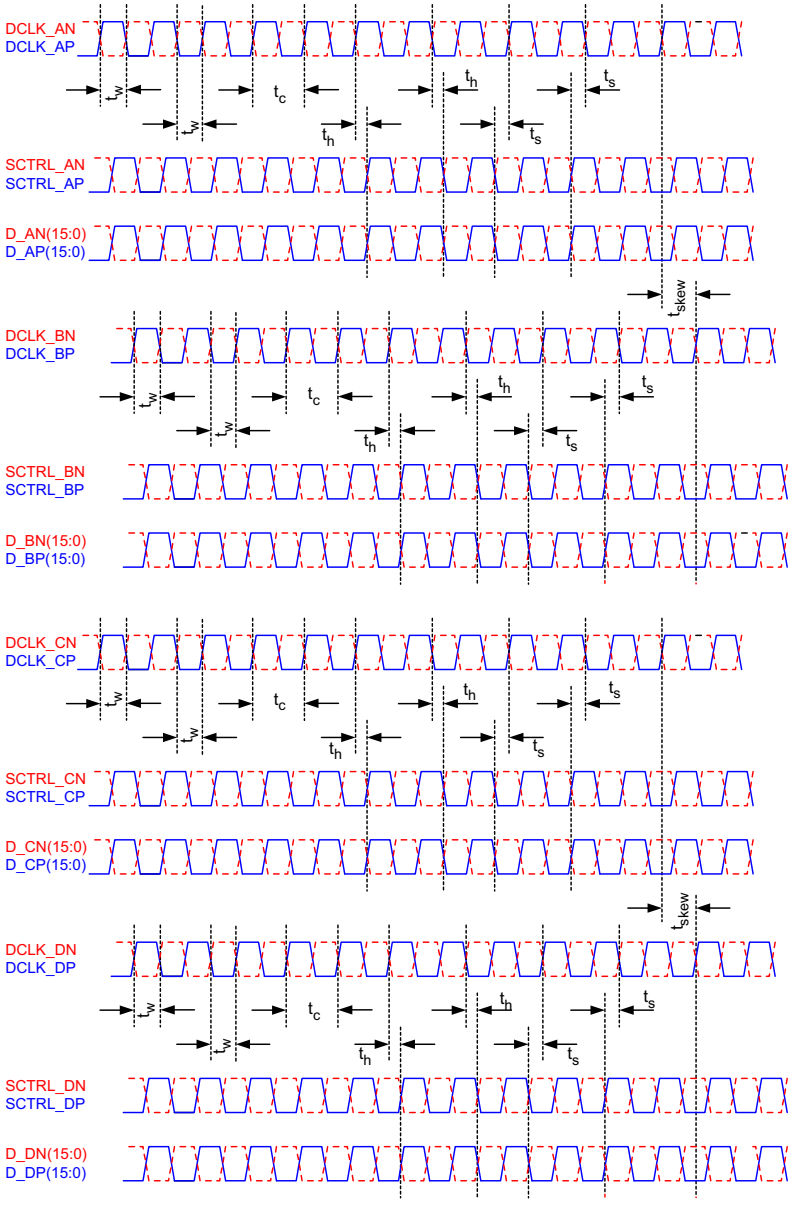


図 7-2. LVDS Timing Waveforms

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7.8 LVDS Waveform Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-3

		MIN	NOM	MAX	UNIT
$\|V_{ID}\|$	Input differential voltage (absolute difference)	100	400	600	mV
V_{CM}	Common mode voltage		1200		mV
V_{LVDS}	LVDS voltage	0		2000	mV
t_r	Rise time (20% to 80%)	100		400	ps
t_r	Fall time (80% to 20%)	100		400	ps

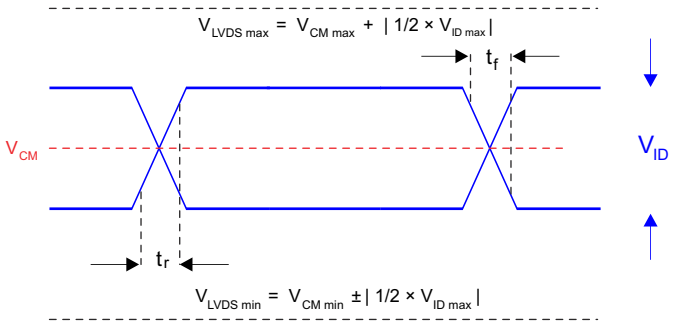


図 7-3. LVDS Waveform Requirements

7.9 Serial Control Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted); see 図 7-4 and 図 7-5

		MIN	NOM	MAX	UNIT
f_{SCP_CLK}	SCP clock frequency	50		500	kHz
t_{SCP_SKEW}	Time between valid SCP_DI and rising edge of SCP_CLK	–300		300	ns
t_{SCP_DELAY}	Time between valid SCP_DO and rising edge of SCP_CLK			960	ns
$t_{\overline{SCP_EN}}$	Time between falling edge of $\overline{SCP_EN}$ and the first rising edge of SCP_CLK	30			ns
$t_{_SCP}$	Rise time for SCP signals			200	ns
t_{f_SCP}	Fall time for SCP signals			200	ns

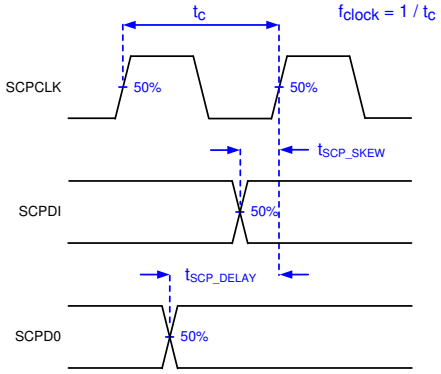


図 7-4. Serial Communications Bus Timing Parameters

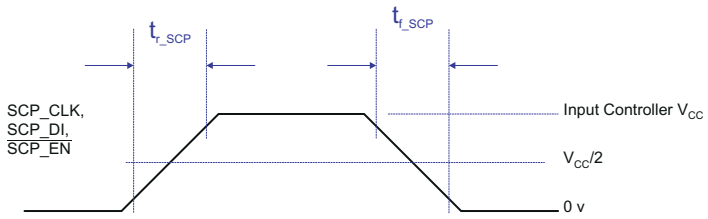


図 7-5. Serial Communications Bus Waveform Requirements

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7.10 Systems Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal interface area (see 図 7-6)			156	N
	Electrical interface area (see 図 7-6)			1334	N
	Datum *A* Interface area (see 図 7-6)			712	N

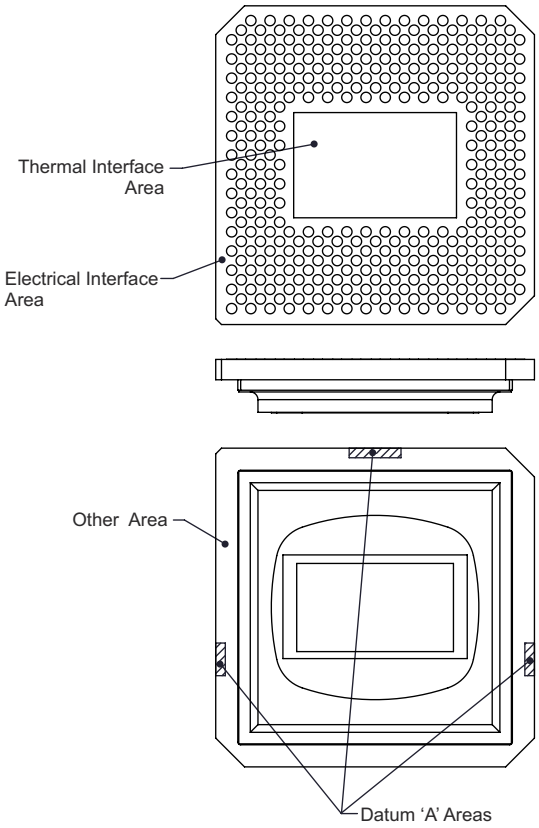


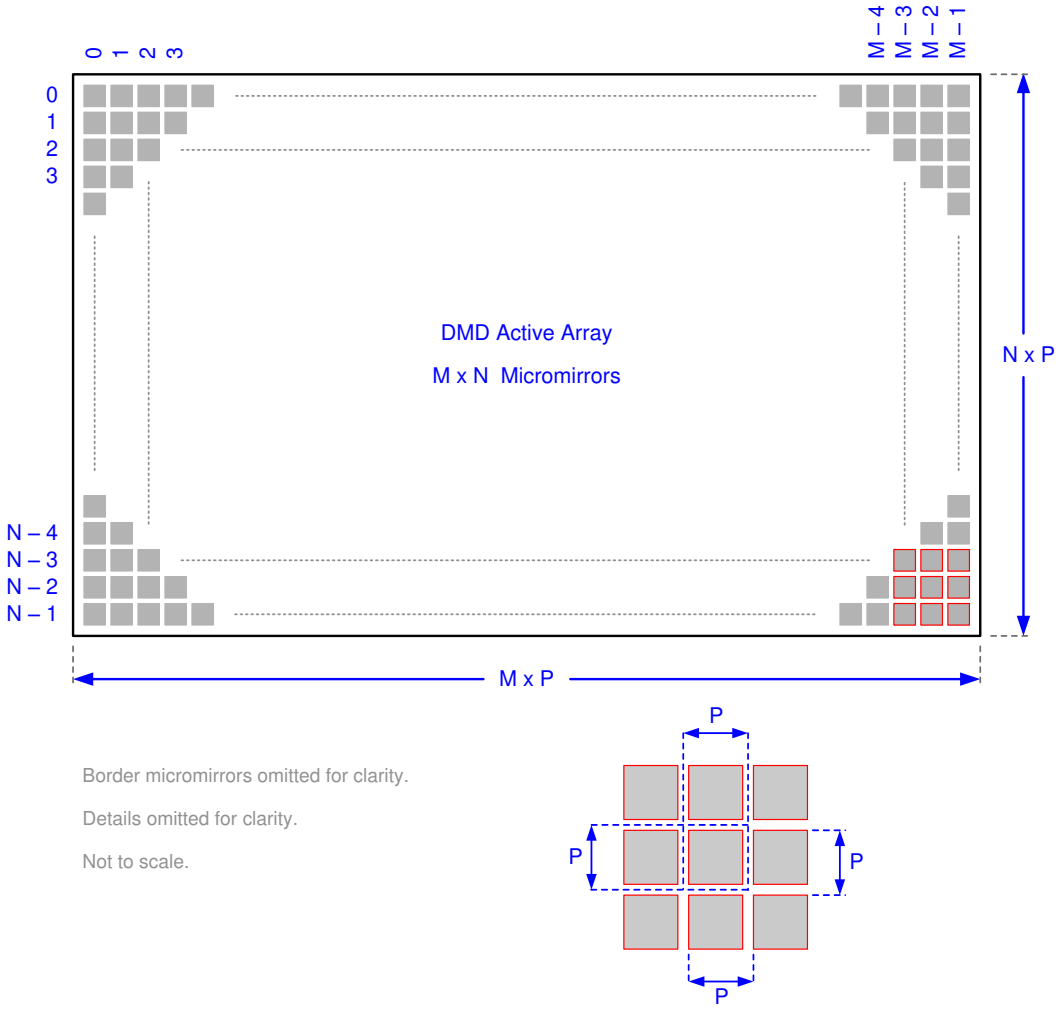
図 7-6. System Interface Loads

7.11 Micromirror Array Physical Characteristics

See *Mechanical, Packaging and Orderable Information* for additional details.

			VALUE	UNIT
M	Number of active micromirror columns (1)		1920	micromirrors
N	Number of active micromirror rows (1)		1080	micromirrors
P	Micromirror (pixel) pitch (1)		10.8	µm
	Micromirror active array width (1)	M × P	20.736	mm
	Micromirror active array height (1)	N × P	11.664	mm
	Micromirror array border (1) (2)	Pond of micromirrors (POM)	10	micromirrors/side

(1) See 図 7-7.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to the *セクション 7.11* table for M, N, and P specifications.

図 7-7. Micromirror Array Physical Characteristics

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7.12 Micromirror Array Optical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
a	Micromirror tilt angle	DMD parked state (1) (2) (3), See *Micromirror Landed Positions and Light Paths section*			0	degrees
		DMD landed state (1) (4) (5) See *Micromirror Landed Positions and Light Paths section*			12	
β	Micromirror tilt angle variation (1) (4) (6) (7) (8)	See *Micromirror Landed Positions and Light Paths section*	-1		1	degrees
		Micromirror crossover time (9)		3		µs
		Micromirror switching time (10)		12.5		µs
		Array switching time at 400 MHz with global reset (11)		56		µs
	Non-operating micromirrors (12)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (13)	See *Micromirror Landed Positions and Light Paths section*	44	45	46	degrees
	Micromirror array optical efficiency (14) (15)	363 to 420 nm, with all micromirrors in the ON state		70%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Parking the micromirror array returns all of the micromirrors to an essentially flat (0°) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is parked, the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums, as shown in *Mechanical, Packaging and Orderable Information*.
(5) When the micromirror array is landed, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in an nominal angular position of +12°. A binary value of 0 results in a micromirror landing in an nominal angular position of –12°.
(6) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variation.
(9) Micromirror crossover time is the transition time from landed to landed during a crossover transition and primarily a function of the natural response time of the micromirrors.
(10) Micromirror switching time is the time after a micromirror clocking pulse until the micromirrors can be addressed again. It included the micromirror settling time.
(11) Array switching is controlled and coordinated by the DLPC410 (DLPS024) and DLPA200 (DLPS015). Nominal switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed (array loaded plus reset and mirror settling time).
(12) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12° position to +12° or vice versa.
(13) Measured relative to the package datums 'B' and 'C', shown in the *Mechanical, Packaging and Orderable Information*.
(14) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:

- Illumination wavelength, bandwidth/line-width, degree of coherence
- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or path
- Aberrations present in the projection path

The specified nominal DMD optical efficiency is based on the following use conditions:

- UV illumination (363 to 420 nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f / 3.0 illumination aperture

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- *ƒ* / 2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 94%
- Micromirror array diffraction efficiency: nominally 85%
- Micromirror surface reflectivity: nominally 89%
- Window transmission: nominally 98% (single pass, through two surface transitions)

(15) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

7.13 Chipset Component Usage Specification

The DLP9500UV is a component of one or more DLP chipsets. Reliable function and operation of the DLP9500UV requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

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8 Detailed Description

8.1 Overview

Optically, the DLP9500UV consists of 2,073,600 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors), organized in a two-dimensional array of 1920 micromirror columns by 1080 micromirror rows. Each aluminum micromirror is approximately 10.8 microns in size (see the *Micromirror Pitch* in the DMD Micromirror Array and Hinge-Axis Orientation section and is switchable between two discrete angular positions: –12° and 12°. The angular positions are measured relative to a 0° flat state, which is parallel to the array plane (see Micromirror Landed Positions and Light paths section). The tilt direction is perpendicular to the hinge-axis, which is positioned diagonally relative to the overall array. The On State landed position is directed toward row 0, column 0 (upper left) corner of the device package (see the *Micromirror Hinge-Axis Orientation* in *DMD Micromirror Array, Pitch Hinge-Axis Orientation*). In the field of visual displays, the 1920 × 1080 pixel resolution is referred to as 1080p.

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse will result in the corresponding micromirror switching to a 12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse will result in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a micromirror clocking pulse to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror clocking pulses are generated externally by two DLPA200s, with application of the pulses being coordinated by the DLPC410 controller.

Around the perimeter of the 1920 by 1080 array of micromirrors is a uniform band of border micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1920 by 1080 active array.

図 8-1 shows a DLPC410 and DLP9500UV chipset block diagram. The DLPC410 and DLPA200s control and coordinate the data loading and micromirror switching for reliable DLP9500UV operation. The DLPR410 is the programmed PROM required to properly configure the DLPC410 controller. For more information on the chipset components, see *セクション 9*. For a typical system application using the DLP Discovery 4100 chipset including a DLP9500UV, see 図 9-2.

8.2 Functional Block Diagram

図 8-1 shows a simplified system block diagram with the use of the DLPC410 with the following chipset components:

DLPC410	Xilinx [XC5VLX30] FPGA configured to provide high-speed DMD data and control, and DLPA200 timing and control
DLPR410	[XCF16PFSG48C] serial flash PROM contains startup configuration information (EEPROM)
DLPA200	Two DMD micromirror drivers for the DLP9500UV DMD
DLP9500UV	Spatial light modulator (DMD)

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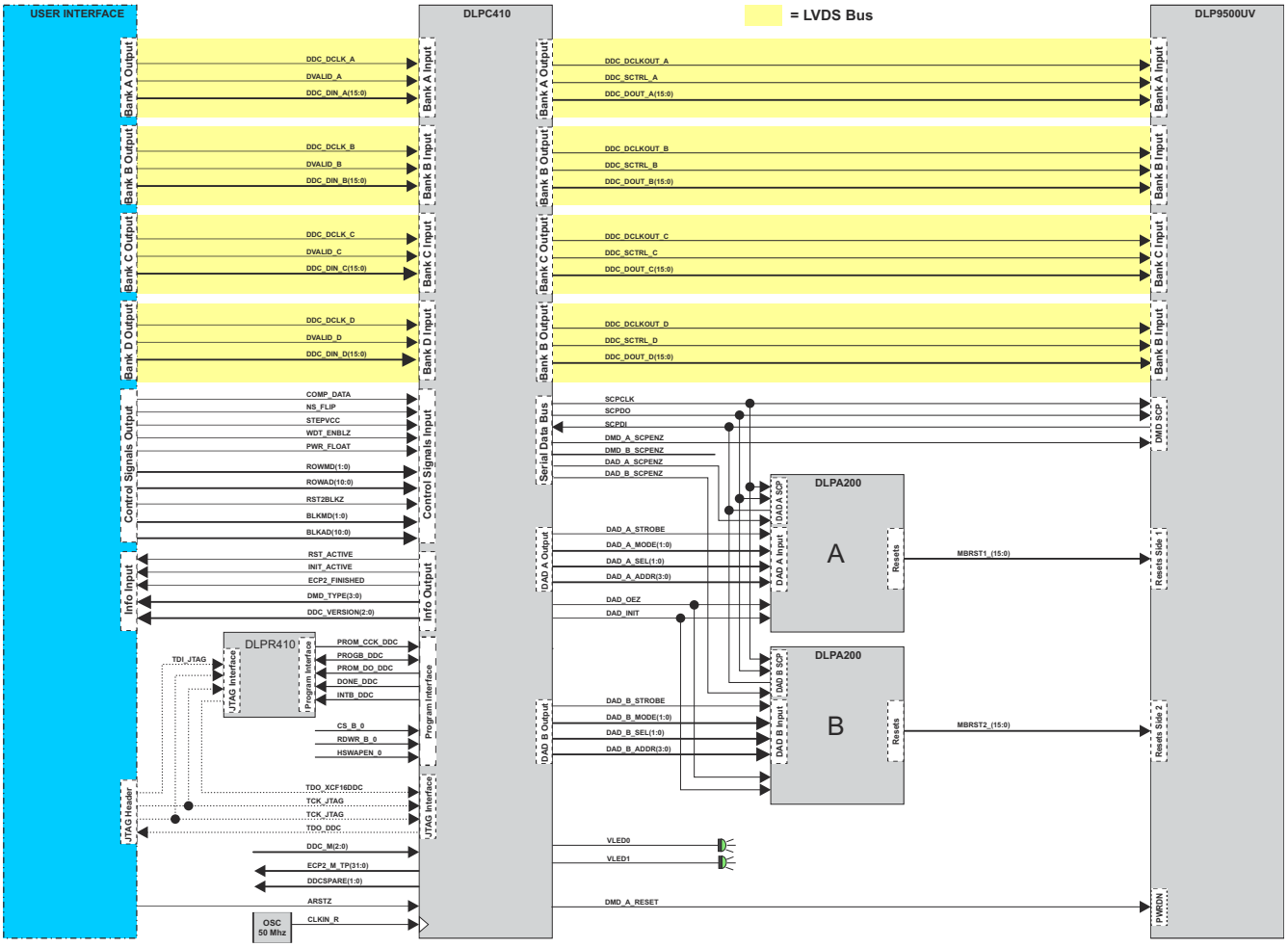


図 8-1. DLPC410, DLPA200, DLPR410, and DLP9500UV Functional Block Diagram

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8.3 Feature Description

表 8-1. DMD Overview

DMD	ARRAY	SINGLE BLOCK MODE (Patterns/s)	GLOBAL RESET MODE (Patterns/s)	DATA RATE (Giga Pixels/s)	MIRROR PITCH
DLP9500UV - 0.95" 1080p	1920 × 1080	23148 (1)	17857	48	10.8 µm

(1) This is for single block mode resets.

8.3.1 DLPC410 - Digital Controller for DLP Discovery 4100 Chipset

The DLPC410 chipset includes the DLPC410 controller which provides a high-speed LVDS data and control interface for DMD control. This interface is also connected to a second FPGA used to drive applications (not included in the chipset). The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, see the DLPC410 data sheet (DLPS024).

8.3.2 DLPA200 - DMD Micromirror Drivers

DLPA200 micromirror drivers provide the micromirror clocking pulse driver functions for the DMD. Two drivers are required for DLP9500UV.

The DLPA200 is designed to work with multiple DLP chipsets. Although the DLPA200 contains 16 MBSRT output pins, only 15 lines are used with the DLP9500 chipset. For more information see セクション Pin Functions and the DLPA200 data sheet (DLPS015).

8.3.3 DLPR410 - PROM for DLP Discovery 4100 Chipset

The DLPC410 controller is configured at startup from the DLPR410 PROM. The contents of this PROM can not be altered. For more information, see the DLPR410 data sheet (DLPS027) the DLPC410 data sheet (DLPS024).

8.3.4 DLP9500 - DLP 0.95 1080p 2xLVDS UV Type-A DMD 1080p DMD

8.3.4.1 DLP9500UV 1080p Chipset Interfaces

This section will describe the interface between the different components included in the chipset. For more information on component interfacing, see *セクション 9*.

8.3.4.1.1 DLPC410 Interface Description

8.3.4.1.1.1 DLPC410 IO

表 8-2 describes the inputs and outputs of the DLPC410 to the user. For more details on these signals, see the DLPC410 data sheet (DLPS024).

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表 8-2. Input/Output Description

PIN NAME	DESCRIPTION	I/O
$\overline{\text{ARST}}$	Asynchronous active low reset	I
CLKIN_R	Reference clock, 50 MHz	I
DIN_[A,B,C,D](15:0)	LVDS DDR input for data bus A,B,C,D (15:0)	I
DCLKIN[A,B,C,D]	LVDS inputs for data clock (200 - 400 MHz) on bus A, B, C, and D	I
DVALID[A,B,C,D]	LVDS input used to start write sequence for bus A, B, C, and D	I
ROWMD(1:0)	DMD row address and row counter control	I
ROWAD(10:0)	DMD row address pointer	I
BLK_AD(3:0)	DMD mirror block address pointer	I
BLK_MD(1:0)	DMD mirror block reset and clear command modes	I
PWR_FLOAT	Used to float DMD mirrors before complete loss of power	I
DMD_TYPE(3:0)	DMD type in use	O
RST_ACTIVE	Indicates DMD mirror reset in progress	O
INIT_ACTIVE	Initialization in progress.	O
VLED0	System “heartbeat” signal	O
VLED1	Denotes initialization complete	O

8.3.4.1.1.2 Initialization

The *INIT_ACTIVE* (表 8-2) signal indicates that the DLP9500UV, DLPA200s, and DLPC410 are in an initialization state after power is applied. During this initialization period, the DLPC410 is initializing the DLP9500UV and DLPA200s by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles should not be asserted during the initialization.

During initialization the user must send a training pattern to the DLPC410 on all data and DVALID lines to correctly align the data inputs to the data clock. For more information, see the interface training pattern information in the DLPC410 data sheet.

8.3.4.1.1.3 DMD Device Detection

The DLPC410 automatically detects the DMD type and device ID. DMD_TYPE (表 8-2) is an output from the DLPC410 that contains the DMD information.

8.3.4.1.1.4 Power Down

To ensure long term reliability of the DLP9500UV, a shutdown procedure must be executed. Prior to power removal, assert the PWR_FLOAT (表 8-2) signal and allow approximately 300 µs for the procedure to complete. This procedure assures the mirrors are in a flat state.

8.3.4.1.2 DLPC410 to DMD Interface

8.3.4.1.2.1 DLPC410 to DMD IO Description

表 8-3 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

表 8-3. DLPC410 to DMD I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
DDC_DOUT_[A,B,C,D](15:0)	LVDS DDR output to DMD data bus A,B,C,D (15:0)	O
DDC_DCLKOUT_[A,B,C,D]	LVDS output to DMD data clock A,B,C,D	O
DDC_SCTRL_[A,B,C,D]	LVDS DDR output to DMD data control A,B,C,D	O

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8.3.4.1.2.2 Data Flow

図 8-2 shows the data traffic through the DLPC410. Special considerations are necessary when laying out the DLPC410 to allow best signal flow.

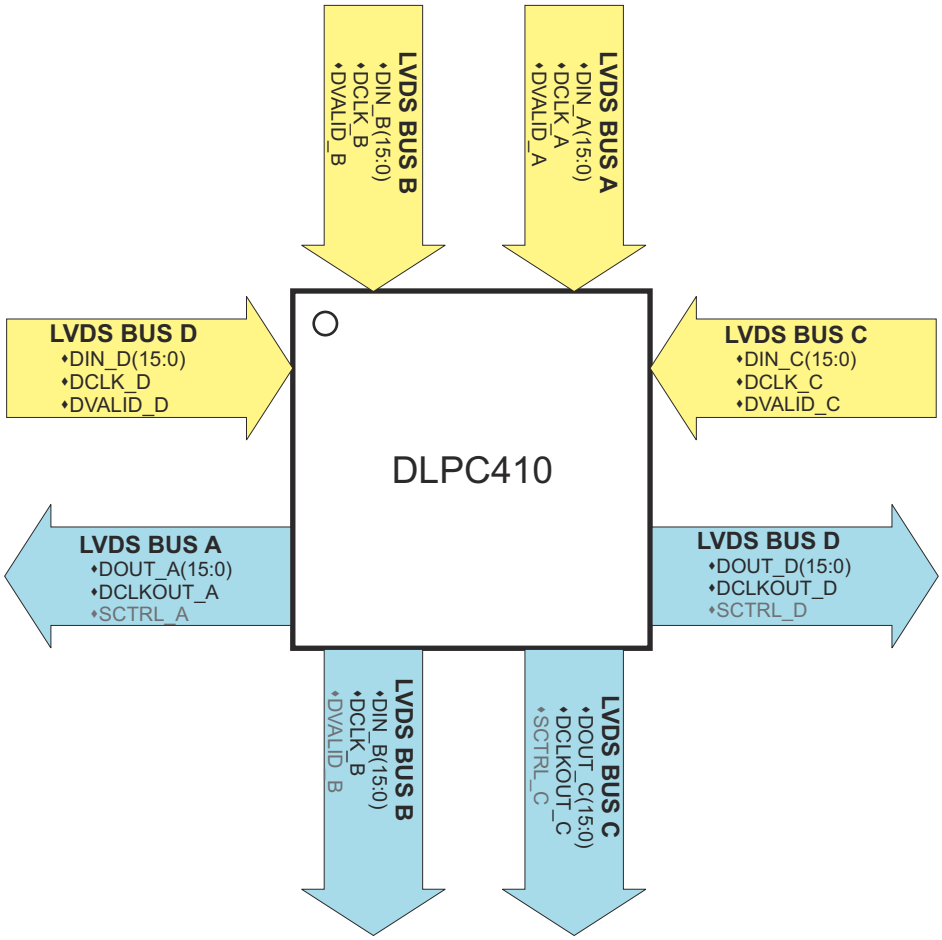


図 8-2. DLPC410 Data Flow

Four LVDS buses transfer the data from the user to the DLPC410. Each bus has its data clock that is input edge aligned with the data (DCLK). Each bus also has its own validation signal that qualifies the data input to the DLPC410 (DVALID).

Output LVDS buses transfer data from the DLPC410 to the DMD. Output buses LVDS C and LVDS D are used in addition to LVDS A and LVDS B with the DLP9500UV.

8.3.4.1.3 DLPC410 to DLPA200 Interface

8.3.4.1.3.1 DLPA200 Operation

The DLPA200 DMD micromirror driver is a mixed-signal application-specific integrated circuit (ASIC) that combines the necessary high-voltage power supply generation and micromirror clocking pulse functions for a family of DMDs. The DLPA200 is programmable and controllable to meet all current and anticipated DMD requirements.

The DLPA200 operates from a 12-V power supply input. For more detailed information on the DLPA200, see the DLPA200 data sheet.

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8.3.4.1.3.2 DLPC410 to DLPA200 IO Description

The serial communications port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of commands from the DLPC410 to the DLPA200s.

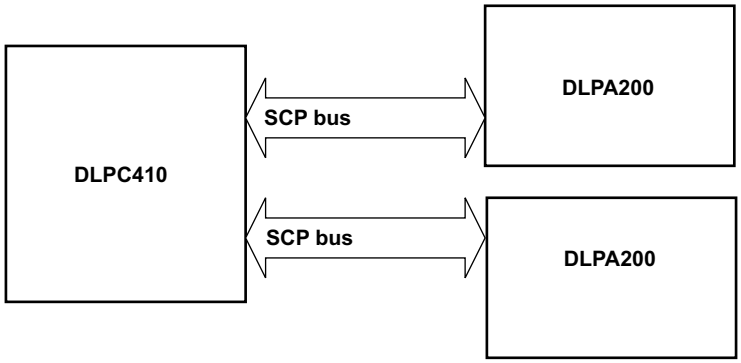


図 8-3. Serial Port System Configuration

Five signal lines are associated with the SCP bus: $\overline{\text{SCPEN}}$, SCPCK, SCPDI, SCPDO, and $\overline{\text{IRQ}}$.

表 8-4 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

表 8-4. DLPC410 to DLPA200 I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
$\overline{\text{A_SCPEN}}$	Active-low chip select for DLPA200 serial bus	O
A_STROBE	DLPA200 control signal strobe	O
A_MODE(1:0)	DLPA200 mode control	O
A_SEL(1:0)	DLPA200 select control	O
A_ADDR(3:0)	DLPA200 address control	O
$\overline{\text{B_SCPEN}}$	Active-low chip select for DLPA200 serial bus (2)	O
B_STROBE	DLPA200 control signal strobe (2)	O
B_MODE(1:0)	DLPA200 mode control	O
B_SEL(1:0)	DLPA200 select control	O
B_ADDR(3:0)	DLPA200 address control	O

The DLPA200 provides a variety of output options to the DMD by selecting logic control inputs: MODE[1:0], SEL[1:0] and reset group address A[3:0] (表 8-4). The MODE[1:0] input determines whether a single output, two outputs, four outputs, or all outputs, will be selected. Output levels (VBIAS, VOFFSET, or VRESET) are selected by SEL[1:0] pins. Selected outputs are tri-stated on the rising edge of the STROBE signal and latched to the selected voltage level after a break-before-make delay. Outputs will remain latched at the last micromirror clocking pulse waveform level until the next micromirror clocking pulse waveform cycle.

8.3.4.1.4 DLPA200 to DLP9500UV Interface

8.3.4.1.4.1 DLPA200 to DLP9500UV Interface Overview

The DLPA200 generates three voltages: VBIAS, VRESET, and VOFFSET that are supplied to the DMD MBRST lines in various sequences through the micromirror clocking pulse driver function. VOFFSET is also supplied directly to the DMD as DMDVCC2. A fourth DMD power supply, DMDVCC, is supplied directly to the DMD by regulators.

The function of the micromirror clocking pulse driver is to switch selected outputs in patterns between the three voltage levels (VBIAS, VRESET and VOFFSET) to generate one of several micromirror clocking pulse waveforms. The order of these micromirror clocking pulse waveform events is controlled externally by the logic

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control inputs and timed by the STROBE signal. DLPC410 automatically detects the DMD type and then uses the DMD type to determine the appropriate micromirror clocking pulse waveform.

A direct micromirror clocking pulse operation causes a mirror to transition directly from one latched state to the next. The address must already be set up on the mirror electrodes when the micromirror clocking pulse is initiated. Where the desired mirror display period does not allow for time to set up the address, a micromirror clocking pulse with release can be performed. This operation allows the mirror to go to a relaxed state regardless of the address while a new address is set up, after which the mirror can be driven to a new latched state.

A mirror in the relaxed state typically reflects light into a system collection aperture and can be thought of as *off* although the light is likely to be more than a mirror latched in the *off* state. System designers should carefully evaluate the impact of relaxed mirror conditions on optical performance.

8.3.5 Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 8-4 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving. All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

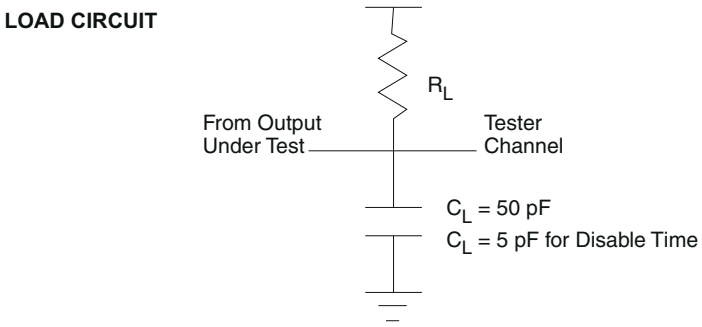


図 8-4. Test Load Circuit for AC Timing Measurements

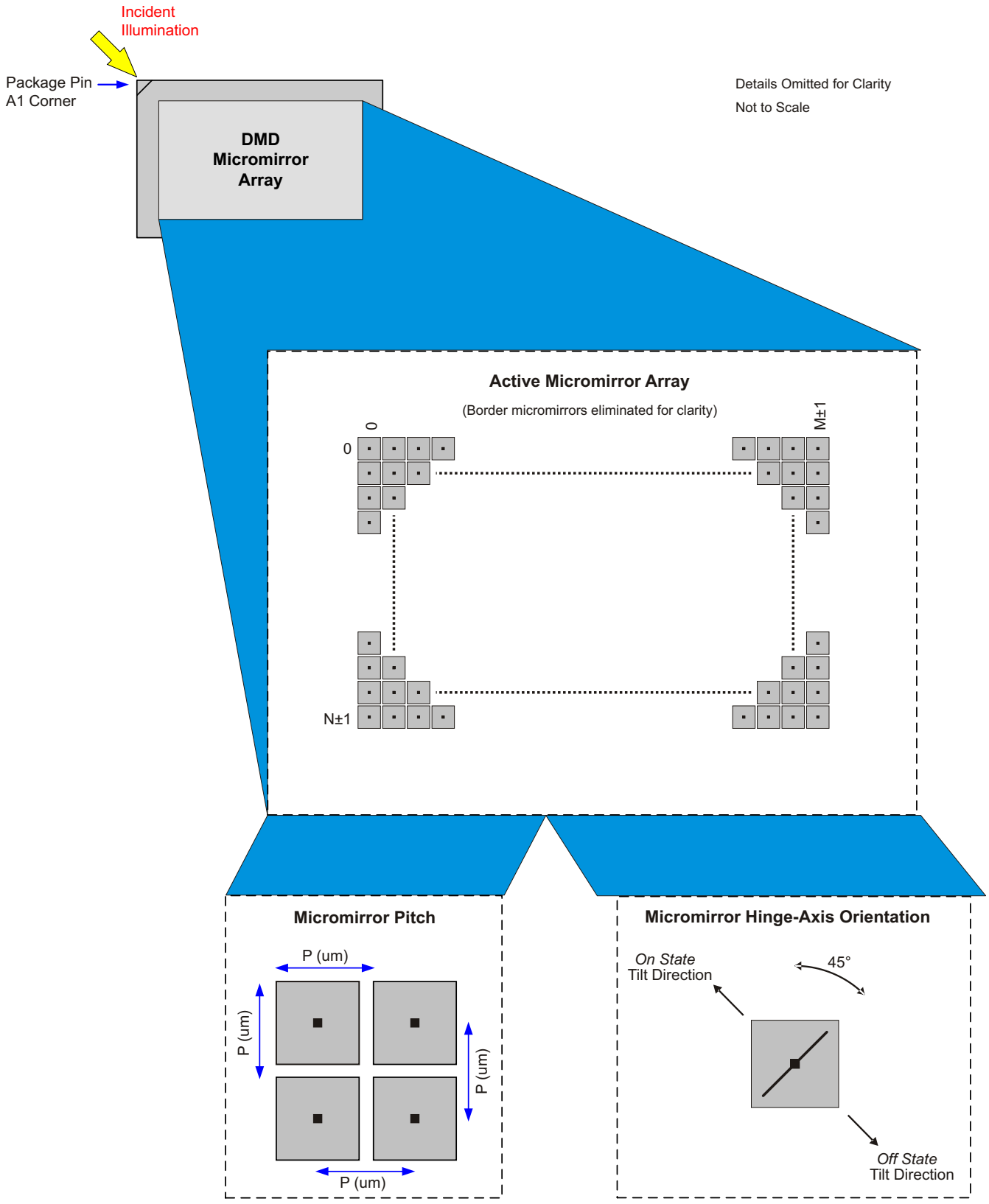


図 8-5. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation

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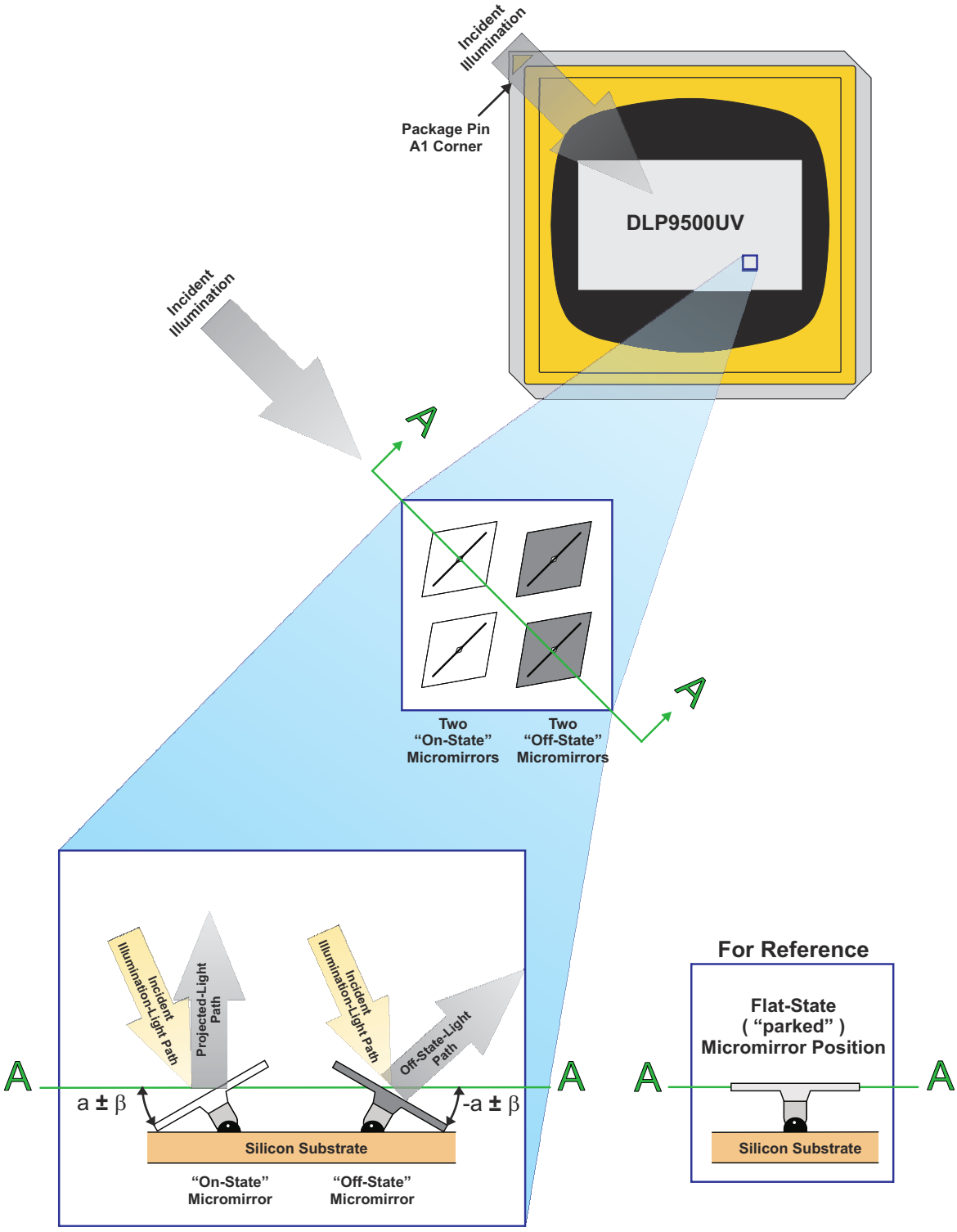


図 8-6. Micromirror Landed Positions and Light Paths

8.4 Device Functional Modes

The DLP9500UV has only one functional mode; it is set to be highly optimized for low latency and high speed in generating mirror clocking pulses and timings.

When operated with the DLPC410 controller in conjunction with the DLPA200 drivers, the DLP9500UV can be operated in several display modes. The DLP9500UV is loaded as 15 blocks of 72 rows each. The first 64 bits of pixel data and last 64 bits of pixel data for all rows are not visible. Below is a representation of how the image is loaded by the different micromirror clocking pulse modes. 図 8-7, 図 8-8, 図 8-9, and 図 8-10 show how the image is loaded by the different micromirror clocking pulse modes.

There are four micromirror clocking pulse modes that determine which blocks are *reset* when a micromirror clocking pulse command is issued:

- Single block mode
- Dual block mode
- Quad block mode
- Global mode

8.4.1 Single Block Mode

In single block mode, a single block can be loaded and reset in any order. After a block is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

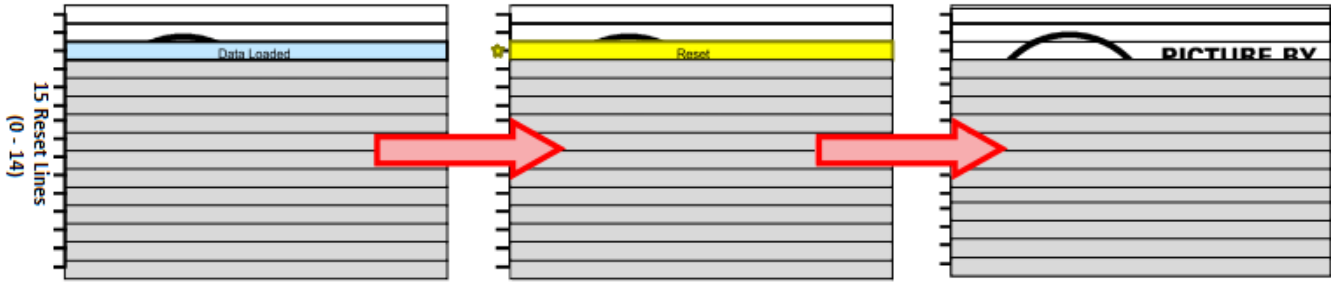


図 8-7. Single Block Mode

8.4.2 Dual Block Mode

In dual block mode, reset blocks are paired together as follows (0-1), (2-3), (4-5), (6-7), (8-9), (10-11), (12-13), and (14). These pairs can be reset in any order. After data is loaded a pair can be reset to transfer the information to the mechanical state of the mirrors.

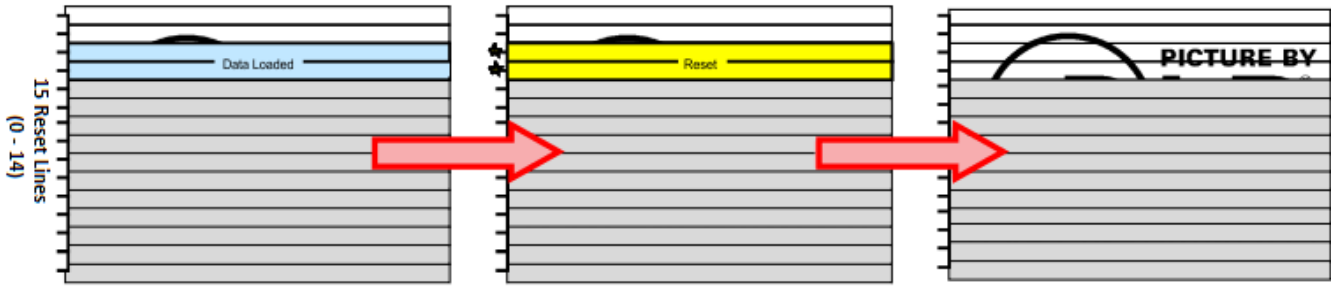


図 8-8. Dual Block Mode

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8.4.3 Quad Block Mode

In quad block mode, reset blocks are grouped together in fours as follows (0-3), (4-7), (8-11) and (12-14). Each quad group can be randomly addressed and reset. After a quad group is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

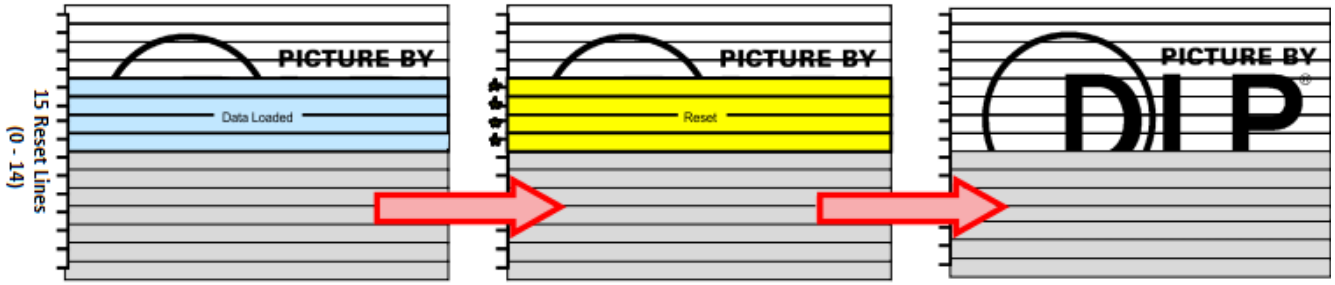


図 8-9. Quad Block Mode

8.4.4 Global Block Mode

In global mode, all reset blocks are grouped into a single group and reset together. The entire DMD must be loaded with the desired data before issuing a Global Reset to transfer the information to the mechanical state of the mirrors.

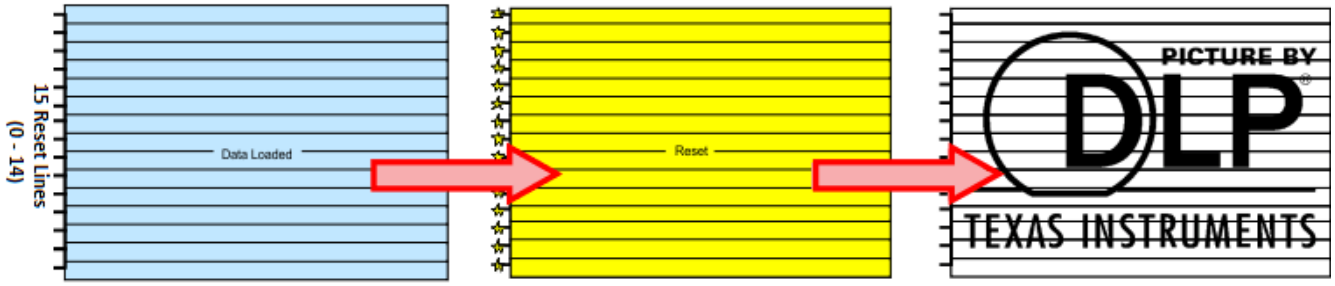


図 8-10. Global Mode

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8.5 Window Characteristics and Optics

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TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

8.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

8.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination, projection pupils, or both to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the *ON* optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

8.5.3 Pupil Match

TI recommends the exit pupil of the illumination is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

8.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the optical architecture of a particular system, overfill light may have to be further reduced below the suggested 10% level to be acceptable.

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8.6 Micromirror Array Temperature Calculation

8.6.1 Thermal Test Points

The temperature of the DMD case can be measured directly. For consistency, thermal test point locations 1, 2, and 3 are defined as shown in 図 8-11.

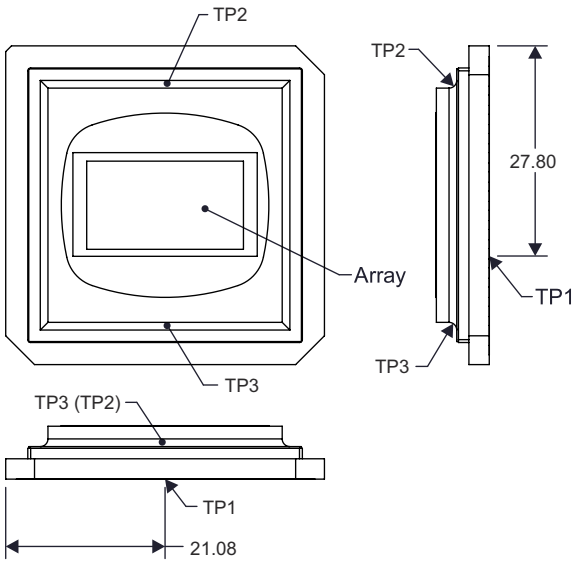


図 8-11. Thermal Test Points

8.6.2 Micromirror Array Temperature Calculation - Lumens Based

Active array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points on the outside of the package, package thermal resistance, electrical power, and illumination heat load. The relationship between array temperature and the reference ceramic temperature (test point number 1 in 図 8-11) is provided by the following equations:

T_{Array} = Computed DMD active array temperature

= Measured Ceramic temperature at location (test point number 1) + (Temperature increase due to power incident to the array × array-to-ceramic resistance)

$= T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic})$

where

- $T_{Ceramic}$ = Measured ceramic temperature (°C) at location (test point number 1)
- $R_{Array\text{-}To\text{-}Ceramic}$ = DMD package thermal resistance from array to outside ceramic (°C/W)
- Q_{Array} = Total DMD array power, which is both electrical plus absorbed on the DMD active array (W)

$$Q_{Array} = Q_{Electrical} + (Q_{Illumination} \times \text{DMD absorption constant (0.42)})$$

where

- $Q_{Electrical}$ = Approximate nominal electrical internal power dissipation (W)
- $Q_{Illumination}$ = [Illumination power density × illumination area on DMD] (W)
- DMD absorption constant = 0.42

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation of the DMD is variable and depends on the operating state of mirrors and the intensity of the light source. The DMD absorption constant of 0.42 assumes nominal operation with an illumination distribution of 83.7% on the active array, 11.9% on the array border, and 4.4% on the window aperture. A system aperture may be required to limit power incident on the package aperture since this area absorbs much more efficiently than the array.

Sample Calculation:

- Illumination power density = 2 W/cm^2
- Illumination area = (2.0736 cm × 1.1664 cm) / 83.7% = 2.89 cm^2 (assumes 83.7% on the active array and 16.3% overfill)
- $Q_{Illumination}$= 2 W/cm^2 × 2.89 cm^2 = 5.78 W
- $Q_{Electrical}$ = 4.4 W
- $R_{Array\text{-}To\text{-}Ceramic}$ = 0.5°C/W
- $T_{Ceramic}$ = 20°C (measured on ceramic)
- Q_{Array} = 4.4 W + (5.78 W × 0.42) = 6.83 W
- T_{Array} = 20°C + (6.83 W × 0.5°C/W) = 23.4°C

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from:

- the measurement points (図 8-11)
- the package thermal resistance
- the electrical power
- the illumination heat load

The relationship between micromirror array temperature and the reference ceramic temperature (thermal test point TP1 in 図 8-11) is provided by the following equations:

where

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- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = thermal resistance of DMD package (specified in セクション 7.5) from array to ceramic TP1 (°C/W)
- Q_{ARRAY} = total power (electrical + absorbed) on the array (Watts)
- $Q_{ELECTRICAL}$ = nominal electrical power (Watts)
- $Q_{ILLUMINATION}$ = (C_{L2W} × SL) (Watts)
- C_{L2W} = conversion constant for screen lumens to power on DMD (Watts/lumen)
- SL = measured screen lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 4.4 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The conversion constant C_{L2W} is based on the DMD input illumination characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and an illumination distribution of 83.7% on the active array and 16.3% on the array border. The equations shown above are valid for a system with a total projection efficiency through the projection lens from the DMD to the screen of 87%.

- $T_{Ceramic}$ = 55°C (measured)
- SL = 2000 lm (measured)
- $Q_{ELECTRICAL}$ = 4.4 Watts
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = 0.5 °C/W
- C_{L2W} = 0.00274 W/lm
- Q_{ARRAY} = 4.4 + (0.00274 W/lm × 2000 lm) = 9.88 W
- T_{ARRAY} = 55°C + (9.88 W x 0.5 °C) = 59.9 °C

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8.6.3 Micromirror Array Temperature Calculation - Power Density Based

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from:

- the measurement points (図 8-11)
- the package thermal resistance
- the electrical power
- the illumination heat load

The relationship between array temperature and the reference ceramic temperature (thermal test point TP1 in 図 8-11) is provided by the following equations:

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = thermal resistance of DMD package (specified in セクション 7.5) from array to ceramic TP1 (°C/W)
- Q_{ARRAY} = total power (electrical + absorbed) on the array (Watts)
- $Q_{ELECTRICAL}$ = nominal electrical power (Watts)
- $Q_{INCIDENT}$ = total incident optical power on DMD (Watts)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 4.4 watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for each DMD chip in a system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

8.6.4

- $T_{Ceramic}$ = 20°C (measured)
- $ILL_{DENSITY}$ = 11 Watts per cm^2 (optical power on DMD per unit area) (measured)
- Overfill = 16.3% (optical design)
- $Q_{ELECTRICAL}$ = 4.4 Watts
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = 0.5 °C/W
- Area of array = (2.0736 cm x 1.1664 cm) = 2.419 cm^2
- ILL_{AREA} = 2.419 cm^2 / (83.7%) = 2.89 cm^2
- $Q_{INCIDENT}$ =11 W/cm^2 x 2.89 cm^2 = 31.79 W
- Q_{ARRAY} = 4.4 W + (0.42 x 31.79 W) = 17.75 W
- T_{ARRAY} = 20°C + (17.75 W x 0.5 °C) = 28.9 °C

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8.7 Micromirror Landed-On and Landed-Off Duty Cycle

8.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On−state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (on or off), the two numbers (percentages) always add to 100.

8.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the usable life of the DMD.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

8.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD's usable life.

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a give long-term average landed duty.

8.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 8-5.

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表 8-5. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

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9 Application and Implementation

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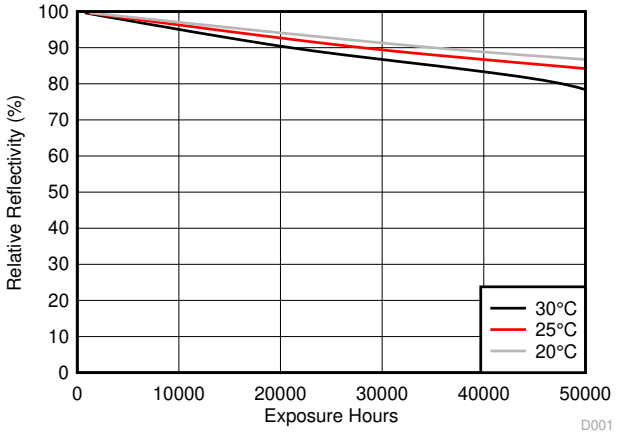
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9.1 Application Information

The DLP9500UV devices must be coupled with the DLPC410 controller to provide a reliable solution for many different applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC410. Applications of interest include 3D printing, lithography, medical systems, and compressive sensing.

9.1.1 DMD Reflectivity Characteristics

TI assumes no responsibility for end-equipment reflectivity performance. Achieving the desired end-equipment reflectivity performance involves making trade-offs between numerous component and system design parameters. Typical DMD reflectivity characteristics over UV exposure times are represented in 図 9-1.



2.3 W/cm^2, 363 to 400 nm, 25°C

図 9-1. Nominal DMD Relative Reflectivity Percentage vs Total Exposure Hours

DMD reflectivity includes micromirror surface reflectivity and window transmission. The DMD was characterized for DMD reflectivity using a broadband light source (200-W metal-halide lamp). Data is based off of a 2.3 W/cm^2 UV exposure at the DMD surface (365 nm peak output) using a 363 nm high pass filter between the light source and the DMD. (Contact your local Texas Instruments representative for additional information about power density measurements and UV filter details.)

9.1.1.1 Design Considerations Influencing DMD Reflectivity

Optimal, long-term performance of the digital micromirror device (DMD) can be affected by various application parameters. The following is a list of some of these application parameters and includes high level design recommendations that may help extend relative reflectivity from time zero:

- Illumination spectrum – using longer wavelengths for operation while preventing shorter wavelengths from striking the DMD
- Illumination power density – using lower power density
- DMD case temperature – operating the DMD with the case temperature at the low end of its specification

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- Cumulative incident illumination – Limiting the total hours of UV illumination exposure when the DMD is not actively steering UV light in the application. For example, a design might include a shutter to block the illumination or LED illumination where the LEDs can be strobed off during periods not requiring UV exposure.
- Micromirror landed duty cycle – applying a 50/50 duty cycle pattern during periods where operational patterns are not required.

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9.2 Typical Application

The DLP9500UV DMD is designed with a window which allows transmission of ultraviolet (UV) light. This makes it well suited for UV applications requiring fast, spatially programmable light patterns using the micromirror array. UV wavelengths can affect the DMD differently than visible wavelengths. There are system level considerations which should be leveraged when designing systems using this DMD.

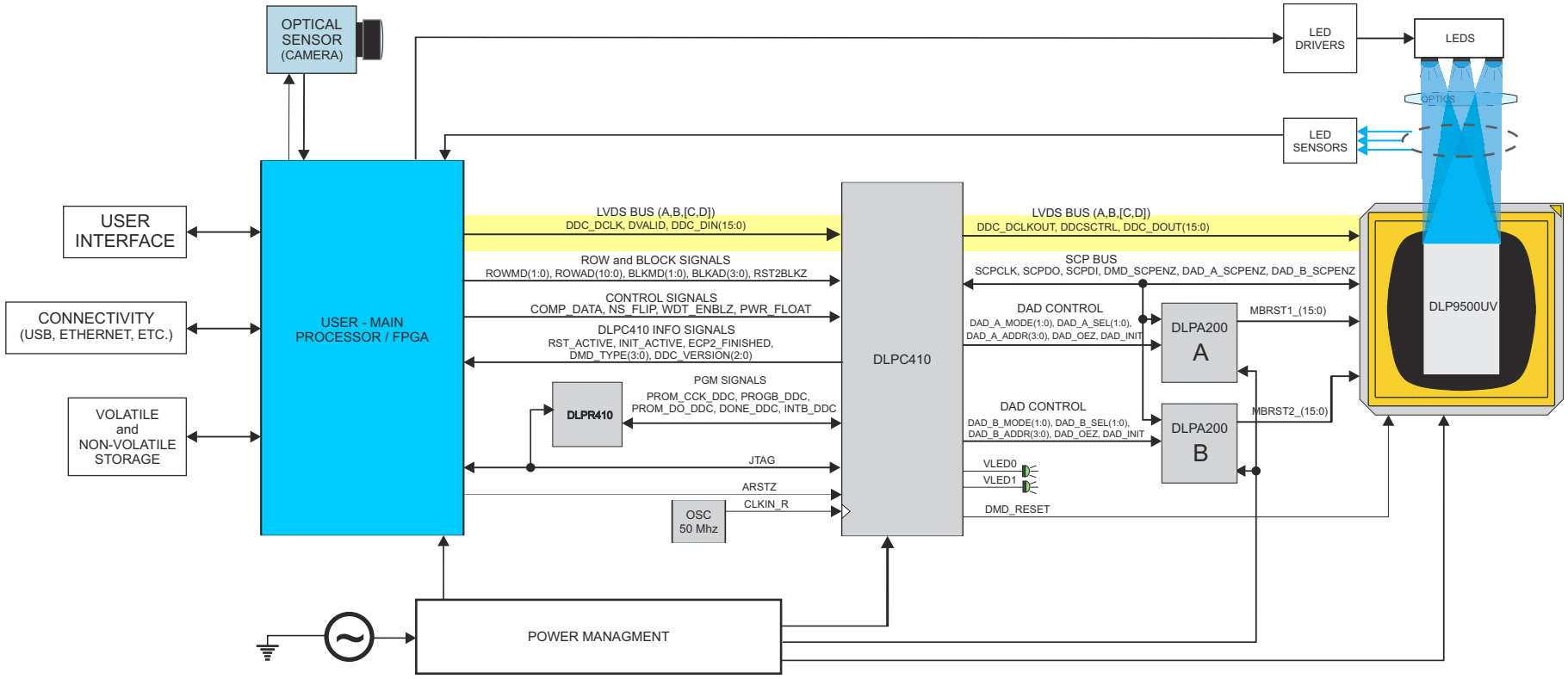


図 9-2. DLPC410 and DLP9500UV Embedded Example Block Diagram

9.2.1 Design Requirements

All applications using the DLP9500UV chipset require both the controller and the DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC410 configuration and support firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC410 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface
  - Reference clock
  - Program interface
- DLP9500UV interfaces:
  - DLPC410 to DLP9500UV digital data
  - DLPC410 to DLP9500UV control interface
  - DLPC410 to DLP9500UV micromirror reset control interface
  - DLPC410 to DLPA200 micromirror driver
  - DLPA200 to DLP9500UV micromirror reset

9.2.1.1 Device Description

The DLP9500UV 1080p chipset offers developers a convenient way to design a wide variety of industrial, medical, telecom and advanced display applications by delivering maximum flexibility in formatting data, sequencing data, and light patterns.

The DLP9500UV 1080p chipset includes the following four components: DMD digital controller (DLPC410), EEPROM (DLPR410), DMD micromirror driver (DLPA200), and a DMD (DLP9500UV).

DLPC410 Digital Controller for DLP Discovery 4100 chipset

- Provides high speed 2XLVDS data and control interface to the user
- Drives mirror clocking pulse and timing information to the DLPA200
- Supports random row addressing
- Controls illumination

DLPR410 PROM for DLP Discovery 4100 chipset

- Contains startup configuration information for the DLPC410

DLPA200 DMD Micromirror Driver

- Generates micromirror clocking pulse control (sometimes referred to as a reset) of 15 banks of DMD mirrors. (Two are required for the DLP9500UV).

DLP9500UV DLP 0.95 1080p 2xLVDS UV Type-A DMD

- Steers light in two digital positions (+12° and –12°) using 1920 × 1080 micromirror array of aluminum mirrors.

表 9-1. DLP DLP9500UV Chipset Configurations

QUANTITY	TI PART	DESCRIPTION
1	DLP9500UV	DLP 0.95 1080p 2xLVDS UV Type-A DMD
1	DLPC410	Digital Controller for DLP Discovery 4100 chipset
1	DLPR410	PROM for DLP Discovery 4100 chipset
2	DLPA200	DMD Micromirror Driver

Reliable function and operation of DLP9500UV 1080p chipsets require the components be used in conjunction with each other. This document describes the proper integration and use of the DLP9500UV 1080p chipset components.

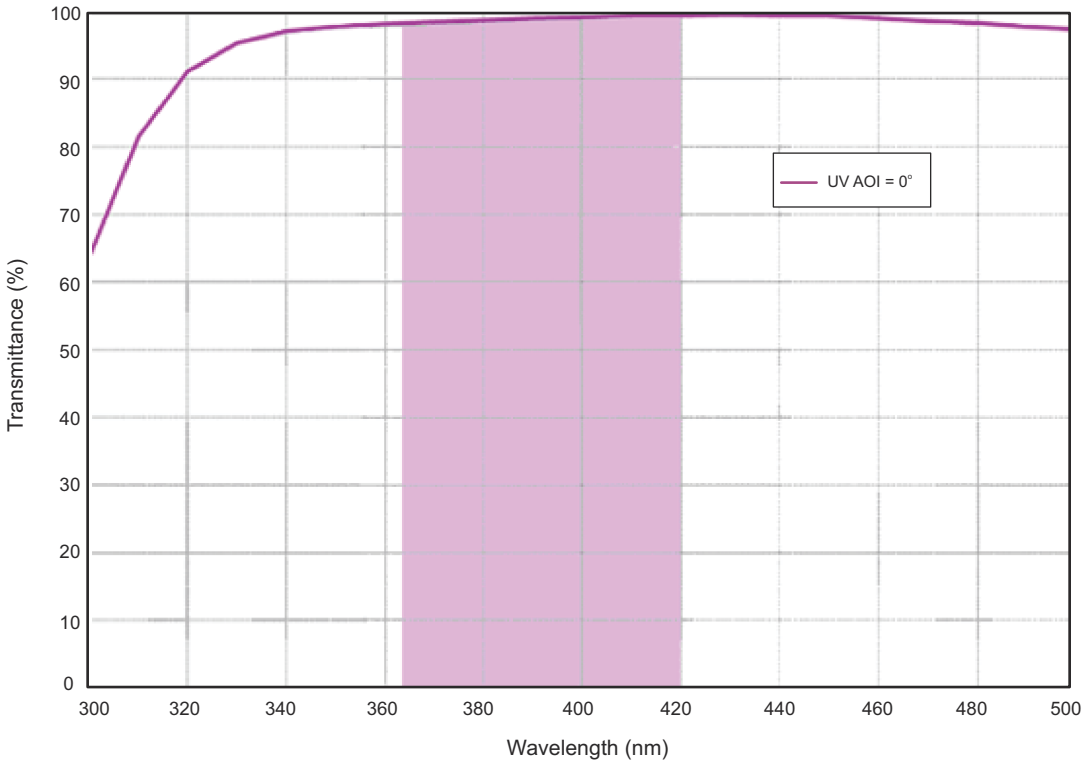
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The DLP9500UV 1080p chipset can be combined with a user programmable application FPGA (not included) to create high performance systems.

9.2.2 Detailed Design Procedure

The DLP9500UV DMD is designed with a window which allows transmission of UV light. This makes it well suited for UV applications requiring fast, spatially programmable light patterns using the micromirror array. UV wavelengths can affect the DMD differently than visible wavelengths. There are system level considerations which should be leveraged when designing systems using this DMD.

9.2.3 Application Curve



Type A UVA on 7056 glass (3 mm thick)

図 9-3. Corning 7056 UV Window Transmittance (Maximum Transmission Region)

10 Power Supply Recommendations

10.1 Power-Up Sequence (Handled by the DLPC410)

The sequence of events for DMD system power-up is:

1. Apply logic supply voltages to the DLPA200 and to the DMD according to DMD specifications.
2. Place DLPA200 drivers into high impedance states.
3. Turn on DLPA200 bias, offset, or reset supplies according to driver specifications.
4. After all supply voltages are assured to be within the limits specified and with all micromirror clocking pulse operations logically suspended, enable all drivers to either VOFFSET or VBIAS level.
5. Begin micromirror clocking pulse operations.

10.2 DMD Power-Up and Power-Down Procedures

Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP9500UV power-up and power-down procedures are defined by the DLPC410 data sheet (DLPS024). These procedures must be followed to ensure reliable operation of the device.

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11 Layout

11.1 Layout Guidelines

The DLP9500UV is part of a chipset that is controlled by the DLPC410 in conjunction with the DLPA200. These guidelines are targeted at designing a PCB board with these components.

11.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50 Ω ±10% except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn) which should be matched to 100 Ω ±10% across each pair.

11.1.2 PCB Signal Routing

When designing a PCB board for the DLP9500UV controlled by the DLPC410 in conjunction with the DLPA200s, the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces should not cross over slots in adjacent power and/or ground planes.

表 11-1. Important Signal Trace Constraints

SIGNAL	CONSTRAINTS
LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn)	P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example DMD_DAT_Ann to DMD_DAT_Bnn) Trace width: 4 mil (0.1 mm) Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm) Maximum recommended trace length <6 inches (150 mm)

表 11-2. Power Trace Widths and Spacing

SIGNAL NAME	MINIMUM TRACE WIDTH	MINIMUM TRACE SPACING	LAYOUT REQUIREMENTS
GND	Maximize	5 mil (0.13 mm)	Maximize trace width to connecting pin as a minimum
VCC, VCC2	20 mil (0.51 mm)	10 mil (0.25 mm)	
MBRST[14:0]	11 mil (0.28 mm)	15 mil (0.38 mm)	

11.1.3 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

11.1.4 PCB Layout Guidelines

A target impedance of 50 Ω for single ended signals and 100 Ω between LVDS signals is specified for all signal layers.

11.1.4.1 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. The LVDS signals should have 100 Ω differential impedance. The differential signals should be matched but kept as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary.

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11.1.4.1.1 Trace Length Matching

The DLPC410 DMD data signals require precise length matching. Differential signals should have impedance of 100 Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 100 mils with a relative propagation delay of ±25 mil between the p and n. Matching all signals exactly will maximize the channel margin. The signal path through all boards, flex cables and internal DMD routing must be considered in this calculation.

11.1.4.2 DLP9500UV Decoupling

General decoupling capacitors for the DLP9500UV should be distributed around the PCB and placed to minimize the distance from IC voltage and ground pads. Each decoupling capacitor (0.1 µF recommended) should have vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. The power and ground pads of the DLP9500UV should be tied to the voltage and ground planes with their own vias.

11.1.4.2.1 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. TI recommends that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin or pins. The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by using low ESR and low ESL capacitors.

11.1.4.3 VCC and VCC2

The VCC pins of the DMD should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the DMD's VCC2 and ground pads. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

11.1.4.4 DMD Layout

See the respective sections in this data sheet for package dimensions, timing and pin out information.

11.1.4.5 DLPA200

The DLPA200 generates the micromirror clocking pulses for the DMD. The DMD-drive outputs from the DLPA200 (MBRST[29:0] should be routed with minimum trace width of 11 mil and a minimum spacing of 15 mil. The VCC and VCC2 traces from the output capacitors to the DLPA200 should also be routed with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet DLPS015 for mechanical package and layout information.

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11.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, 図 11-1 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

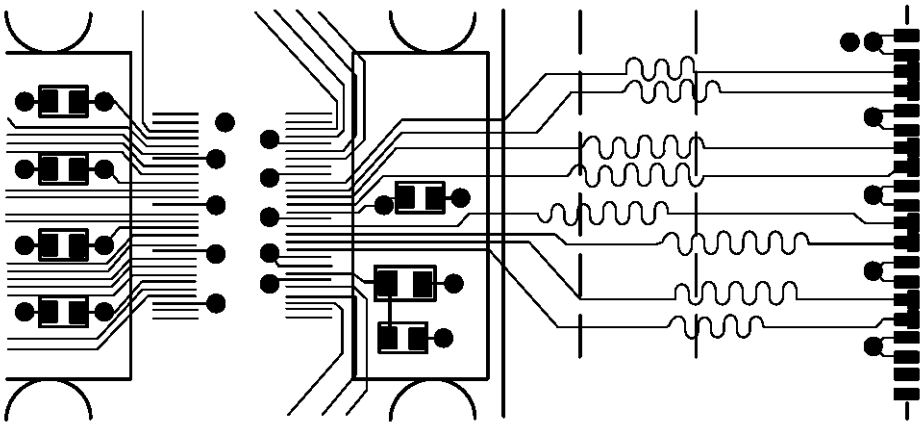


図 11-1. Mitering LVDS Traces to Match Lengths

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

図 12-1 provides a legend of reading the complete device name for any DLP device.

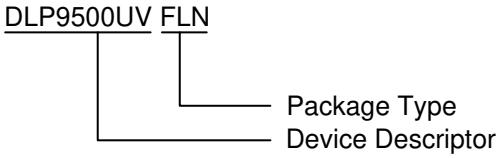


図 12-1. Device Nomenclature

12.1.2 Device Marking

図 12-2 shows the device marking fields.

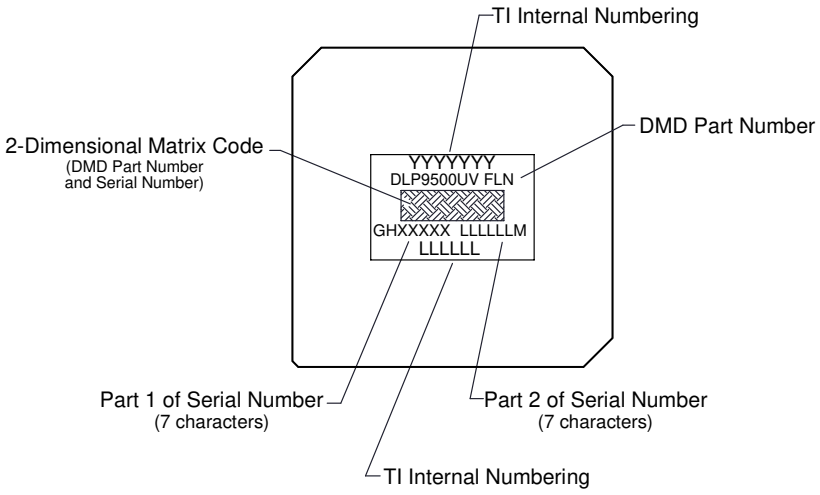


図 12-2. DLP9500UV Device Marking

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12.2 Documentation Support

12.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP9500UV device.

- DLPC410 Digital Controller for DLP Discovery 4100 chipset data sheet
- DLPA200 DMD Micromirror Driver data sheet
- DLPR410 PROM for DLP Discovery 4100 chipset data sheet

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP9500UV	Click here	Click here	Click here	Click here	Click here
DLPA200	Click here	Click here	Click here	Click here	Click here
DLPC410	Click here	Click here	Click here	Click here	Click here
DLPR410	Click here	Click here	Click here	Click here	Click here

12.4 サポート・リソース

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12.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP9500UVFLN	ACTIVE	CLGA	FLN	355	12	RoHS & Green	NI-PD-AU	N / A for Pkg Type	20 to 30		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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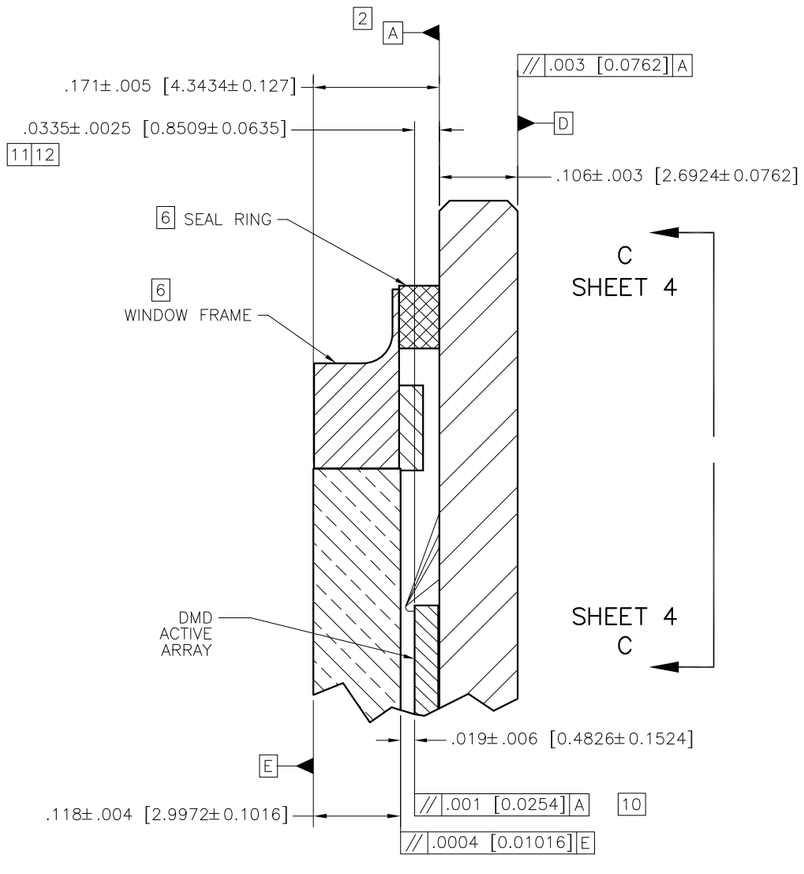
DWG NO 2506491 SH 1

REVISIONS

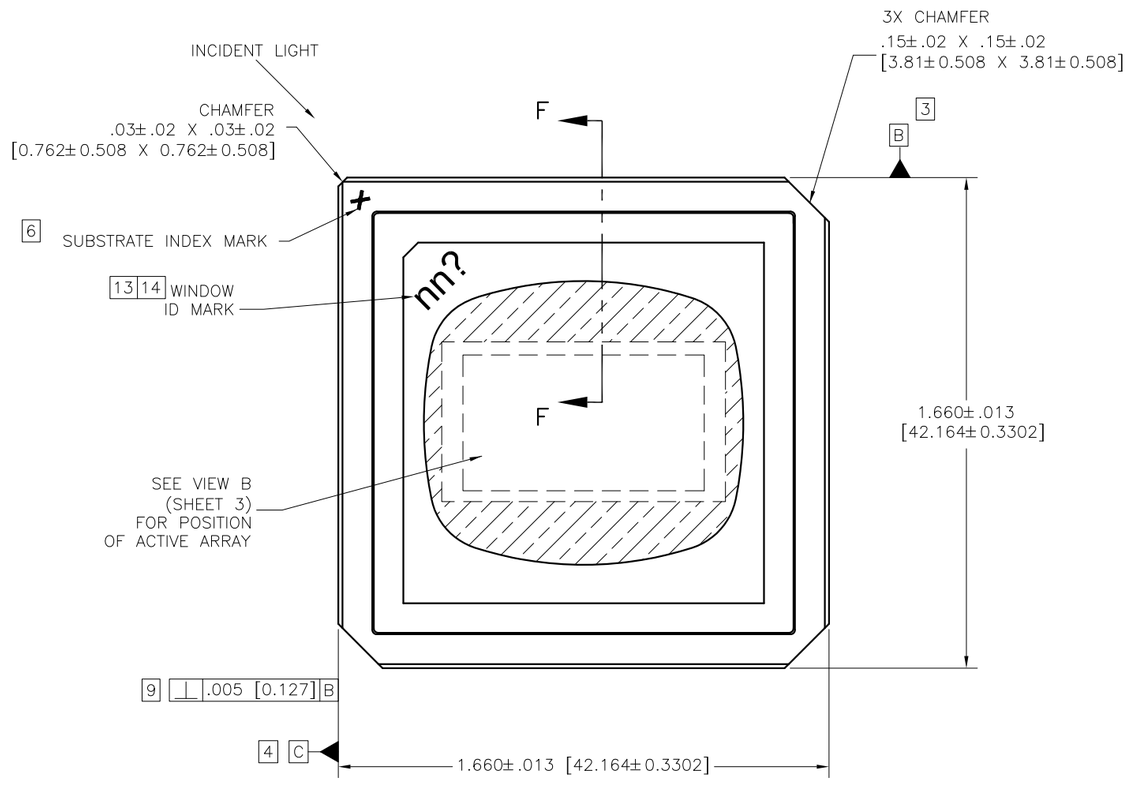
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2055418, INITIAL RELEASE	2/28/05	M. AVERY
B	ECO 2150560, ADD NOTE 15.	05/12/15	M. AVERY
C	ECO 2179667, DELETE NOTE 7.	02/18/19	B. HASKETT
D	ECO 2183329, UPDATE NOTE 14 FOR UV WINDOWS.	09/27/19	B. HASKETT

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW A (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW A (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW A (SHEET 2).
5. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE SURFACE.
6. SUBSTRATE INDEX MARK, BACK INDEX PAD, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
7. (DELETED)
8. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
9. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
10. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
11. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
12. DMD ACTIVE ARRAY ROTATION AND LOCATION DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
13. WINDOW SHALL BE ORIENTED SUCH THAT I.D. MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
14. n AND ? ARE WILD CARD CHARACTERS. nn=25 FOR STANDARD VISIBLE WINDOWS; nn=32 FOR UV-TRANSMISSIVE WINDOWS. ? CAN BE ANY LETTER.
15. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE SYMBOLIZATION PAD, AS SHOWN. SUBSTRATES WITH Ni/Pd/Au SHALL HAVE THE SAME MARKING, BUT ROTATED UPSIDE-DOWN.



SECTION F–F
SCALE 10/1



PARTS LIST

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES[MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005[0.127]
  2 PLACE DECIMALS ±.01[0.254]
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 ± .004 ± .001	.126 THRU .250 ± .005 ± .001	.251 THRU .500 ± .006 ± .001
.501 THRU .750 ± .008 ± .001	.751 THRU 1.000 ± .010 ± .001	1.001 THRU 2.000 ± .012 ± .001

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

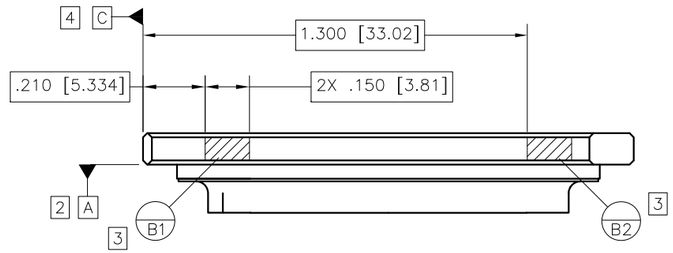
DWN M. AVERY DATE 2/28/05
ENGR M. AVERY 2/28/05
QA
APVD

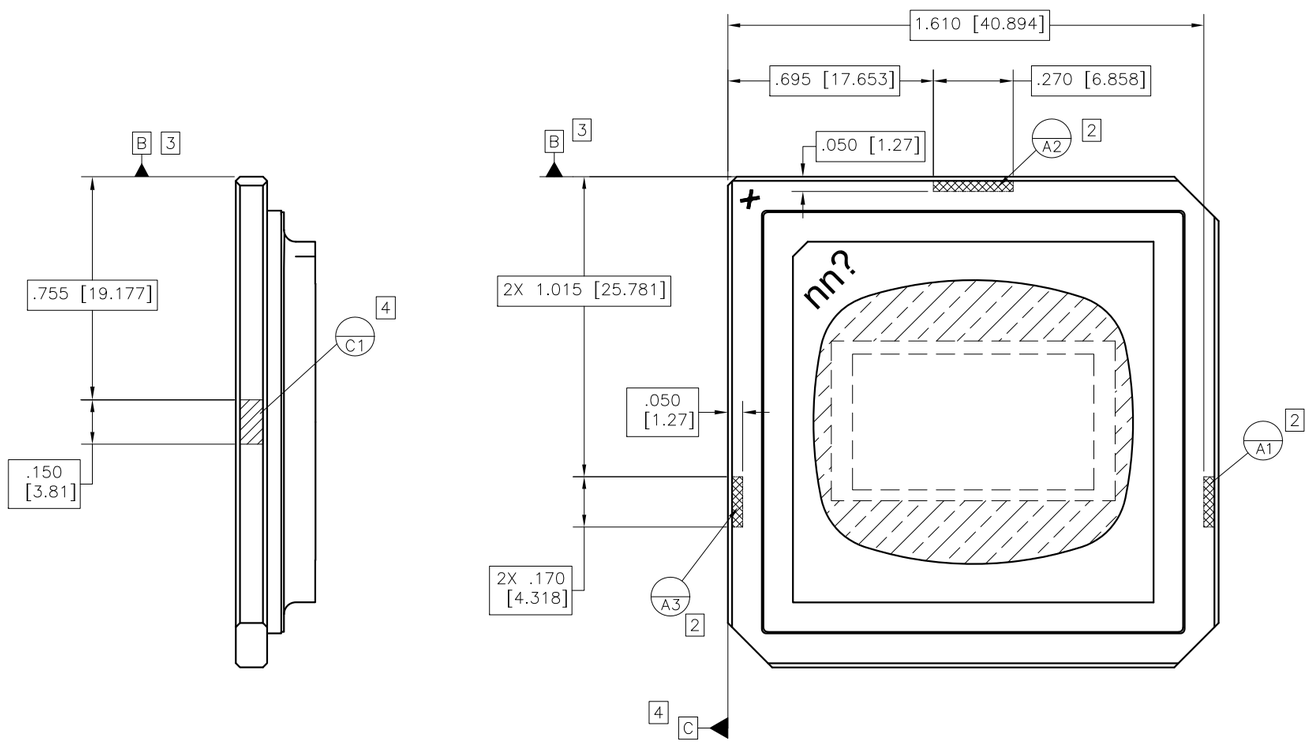
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.95" 1080p TYPE A
(FLN PACKAGE)

SIZE D | DRAWING NO 2506491 | REV D
SCALE 4/1 | SHEET 1 OF 4

ACED1g

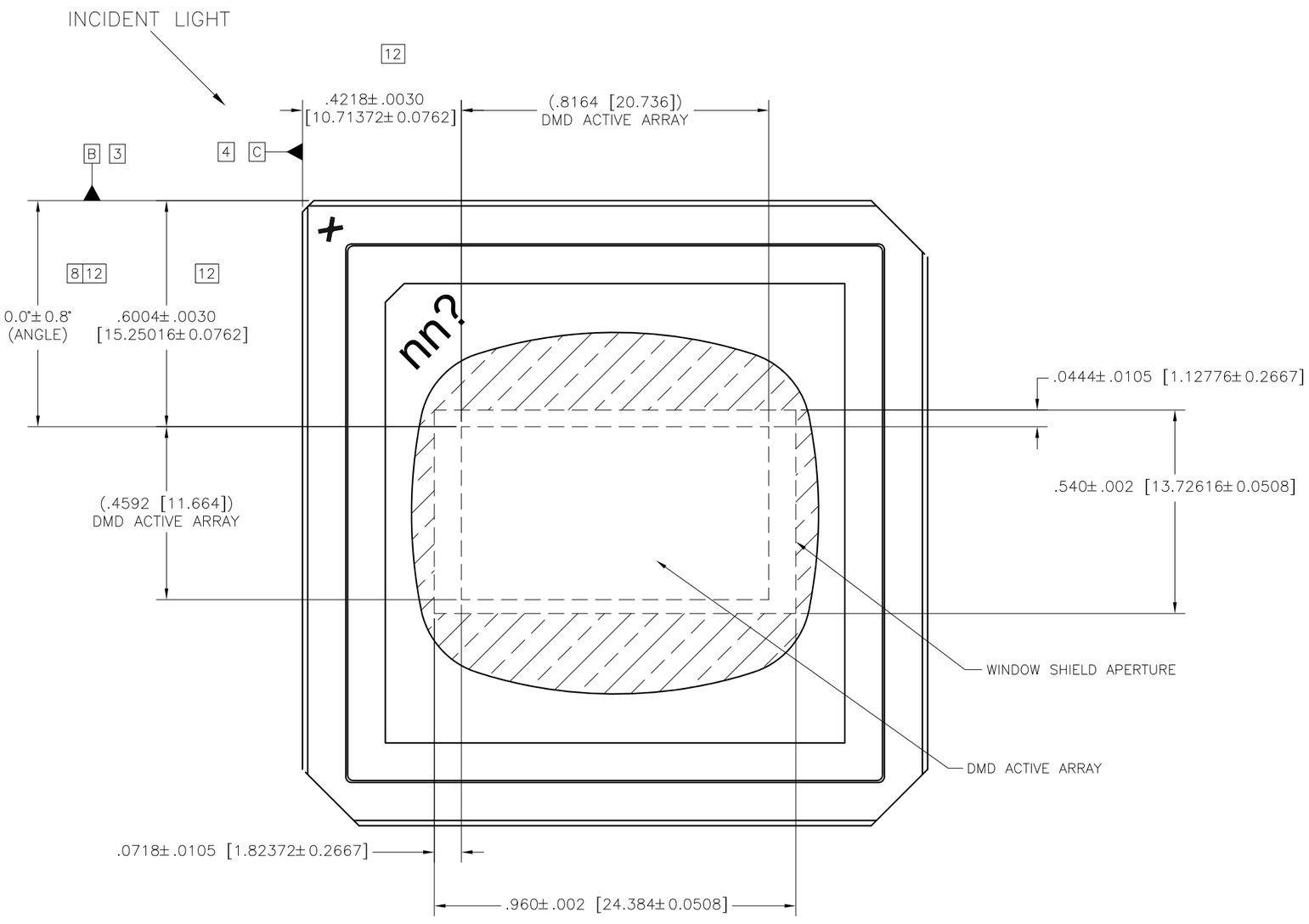




VIEW A (SHEET 1 NOTES)
DATUM A, B AND C DETAILS

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D		DRAWING NO 2506491	REV D
		SCALE 4/1		SHEET 2	

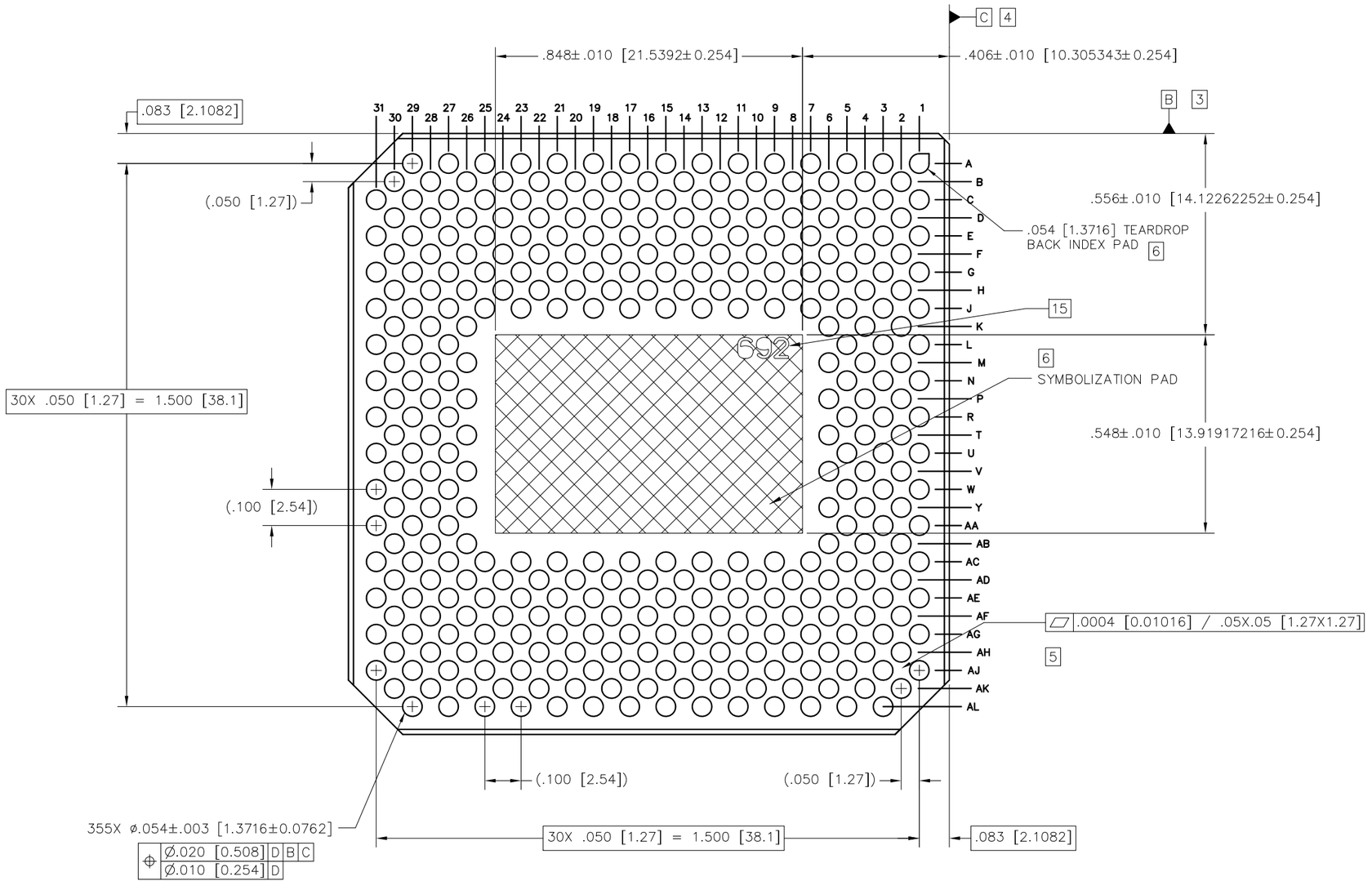
ACED2c



VIEW B (SHEET 1)
POSITION OF ACTIVE ARRAY
SCALE 6/1

Texas Instruments, Dallas, Texas	DWN	DATE	SIZE D		DRAWING NO 2506491	REV D
	ISSUE DATE		SCALE 4/1		SHEET 3	

ACED2c



VIEW C–C (SHEET 1)
BACK PADS
SCALE 6/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2506491	REV D
		SCALE 4/1	SHEET 4	

ACED2c

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