# DLPC200 DLPデジタル・コントローラ、DLP5500 DMD用

## 1 特長

- DLP5500 DMDの高信頼性動作に必要
- 2つの24ビット入力ポート(RGB888)によりデータをリアルタイムでストリーミング
  - ポート1はHDMI入力に対応
  - ポート2は拡張カード経由の入力に対応
- 高速のパターン・シーケンス・モード
  - パターン・データを直接デバイスにダウンロード
  - 5000Hzまでの、1ビットのバイナリ・パターン速度
  - 700Hzまでの、8ビットのグレイスケール・パターン速度
  - マイクロミラーへの1対1の入力マッピング
  - パターンの順序変更をプログラム可能
- カメラやセンサと簡単に同期
  - 3つの構成可能な出力トリガ
  - 2つの構成可能な入力トリガ
- 複数の構成インターフェイス
  - $I^2C$経由のEDIDをサポート
  - USBおよびSPIデバイスの制御

## 2 アプリケーション

- マシン・ビジョン
  - 3D深度測定およびキャプチャ
  - ロボット誘導
  - インライン表面検査
  - ピック・アンド・プレース
- 3Dプリンタ
- 医療用計測機器
  - 3D歯科用スキャナ
  - 導管イメージング
  - マイクロスコープ
- コンピュータ・トゥ・プレート・プリンタ
- 3Dバイオメトリクス
  - 指紋認識
  - 顔認識

## 3 概要

DLPC200は画像処理、制御、およびDMDデータのフォーマットを行い、0.55 XGA DMD (DLP5500)を駆動します。

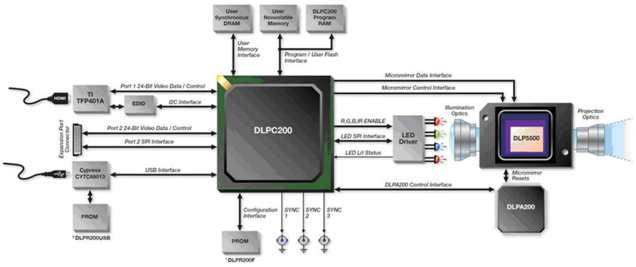
このデジタル・コントローラにより、信頼性が高く独立した高速マイクロミラー制御を行え、立体照明、ディスプレイ、その他空間光変調器(SLM)アプリケーションが可能になります。DLPC200はソリッドステート照明(SSI)を使用して、バイナリで5000Hz、または8ビット・グレイスケールで700Hzまでのパターン速度に対応できます。

簡単にプログラム可能なデバイスで、ユーザーはチップセットを外部ソース(センサ、カメラ、プロセッサなど)と接続して同期させることができ、高精度の3Dマシン・ビジョン・アプリケーションを設計できます。複数の構成インターフェイスが存在するため、外部および組み込みの入力ソースを柔軟に使用できます。カスタム・パターンの読み込みと保存を簡単に行えるため、DLPC200は高度な照明制御アプリケーションに理想的です。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| DLPC200 | BGA (780) | 29.00mm×29.00mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision E (August 2014)** から **Revision F** に変更 **Page**

- Added "(does not tristate)" to pin function entry SLAVE_SPI_MISO ... 8
- Deleted the active low indicator in the SLAVE_SPI_ACK in SPI Slave Interface Timing Requirements ... 27
- Changed SPI Timing Figure to reflect that the SLAVE_SPI_MISO signal does not tristate ... 27
- Changed SPI Timing Figure to reflect that SLAVE_SPI_ACK is an active high signal ... 27
- Removed active low indicator from the SLAVE_SPI_ACK signal in SPI Slave Interface ... 40
- Added clarifying note on the operation of the SLAVE_SPI_MOSI signal in SPI Slave Interface ... 40

**Revision D (March 2012)** から **Revision E** に変更 **Page**

- 「*取り扱い定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Updated descriptions in Pin Functions table ... 6
- Added Grounding scheme for Video Port 1 signals if not used ... 6
- Added Grounding scheme for video port 2 signals if not used ... 7
- Added Connection scheme for EDID and USB if not used ... 8
- Added Connection scheme for LED illumination Control if not used ... 15
- Added recommendation for 1-kΩ pullup to 3.3 V ... 15
- Changed from "recommend grounding" to "recommend 10-kΩ pulldown to DGND" for RSVD_S1, RSVD_S2, RSVD_S3, RSVD_X11, RSVD_S20, and RSVD_S21 ... 17


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- Changed description for RSVD_S0 from "do not connect" to "can be left open, recommend 10-kΩ pullup to 2.5 V" ..... 17
- Changed pin description for RSVD_x15 and RSVD_X13 from "do not connect" to "do not leave open, required: 49.4-Ω pullup to 1.8 V" ..... 17
- Changed pin description for RSVD_X14 and RSVD_X12 from "do not connect" to "do not leave open, required: 49.9-Ω pulldown to DGND" ..... 17
- Changed from "do not connect" to "can be left open, recommend 10-kΩ pullup to 1.8 V" for RSVD_S4 ..... 17
- Changed pin description for RSVD_S18 and RSVD_S19 from "do not connect" to "can be left open, recommend 10-kΩ pullup to 2.5 V" ..... 18
- Deleted Case Temperature thermal resistance ..... 20
- Changed Micron MT47H32M16-25E replaces now obsolete MT47H32M16R ..... 43
- Added Note about LED enabling after initilization is complete ..... 45
- Added Heat Sink section ..... 47

**Revision C (February 2012) から Revision D に変更** **Page**

- Changed the $\overline{ADV}$ time line in Figure 6 ..... 28

**Revision B (December 2010) から Revision C に変更** **Page**

- Changed typo on pin number for PORT1_D10 Pin ..... 6
- Changed typo on pin number for USB_CLK Pin ..... 8
- Changed I/O type to $B_2$ for USB interface data bus Pins ..... 8
- Added pin number A15 to PINFUNCTIONS table ..... 8
- Changed I/O type to $B_2$ for Flash/SRAM data Pins ..... 11
- Corrected the I/O type to $O_3$ on $\overline{CFG_CS0}$ terminal pin ..... 16
- Added pin number AB17, U7, U8, and AD15 to Pin Functions table ..... 17
- Changed location of Absolute Maximum Ratings and Recommended Operating Conditions Tables in document ..... 20
- Changed MIN and MAX $T_J$ values in *Recommended Operating Conditions* ..... 20
- Added $V_{CC33}$ and $V_{REF_B2-4}$ pins to *Recommended Operating Conditions* ..... 20
- Changed Input Port Interface figure ..... 22
- Changed SPI *Slave Interface Timing Requirements* table ..... 27
- Added SPI Timing diagram ..... 27
- Changed $\overline{RST}$signal timing in Parallel Flash Write Timing diagram ..... 29
- Changed signal notations in *Serial Flash Interface Timing Requirements* table ..... 30
- Changed signal notations in Flash Memory Interface Timing diagram ..... 30
- Changed signal notations in DLPA200 I/F Timing diagram ..... 32
- Changed Typical Application diagram ..... 38
- Changed paragraph about read mode in *Parallel Flash Memory Interface* ..... 41
- Deleted SRAM Interface Timing diagram and provided reference to the OEM data sheet ..... 41
- Replaced "DAD" with "DLPA200" ..... 42
- 変更ドキュメント内でデバイス・マーキングの位置を ..... 48

**Revision A (May 2010) から Revision B に変更** **Page**

- Changed typo on pin number for MEM_D43 Pin ..... 14
- Changed typo on pin number for MEM_D62 Pin ..... 14
- Added part number used for EEPROM ..... 40
- Changed part number for Winbond part ..... 41

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- Added new section for Power-Down Requirements ..... 45

**2010年4月発行のものから更新** **Page**

- Added / changed pin names, updated descriptions in Pin Functions table ..... 6
- Changed junction temperature and notated need for heat sink ..... 20
- Deleted unused types, updated values in I/O Characteristics table ..... 21
- Changed parameter names to match figure ..... 34
- Added new section for Power-Up Requirements ..... 45
- 変更「関連文書」のTI文書番号をDLPS012からDLPZ004に ..... 48


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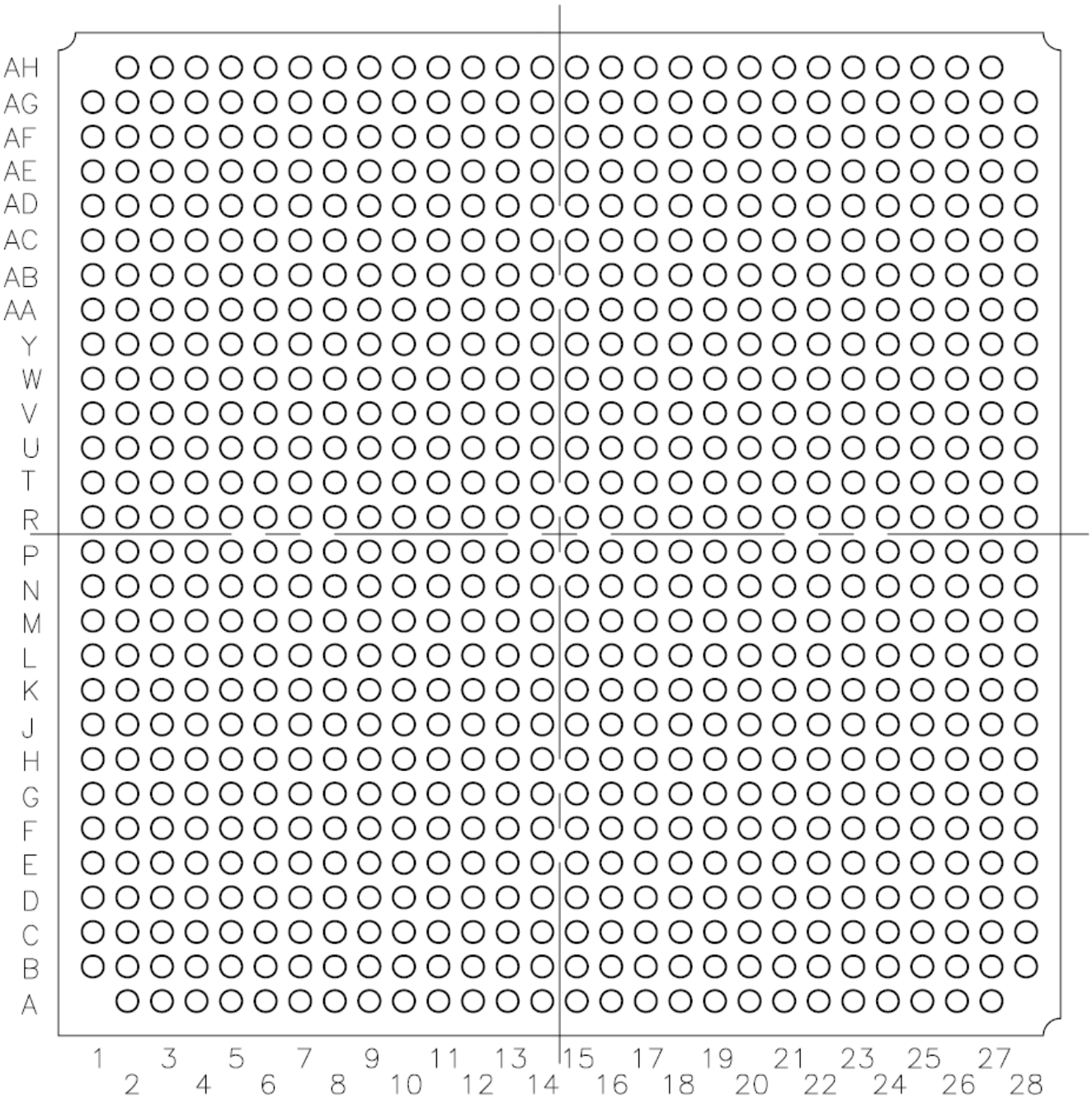
# 5 Pin Configuration and Functions

**BGA**
**780 PINS**

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## Pin Functions

| PIN | | I/O TYPE(1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **PORT 1 VIDEO DATA AND CONTROL**(2) | | | | |
| PORT1_CLK | J2 | $I_3$ | | Pixel clock (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_VSYNC | N3 | | PORT1_CLK | Vertical sync; weak pullup applied |
| PORT1_HSYNC | P1 | | PORT1_CLK | Horizontal sync; weak pullup applied |
| PORT1_IVALID | P2 | | PORT1_CLK | Data valid (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D0 | D2 | | PORT1_CLK | Pixel data – Blue 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D1 | D3 | | PORT1_CLK | Pixel data – Blue 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D2 | F5 | | PORT1_CLK | Pixel data – Blue 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D3 | D1 | | PORT1_CLK | Pixel data – Blue 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D4 | F3 | | PORT1_CLK | Pixel data – Blue 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D5 | G4 | | PORT1_CLK | Pixel data – Blue 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D6 | F1 | | PORT1_CLK | Pixel data – Blue 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D7 | G3 | | PORT1_CLK | Pixel data – Blue 7 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D8 | H5 | | PORT1_CLK | Pixel data – Green 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D9 | H4 | | PORT1_CLK | Pixel data – Green 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D10 | G2 | | PORT1_CLK | Pixel data – Green 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D11 | J4 | | PORT1_CLK | Pixel data – Green 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D12 | H3 | | PORT1_CLK | Pixel data – Green 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D13 | J3 | | PORT1_CLK | Pixel data – Green 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D14 | K3 | | PORT1_CLK | Pixel data – Green 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D15 | L1 | | PORT1_CLK | Pixel data – Green 7 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D16 | L3 | | PORT1_CLK | Pixel data – Red 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D17 | L4 | | PORT1_CLK | Pixel data – Red 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D18 | M4 | | PORT1_CLK | Pixel data – Red 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D19 | K1 | | PORT1_CLK | Pixel data – Red 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D20 | M1 | | PORT1_CLK | Pixel data – Red 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D21 | K2 | | PORT1_CLK | Pixel data – Red 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D22 | M2 | | PORT1_CLK | Pixel data – Red 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_D23 | M3 | | PORT1_CLK | Pixel data – Red 7 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_HPD | E15 | $B_2$ | | HDMI hotplug detect, (if not used, apply 10-kΩ pulldown to DGND) |
| PORT1_SYNCDET | J22 | | | HDMI input sync detect, (if not used, apply 10-kΩ pulldown to DGND) |

(1) See *I/O Electrical Characteristics* for more detail.
(2) 24-bit data is mapped according to RGB888 pixel format. See Figure 13.


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## Pin Functions (continued)

| PIN | | I/O TYPE(1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **PORT 2 VIDEO DATA AND CONTROL**(2) | | | | |
| PORT2_CLK | Y2 | $I_1$ | | Pixel clock (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_VSYNC | AF2 | | PORT2_CLK | Vertical sync; weak pullup applied |
| PORT2_HSYNC | AB6 | | PORT2_CLK | Horizontal sync; weak pullup applied |
| PORT2_IVALID | W1 | | PORT2_CLK | Data valid (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D0 | Y1 | | PORT2_CLK | Pixel data – Blue 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D1 | AE1 | | PORT2_CLK | Pixel data – Blue 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D2 | U2 | | PORT2_CLK | Pixel data – Blue 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D3 | AD12 | | PORT2_CLK | Pixel data – Blue 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D4 | AB1 | | PORT2_CLK | Pixel data – Blue 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D5 | V3 | | PORT2_CLK | Pixel data – Blue 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D6 | U5 | | PORT2_CLK | Pixel data – Blue 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D7 | T3 | | PORT2_CLK | Pixel data – Blue 7 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D8 | AD1 | | PORT2_CLK | Pixel data – Green 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D9 | AA3 | | PORT2_CLK | Pixel data – Green 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D10 | R6 | | PORT2_CLK | Pixel data – Green 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D11 | W3 | | PORT2_CLK | Pixel data – Green 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D12 | AB5 | | PORT2_CLK | Pixel data – Green 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D13 | AD3 | | PORT2_CLK | Pixel data – Green 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D14 | AD5 | | PORT2_CLK | Pixel data – Green 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D15 | AD4 | | PORT2_CLK | Pixel data – Green 7 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D16 | AE5 | | PORT2_CLK | Pixel data – Red 0 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D17 | AC11 | | PORT2_CLK | Pixel data – Red 1 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D18 | AB8 | | PORT2_CLK | Pixel data – Red 2 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D19 | AC7 | | PORT2_CLK | Pixel data – Red 3 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D20 | AG4 | | PORT2_CLK | Pixel data – Red 4 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D21 | AE4 | | PORT2_CLK | Pixel data – Red 5 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D22 | AF5 | | PORT2_CLK | Pixel data – Red 6 (if not used, apply 10-kΩ pulldown to DGND) |
| PORT2_D23 | AF3 | | PORT2_CLK | Pixel data – Red 7 (if not used, apply 10-kΩ pulldown to DGND) |
| **SYNC IN/SYNC OUT** | | | | |
| PORT1_Trig_in | F2 | $I_3$ | PORT1_CLK | Alternate sync for port 1; treated as Vsync; weak pullup applied |
| PORT1_Sync_out | H6 | $O_3$ | Async | Reserved for future use |
| PORT2_Trig_in | AB7 | $I_1$ | PORT2_CLK | Alternate sync for port 2; treated as vsync; weak pullup applied |
| PORT2_Sync_out | Y3 | $O_1$ | Async | Reserved for future use |

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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **CONTROL INTERFACES ($I^2C$, USB, SPI)** | | | | |
| USB_CLK | B15 | $I_3$ | | USB clock input (48 MHz), feeds a PLL (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL0 | B17 | $I_3$ | USB_CLK | USB I/F FIFO programmable level (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL1 | A26 | $I_3$ | USB_CLK | USB I/F FIFO-full flag (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL2 | D22 | $I_3$ | USB_CLK | USB I/F FIFO-empty flag (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL3 | C19 | $I_3$ | USB_CLK | Reserved for future use (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL4 | D16 | $I_3$ | USB_CLK | Reserved for future use (if not used, apply 10-kΩ pulldown to DGND) |
| USB_CTRL5 | G17 | $I_3$ | USB_CLK | Reserved for future use (if not used, apply 10-kΩ pulldown to DGND) |
| USB_FD0 | G16 | $B_2$ | USB_CLK | USB interface data bus (if not used, apply 10-kΩ pulldown to DGND) |
| USB_FD1 | C26 | | | |
| USB_FD2 | F17 | | | |
| USB_FD3 | C22 | | | |
| USB_FD4 | E18 | | | |
| USB_FD5 | B18 | | | |
| USB_FD6 | F18 | | | |
| USB_FD7 | E19 | | | |
| USB_FD8 | B23 | | | |
| USB_FD9 | D25 | | | |
| USB_FD10 | C21 | | | |
| USB_FD11 | D24 | | | |
| USB_FD12 | B19 | | | |
| USB_FD13 | E25 | | | |
| USB_FD14 | G18 | | | |
| USB_FD15 | C15 | | | |
| USB_PA02 | D23 | $O_3$ | USB_CLK | USB I/F FIFO output enable for reads (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_PA04 | G15 | $O_3$ | USB_CLK | USB I/F FIFO address(0) (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_PA05 | A22 | $O_3$ | USB_CLK | USB I/F FIFO address(1) (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_PA06 | A25 | $O_3$ | USB_CLK | USB I/F FIFO packet end trigger |
| USB_RDY0 | C16 | $O_3$ | USB_CLK | USB I/F FIFO read enable (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_RDY1 | C17 | $O_3$ | USB_CLK | USB I/F FIFO write enable (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_RDY2 | B26 | $O_3$ | USB_CLK | Reserved for future use (if not used, apply 10-kΩ pullup to 3.3 V) |
| USB_RSVD_14 | A15 | $I_3$ | USB_CLK | Reserved for future use (if not used, apply 10-kΩ pulldown to DGND) |
| I2C_SCL | C25 | $B_2$ | | Master $I^2C$ clock - 400 kHz. Requires external pullup |
| I2C_SDA | D18 | $B_2$ | I2C_SCL | Master $I^2C$ data - 400 kHz. Requires external pullup |
| EDID_I2C_SCL | F8 | $B_2$ | | HDMI EDID $I^2C$ clock. 400 kHz. Requires external pullup (if EDID is not used, must be pulled up to 3.3 V through a 47-kΩ resistor) |
| EDID_I2C_SDA | D6 | $B_2$ | EDID_I2C_SCL | HDMI EDID $I^2C$ data. 400-kHz. Requires external pullup (if EDID is not used, must be pulled up to 3.3 V through a 47-kΩ resistor.) |
| SLAVE_SPI_CLK | B14 | $I_3$ | | Slave SPI clock |
| $\overline{\text{SLAVE_SPI_CS}}$ | C14 | $I_3$ | SLAVE_SPI_CLK | Slave SPI chip select; weak pullup applied |
| SLAVE_SPI_MISO | D14 | $O_3$ | SLAVE_SPI_CLK | Slave SPI data OUT (does not tristate) |
| SLAVE_SPI_MOSI | E14 | $I_3$ | SLAVE_SPI_CLK | Slave SPI data IN; weak pullup applied |
| $\overline{\text{SLAVE_SPI_SOP}}$ | F21 | $I_3$ | SLAVE_SPI_CLK | Reserved for future use |
| SLAVE_SPI_ACK | D20 | $O_3$ | SLAVE_SPI_CLK | Slave SPI data busy |


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**Pin Functions (continued)**

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **DMD INTERFACE** | | | | |
| DMD_DAT_AP1 | AB27 | $O_4$ | DMD_DCLK_AP, DMD_DCLK_AN | DMD data pins. LVDS pins for data bus A |
| DMD_DAT_AN1 | AB28 | $O_4$ | | |
| DMD_DAT_AP3 | Y25 | $O_4$ | | |
| DMD_DAT_AN3 | Y26 | $O_4$ | | |
| DMD_DAT_AP5 | W25 | $O_4$ | | |
| DMD_DAT_AN5 | W26 | $O_4$ | | |
| DMD_DAT_AP7 | W28 | $O_4$ | | |
| DMD_DAT_AN7 | W27 | $O_4$ | | |
| DMD_DAT_AP9 | V27 | $O_4$ | | |
| DMD_DAT_AN9 | V28 | $O_4$ | | |
| DMD_DAT_AP11 | V25 | $O_4$ | | |
| DMD_DAT_AN11 | V26 | $O_4$ | | |
| DMD_DAT_AP13 | V23 | $O_4$ | | |
| DMD_DAT_AN13 | V24 | $O_4$ | | |
| DMD_DAT_AP15 | T26 | $O_4$ | | |
| DMD_DAT_AN15 | U27 | $O_4$ | | |
| DMD_DCLK_AP | T25 | $O_4$ | | DMD data clock. LVDS clock for data bus A |
| DMD_DCLK_AN | U28 | $O_4$ | | DMD data clock. LVDS clock for data bus A |
| DMD_SCTRL_AP | R25 | $O_4$ | DMD_DCLK_AP, DMD_DCLK_AN | DMD data serial-control signal bus A (LVDS) |
| DMD_SCTRL_AN | R26 | O | | |
| DMD_DAT_BP1 | AC24 | $O_4$ | DMD_DCLK_BP, DMD_DCLK_BN | DMD data pins. LVDS pins for data bus B |
| DMD_DAT_BN1 | AC25 | $O_4$ | | |
| DMD_DAT_BP3 | AC26 | $O_4$ | | |
| DMD_DAT_BN3 | AD26 | $O_4$ | | |
| DMD_DAT_BP5 | AE27 | $O_4$ | | |
| DMD_DAT_BN5 | AE28 | $O_4$ | | |
| DMD_DAT_BP7 | AD27 | $O_4$ | | |
| DMD_DAT_BN7 | AD28 | $O_4$ | | |
| DMD_DAT_BP9 | Y23 | $O_4$ | | |
| DMD_DAT_BN9 | Y24 | $O_4$ | | |
| DMD_DAT_BP11 | AC27 | $O_4$ | | |
| DMD_DAT_BN11 | AC28 | $O_4$ | | |
| DMD_DAT_BP13 | AB25 | $O_4$ | | |
| DMD_DAT_BN13 | AB26 | $O_4$ | | |
| DMD_DAT_BP15 | AA25 | $O_4$ | | |
| DMD_DAT_BN15 | AA26 | $O_4$ | | |
| DMD_DCLK_BP | U25 | $O_4$ | | DMD data clock. LVDS clock for data bus B |
| DMD_DCLK_BN | U26 | $O_4$ | | |
| DMD_SCTRL_BP | T21 | $O_4$ | DMD_DCLK_AP, DMD_DCLK_AN | DMD data serial-control signal bus B (LVDS) |
| DMD_SCTRL_BN | T22 | $O_4$ | | |
| $\overline{\text{DMD_PWRDN}}$ | P26 | $O_3$ | ASYNC | DMD power down (active-low) |
| $\overline{\text{RST_IRQ}}$ | M25 | $I_3$ | ASYNC | DLPA200 interrupt (active-low) |
| $\overline{\text{RST_OE}}$ | M28 | $O_3$ | ASYNC | DLPA200 output enable |
| $\overline{\text{RST_RST}}$ | H24 | $O_3$ | ASYNC | DLPA200 reset |
| RST_STROBE | G28 | $O_3$ | | DLPA200 strobe |

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## Pin Functions (continued)

| PIN | | I/O TYPE(1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **DMD INTERFACE (CONTINUED)** | | | | |
| RST_SEL0 | G27 | $O_3$ | RST_STROBE | DLPA200 voltage select |
| RST_SEL1 | G26 | | | |
| RST_MODE0 | L24 | $O_3$ | RST_STROBE | DLPA200 mode select |
| RST_MODE1 | L23 | | | |
| RST_A0 | K25 | $O_3$ | RST_STROBE | DLPA200 address |
| RST_A1 | J26 | | | |
| RST_A2 | J25 | | | |
| RST_A3 | K26 | | | |
| SCP_DMD_RST_DO | G25 | $O_3$ | SCP_DMD_RST_CLK | SCP data out (write data) |
| SCP_DMD_RST_DI | H26 | $I_3$ | SCP_DMD_RST_CLK | SCP data in (read data) |
| $\overline{\text{SCP_DMD_EN}}$ | L25 | $O_3$ | SCP_DMD_RST_CLK | DMD SCP chip select |
| $\overline{\text{SCP_RST_EN}}$ | H23 | $O_3$ | SCP_DMD_RST_CLK | DLPA200 SCP chip select |
| SCP_DMD_RST_CLK | H25 | $O_3$ | | DMD/DLPA200 SCP clock, 125 kHz |
| **STATIC RAM INTERFACE** | | | | |
| $\overline{\text{FLASH_CE}}$ | D12 | $O_3$ | ASYNC | Flash chip enable |
| FLASH_SRAM_A0 | D13 | $O_3$ | $\overline{\text{FLASH_SRAM_WE}}$ | Flash/SRAM address |
| FLASH_SRAM_A1 | A11 | | | |
| FLASH_SRAM_A2 | C11 | | | |
| FLASH_SRAM_A3 | D11 | | | |
| FLASH_SRAM_A4 | A12 | | | |
| FLASH_SRAM_A5 | B12 | | | |
| FLASH_SRAM_A6 | D10 | | | |
| FLASH_SRAM_A7 | A10 | | | |
| FLASH_SRAM_A8 | B10 | | | |
| FLASH_SRAM_A9 | B8 | | | |
| FLASH_SRAM_A10 | C8 | | | |
| FLASH_SRAM_A11 | A7 | | | |
| FLASH_SRAM_A12 | B7 | | | |
| FLASH_SRAM_A13 | A4 | | | |
| FLASH_SRAM_A14 | D7 | | | |
| FLASH_SRAM_A15 | C6 | | | |
| FLASH_SRAM_A16 | D8 | | | |
| FLASH_SRAM_A17 | B6 | | | |
| FLASH_SRAM_A18 | C7 | | | |
| FLASH_SRAM_A19 | A8 | | | |
| FLASH_SRAM_A20 | C4 | | | |
| FLASH_SRAM_A21 | B3 | | | |
| FLASH_SRAM_A22 | A3 | | | |
| FLASH_SRAM_A23 | C5 | | | |
| FLASH_SRAM_A24 | D5 | | | |
| FLASH_SRAM_A25 | B4 | | | |
| FLASH_SRAM_A26 | D4 | | | |


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**Pin Functions (continued)**

| PIN | | I/O TYPE(1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **STATIC RAM INTERFACE (CONTINUED)** | | | | |
| FLASH_SRAM_D0 | E11 | $B_2$ | $\overline{\text{FLASH_SRAM_WE}}$ | Flash/SRAM data |
| FLASH_SRAM_D1 | F10 | | | |
| FLASH_SRAM_D2 | E10 | | | |
| FLASH_SRAM_D3 | G9 | | | |
| FLASH_SRAM_D4 | E8 | | | |
| FLASH_SRAM_D5 | E7 | | | |
| FLASH_SRAM_D6 | E5 | | | |
| FLASH_SRAM_D7 | E4 | | | |
| FLASH_SRAM_D8 | F11 | | | |
| FLASH_SRAM_D9 | E12 | | | |
| FLASH_SRAM_D10 | F12 | | | |
| FLASH_SRAM_D11 | G12 | | | |
| FLASH_SRAM_D12 | G13 | | | |
| FLASH_SRAM_D13 | H13 | | | |
| FLASH_SRAM_D14 | F14 | | | |
| FLASH_SRAM_D15 | G14 | | | |
| $\overline{\text{FLASH_SRAM_OE}}$ | C10 | $O_3$ | | Flash output enable |
| FLASH_SRAM_RDY | C13 | $I_3$ | | Flash wait |
| $\overline{\text{FLASH_SRAM_RST}}$ | C12 | $O_3$ | | Flash reset |
| $\overline{\text{FLASH_SRAM_WE}}$ | A6 | $O_3$ | | Flash write enable |
| $\overline{\text{SRAM_CE}}$ | B11 | $O_3$ | | SRAM chip enable |
| $\overline{\text{SRAM_LB}}$ | D9 | $O_3$ | | SRAM lower byte enable |
| $\overline{\text{SRAM_UB}}$ | C9 | $O_3$ | | SRAM upper byte enable |
| **SDRAM INTERFACE** | | | | |
| MEM_CLK_P0 | R2 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_N0 | R1 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_P1 | U3 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_N1 | U4 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_P2 | AC5 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_N2 | AC4 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_P3 | AE14 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CLK_N3 | AF14 | $O_5$ | | DDR2 memory, differential memory clock |
| MEM_CKE0 | AF12 | $O_5$ | | |
| MEM_BA0 | Y19 | $O_5$ | MEM_CLK | |
| MEM_BA1 | AD21 | $O_5$ | MEM_CLK | |
| MEM_BA2 | AE7 | $O_5$ | MEM_CLK | |

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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **SDRAM INTERFACE (CONTINUED)** | | | | |
| MEM_A0 | AD24 | $O_5$ | MEM_CLK | DDR2 memory, multiplexed row and column address. The memory in the kit is 512 Mb in ×16 mode, 8 Meg × 16 bits × 4 banks. Only A(12:0) and BA(1:0) are currently used. A(15:13) and BA(2) are reserved for future use (RFU). |
| MEM_A1 | AF21 | | | |
| MEM_A2 | AG23 | | | |
| MEM_A3 | AE8 | | | |
| MEM_A4 | AG12 | | | |
| MEM_A5 | AF23 | | | |
| MEM_A6 | AC17 | | | |
| MEM_A7 | AA16 | | | |
| MEM_A8 | AE23 | | | |
| MEM_A9 | AE22 | | | |
| MEM_A10 | AE16 | | | |
| MEM_A11 | AD25 | | | |
| MEM_A12 | AF19 | | | |
| MEM_A13 | AH10 | | | |
| MEM_A14 | AA8 | | | |
| MEM_A15 | AD11 | | | |
| $\overline{\text{MEM_CAS}}$ | AG19 | $O_5$ | MEM_CLK | Column address strobe, active low |
| $\overline{\text{MEM_RAS}}$ | AE20 | $O_5$ | MEM_CLK | Row address strobe, active low |
| $\overline{\text{MEM_CS0}}$ | AF13 | $O_5$ | MEM_CLK | Chip select, active low |
| $\overline{\text{MEM_WE}}$ | AG25 | $O_5$ | MEM_CLK | Write enable, active low |
| MEM_ODT | AH12 | $O_5$ | MEM_CLK | |
| MEM_DM0 | W2 | $O_5$ | MEM_CLK | |
| MEM_DM1 | AE2 | $O_5$ | MEM_CLK | |
| MEM_DM2 | AH6 | $O_5$ | MEM_CLK | |
| MEM_DM3 | AF7 | $O_5$ | MEM_CLK | |
| MEM_DM4 | AE13 | $O_5$ | MEM_CLK | |
| MEM_DM5 | AH18 | $O_5$ | MEM_CLK | |
| MEM_DM6 | AF24 | $O_5$ | MEM_CLK | |
| MEM_DM7 | AG26 | $O_5$ | MEM_CLK | |
| MEM_DS0 | AB2 | $B_1$ | MEM_CLK_P0 | |
| MEM_DS1 | AE3 | $B_1$ | MEM_CLK_N0 | |
| MEM_DS2 | AD7 | $B_1$ | MEM_CLK_P1 | |
| MEM_DS3 | AE10 | $B_1$ | MEM_CLK_N1 | |
| MEM_DS4 | AF11 | $B_1$ | MEM_CLK_P2 | |
| MEM_DS5 | AF17 | $B_1$ | MEM_CLK_N2 | |
| MEM_DS6 | AE18 | $B_1$ | MEM_CLK_P3 | |
| MEM_DS7 | AF26 | $B_1$ | MEM_CLK_N3 | |


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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **SDRAM INTERFACE (CONTINUED)** | | | | |
| MEM_D0 | R3 | $B_1$ | MEM_DS0, MEM_DS1 | |
| MEM_D1 | R4 | $B_1$ | | |
| MEM_D2 | T4 | $B_1$ | | |
| MEM_D3 | R5 | $B_1$ | | |
| MEM_D4 | U1 | $B_1$ | | |
| MEM_D5 | V4 | $B_1$ | | |
| MEM_D6 | V2 | $B_1$ | | |
| MEM_D7 | V1 | $B_1$ | | |
| MEM_D8 | U6 | $B_1$ | | |
| MEM_D9 | Y4 | $B_1$ | | |
| MEM_D10 | AC2 | $B_1$ | | |
| MEM_D11 | AC1 | $B_1$ | | |
| MEM_D12 | AC3 | $B_1$ | | |
| MEM_D13 | AD2 | $B_1$ | | |
| MEM_D14 | AB3 | $B_1$ | | |
| MEM_D15 | AA4 | $B_1$ | | |
| MEM_D16 | AE6 | $B_1$ | MEM_DS2, MEM_DS3 | |
| MEM_D17 | AF4 | $B_1$ | | |
| MEM_D18 | AG3 | $B_1$ | | |
| MEM_D19 | AH3 | $B_1$ | | |
| MEM_D20 | AF6 | $B_1$ | | |
| MEM_D21 | AH4 | $B_1$ | | |
| MEM_D22 | AD8 | $B_1$ | | |
| MEM_D23 | AG6 | $B_1$ | | |
| MEM_D24 | AB9 | $B_1$ | | |
| MEM_D25 | AD10 | $B_1$ | | |
| MEM_D26 | AG7 | $B_1$ | | |
| MEM_D27 | AH7 | $B_1$ | | |
| MEM_D28 | AC8 | $B_1$ | | |
| MEM_D29 | AA10 | $B_1$ | | |
| MEM_D30 | AG8 | $B_1$ | | |
| MEM_D31 | AH8 | $B_1$ | | |

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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **SDRAM INTERFACE (CONTINUED)** | | | | |
| MEM_D32 | AF8 | $B_1$ | MEM_DS4, MEM_DS5 | |
| MEM_D33 | AE9 | $B_1$ | | |
| MEM_D34 | AF10 | $B_1$ | | |
| MEM_D35 | AG10 | $B_1$ | | |
| MEM_D36 | AE12 | $B_1$ | | |
| MEM_D37 | AE11 | $B_1$ | | |
| MEM_D38 | AG11 | $B_1$ | | |
| MEM_D39 | AH11 | $B_1$ | | |
| MEM_D40 | AC15 | $B_1$ | | |
| MEM_D41 | AF15 | $B_1$ | | |
| MEM_D42 | AG17 | $B_1$ | | |
| MEM_D43 | AH17 | $B_1$ | | |
| MEM_D44 | AF16 | $B_1$ | | |
| MEM_D45 | AB16 | $B_1$ | | |
| MEM_D46 | AE17 | $B_1$ | | |
| MEM_D47 | AG18 | $B_1$ | | |
| MEM_D48 | AH19 | $B_1$ | MEM_DS6, MEM_DS7 | |
| MEM_D49 | AD17 | $B_1$ | | |
| MEM_D50 | AG21 | $B_1$ | | |
| MEM_D51 | AH21 | $B_1$ | | |
| MEM_D52 | AG22 | $B_1$ | | |
| MEM_D53 | AH22 | $B_1$ | | |
| MEM_D54 | AH23 | $B_1$ | | |
| MEM_D55 | AE19 | $B_1$ | | |
| MEM_D56 | AF25 | $B_1$ | | |
| MEM_D57 | AF20 | $B_1$ | | |
| MEM_D58 | AD18 | $B_1$ | | |
| MEM_D59 | AE21 | $B_1$ | | |
| MEM_D60 | AE25 | $B_1$ | | |
| MEM_D61 | AH25 | $B_1$ | | |
| MEM_D62 | AF22 | $B_1$ | | |
| MEM_D63 | AE24 | $B_1$ | | |


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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **LED DRIVER INTERFACE** | | | | |
| PWM0 | C27 | $O_3$ | Async | PWM signal used to control the LED current (if not used, apply 10-kΩ pulldown to DGND) |
| PWM1 | D28 | $O_3$ | Async | PWM signal used to control the LED current (if not used, apply 10-kΩ pulldown to DGND) |
| PWM2 | D27 | $O_3$ | Async | PWM signal used to control the LED current (if not used, apply 10-kΩ pulldown to DGND) |
| PWM3 | D26 | $O_3$ | Async | PWM signal used to control the LED current (if not used, apply 10-kΩ pulldown to DGND) |
| LED_IR_EN | E28 | $O_3$ | Async | IR LED enable strobe. Controlled by programmable DMD sequence timing (active high), (if not used, apply 1-kΩ pulldown to DGND) |
| LED_RED_EN | F28 | $O_3$ | Async | RED LED enable strobe. Controlled by programmable DMD sequence timing (active high), (if not used, apply 1-kΩ pulldown to DGND) |
| LED_GRN_EN | E27 | $O_3$ | Async | Green LED enable strobe. Controlled by programmable DMD sequence timing (active high), (if not used, apply 1-kΩ pulldown to DGND) |
| LED_BLU_EN | F27 | $O_3$ | Async | Blue LED enable strobe. Controlled by programmable DMD sequence timing (active high), (if not used, apply 1-kΩ pulldown to DGND) |
| LED_SUBFRAME | E26 | $O_3$ | Async | Subframe signal used by LED driver. Controlled by programmable DMD sequence timing (active high), (if not used, apply 1-kΩ pulldown to DGND) |
| SYNC_0 | F26 | $O_3$ | Async | Extra strobe. Controlled by programmable DMD sequence timing (active-high) |
| SYNC_1 | F25 | $O_3$ | Async | Extra strobe. Controlled by programmable DMD sequence timing (active-high) |
| SYNC_2 | F24 | $O_3$ | Async | Extra strobe. Controlled by programmable DMD sequence timing (active-high) |
| $\overline{\text{LED_EN}}$ | L28 | $O_3$ | Async | LED driver enable. Active-low output control to external LED drive logic, recommend 1-kΩ pullup to 3.3 V |
| LED_SYNC | M21 | $O_3$ | Async | Reserved for future use; weak pullup applied |
| LED_SYNCEN | C24 | $O_3$ | Async | Inverted $\overline{\text{LED_LIT}}$ signal (if not used, apply 10-kΩ pulldown to DGND) |
| $\overline{\text{LED_LIT}}$ | J28 | $I_3$ | Async | LED driver status, (if not used, apply 1-kΩ pulldown to DGND) |
| LED_SENS | K27 | $I_3$ | Async | Reserved for future use (if not used, apply 1-kΩ pulldown to DGND) |
| LED_SPI_CLK | N26 | $O_3$ | Async | LED SPI master clock (if not used, apply 1-kΩ pullup to 3.3 V) |
| $\overline{\text{LED_SPI_CS}}$ | M26 | $O_3$ | LED_SPI_CLK | LED SPI master chip select (if not used, apply 1-kΩ pullup to 3.3 V) |
| LED_SPI_DIR | P25 | $O_3$ | LED_SPI_CLK | LED SPI master driver direction (if not used, apply 1-kΩ pullup to 3.3 V) |
| LED_SPI_MISO | L27 | $I_3$ | LED_SPI_CLK | LED SPI master data IN (if not used, apply 1-kΩ pullup to 3.3 V) |
| LED_SPI_MOSI | L26 | $O_3$ | LED_SPI_CLK | LED SPI master data OUT; weak pullup applied |

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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **SYSTEM INTERFACES** | | | | |
| $\overline{\text{CFG_CSO}}$ | E2 | $O_3$ | CFG_DCLK | Chip-select output for an external serial configuration device. Active low |
| CFG_CLK | P3 | $O_3$ | CFG_DCLK | Configuration serial EPROM data clock |
| CFG_ASDI | N7 | $I_3$ | CFG_DCLK | Data input from an external serial configuration device. Provides configuration data for the device |
| CFG_ASDO | F4 | $O_3$ | CFG_DCLK | Serial data output. This pin sends address and control information to the external PROM during configuration. |
| $\overline{\text{CFG_STATUS}}$ | M6 | $O_3$ | CFG_DCLK | Configuration status pin |
| CFG_DONE | P24 | $O_3$ | CFG_DCLK | Configuration-done status pin. Signal goes high at the end of configuration. |
| CFG_MSEL0 | N22 | $I_3$ | Async | Configuration-mode selection signals |
| CFG_MSEL1 | P23 | | | |
| CFG_MSEL2 | M22 | | | |
| CFG_MSEL3 | P22 | | | |
| $\overline{\text{CFG_CE}}$ | R8 | $I_3$ | Async | Chip enable. Active-low |
| $\overline{\text{CFG_EN}}$ | P4 | $I_3$ | Async | Configuration control. Configuration starts when a low-to-high transition is detected at this pin. |
| $\overline{\text{CFG_CEO}}$ | P28 | $O_3$ | Async | |
| REF_CLK | J27 | $I_3$ | | 50-MHz reference clock, 3.3 V |
| $\overline{\text{RESET}}$ | A14 | $I_3$ | Async | Device reset (active-low) |
| PWR_GOOD | A23 | $I_3$ | Async | System power-good indicator |
| **RESERVED** | | | | |
| RSVD_H10 | N4 | $B_2$ | | GPIO |
| RSVD_H11 | L2 | $B_2$ | | GPIO |
| RSVD_H12 | K4 | $B_2$ | | GPIO |
| RSVD_H6 | G1 | $B_2$ | | GPIO |
| RSVD_H5 | G5 | $B_2$ | | GPIO |
| RSVD_H4 | G6 | $B_2$ | | GPIO |
| RSVD_H2 | E1 | $B_2$ | | GPIO |
| RSVD_H1 | C2 | $B_2$ | | GPIO |
| RSVD_T0 | E22 | | | These I/Os can be left open or unconnected for normal operation. |
| RSVD_T1 | D21 | | | |
| RSVD_T2 | A21 | | | |
| RSVD_T3 | C18 | | | |
| RSVD_T4 | B22 | | | |
| RSVD_T5 | B21 | | | |
| RSVD_T6 | D17 | | | |
| RSVD_T7 | E21 | | | |
| RSVD_TC | M24 | | | |
| RSVD_D0 | A17 | $I_3$ | | Reserved for future use, do not connect |
| RSVD_D1 | D15 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_D2 | E17 | $I_3$ | | Reserved for future use, do not connect |
| RSVD_D3 | F15 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_H3 | E3 | $I_3$ | | Reserved for future use, can be left open, recommend grounding |
| RSVD_H7 | H7 | $I_3$ | | Reserved for future use, can be left open, recommend grounding |
| RSVD_H8 | L5 | $I_3$ | | Reserved for future use, can be left open, recommend grounding |
| RSVD_H9 | M5 | $I_3$ | | Reserved for future use, can be left open, recommend grounding |


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## Pin Functions (continued)

| PIN | | I/O TYPE (1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **RESERVED (CONTINUED)** | | | | |
| RSVD_H13 | J1 | $I_3$ | | Reserved for future use, can be left open, recommend grounding |
| RSVD_P0 | P7 | $I_4$ | | Reserved for future use, do not connect |
| RSVD_P1 | P6 | $O_2$ | | Reserved for future use, do not connect |
| RSVD_P2 | P8 | $I_4$ | | Reserved for future use, do not connect |
| RSVD_P3 | P5 | $I_4$ | | Reserved for future use, do not connect |
| RSVD_G0 | C23 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G1 | F19 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G2 | M27 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G3 | N21 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G4 | P27 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G5 | A18 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_G6 | A19 | $O_3$ | | Reserved for future use, do not connect |
| RSVD_S1 | AG14 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_S2 | AG15 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_S3 | AH14 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_X11 | AH15 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_S20 | Y27 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_S21 | Y28 | | | Unused input only, can be left open, recommend 10-kΩ pulldown to DGND |
| RSVD_X9 | AA22 | | | Reserved for future use, do not connect |
| RSVD_S0 | AA24 | | | Reserved for future use, can be left open, recommend 10-kΩ pullup to 2.5 V |
| RSVD_X10 | AB23 | | | Reserved for future use, do not connect |
| RSVD_X6 | AB24 | | | Reserved for future use, do not connect |
| RSVD_X3 | AC21 | | | Reserved for future use, do not connect |
| RSVD_X15 | AA17 | | | Reserved, do not leave open, required: 49.4-Ω pullup to 1.8 V |
| RSVD_X14 | AB17 | | | Reserved, do not leave open, required: 49.9-Ω pulldown to DGND |
| RSVD_X13 | U7 | | | Reserved, do not leave open, required: 49.4-Ω pullup to 1.8V |
| RSVD_X12 | U8 | | | Reserved, do not leave open, required: 49.9-Ω pulldown to DGND |
| RSVD_X2 | AE15 | | | Reserved for future use, do not connect |
| RSVD_X0 | AF18 | | | Reserved for future use, do not connect |
| RSVD_X1 | AD15 | | | Reserved for future use, do not connect |
| RSVD_X8 | AF27 | | | Reserved for future use, do not connect |
| RSVD_X4 | AF9 | | | Reserved for future use, do not connect |
| RSVD_S4 | AH26 | | | Reserved for future use, can be left open, recommend 10-kΩ pullup to 1.8 V |
| RSVD_S5 | B25 | | | Reserved for future use, do not connect |
| RSVD_S6 | C20 | | | Reserved for future use, do not connect |
| RSVD_S8 | D19 | | | Reserved for future use, do not connect |
| RSVD_X5 | E24 | | | Reserved for future use, do not connect |
| RSVD_S10 | F22 | | | Reserved for future use, do not connect |

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## Pin Functions (continued)

| PIN | | I/O TYPE(1) | CLOCK SYSTEM | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| **RESERVED (CONTINUED)** | | | | |
| RSVD_S11 | K28 | | | Reserved for future use, do not connect |
| RSVD_S14 | N25 | | | Reserved for future use, do not connect |
| RSVD_X7 | R24 | | | Reserved for future use, do not connect |
| RSVD_S16 | R27 | | | Reserved for future use, do not connect |
| RSVD_S17 | R28 | | | Reserved for future use, do not connect |
| RSVD_S18 | U23 | | | Reserved for future use, can be left open, recommend 10-kΩ pullup to 2.5 V |
| RSVD_S19 | U24 | | | Reserved for future use, can be left open, recommend 10-kΩ pullup to 2.5 V |
| **POWER AND GROUND**(3) | | | | |
| P1P2V | | PWR | N/A | 1.2-V core power |
| P2P5V_DPLL | | PWR | N/A | 2.5-V filtered power for internal PLL |
| P1P8V | | PWR | N/A | 1.8-V I/O power |
| P2P5V | | PWR | N/A | 2.5-V I/O power |
| P3P3V | | PWR | N/A | 3.3-V I/O power |
| GND | | PWR | N/A | Common digital ground |
| GNDA | | PWR | N/A | Common PLL ground |

(3) Unused inputs should be pulled down to ground through an external resistor.


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**Power and Ground Pins**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NUMBER | |
| **INPUT POWER AND GROUND PINS** | | |
| VCC_1P2V | K9, K11, K13, K15, K17, K19, L10, L12, L14, L16, L18, L20, M9, M11, M13, M15, M17, M19, N10, N12, N14, N16, N18, N20, P9, P11, P13, P15, P17, P19, R10, R12, R14, R16, R18, R20, T9, T11, T13, T15, T17, T19, U10, U12, U14, U16, U18, U20, V9, V11, V13, V15, V17, V19, W10, W12, W14, W16, W18, W20 | 1.2-V power supply for core logic |
| VCC_2P5V | AA28, AG28, T24, T28, W24 | 2.5-V power supply for I/Os on bank 5 |
| VCC_1P8V | AA1, AG1, T1, T5, W5, AA11, AD6, AD9, AD13, AH2, AH5, AH9, AH13, AA18, AD16, AD20, AD23, AH16, AH20, AH24, AH27 | 1.8-V power supply for I/Os on banks 2, 3, 4 |
| VCC_3P3V | B1, H1, K5, N1, N5, B28, H28, K24, N24, N28 A16, A20, A24, A27, E16, E20, E23, H18, A2, A5, A9, A13, E6, E9, E13, H11 | 3.3-V power supply for I/Os on banks 1, 6, 7, 8 |
| VCCA | Y8, J21, J8, Y21 | 2.5-V power supply for the internal PLL analog supply |
| VCCD_PLL | Y9, J20, J9, Y20 | 1.2-V power supply for the internal PLL digital supply |
| VREF_B2 | T7, T8, AB4 | DDR2 VREF 0.9 V. The SDRAM specification provides guidelines on how these references should be connected. It is not just any 0.9-V source on the board. |
| VREF_B3 | AB13, AB11, Y10 | DDR2 VREF 0.9 V. The SDRAM specification provides guidelines on how these references should be connected. It is not just any 0.9-V source on the board. |
| VREF_B4 | AB20, AC18, AA15 | DDR2 VREF 0.9 V. The SDRAM specification provides guidelines on how these references should be connected. It is not just any 0.9-V source on the board. |
| DGND | K10, K12, K14, K16, K18, K20, L9, L11, L13, L15, L17, L19, M10, M12, M14, M16, M18, M20, N9, N11, N13, N15, N17, N19, P10, P12, P14, P16, P18, P20, R9, R11, R13, R15, R17, R19, T10, T12, T14, T16, T18, T20, U9, U11, U13, U15, U17, U19, V10, V12, V14, V16, V18, V20, W9, W11, W13, W15, W17, W19, AA2, AA27, AC6, AC9, AC13, AC16, AC20, AC23, AF1, AF28, AG2, AG5, AG9, AG13, AG16, AG20, AG24, AG27, B2, B5, B9, B13, B16, B20, B24, B27, C1, C28, F6, F9, F13, F16, F20, F23, H2, H27, J11, J18, K6, K23, N2, N6, N23, N27, T2, T6, T23, T27, W6, W23, Y11, Y18 | Common ground |
| DGND2 | H9, H20, AA9, AA20 | Analog ground return for the PLL (This should not be connected to the common ground GND.) |
| NC | C3, F7, G7, G8, G10, G11, G19, G20, G21, G22, G23, G24, H8, H10, H12, H14, H15, H16, H17, H19, H21, H22, J5, J6, J7, J10, J12, J13, J14, J15, J16, J17, J19, J23, J24, K7, K8, K21, K22, L6, L7, L8, L21, L22, M7, M8, M23, N8, P21, R7, R21, R22, R23, U21, U22, V5, V6, V7, V8, V21, V22, W4, W7, W8, W21, W22, Y5, Y6, Y7, Y12, Y13, Y14, Y15, Y16, Y17, Y22, AA5, AA6, AA7, AA12, AA13, AA14, AA19, AA21, AA23, AB10, AB12, AB14, AB15, AB18, AB19, AB21, AB22, AC10, AC12, AC14, AC19, AC22, AD14, AD19, AD22, AE26 | No-connect pins |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC12}$ | Supply voltage (2) | –0.5 | 1.8 | V |
| $V_{CCIO18}$ | | –0.5 | 3.9 | |
| $V_{CCA25_DPLL}$ | | –0.5 | 3.75 | |
| $V_{CCD_PLL1-4}$ | | –0.5 | 1.8 | |
| $V_I$ | Input voltage(3) (1.8 V, 2.5 V, 3.3 V) | –0.5 | 3.95 | V |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, and at the device, not at the power supply.
(3) Applies to external input and bidirectional buffers.

## 6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –2000 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC12}$ | 1.2-V supply voltage, core logic | 1.15 | 1.2 | 1.25 | V |
| $V_{CC18}$ | 1.8-V supply voltage, HSTL output buffers | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA25_DPLL}$ | 2.5-V analog voltage for PLL regulator | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD_PLL1-4}$ | 1.2-V supply voltage, for PLL | 1.15 | 1.2 | 1.25 | V |
| $V_{CC33}$ | 3.3-V supply voltage | 3.135 | 3.3 | 3.465 | V |
| $V_{REF_B2-4}$ | 0.9-V reference voltage, for DDR2 SDRAM | 0.833 | 0.9 | 0.969 | V |
| $V_I$ | Input voltage | –0.5 | | 3.6 | V |
| $V_O$ | Output voltage | 0 | | $V_{CCIO}$ | V |
| $t_{Ramp}$ | Power supply ramp time | 50 µs | | 3 ms | — |
| $T_J$ | Operating junction temperature(1) | –20 | | 85 | °C |

(1) Heat sink not required for 0°C to 55°C, but for 55°C to 85°C, TI recommends a low-profile (15-mm) heat sink.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | | DLPC200 BGA 780 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | Natural convection | 16.9 | °C/W |
| | | 100 CFM | 13.5 | |
| | | 200 CFM | 11.8 | |
| | | 400 CFM | 10.5 | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | 3.3 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | 5.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 I/O Electrical Characteristics

All inputs and outputs are LVCMOS

| I/O TYPE (1) | | TEST CONDITIONS | $V_{IL}$(V) | | $V_{IH}$(V) | | $V_{OH}$(V) | $V_{OL}$(V) | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $I_1$ | Input LVCMOS | $V_{CCIO}$ = 1.8 V | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 2.25 | | | V |
| $I_2$ | Input LVCMOS | $V_{CCIO}$ = 2.5 V | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.3 | | | V |
| $I_3$ | Input LVCMOS | $V_{CCIO}$ = 3.3 V | –0.3 | 0.8 | 1.7 | 3.6 | | | V |
| $I_4$ | Input LVTTL | $V_{CCIO}$ = 3.3 V | –0.3 | 0.8 | 1.7 | 3.6 | | | V |
| $O_1$ | Output LVCMOS | $V_{CCIO}$ = 1.8 V | | | | | $V_{CCIO}$ – 0.45 | 0.45 | V |
| $O_2$ | Output LVTTL | $V_{CCIO}$ = 3.3 V | | | | | 2.4 | 0.45 | V |
| $O_3$ | Output LVCMOS | $V_{CCIO}$ = 3.3 V | | | | | $V_{CCIO}$ – 0.2 | 0.2 | V |
| $O_4$ | Output LVDS | $V_{CCIO}$ = 3.3 V | | | | | $V_{CCIO}$ – 0.3 | 0.3 | V |
| $O_5$ | Output SSTL-18 Class I | $V_{CCIO}$ = 1.8 V | | | | | 1.484 | 0.398 | V |
| $B_1$ | Bidirectional SSTL-18 Class I | $V_{CCIO}$ = 1.8 V | | 0.844 | 1.094 | | 1.484 | 0.398 | V |
| $B_2$ | Bidirectional LVCMOS | $V_{CCIO}$ = 3.3 V | –0.3 | 0.8 | 1.7 | 3.6 | $V_{CCIO}$ – 0.2 | 0.2 | V |

(1) Cross reference to I/O assignments

## 6.6 Video Input Pixel Interface Timing Requirements

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{pclock}$ | Clock frequency, PORTx_CLK | | | 80 | MHz |
| $t_{p_wh}$ | Pulse duration, high | 45% to 55% reference points (signal) | 5.6 | | ns |
| $t_{p_wl}$ | Pulse duration, low | 45% to 55% reference points (signal) | 5.6 | | ns |
| $t_{p_su}$ | Setup time, PORTx_D(23–0) valid before PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_h}$ | Hold time, PORTx_D(23–0) valid after PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_su}$ | Setup time, PORTx_VSYNC valid before PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_h}$ | Hold time, PORTx_VSYNC valid after PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_su}$ | Setup time, PORTx_HSYNC valid before PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_h}$ | Hold time, PORTx_HSYNC valid after PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_su}$ | Setup time, PORTx_IVALID valid before PORTx_CLK | See (1) | 1.5 | | ns |
| $t_{p_h}$ | Hold time, PORTx_IVALID valid after PORTx_CLK | See (1) | 1.5 | | ns |

(1) PCLK may be inverted from that shown in Figure 1. In that case, the same specifications in the table are valid except now referenced to the falling edge of the clock. If the falling edge of PCLK is used, a USB or SPI command must be sent to tell the DLPC200 to use the falling edge of PCLK.

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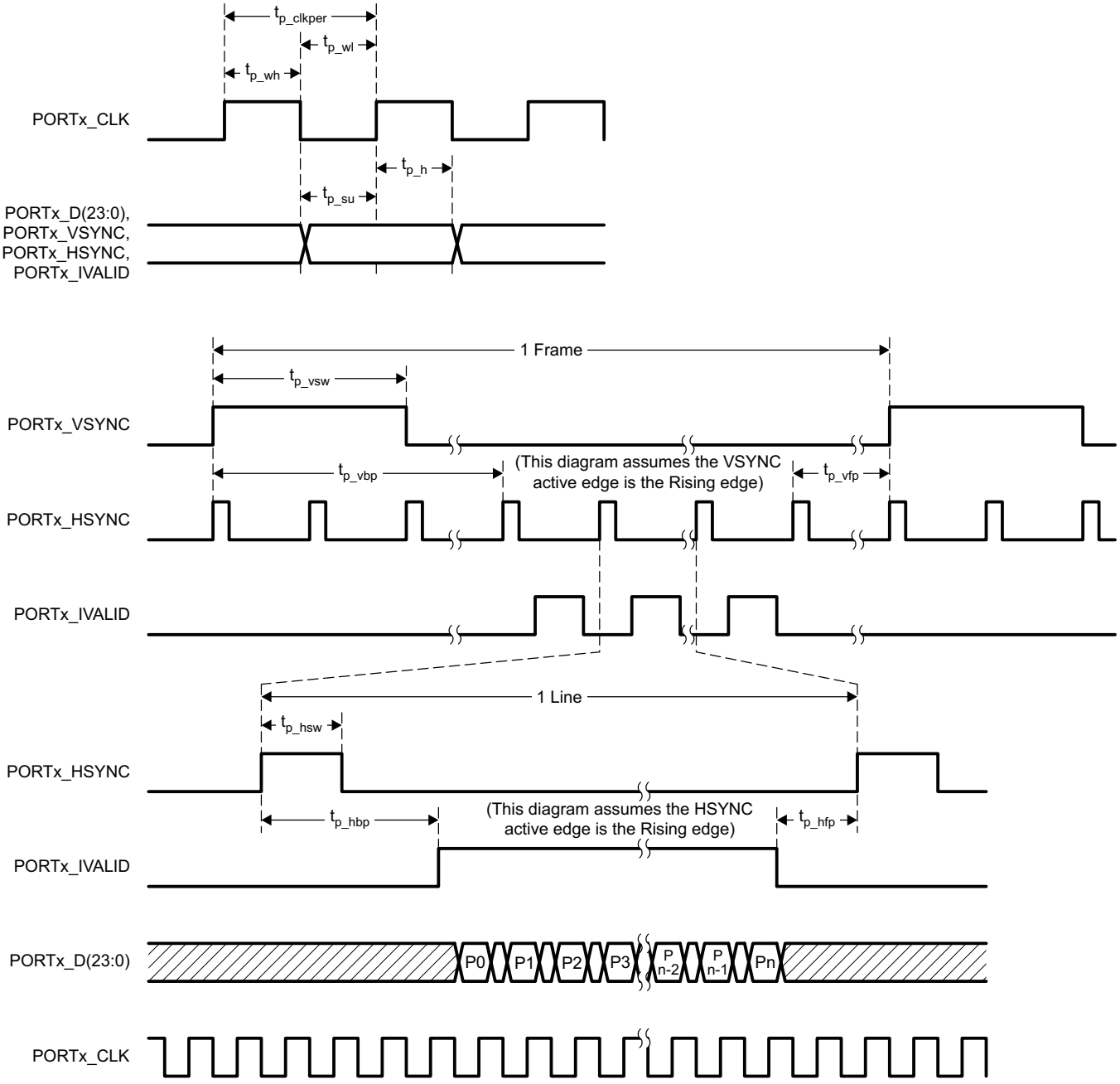


**Figure 1. Input Port Interface**

See *Pin Configuration and Functions* for the proper connection schema if a video input port will not be used.


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## 6.7 I²C Interface Timing Requirements

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{scl}$ | I²C clock frequency | | 0 | 400 | kHz |
| $t_{sch}$ | I²C clock high time | | 1 | | ms |
| $t_{scl}$ | I²C clock low time | | 1 | | ms |
| $t_{sp}$ | I²C spike time | | | 20 | ns |
| $t_{sds}$ | I²C serial-data setup time | | 100 | | ns |
| $t_{sdh}$ | I²C serial-data hold time | | 100 | | ns |
| $t_{icr}$ | I²C input rise time | | 100 | | ns |
| $t_{ocf}$ | I²C output fall time | 50 pF | 30 | 200 | ns |
| $t_{buf}$ | I²C bus free time between stop and start conditions | | 1.3 | | ms |
| $t_{sts}$ | I²C start or repeat start condition setup | | 1 | | ms |
| $t_{sth}$ | I²C start or repeat start condition hold | | 1 | | ms |
| $t_{sph}$ | I²C stop condition setup | | 1 | | ms |
| $t_{vd}$ | Valid-data time | SCL low to SDA output valid | | 1 | ms |
| | Valid-data time of ACK condition | ACK signal from SCL low to SDA (out) low | | 1 | ms |
| $t_{sch}$ | I²C bus capacitive load | | 0 | 100 | pF |

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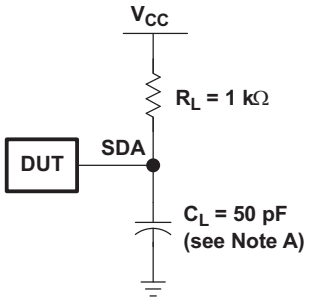
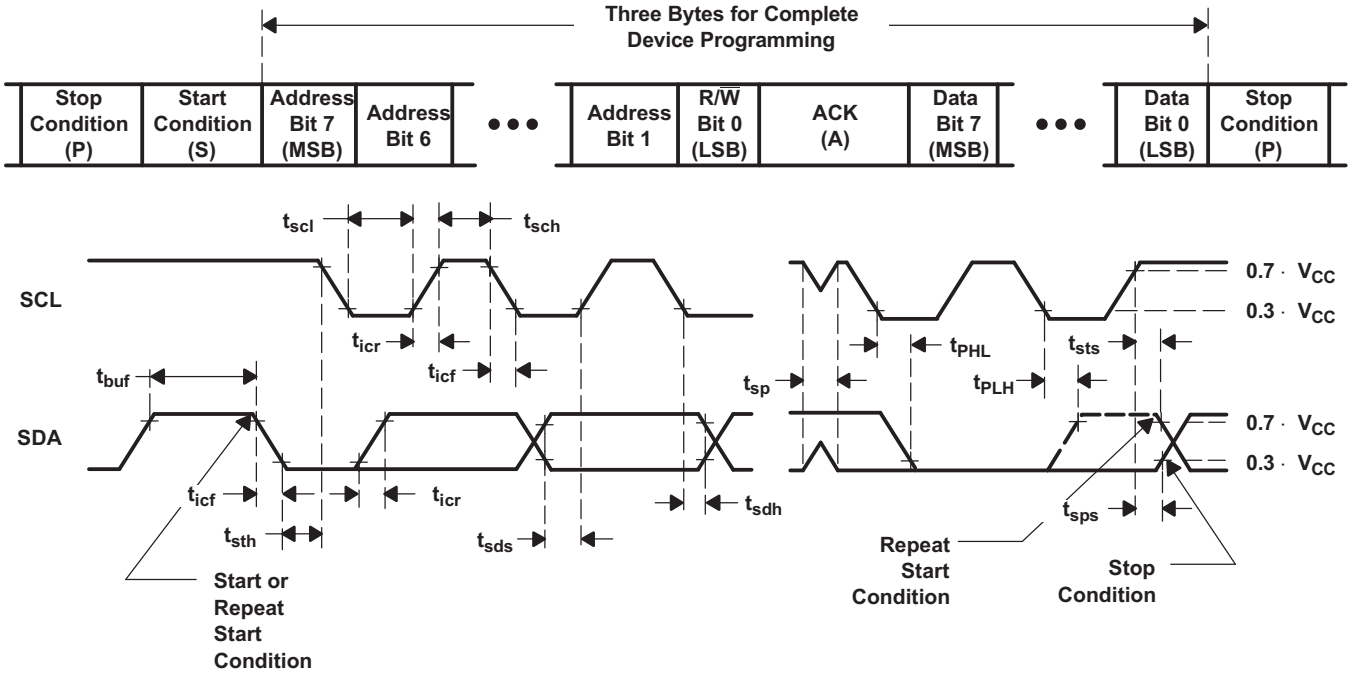



SDA LOAD CONFIGURATION




VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|---|---|
| 1 | $I^2C$ address |
| 2, 3 | P-port data |

**Figure 2. $I^2C$ Interface Load Circuit and Voltage Waveforms**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## 6.8 USB Read Interface Timing Requirements

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CL}$ | 1 / CLKOUT frequency | | 20.8 | | ns |
| $t_{AV}$ | Delay from clock to valid address | | | 10.7 | ns |
| $t_{STBL}$ | Clock to USB_RDY0 LOW | | | 11 | ns |
| $t_{STBH}$ | Clock to USB_RDY0 HIGH | | | 11 | ns |
| $t_{SCSL}$ | Clock to USB_PA02 LOW | | | 13 | ns |
| $t_{DSU}$ | Data setup to clock | 9.6 | | | ns |
| $t_{DH}$ | Data hold time | 0 | | | ns |
| $t_{ACC1}$ | Valid USB_PA04 to valid USB_FDC | 43 | | | ns |

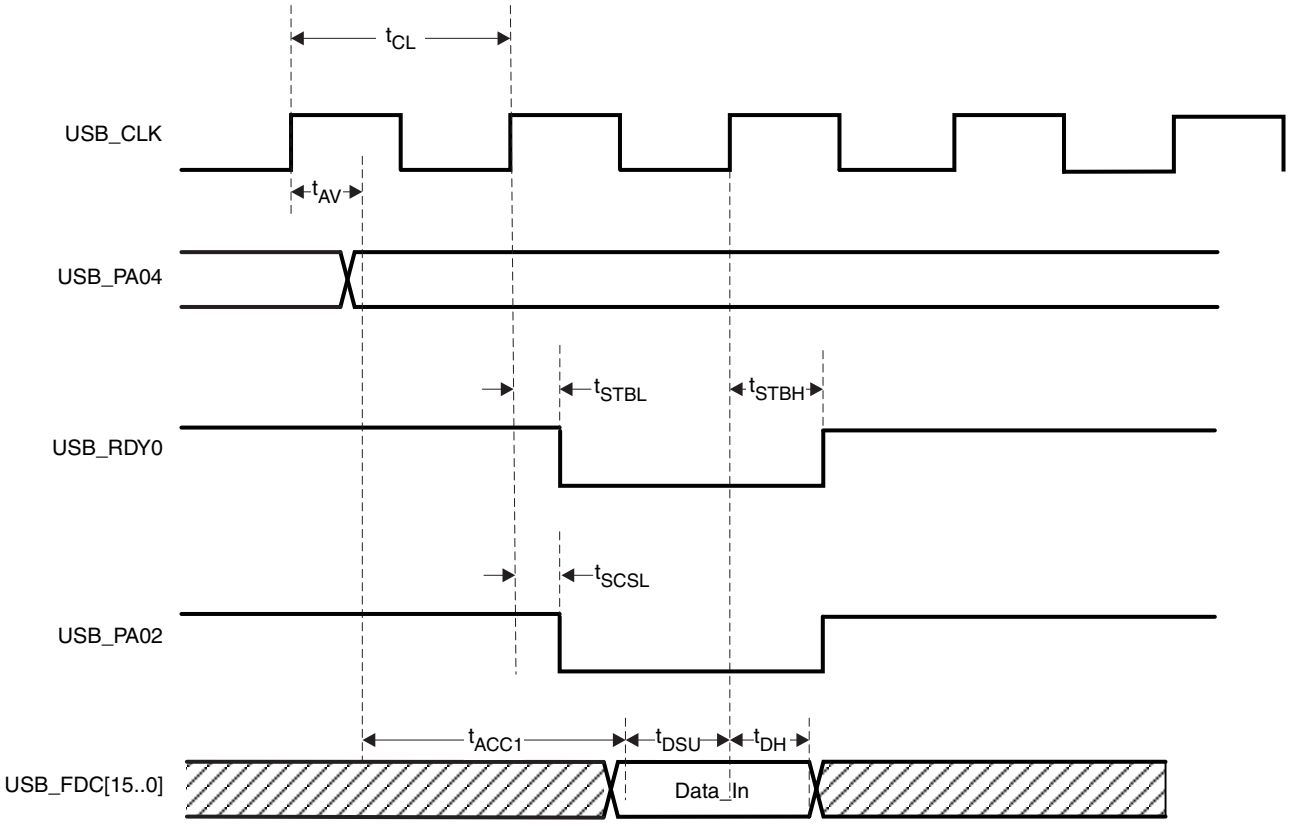


**Figure 3. USB Read Timing**

## 6.9 USB Write Interface Timing Requirements

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AV}$ | Delay from clock to valid address | 0 | 10.7 | ns |
| $t_{STBL}$ | Clock to USB_RDY1 pulse LOW | 0 | 11.2 | ns |
| $t_{STBH}$ | Clock to USB_RDY1 pulse HIGH | 0 | 11.2 | ns |
| $t_{SCSL}$ | Clock to USB_PA02 pulse LOW | | 13 | ns |
| $t_{ON1}$ | Clock to data turn on | 0 | 13.1 | ns |
| $t_{OFF1}$ | Clock to data hold time | 0 | 13.1 | ns |

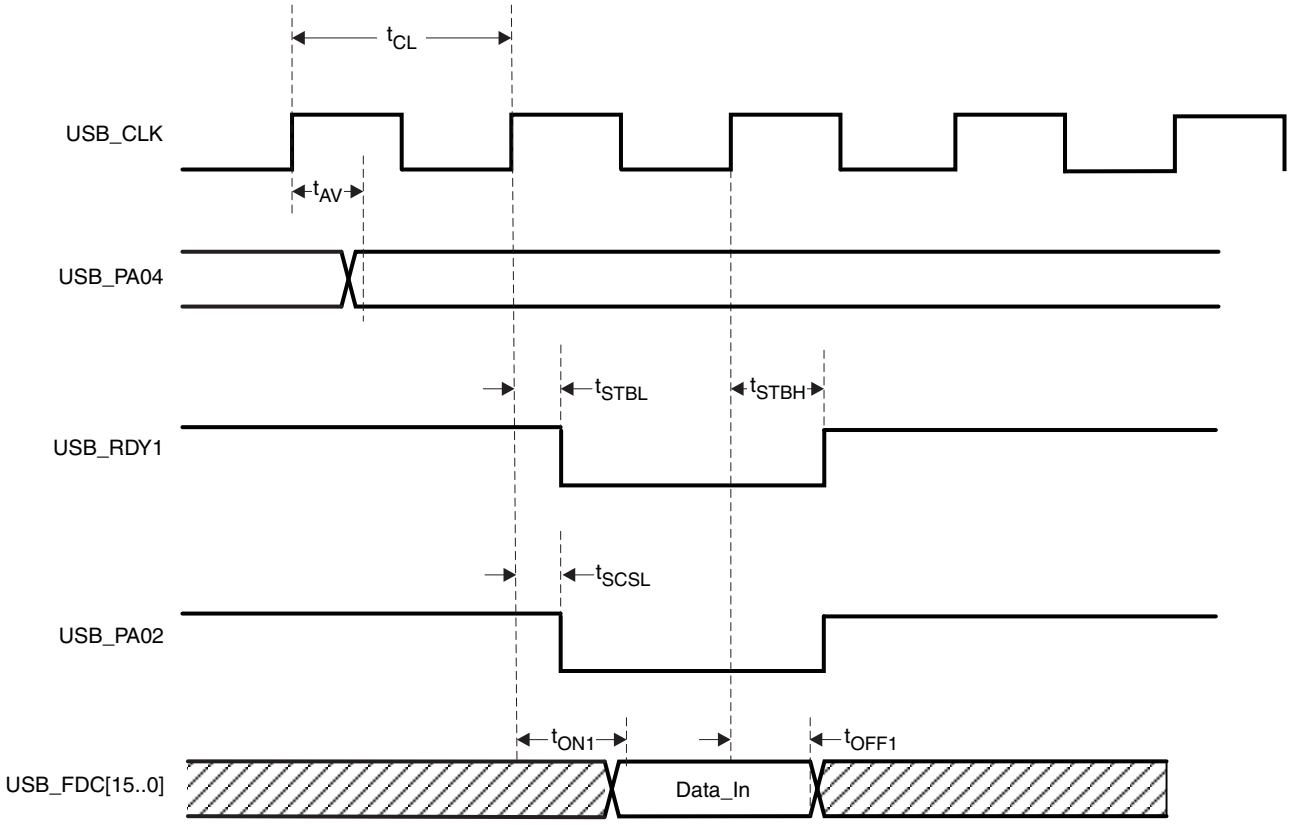


**Figure 4. USB Write Timing**

See *Pin Configuration and Functions* for the proper connection schema if the USB interface will not be used.


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## 6.10 SPI Slave Interface Timing Requirements

| | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, SLAVE_SPI_CLK | | 5 | MHz |
| $t_{p_clkper}$ | Clock period, SLAVE_SPI_CLK | 200 | | ns |
| $t_{p_wh}$ | Pulse duration high, SLAVE_SPI_CLK | 10 | | ns |
| $t_{p_wl}$ | Pulse duration low, SLAVE_SPI_CLK | 10 | | ns |
| $t_{c_su}$ | Setup time, $\overline{\text{SLAVE_SPI_CS}}$ | 6 | | ns |
| $t_{c_h}$ | Hold time, $\overline{\text{SLAVE_SPI_CS}}$ | 3 | | ns |
| $t_{i_su}$ | Setup time, SLAVE_SPI_MOSI | 10 | | ns |
| $t_{i_h}$ | Hold time, SLAVE_SPI_MOSI | 10 | | ns |
| $t_{o_su}$ | Setup time, SLAVE_SPI_MISO | 10 | | ns |
| $t_{o_h}$ | Hold time, SLAVE_SPI_MISO | 10 | | ns |
| $t_{a_su}$ | Setup time, SLAVE_SPI_ACK | 7 | | ns |
| $t_{a_h}$ | Hold time, SLAVE_SPI_ACK | 7 | | ns |

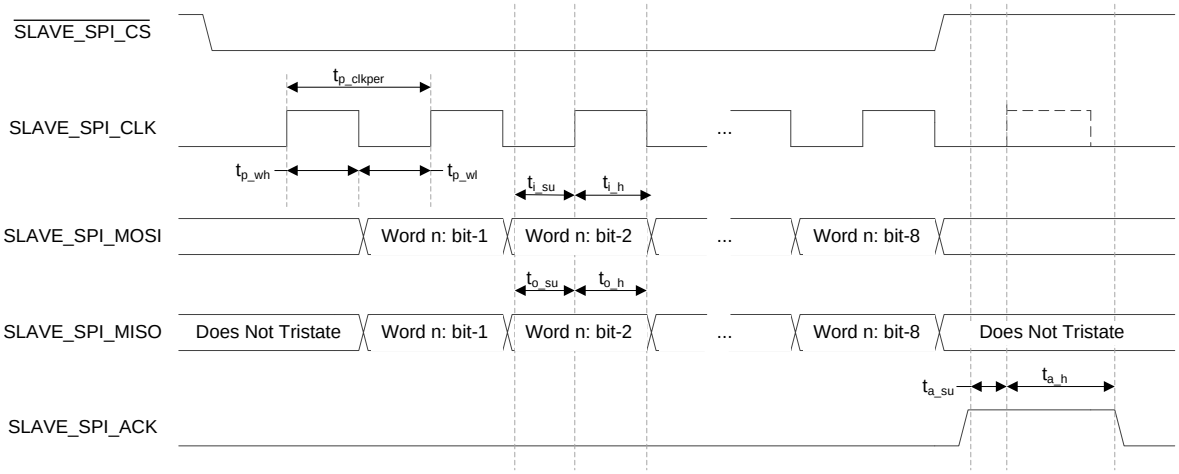


**Figure 5. SPI Timing**

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## 6.11 Parallel Flash Interface Timing Requirements

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AVAV}$ | Read cycle time | | 110 | ns |
| $t_{AVQV}$ | Address to output valid | | 110 | ns |
| $t_{ELQV}$ | $\overline{CE}$ low to output valid | | 110 | ns |
| $t_{GLQV}$ | $\overline{OE}$ low to output valid | | 25 | ns |
| $t_{PHQV}$ | $\overline{RST}$ high to output valid | | 150 | ns |
| $t_{GLTV}$ | $\overline{OE}$ low to WAIT valid | | 17 | ns |
| $t_{PHWL}$ | $\overline{RST}$ high recovery to $\overline{WE}$ low | 150 | | ns |
| $t_{ELWL}$ | $\overline{CE}$ setup to $\overline{WE}$ low | 0 | | ns |
| $t_{WLWH}$ | $\overline{WE}$ write pulse width low | 50 | | ns |
| $t_{DVWH}$ | Data setup to $\overline{WE}$ high | 50 | | ns |
| $t_{AVWH}$ | Address setup to $\overline{WE}$ high | 50 | | ns |
| $t_{WHEH}$ | $\overline{CE}$ hold from $\overline{WE}$ high | 0 | | ns |
| $t_{PWDHX}$ | Data hold from $\overline{WE}$ high | 0 | | ns |
| $t_{WHAX}$ | Address hold from $\overline{WE}$ high | 0 | | ns |

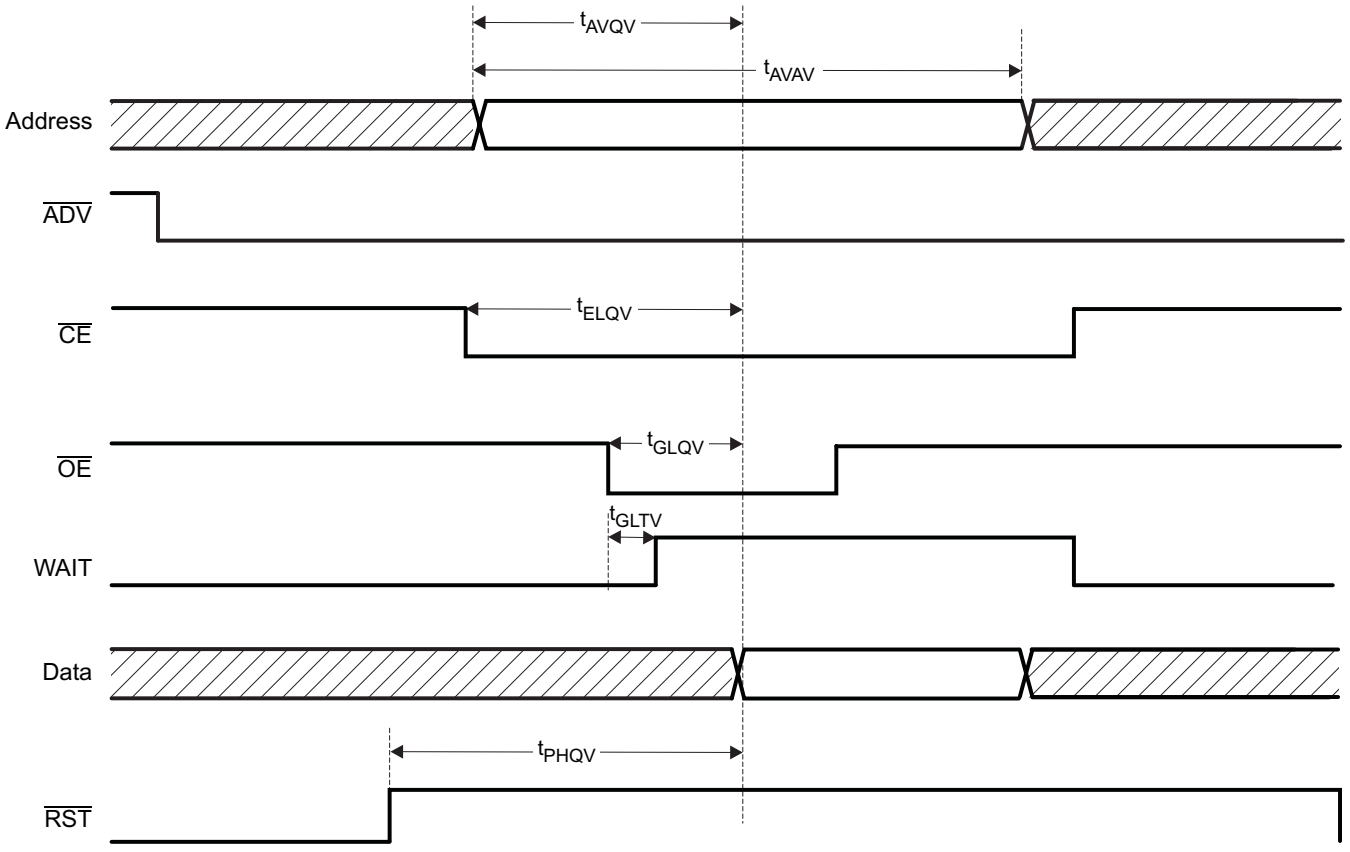


**Figure 6. Parallel Flash Read Timing**


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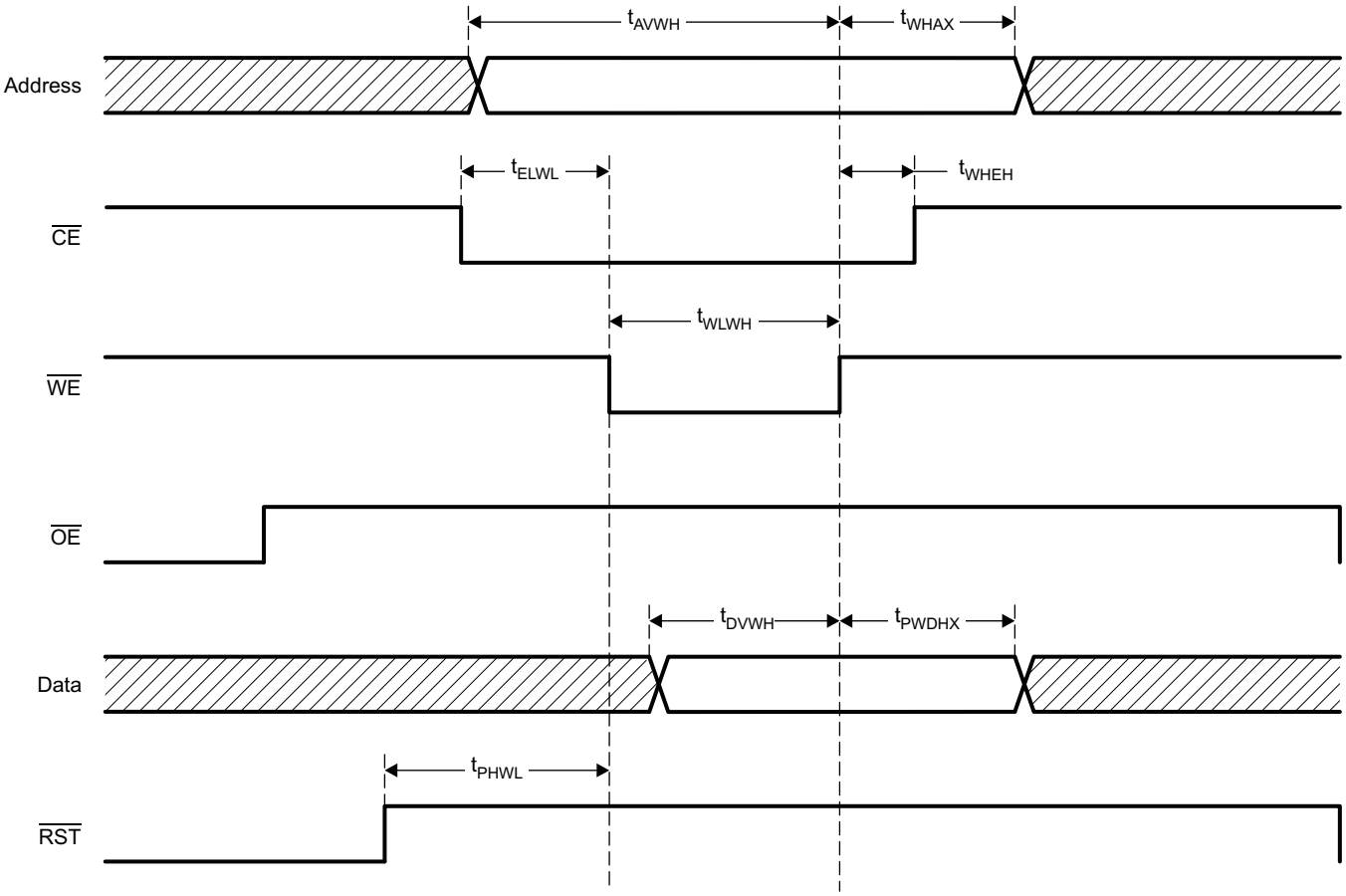


**Figure 7. Parallel Flash Write Timing**

## 6.12 Serial Flash Interface Timing Requirements

The DLPC200 controller flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal).

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, CFG_CLK | dc | 33 | MHz |
| $t_{p_clkper}$ | Clock period, CFG_CLK | | 30.03 | ns |
| $t_{p_wh}$ | Pulse duration low, CFG_CLK | 6 | | ns |
| $t_{p_wl}$ | Pulse duration high, CFG_CLK | 6 | | ns |
| $t_{p_su}$ | Setup time – CFG_ASDI/CFG_ASDO valid before CFG_CLK rising edge | 2 | | ns |
| $t_{p_h}$ | Hold time – CFG_ASDI/CFG_ASDO valid after CFG_CLK rising edge | 5 | | ns |

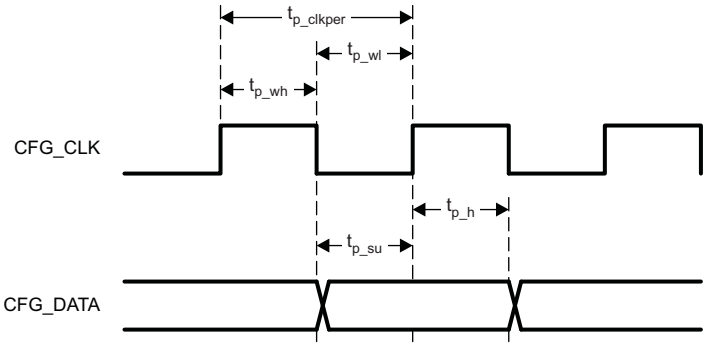


**Figure 8. Flash Memory Interface Timing**


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## 6.13 Static RAM Interface Timing Requirements

The DLPC200 controller static RAM (SRAM) interface consists of a high performance CMOS SRAM organized as 128K words by 16 bits (2 Mb).

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{RC}$ | Read cycle time | 10 | | ns |
| $t_{AA}$ | Address to data valid | | 10 | ns |
| $t_{OHA}$ | Data hold from address change | 3 | | ns |
| $t_{WC}$ | Write cycle time | 10 | | ns |
| $t_{SCE}$ | CE low to write end | 7 | | ns |
| $t_{AW}$ | Address setup to write end | 7 | | ns |
| $t_{HA}$ | Address hold from write end | 0 | | ns |
| $t_{SA}$ | Address setup to write start | 0 | | ns |
| $t_{PWE}$ | WE pulse duration | 7 | | ns |
| $t_{SD}$ | Data setup to write end | 5 | | ns |
| $t_{HD}$ | Data hold from write end | 0 | | ns |

## 6.14 DMD Interface Timing Requirements

The DLPC200-DMD interface consists of a 200 MHz (nominal) DDR output-only interface with LVDS signaling.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, DCLK_A and DCLK_B | | 200 | | MHz |
| $t_{p_clkper}$ | Clock period, DCLK_A and DCLK_B | | 5 | | ns |
| $t_{p_wh}$ | Pulse duration low, DCLK_A and DCLK_B | | 1.25 | | ns |
| $t_{p_wl}$ | Pulse duration high, DCLK_A and DCLK_B | | 1.25 | | ns |
| $t_{skew}$ | Channel B relative to channel A | –1.25 | | 1.25 | ns |
| $t_{p_su}$ | Output setup time – D_A(0:15) and D_B(0:15) relative to both rising and falling edges of DCLK_A and DCLK_B, respectively | 0.35 | | | ns |
| $t_{p_h}$ | Output hold time – D_A(0:15) and D_B(0:15) relative to both rising and falling edges of DCLK_A and DCLK_B, respectively | 0.35 | | | ns |

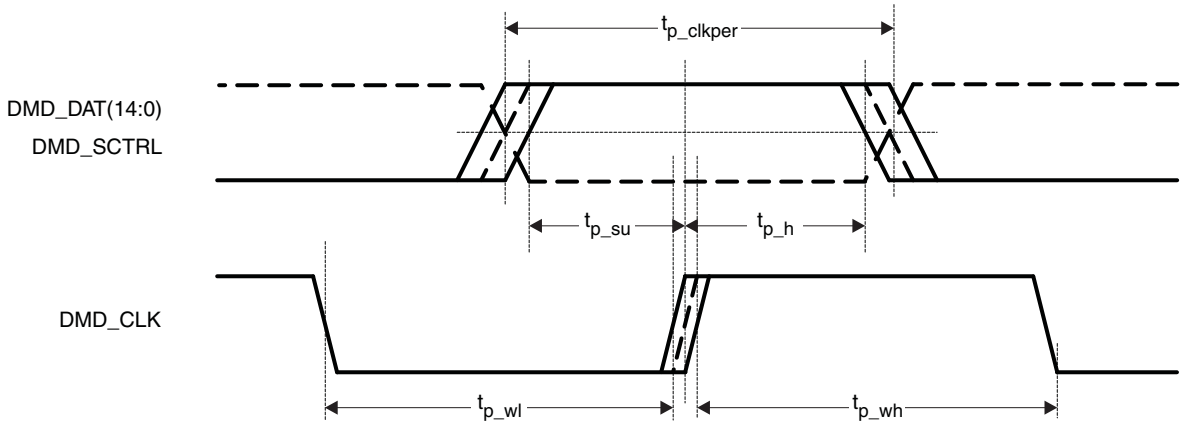


**Figure 9. DMD I/F Timing**

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## 6.15 DLPA200 Interface Timing Requirements

The DLPC200 interface to the DLPA200 consists of a 125 kHz (nominal) serial communications port (SCP).

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency | | 125 | 125 | kHz |
| $t_{p_clkper}$ | Clock period | | | 8 | us |
| $t_{p_wh}$ | Pulse duration low | | | 4 | us |
| $t_{p_wl}$ | Pulse duration high | | | 4 | us |
| $t_{p_su}$ | SCPDI setup time | 7.3 | | | ns |
| $t_{p_h}$ | SCPDI hold time | 5.7 | | | ns |

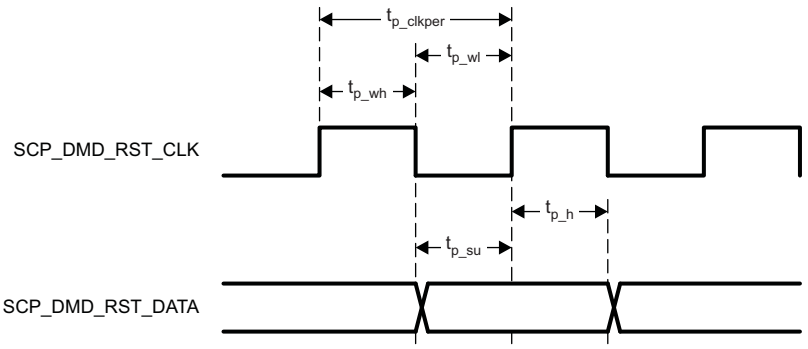


**Figure 10. DLPA200 I/F Timing**


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## 6.16 DDR2 SDR Memory Interface Timing Requirements

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{CYCLE}$ | Cycle time reference | 5 | 8 | ns |
| $t_{CH}$ | CK high pulse duration(1) | 2.4 | 4.16 | ns |
| $t_{CL}$ | CK low pulse duration(1) | 2.4 | 4.16 | ns |
| $t_{CMS}$ | Command setup | 200 | | ps |
| $t_{CMH}$ | Command hold | 275 | | ps |
| $t_{AS}$ | Address setup | 400 | | ps |
| $t_{AH}$ | Address hold | 400 | | ps |
| $t_{DS}$ | Write data setup | 1.5 | | ns |
| $t_{DH}$ | Write data hold | 1.5 | | ns |
| $t_{AC}$ | Read data access time | –450 | 450 | ps |
| $t_{OH}$ | Read data hold time | | 340 | ps |
| $t_{LZ}$ | Read data low-impedance time | –900 | 450 | ps |
| $t_{HZ}$ | Read data high-impedance time | | 450 | ps |

(1) Output setup/hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold need be considered in system timing analysis.

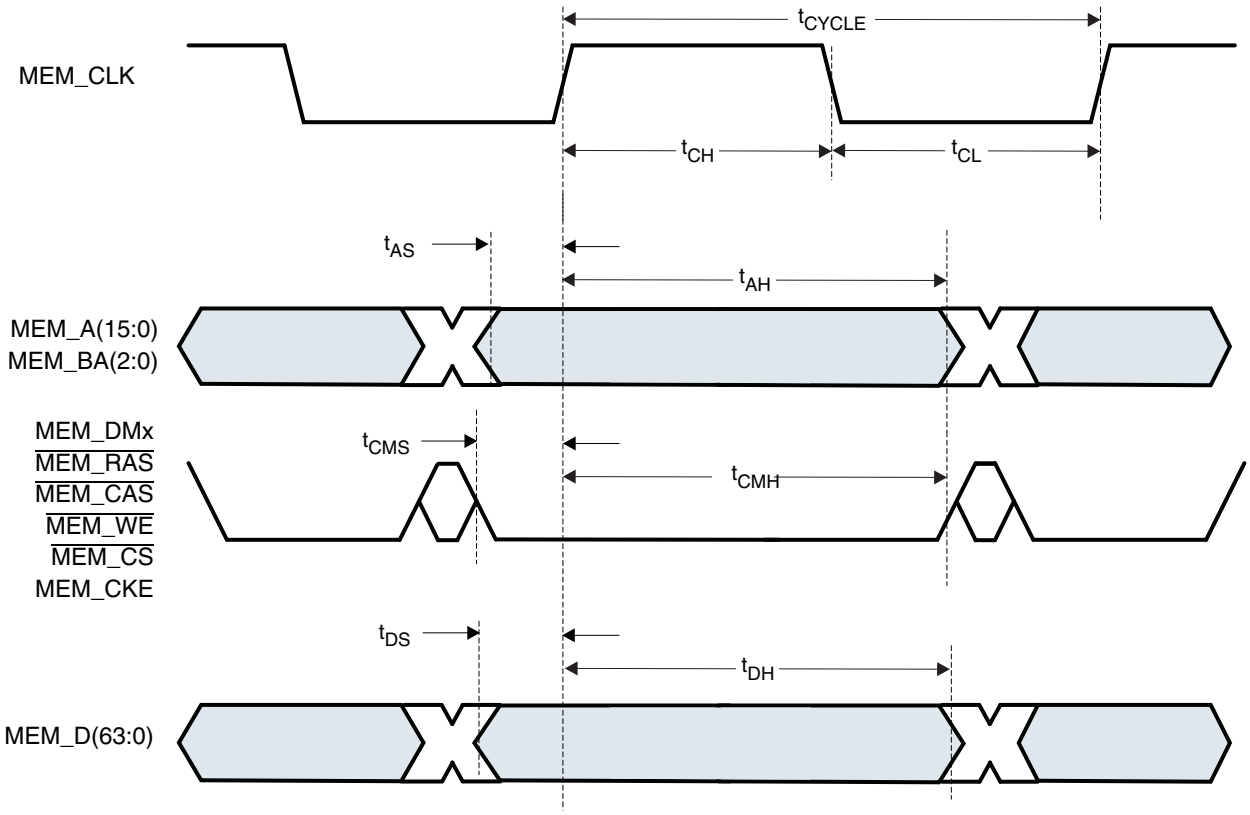


**Figure 11. SDR Memory I/F Write Timing**

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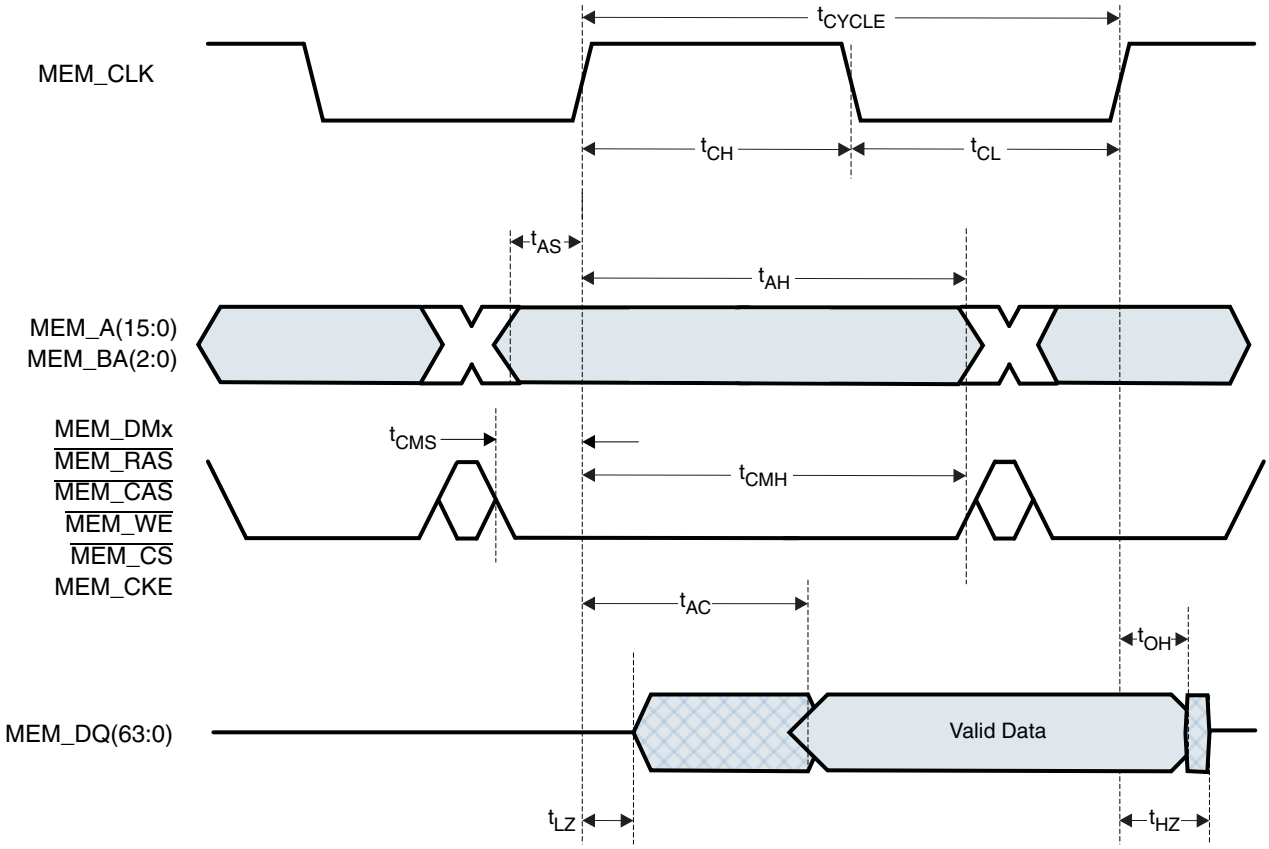


**Figure 12. SDR Memory I/F Read Timing**

## 6.17 Video Input Pixel Interface – Image Sync and Blanking Requirements

Figure 13 shows how pixels should be mapped to the input data bus for both port 1 and port 2.

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{p_vsw}$ | Vertical sync duration | 1 | | clocks |
| $t_{p_vbp}$ | Vertical back porch | 14 | | lines |
| $t_{p_vfp}$ | Vertical front porch | 2 | | lines |
| $t_{p_hsw}$ | Horizontal sync duration | 1 | | clocks |
| $t_{p_hbp}$ | Horizontal back porch | 64 | | clocks |
| $t_{p_hfp}$ | Horizontal front porch | 75 | | clocks |

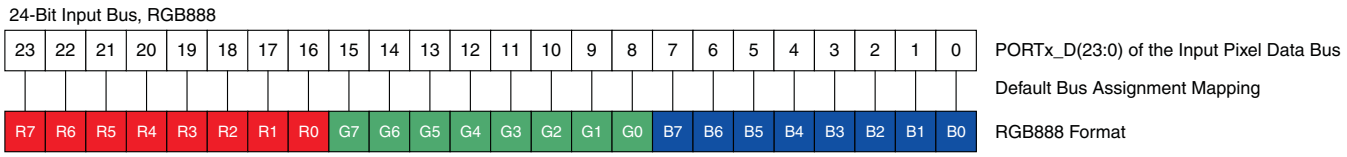


**Figure 13. Pixel Mapping**


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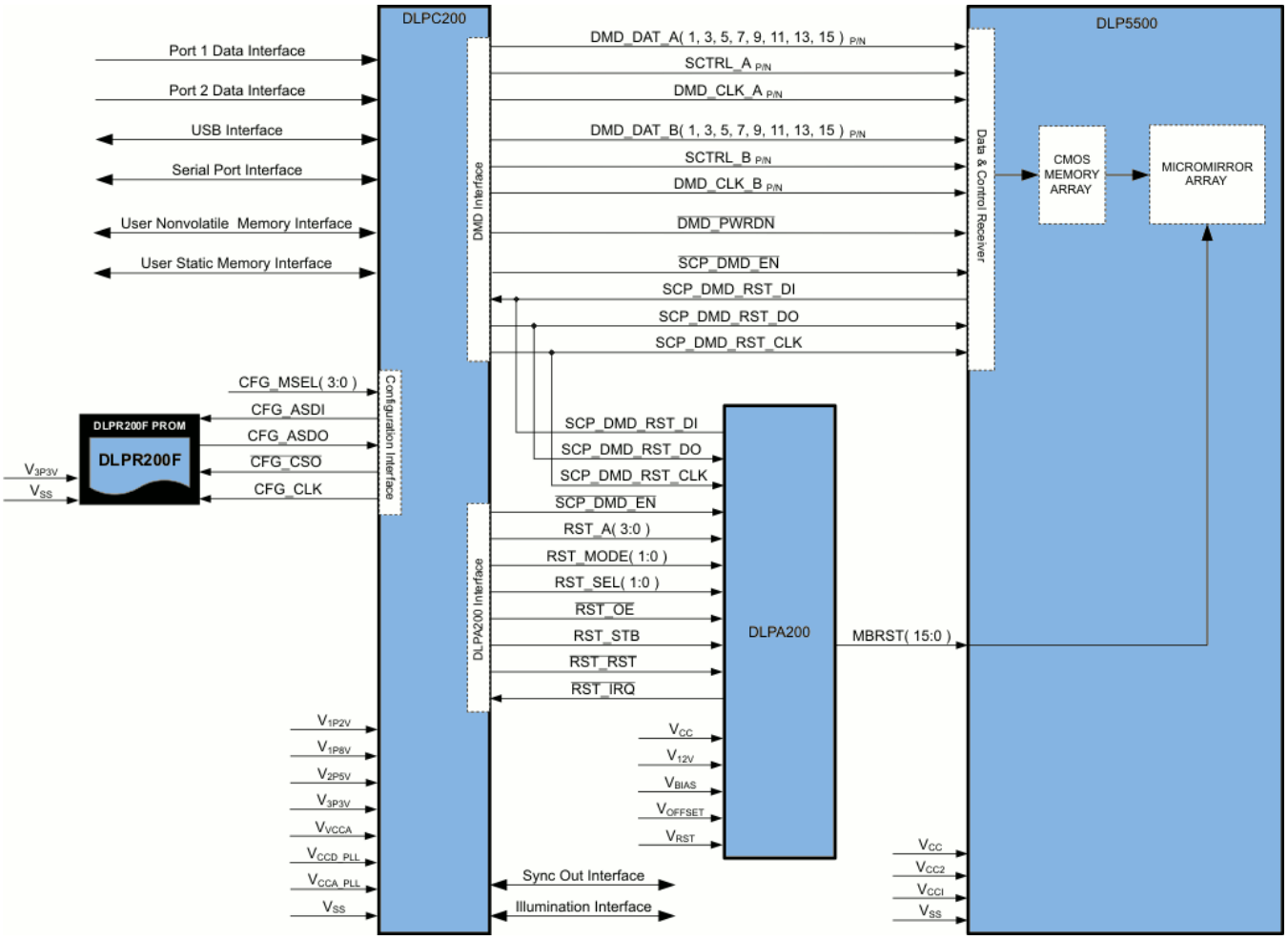
# 7 Detailed Description

## 7.1 Overview

In DLP-based solutions, image data is 100% digital from the DLPC200 inputs to the image on the DMD. Patterns stay in digital form and are not converted into an analog signal. The DLPC200 controller processes the digital input and converts the data into a format needed by the DMD. The DMD steers light by using binary pulse-duration modulation (PWM) for each micromirror. For further details, refer to DMD data sheet (DLPS013 for the DLP5500 DMD).

The DLPC200 only accepts 1024 × 768 (XGA) formatted data for both video and structured light modes. The functionality of this controller is well-suited for techniques such as structured light, additive manufacturing, or digital exposure.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Frame Rates

The digital input interface levels for image data are nominally 1.8 or 3.3 V. Port 1 input is 3.3 V and port 2 input is 1.8 V.

DLPR200F firmware is provided by TI to support the operation of video and structured light mode.

## Feature Description (continued)

**Table 1. Frame Rates**

| MODE | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Structured light | 1 bit per pixel | 6 | 5000 | Hz |
| | 8 bits per pixel | 6 | 700 | |
| Video | | 6 | 60 | Hz |

## 7.4 Device Functional Modes

The DLPC200 has two basic functional mode types: video and structured light.

### 7.4.1 Video Modes

The controller accepts RGB-8-8-8 input to port 1 or port 2 through a selectable MUX. XGA video information is displayed on the DMD at 6 to 60 fps.

An internal pattern generator can generate RGB-8-8-8 video patterns into an internal selectable MUX for verification and debug purposes.

### 7.4.2 Structured Light Modes

The DLPC200 provides two structured light modes: static image buffer and real-time structured light.

#### *7.4.2.1 Static Image Buffer Mode*

Image data can be loaded into parallel flash memory to load to DDR2 memory at startup to be displayed, or can be loaded over USB or the SPI port directly to DDR2 memory to be displayed. Binary (1-bit) or grayscale (8-bit) patterns can be displayed. The memory will hold 960 binary patterns or 120 grayscale patterns.

#### *7.4.2.2 Real Time Structured Light Mode*

RGB-8-8-8 60 fps data can be input into port 1 or port 2 and reinterpreted as up to 24 binary (1-bit) patterns or three grayscale (8-bit) patterns. The specified number of patterns is displayed equally during the exposure time specified. Any unused RGB-8-8-8 data in the video frame must be filled with data, usually 0s.

For example, during one video frame (16.67 ms), 12 binary patterns of the 24 RGB bits are requested to be displayed during half of the video frame time (exposure time = 8.33 ms). Each of the eight red bits and the four most significant green bits are displayed as a binary pattern for 694 µs each. The remaining bits are ignored and the remaining 8.33 ms of the frame will be dark.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# 8 Application and Implementation

## 8.1 Application Information

The DLPC200 is used in conjunction with the DLPA200 driver to drive to the DLP5500 (0.55-inch XGA DMD). This combination can be used for a number of applications from 3D printers to microscopes.

The most common application is for 3D structured light measurement applications. In this application, patterns (binary, grayscale, or even full color) are projected onto the target and the distortion of the patterns are recorded by an imaging device to extract 3D (x, y, z) surface information.

## 8.2 Typical Application

A schematic is shown in Figure 14 for projecting RGB and IR structured light patterns onto a measurement target. Typically, an imaging device is triggered through one of the three syncs to record the data as each pattern is displayed.

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## Typical Application (continued)

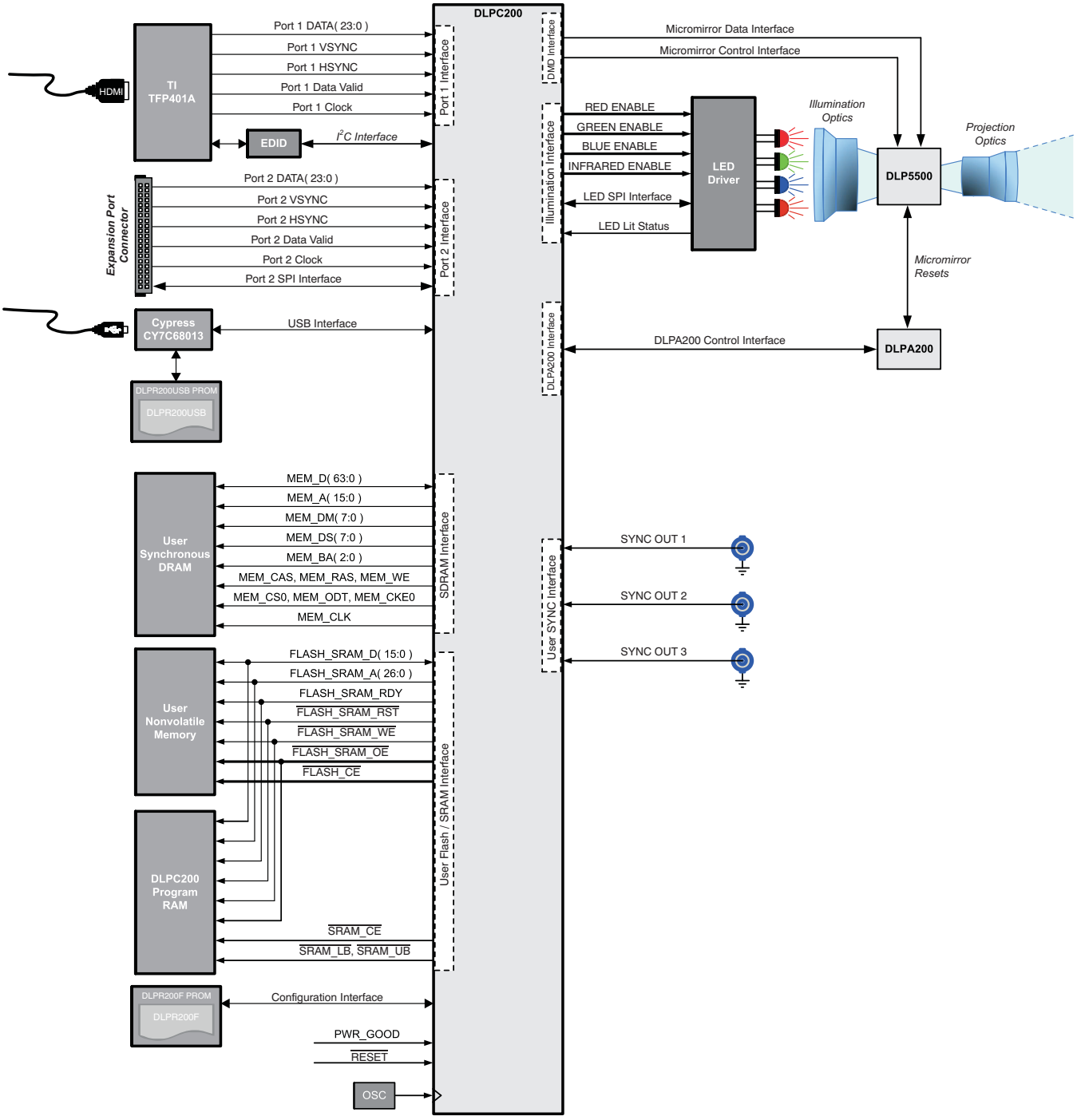


**Figure 14. Typical RGB + IR Structured Light Application**

### 8.2.1 Design Requirements

All applications using the DLP 0.55-inch XGA chipset require the DLPC200 controller, the DLPA200 driver, and the DLP5500 DMD for correct operation. The system also requires user supplied SRAM and a configuration PROM programmed with the DLPR200F program file and a 50-MHz oscillator is for operation.


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## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 DLPC200 System Interfaces*

The DLPC200 supports the following interfaces: extended display identification data (EDID), USB, SPI, parallel flash, serial flash, DDR2 SDRAM, and two RGB888 input ports, which are described in the following subsections.

##### 8.2.2.1.1 DLPC200 Master, $I^2C$ Interface for EDID Programming

The DLPC200 controller $I^2C$ interface is only used to program the HDMI EDID. Upon plugging in an HDMI source, the DMD resolution is compared to the HDMI output resolution programmed in the HDMI EDID PROM. If the two resolutions do not match, then the HDMI EDID is adjusted to match the DMD resolution.

The bidirectional $I^2C$ bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

$I^2C$ communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

On the $I^2C$ bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop). A Stop condition (a low-to-high transition on the SDA input/output while the SCL input is high) is sent by the master.

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. Setup and hold times must be met to ensure proper operation.

**Table 2. Recommended EDID PROM Devices**

| PART NUMBER | MANUFACTURER |
|---|---|
| 24LC02B | Microchip Technology |

##### 8.2.2.1.2 USB Interface

The USB interface consists of a single-chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor running at 48 MHz (nominal) that supports USB 2.0.

##### 8.2.2.1.3 Bus Protocol

USB is a polled bus. The host controller (typically at PC) initiates all data transfers. Each transaction begins when the PC sends a packet. Communications are always through the bulk transfer mode, and 512 bytes of data are always written/read at a time. The packet consists of the following:

- Header (6 bytes)
- Data (505 bytes)
- Checksum (1 byte)

The USB device that is addressed selects itself by decoding the appropriate address fields. The direction of data transfer, either read or write, is specified in the packet header. The source of the transaction then sends a data packet or indicates it has no data to transfer. At the end of either a single packet transfer or a multi-packet transfer, the destination responds with a handshake packet indicating whether the transfer was successful.

The packet header consists of:

- CMD1 – Indicates if packet is write/write response or read/read response
- CMD2 – Groups major functions together
- CMD3 – Provides more information about packet grouping defined in CMD2

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- CMD4 – Used to indicate location of data in a multi-packet transfer
- Len_MSB:Len_LSB – Valid number of bytes of data transferred in packet data

| Header | | | | | | Data | Checksum |
|---|---|---|---|---|---|---|---|
| CMD1<br>1 byte | CMD2<br>1 byte | CMD3<br>1 byte | CMD4<br>1 byte | Len_LSB<br>1 byte | Len_MSB<br>1 byte | 0-505 bytes | 1 byte |

**Figure 15. USB Data Packet**

As discussed previously, the header describes whether the data transaction is to be a read or write and designates the data endpoint. The data portion of the packet carries the payload and is followed by a handshaking mechanism, checksum, that reports if the data was received successfully, or if the endpoint is stalled or not available to accept data.

**Table 3. Recommended USB Devices**

| PART NUMBER | MANUFACTURER |
|---|---|
| CY7C68013A | Cypress |
| 24LC128I/SN | Microchip Technology |

#### 8.2.2.1.4 SPI Slave Interface

The DLPC200 controller SPI interface consists of a 5-MHz input.

The SPI bus specifies five logic signals.

- SLAVE_SPI_CLK – Serial clock (output from master)
- SLAVE_SPI_MOSI – Master output, slave input (output from master)
- SLAVE_SPI_MISO – Master input, slave output (output from slave, does not tristate)
- $\overline{\text{SLAVE_SPI_CS}}$ – Slave select (active low; output from master)
- SLAVE_SPI_ACK – Holdoff signal to indicate that the slave is processing commands and cannot accept new input (output from slave)

The master pulls the slave-select low. During each SPI clock cycle, a full-duplex data transmission occurs:

- The master sends a bit on the MOSI line; the slave reads it from that same line.
- The slave sends a bit on the MISO line; the master reads it from that same line.

Transmissions involve two shift registers, one in the master and one in the slave; they are connected in a ring. Data is shifted out with the most significant bit first, while shifting a new least significant bit into the same register.

After that register has been shifted out, the master and slave have exchanged register values. If there is more data to exchange, the shift registers are loaded with new data and the process repeats. Transmissions may involve any number of clock cycles.

When there is no more data to be transmitted, the master stops toggling its clock. Transmissions consist of packet commands/responses similar to the protocol defined for the USB interface. The SPI slave supports variable-length command and response packets, and a master can initiate multiple such transmissions as needed.

**NOTE**

The SLAVE_SPI_MOSI signal dose not tristate. To use the controller's slave SPI interface in a multi-slave SPI bus an external tristate buffer, like *SN74LVC1G*, must be used on the SLAVE_SPI_MOSI signal.

#### 8.2.2.1.5 Parallel Flash Memory Interface

The controller parallel flash memory interface supports a high-speed NOR device with a 16-bit data bus and up to 1 GB of memory.


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To perform an asynchronous read, an address is driven onto the address bus, and $\overline{CE}$ is asserted. $\overline{WE}$ and $\overline{RST}$ must already have been deasserted. WAIT is configured to be active low and is set to a deasserted state. $\overline{ADV}$ must be held low throughout the read cycle. CLK is not used for asynchronous reads and is ignored. After $\overline{OE}$ is asserted, the data is driven onto DQ[15:0] after an initial access time $t_{AVQV}$ or $t_{GLQV}$ delay.

The WAIT signal indicates data valid when the device is operating in asynchronous mode (RCR.15 = 0). The WAIT signal is only deasserted when data is valid on the bus. When the device is operating in asynchronous non-array read mode, such as read status, read ID, or read query, the WAIT signal is also deasserted when data is valid on the bus. WAIT behavior during asynchronous non-array reads at the end of the word line works correctly only on the first data access.

To perform a write operation, both $\overline{CE}$ and $\overline{WE}$ are asserted while $\overline{RST}$ and $\overline{OE}$ are deasserted. During a write operation, address and data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. When the device is operating in write operations, WAIT is set to a deasserted state as determined by RCR.10.

**Table 4. Recommended Parallel Flash Devices**

| PART NUMBER | MANUFACTURER | SIZE |
|---|---|---|
| JS28F00AP30BF | Numonyx | 128 Mb |

#### 8.2.2.1.6 Serial Flash Memory Interface

Table 5 shows the serial flash parts that were tested by TI and found to work properly with the DLPC200.

**Table 5. Recommended Serial Flash Devices**

| PART NUMBER | MANUFACTURER | SIZE |
|---|---|---|
| M25P64 | Numonyx | 64 Mb |
| W25X64 | Winbond | 64 Mb |

#### 8.2.2.1.7 SRAM Interface

Table 6 shows the serial flash parts that were tested by TI and found to work properly with the DLPC200. See the recommended SRAM data sheet for read and write cycle timing information.

**Table 6. Recommended Static RAM Devices**

| PART NUMBER | MANUFACTURER | SIZE |
|---|---|---|
| CY7C1011DV33 | Cypress | 2 Mb |

#### 8.2.2.1.8 DDR2 SDR Memory Interface

The DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory. It is internally configured as a multibank DRAM. The controller DDR-2 memory interface consists of four 32-Mb by 16-bit wide, DDR-2 interfaces with double-data-rate signaling, operating at 133.33 MHz (nominal). A bidirectional data strobe (DQS, $\overline{DQS}$) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READ commands and by the memory controller during WRITE commands. DQS is edge-aligned with data for READ commands and center-aligned with data for WRITE commands.

The DDR2 SDRAM operates from a differential clock (CK and $\overline{CK}$); the crossing of CK going high and $\overline{CK}$ going low is referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK. Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

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#### 8.2.2.1.9 Projector Image and Control Port Signals

The DLPC200 provides two input ports for graphics and motion video inputs. The following listed signals support the two input interface modes.

Following are the two input image interface modes, signal descriptions, and pins needed on the DLPC200.

- PORT 1, 28 pins (HDMI connector)
  - PORT1_D(23-0) – Projector data
  - PORT1_VSYNC – Vertical sync
  - PORT1_HSYNC – Horizontal sync
  - PORT1_IVALID – Data enable
  - PORT1_CLK – Projector clock (rising edge or falling edge, to capture input data)
- PORT 2, 28 pins (expansion connector)
  - PORT2_D(23-0) – Projector data
  - PORT2_VSYNC – Vertical sync
  - PORT2_HSYNC – Horizontal sync
  - PORT2_IVALID – Data enable
  - PORT2_CLK – Projector clock (rising edge or falling edge, to capture input data)

Two control interfaces, USB and SPI, are provided to configure the DLPC200, as well as to transmit pattern data to memory for structured light mode. Following are the pins needed for the SPI and USB control interfaces.

- USB, 48 MHz
  - USB_CLK – USB clock
  - USB_CTRL1 – FIFO full flag
  - USB_CTRL2 – FIFO empty flag
  - USB_FD(15–0) – USB data
  - USB_PA02 – FIFO output enable for reads
  - USB_PA04 – FIFO address bit
  - USB_PA05 – FIFO address bit
  - USB_RDY1 – Write enable
  - USB_RDY0 – Read enable
- SPI, 5 MHz
  - SLAVE_SPI_CLK – SPI clock
  - SLAVE_SPI_ACK – Busy signal that holds off additional transactions until the slave has completed processing data
  - SLAVE_SPI_MISO – Output from slave
  - SLAVE_SPI_MOSI – Output from master
  - SLAVE_SPI_CS – Slave select

Images are displayed via control of the DMD and DLPA200. The DLPC200 DMD interface consists of a 200-MHz (nominal) half-bus DDR output-only interface with LVDS signaling. The serial communications port (SCP), 125-kHz nominal, is used to read or write control data to both the DMD and the DLPA200. The following listed signals support data transfer to the DMD and DLPA200.

- DMD, 200 MHz
  - DMD_CLK_AP, DMD_CLK_AN – DMD clock for A
  - DMD_CLK_BP, DMD_CLK_BN – DMD clock for B
  - DMD_DAT_AP, DMD_DAT_AN(1, 3, 5, 7, 9, 11, 13, 15) – Data bus A (odd-numbered pins are used for half-bus)
  - DMD_DAT_BP, DMD_DAT_BN(1, 3, 5, 7, 9, 11, 13, 15) – Data bus B (odd-numbered pins are used for half-bus)
  - DMD_SCRTL_AP, DMD_SCRTL_AN – S-control for A
  - DMD_SCRTL_BP, DMD_SCRTL_BN – S-control for B
- DLPA200, 125 kHz


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- SCP_DMD_RST_CLK – SCP clock
- SCP_DMD_EN – Enable DMD communication
- SCP_RST_EN – Enable DLPA200 communication
- SCP_DMD_RST_DI – Input data
- SCP_DMD_RST_DO – Output data

#### 8.2.2.1.10 SDRAM Memory

The DLPC200 requires an external DDR2 SDR SDRAM. The DLPC200 supports the use of four 512-Mb SDRAMs. The requirements for the SDRAMs are:

- SDRAM type: DDR2
- Speed: 133 MHz minimum
- 16-bit interface size: 32 Mb
- Supply voltage: 1.8 V

Table 7 lists the recommended SDRAM devices that have been tested by TI and found to work properly with the DLPC200.

**Table 7. Recommended SDRAM Devices**

| PART NUMBER | MANUFACTURER | SIZE |
|---|---|---|
| MT47H32M16-25E (replaces now obsolete – MT47H32M16R) | Micron | 512 Mb |

### 8.2.3 Application Curve

The DLPC200 is used to control the DLP5500 0.5-inch XGA DMD. This device can be used for numerous applications in the visible range of the spectrum such as 3D printing or structured light. Figure 16 shows single-pass window transmission for 0° and 30° angles of incidence. The area from 420 to 700 nm (light blue) is the range specified for operation of the DLP5500.

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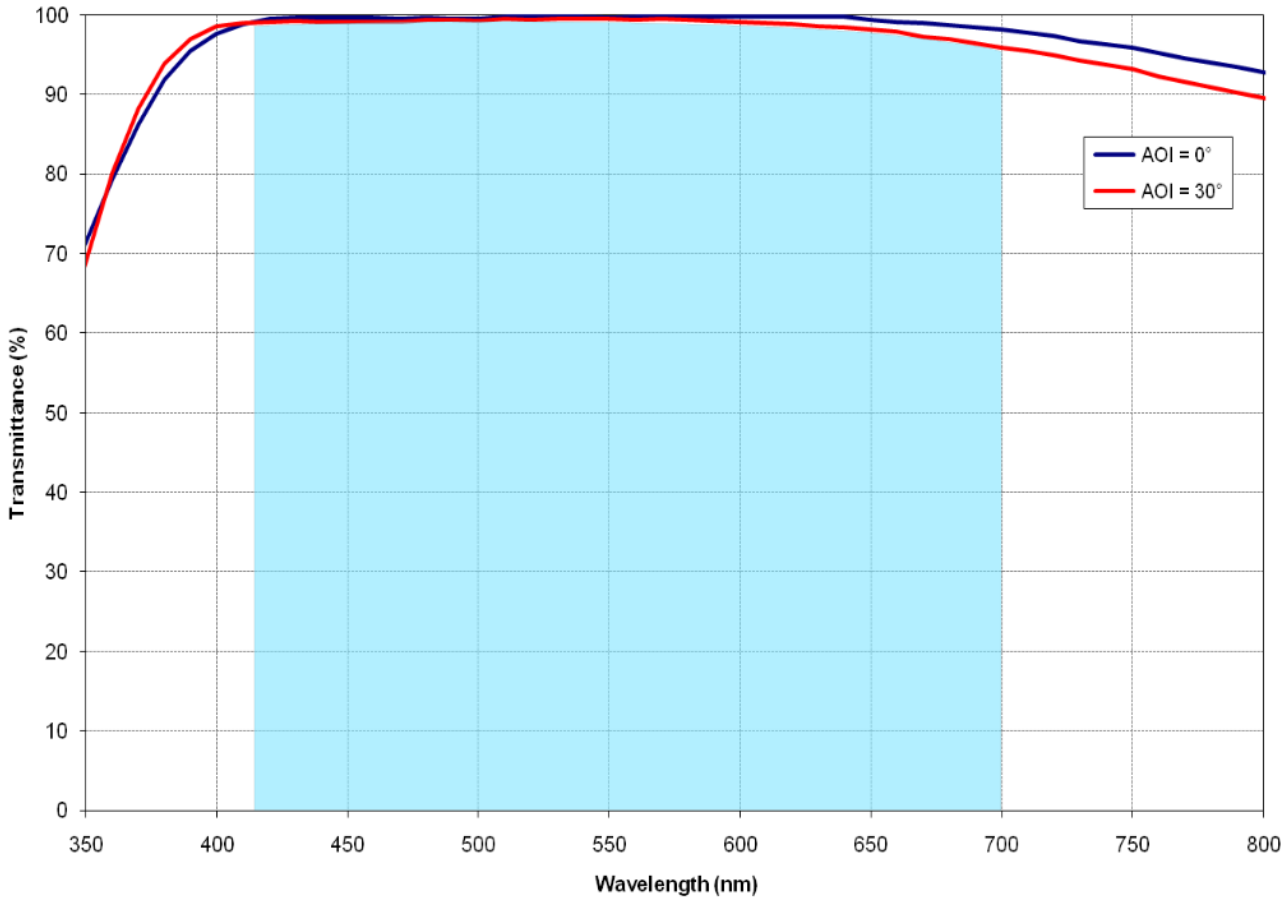


**Figure 16. Window Transmission Curve for the DLP5500**


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# 9 Power Supply Recommendations

## 9.1 Power-Up Requirements

Details about the chip power-up requirements are included in the DLPZ004 chipset data sheet. For the DLPC200, there is a 50-MHz reference clock that must meet the specifications listed in Table 8. Additionally, at power-up, the 3.3-V supply must be stable for 2 s before the global reset (RESET) occurs, and then PWR_GOOD occurs within 20 ms.

The latest revision of the firmware (#DLPR200) does not enable the LEDs over the LED Control interface until initialization is complete and any solution loaded in flash is running.

**Table 8. Reference Clock Oscillator Requirements**

| PART NUMBER | FREQUENCY STABILITY | FREQUENCY | SUPPLY VOLTAGE |
|---|---|---|---|
| ASV-50.000MHZ-E-J-T | ±20 ppm (0.002% or ±0.001 MHz) | 50 MHz | 3.3 V |

## 9.2 Power-Down Requirements

Details about the chip power-down requirements are included in the DLPZ004 chipset data sheet. For the DLPC200, there is a minimum 1-ms delay from the time when PWR_GOOD goes low until any of the supplied voltages can drop below their minimum valid values (see Table 9). This is required so that the DMD can be parked. See Table 9 for more details.

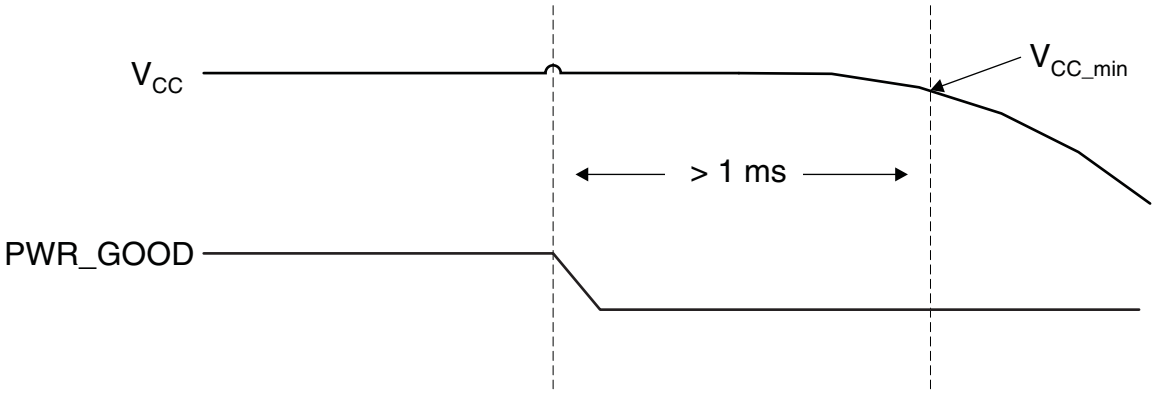


**Figure 17.**

**Table 9. Supply Voltages and Minimum Values**

| $V_{CC}$ | $V_{CC_min}$ | UNIT |
|---|---|---|
| 1.2 | 1.14 | V |
| 1.8 | 1.71 | |
| 2.5 | 2.375 | |
| 3.3 | 3.135 | |

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# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50 Ω ±10% except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn) and DDR2 differential clock pairs (MEM_CLK_nn), which should be matched to 100 Ω ±10% across each pair.

### 10.1.2 PCB Signal Routing

When designing a PCB board for the DLPC200 the following are recommended:

Maintain signal trace corners no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

Do not allow high speed signal traces to cross over slots in adjacent power and/or ground planes.

**Table 10. Important Signal Trace Constraints**

| Signal | Constraints |
|---|---|
| DDR2 differential clock pairs | P-to-N length <12 mils (0.31 mm)<br>Trace width: 30 mil (0.76 mm) |
| DDR2 data | Length within ±150 mils (3.81 mm) relative to DDR2 differential clock<br>Maximum termination signal recommended trace length <0.5 inch (12.7 mm) |
| LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn) | P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example DMD_DAT_Ann to DMD_DAT_Bnn)<br>Trace width: 4 mil (0.1 mm)<br>Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm)<br>Maximum recommended trace length <6 inches (150 mm) |

**Table 11. Power Trace Widths and Spacing**

| Signal Name | Minimum Trace Width | Minimum Trace Spacing | Layout Requirements |
|---|---|---|---|
| GND | Maximize | 5 mil (0.13 mm) | Maximize trace width to connecting pin as a minimum |
| P3P3V | 400 mil (10.2 mm) | 10 mil (0.25 mm) | Create mini plane and connect to devices as necessary with multiple vias |
| P5V, P2P5V, P1P8V, P1P5V, P1P2V | 50 mil (1.3 mm) | 10 mil (0.25 mm) | Create mini planes and connect to devices as necessary with multiple vias |
| P5V, P3P3V, P2P5V, P1P8V, P1P5V, P1P2V | 30 mil (0.76 mm) | 10 mil (0.25 mm) | Stub width to connecting IC pins; maximize width when possible |
| VREF_Bn | 200 mil (5.1 mm) | 30 mil (0.76 mm) | Stub width to connecting IC pins; maximize width when possible |

### 10.1.3 Fiducials

Ffor automatic component insertion fiducials, use 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

## 10.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, Figure 18 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.


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## Layout Example (continued)

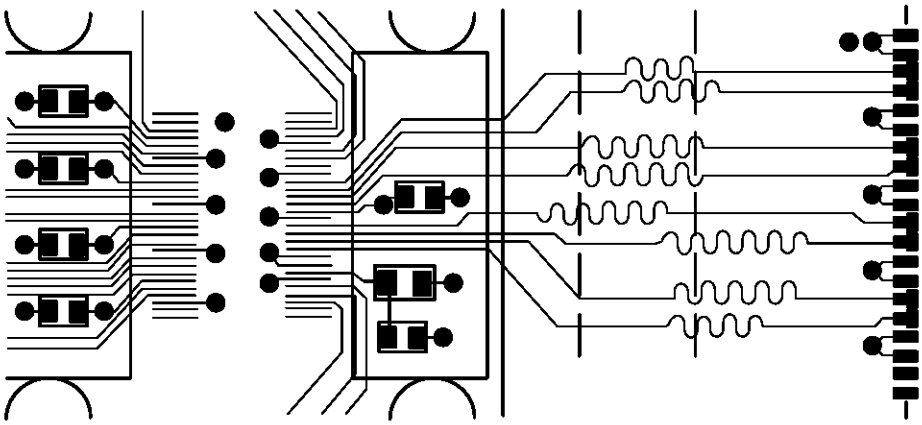

**Figure 18. Mitering LVDS Traces to Match Lengths**

## 10.3 Thermal Considerations

The underlying thermal limitation for the DLPC200 is that the maximum operating junction temperature ($T_J$) not be exceeded (see *Recommended Operating Conditions*). This temperature depends on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC200, and power dissipation of surrounding components. The DLPC200 package is designed primarily to extract heat through the power and ground planes of the PCB; thus, copper content and airflow over the PCB are important factors.

### 10.3.1 Heat Sink

A heat sink not required for operation between 0°C and 55°C ambient, but is required for operation between 55°C and 85°C, TI recommends a low-profile (15-mm) heat sink. See *Thermal Information* for thermal resistance with different airflow values without a heat sink.

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# 11 デバイスおよびドキュメントのサポート

## 11.1 デバイス・サポート

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### 11.1.2 デバイス・マーキング

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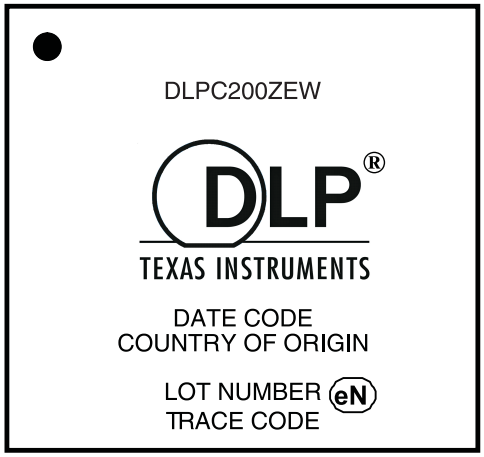


マーキングのキー

1行目: TIの参照番号
2行目: デバイス名
3行目: DLP®ロゴ
4行目: 日付コード
5行目: 製造国
6行目: 組み立てロット番号
7行目: トレース・コード

## 11.2 ドキュメントのサポート

関連文書

- 『DLP 0.55 XGAチップセット』データシート
- 『DLPA200 DMD マイクロミラー・ドライバ』
- 『DLP5500 0.55 XGA DMD』データシート

## 11.3 ドキュメントの更新通知を受け取る方法

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## 11.4 コミュニティ・リソース

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## コミュニティ・リソース (continued)

し、アイディアを検討して、問題解決に役立てることができます。

**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DLPC200ZEW | ACTIVE | BGA | ZEW | 780 | 5 | TBD | Call TI | Call TI | -20 to 85 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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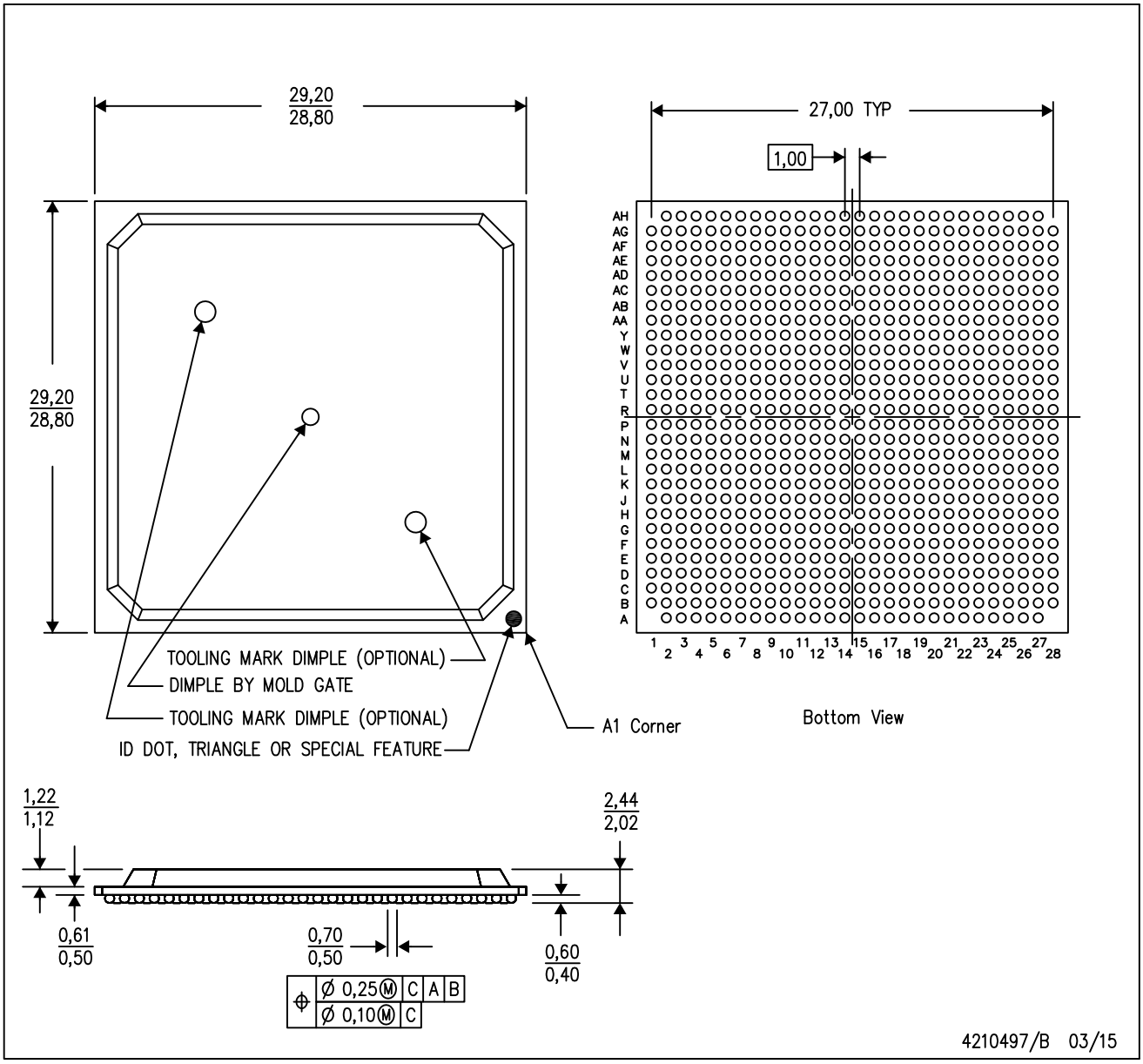
ZEW (S–PBGA–N780) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–034, Variation: AAM–1.
D. This package is Pb–free.

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