DS90UH948-Q1 車載用 2K、FPD-Link III から OpenLDI への HDCP 搭載デシリアライザ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み：
  - デバイス温度グレード 2：-40℃～+105℃の動作時周囲温度範囲
- 最高で 2K (2048x1080) の解像度と 24 ビットの色深度に対応する、最大 192MHz のピクセル・クロック周波数をサポート
- 歪み補正機能を搭載した 1 レーンまたは 2 レーンの FPD-Link III インターフェイス
- シングルまたはデュアルの OpenLDI (LVDS) トランスミッタ
  - シングル・チャネル：最高 96MHz のピクセル・クロック
  - デュアル・チャネル：最高 192MHz のピクセル・クロック
  - 18 ビット RGB または 24 ビット RGB に構成可能
- HDCP 暗号エンジンを内蔵し、キーをオンチップに保存
- HDCP リピータ・アプリケーションに対応
- 機能安全対応
  - ISO 26262 システムの設計に役立つ資料を利用可能
- 4 つの高速 GPIO (それぞれ最高 2Mbps)
- 適応型受信イコライゼーション
  - 1.48GHz で最高 -15.5dB、1.68GHz で最高 -9dB のチャネル挿入損失を補償
  - 温度およびケーブル劣化を自動的に補償
- 最高 3.3Mbps の SPI 制御インターフェイス
- 1Mbps の Fast-Mode Plus 対応の I2C (コントローラ / ターゲット)
- イメージ拡張 (ホワイト・バランスおよびディザリング)
- 7.1 のマルチ I2S (4 データ) チャネルをサポート

2 アプリケーション

- 車載インフォテインメント
  - 集中情報ディスプレイ
  - リアシート・エンターテインメント・システム
  - デジタル計器クラスタ

3 概要

DS90UH948-Q1 は FPD-Link III デシリアライザであり、DS90UH949A/949/947-Q1 シリアライザと組み合わせることで、1 レーンまたは 2 レーンの FPD-Link III ストリームを FPD-Link (OpenLDI) インターフェイスに変換します。このデシリアライザは、コスト効率の優れた 50Ω のシングルエンド同軸、または 100Ω の差動シールド付きツイストペア (STP) ケーブル上で動作できます。1 つまたは 2 つの FPD-Link III シリアル・ストリームからデータを回復し、デュアル・ピクセル FPD-Link (LVDS データ・レーン 8 つ + クロック) に変換して、24 ビットのカラー深度で 2K (2048×1080) までのビデオ解像度に対応できます。これによって、GPU などの HDMI 対応ソースを、既存の LVDS ディスプレイやアプリケーション・プロセッサに接続するためのブリッジとして使用できます。

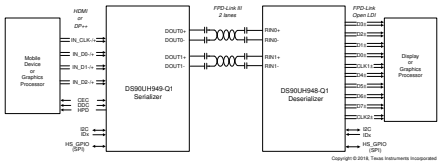
FPD-Link III インターフェイスは、ビデオとオーディオのデータ転送に加えて、I2C および SPI 通信などの全二重制御機能を同じ差動リンク上でサポートします。ビデオ・データと制御を 2 つの差動ペアに統合することで、相互接続のサイズと重量が減少し、システムの設計が簡素化されます。低電圧の差動信号、データのスクランブル処理、およびランダム化を使用することで、EMI が最小限に抑えられます。下位互換モードでは、このデバイスは 1 つの差動リンクを使用し、24 ビット色深度で WXGA および 720p までの解像度に対応できます。

このデバイスは FPD-Link III チャネルを自動的に検出し、特別なトレーニング・パターンを必要とせずに、クロック同期および歪み補正機能を提供します。これによって、PCB 配線、ケーブルのペア間の長さ相違、コネクタの不均衡など、相互接続配線の不一致に起因する位相歪みに対する許容性が保証されます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
DS90UH948-Q1	WQFN (64)	9.00mm × 9.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2020) to Revision D (February 2022)	Page
• 周波数に対する最大チャネル挿入損失を明確化	1
• Clarified the description of the clock and data differential output pins	5
• Changed IDx pin voltage from VDD18 to VDD33	5
• Removed normal mode PASS function since PASS is used only in BIST mode	5
• Updated the inclusive termonologies for SPI and I2C by changing "master" and "slave" wording	5
• Updated the SPI pin names from "MOSI" to "PICO", "MISO" to "POCI", and "SS" to "CS"	5
• Changed the I2S mode names from Slave Mode to Surround Sound Mode, and from Master Mode to Auxiliary Audio Mode	5
• Added some missing units for current and voltage	12
• Modified the list of compatible devices	22
• Removed PASS from the table since PASS functionality is only used for BIST mode	24
• Corrected the Nyquist Frequency for PCLK 192MHz	31
• Added clarification for I2S transport modes	33
• Added clarifying notes for BIST function	39
• Added a clarifying note on using I2C while PATGEN is enabled	40
• Added new section "Dual Swap"	43
• Clarified LVDS mapping names	44
• LVDS Formats table added	44
• Added clarifying notes to LUT contents.	49
• Added LUT Programming Example	50
• Added clarifying notes about I2C access over the BCC	53
• Specified which registers are not being reset when digital reset is applied	56
• Changed default value of register 0x01[2] and added clarifying notes	56
• Changed default value of register 0x03[7]	56
• Changed reset value of register 0x1D, and changed default value for bits [7:4]	56
• Changed reset value for registers 0x1E and 0x1F to 0x00	56

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- Added clarifying note to register 0x22, that surround audio is not supported in repeater mode when 18-bit video mode is enabled....56
- Added minimum value to register 0x26 56
- Changed default value for register 0x45[7:5] and changed to R/W. Added clarifying note. 56
- Changed default value for register 0x4B[3:2] and changed to R/W. Added clarifying note....56
- Added clarifying note to CMLOUT function in register 0x57....56
- Changed default value for register 0xF4....56
- Corrected the name of the Pattern Generation Application Note in the *Related Documentation* section. 106

Changes from Revision B (November 2020) to Revision C (December 2020) **Page**

- 「特長」の箇条書き項目に「機能安全対応」を追加....1

Changes from Revision A (January 2016) to Revision B (November 2018) **Page**

- より高速な 192MHz をサポートするように PCLK 周波数を変更。....1
- 「代表的なアプリケーション」を簡素化し、電源ノードを削除。....1
- Removed bolded pin description name for power supplies. 5
- Added new pin description content to the *Pin Functions* table 5
- Changed the description from VDDIO to V(I2C). 5
- Specified in current instead of resistor for all pulldown resistor 5
- Removed 200-µA minimum ramp time for PDB pin description. 5
- Added the description to clarify the INTB_IN that this pin can be an output driver....5
- Changed pin names from CAP_PLL0 and CAP_PLL1 to RES0 and RES1 respectively. 5
- Removed tablenote from the *Absolute Maximum Ratings* table: For soldering specifications, see product folder at www.ti.com and SNOA549 11
- Added Military/Aerospace tablenote to the *Absolute Maximum Ratings* table 11
- Changed supply voltage maximum for the VDD33 from: 4 V to: 3.96 V 11
- Changed VDD12 abs max from 1.8V to 1.44V. 11
- Changed supply voltage for the VDDIO from: 4 V to: 3.96 V 11
- Added the Added the open-drain voltage, CML output voltage, and FPD-Link III input voltage parameters to the Absolute Maximum Ratings table , open-drain voltage, CML output voltage, and FPD-Link III input voltage parameters to the *Absolute Maximum Ratings* table 11
- Added test conditions to the LVCMOS I/O voltage parameter 11
- Spelled out all GPIOs pin name....11
- Combined the ESD ratings into one *ESD Ratings* table 11
- Removed VDD18 test condition from the supply voltage parameter 11
- Added the open-drain voltage parameter to the *Recommended Operating Conditions* table 11
- Changed open LDI clock frequency (dual link) maximum from: 170 MHz to: 192 MHz 11
- Added the local I2C frequency parameter to the *Recommended Operating Conditions* table 11
- Added test conditions to the supply noise parameter 11
- Changed the total power consumption, normal operation test conditions 12
- Changed "VDD12 = 1.2 V" to "VDD12 = 1.2 V"....12
- Removed the checkerboard vs. PRBS pattern condition and combined typical and worst case together. 12
- Added current specs for PCLK 192 MHz. 12
- Deleted typical value for Vih and Vil in 3.3V LVCMOS I/O....12
- Split out the test conditions in the 3.3-V and 1.8-V LVCMOS I/O parameters 12
- Added strap pin input current parameter to the *DC Electrical Characteristics* table 12
- Deleted typical value for Vih and Vil in 1.8V LVCMOS I/O. 12
- Deleted typical value for Vih and Vil in serial control bus 12
- Added test conditions to the input high level and input low level parameters 12
- Changed "complimentary" to "complementary" 12
- Removed tablenote from the *AC Electrical Characteristics* table: This parameter is specified by characterization and is not tested in production. 15
- Changed differential output eye height from: >300 mV to: 300 mV 15
- Added input jitter tolerance specs. 15

- Removed tablenote from the *Timing Requirements* table: Parameter is specified by bench characterization and is not tested in production. 16
- Changed C_b fast mode plus maximum value from: 550 pF to: 200 pF 16
- Removed tablenote from the *Switching Characteristics* table: Parameter is specified by bench characterization and is not tested in production. 17
- Changed *Deserializer Eye Diagram* graph in the *Typical Characteristics* section..... 21
- Added paragraph explains HSCC mode..... 25
- Changed transmission distance section and insertion loss table..... 31
- Changed PCLK frequncy from 96 MHz to 192 MHz in the diagram "2-lane FPD-link Input, Link OpenLDI Output" in the *Data-Path Configurations* graphic..... 42
- Changed the resistor ratio value for both the *Configuration Select (MODE_SEL0)* and *Configuration Select (MODE_SEL1)* tables..... 42
- Deleted repeated first paragraph LUT contents. 49
- Changed pullup power supply node from "VDDIO" to "V(I2C). 53
- Updated register table format to the latest TI standards in the *Register Maps* section..... 56
- Changed input value from 1.2 V to 1.2 V in typical application drawings 94
- Updated STP diagram. 94
- Updated Coax diagram..... 94
- Simplified the diagram by removing power supplies node. 94
- Added new design parameters to the *Design Requirements* section 97
- Changed VDD12 in Design Parameters 1.2 to 1.2..... 97
- Changed *CML Interconnect Guidelines* section title to *FPD-Link III Interconnect Guidelines* 98
- Added *AV Mute Prevention* section 98
- Added *Prevention of I2C Errors During Abrupt System Faults* section 99
- Moved the *Power Sequence* graphic to the *Power Supply Recommendations* 100
- Removed power supplies columns and changed the parameters in the *Power-Up Sequencing Constraints* table according to the diagram. 100
- Moved the *PCB Layout and Power System Considerations* content to the *Layout Guidelines* section 102
- Added *Ground* and *Routing FPD-Link III Signal Traces* sections to the *Layout* section..... 102
- Added Added FPD-Link training videos to the *Related Documentation* section. 106

Changes from Revision * (October 2014) to Revision A (January 2016) — Page

- Added shared pins description on SPI pins 5
- Added shared pins description on GPIO pins 5
- Added shared pins description on D_GPIO pins 5
- Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". 5
- Added shared pins description on slave mode I2S pins 5
- Added shared pins description on Controller mode I2S pins 5
- Added legend for I/O TYPE..... 5
- Moved Storage Temperature Range from ESD to *Absolute Maximum Ratings* table 11
- Added ESD Ratings table..... 11
- Changed IDD12Z limit from 8mA to 30mA per PE re-characterization 12
- Changed V_{OS} from 1.0V to 1.125V 12
- Changed V_{OS} from 1.5V to 1.375V 12
- Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns 16
- Changed text from: AEQ_FLOOR value to: ADAPTIVE_EQ_FLOOR_VALUE 32
- Added Image Enhancement Features section 49
- Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show ‘Strap’ as their default value in this table." 56
- Corrected 0x02[7]register default value from "0" to "1" 56
- Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*" 56
- Corrected 0x02[4] register default value from 0 to 1 56
- Added "Loaded from remote SER" in register 0x07[7:1] function column..... 56

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- Changed from Reserved to Rev-ID in register 0x1D Function column 56
- On register 0x22 added "(Loaded from remote SER)" 56
- Corrected in register 0x24[3] 0: Bist configured through "bit 0" to "bits 2:0" in description 56
- Added in register 0x24[2:1] additional description 56
- Changed in register 0x24[1] description to "internal" 56
- Changed in register 0x24[2] description to "internal" 56
- On register 0x28 added "Loaded from remote SER" 56
- Added clarification description on register 0x37 MODE_SEL 56
- Merged on 0x45 bits[7:4} and bits[3:0] default value: 0x08 56
- Added Power Sequence section 100

5 Pin Configuration and Functions

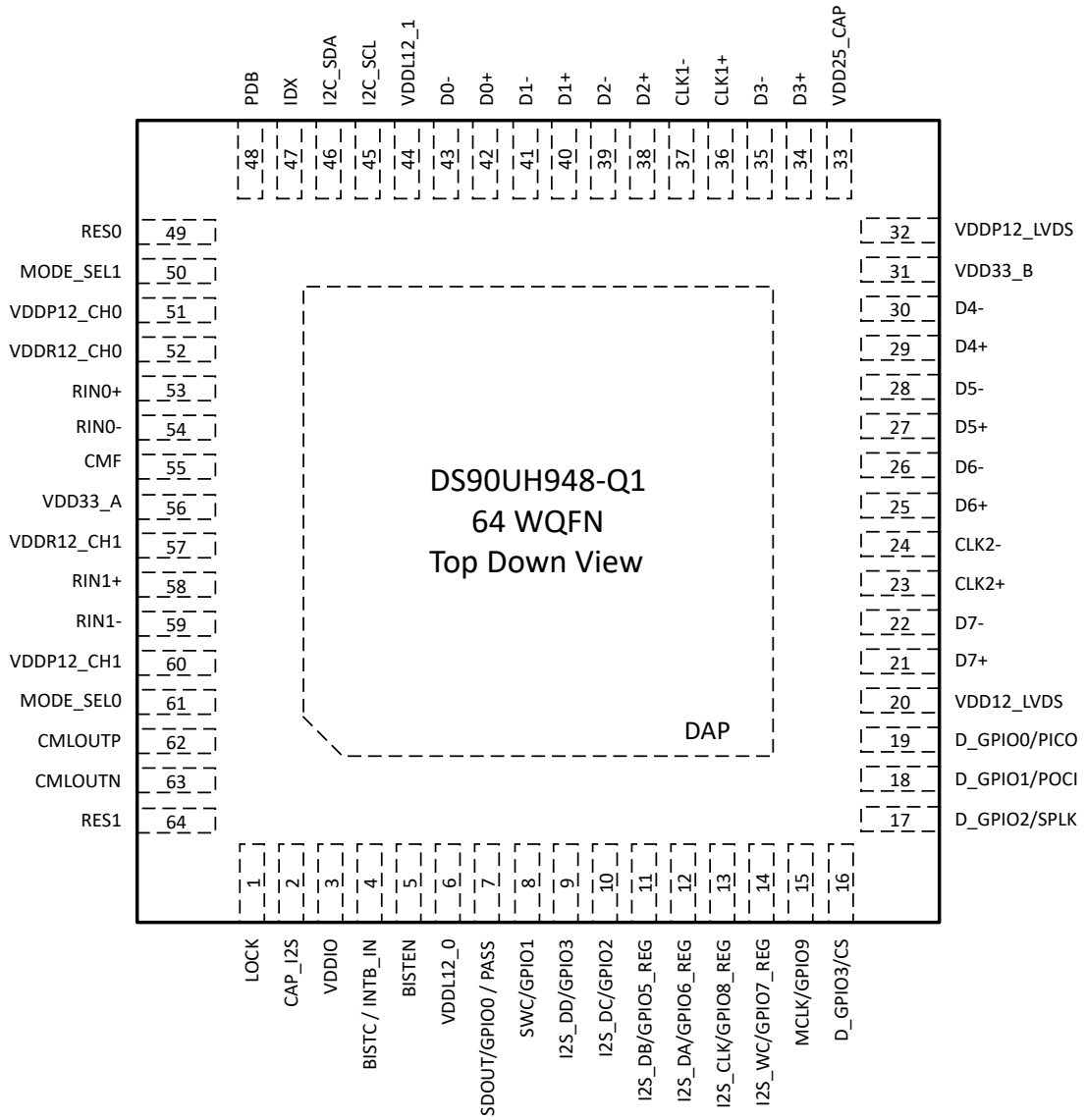

図 5-1. NKD Package
64-Pin WQFN
Top View

表 5-1. Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
OLDI OUTPUT PINS			
CLK1– CLK1+	37 36	O, LVDS	Clock differential output pins This pair requires an external 100-Ω termination for LVDS. Leave unused pins as No Connect or terminate each differential pair with 100 ohms
CLK2– CLK2+	24 23	O, LVDS	
D0– D0+	43 42	O, LVDS	Differential data output pins This pair requires an external 100-Ω termination for LVDS. Leave unused pins as No Connect or terminate each differential pair with 100 ohms
D1– D1+	41 40	O, LVDS	
D2– D2+	39 38	O, LVDS	
D3– D3+	35 34	O, LVDS	
D4– D4+	30 29	O, LVDS	
D5– D5+	28 27	O, LVDS	
D6– D6+	26 25	O, LVDS	
D7– D7+	22 21	O, LVDS	
FPD-LINK III INTERFACE			
RIN0–	54	I/O	FPD-Link III RX Port 0 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see 図 8-4 and 図 8-5). It must be AC-coupled per 表 8-1. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
RIN0+	53	I/O	
RIN1–	59	I/O	FPD-Link III RX Port 1 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see 図 8-4 and 図 8-5). It must be AC-coupled per 表 8-1. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
RIN1+	58	I/O	
CMF	55	I/O	Common mode filter – connect 0.1-µF capacitor to GND
I2C PINS			
I2C_SDA	46	I/O, OD	I2C Data Input / Output Interface pin. See *セクション 7.6.1*. Open drain output; this pin must have an external pullup resistor to V_{I2C} **DO NOT FLOAT.** Recommend a 2.2 kΩ or 4.7 kΩ pullup to 1.8 V or 3.3 V respectively. See *I2C Bus Pullup Resistor Calculation* (SLVA689).
I2C_SCL	45	I/O, OD	I2C Data Input / Output Interface pin. See *セクション 7.6.1*. Open drain output; this pin must have an external pullup resistor to V_{I2C} **DO NOT FLOAT.** Recommend a 2.2 kΩ or 4.7 kΩ pullup to 1.8 V or 3.3 V respectively. See *I2C Bus Pullup Resistor Calculation* (SLVA689).
IDx	47	I, S	I2C Serial Control Bus Device ID Address Select configuration pin Connect to an external pullup to VDD33 and a pulldown to GND to create a voltage divider. See 表 7-11.
SPI PINS			
PICO (D_GPIO0)	19	I/O, PD	SPI Controller Output, Peripheral Input pin (function programmed through register) It is a multifunction pin (shared with D_GPIO0) with a weak internal pulldown (3µA). Pin function is programmed through registers. If unused, tie to an external pulldown.
POCI (D_GPIO1)	18	I/O, PD	SPI Controller Input, Peripheral Output pin (function programmed through register) It is a multifunction pin (shared with D_GPIO1) with a weak internal pulldown (3µA). Pin function is programmed through registers. If unused, tie to an external pulldown.
SPLK (D_GPIO2)	17	I/O, PD	SPI Clock pin (function programmed through register) It is a multifunction pin (shared with D_GPIO2) with a weak internal pulldown (3µA). Pin function is programmed through registers. If unused, tie to an external pulldown.

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表 5-1. Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
CS (D_GPIO3)	16	I/O, PD	SPI Peripheral Select pin (function programmed through register) It is a multifunction pin (shared with D_GPIO0) with a weak internal pulldown (3μA). Pin function is programmed through registers. If unused, tie to an external pulldown.
CONTROL PINS			
MODE_SEL0	61	I, S	Mode Select 0 configuration pin Connect to external pullup to VDD33 and pulldown to GND to create a voltage divider. See Configuration Select (MODE_SEL0) 表 7-8.
MODE_SEL1	50	I, S	Mode Select 1 configuration pin Connect to external pullup to VDD33 and pulldown to GND to create a voltage divider. See Configuration Select (MODE_SEL1) 表 7-9.
PDB	48	I, PD	Inverted Power-Down input pin Typically connected to a processor GPIO with a pulldown. When PDB input is brought HIGH, the device is enabled and internal registers and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN with an weak (>100-kΩ) internal pulldown enabled. PDB should remain low until after power supplies are applied and reach minimum required levels. PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down When the device is in the POWER DOWN state, the LVCMOS outputs are in tri-state, the PLL is shut down, and IDD is minimized.
BISTEN	5	I, PD	BIST Enable pin 0: BIST mode is disabled 1: BIST mode is enabled It is a configuration pin with a weak internal pulldown (3μA). If unused, tie to an external pulldown. See *セクション 7.3.15* for more information.
BISTC (INTB_IN)	4	I, PD	BIST Clock Select pin (function programmed through register) 0: PCLK 1: 33 MHz It is a multifunction pin (shared with INTB_IN) with a weak internal pulldown (3μA). Pin function is programmed through registers. If unused, tie to an external pulldown.
INTB_IN (BISTC)	4	I, PD	Interrupt Input pin (default function). It is a multifunction pin (shared with BISTC) with a weak internal pulldown (3μA). Pin function is programmed through registers. If unused, tie to an external pulldown. The INTB_IN pin may act as an output driver and pull low when PDB is low (see *セクション 7.3.8*).
GPIO PINS			
GPIO0 (SDOUT)	7	I/O	General Purpose Input / Output 0 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with SDOUT) with a weak internal pulldown (3 μA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO1 (SWC)	8	I/O	General Purpose Input / Output 1 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with SWC) with a weak internal pulldown (3 μA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO2 (I2S_DC)	10	I/O	General Purpose Input / Output 2 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with I2S_DC) with a weak internal pulldown (3 μA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO3 (I2S_DD)	9	I/O	General Purpose Input / Output 3 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with I2C_DD) with a weak internal pulldown (3 μA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO9 (MCLK)	15	I/O	General Purpose Input / Output 9 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with MCLK) with a weak internal pulldown (3 μA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
HIGH-SPEED GPIO PINS			

表 5-1. Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
D_GPIO0 (PICO)	19	I/O	High-Speed General Purpose Input / Output 0 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with PICO) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
D_GPIO1 (POCI)	18	I/O	High-Speed General Purpose Input / Output 1 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with POCI) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
D_GPIO2 (SPLK)	17	I/O	High-Speed General Purpose Input / Output 2 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with SPLK) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
D_GPIO3 (CS)	16	I/O	High-Speed General Purpose Input / Output 3 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with CS) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See セクション 7.3.9. If unused, tie to an external pulldown.
REGISTER ONLY GPIO PINS			
GPIO5_REG (I2S_DB)	11	I/O	High-Speed General Purpose Input / Output 5 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_DB) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO6_REG (I2S_DA)	12	I/O	High-Speed General Purpose Input / Output 6 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_DA) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO7_REG (I2S_WC)	14	I/O	High-Speed General Purpose Input / Output 7 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_WC) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
GPIO8_REG (I2S_CLK)	13	I/O	High-Speed General Purpose Input / Output 8 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_CLK) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *セクション 7.3.9*. If unused, tie to an external pulldown.
SURROUND SOUND (SS) MODE LOCAL I2S CHANNEL PINS			
I2S_WC (GPIO7_REG)	14	O	SS Mode I2S Word Clock Output pin (function programmed through register) It is a multifunction pin (shared with GPIO7_REG). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
I2S_CLK (GPIO8_REG)	13	O	SS Mode I2S Clock Output pin (function programmed through register) **NOTE: Disable I2S data jitter cleaner, when using these pins, through the register bit I2S Control: 0x2B[7]=1** It is a multifunction pin (shared with GPIO8_REG). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
I2S_DA (GPIO6_REG)	12	O	SS Mode I2S Data Output pin (function programmed through register) It is a multifunction pin (shared with GPIO6_REG). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
I2S_DB (GPIO5_REG)	11	O	SS Mode I2S Data Output pin (function programmed through register) It is a multifunction pin (shared with GPIO5_REG). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.

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表 5-1. Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
I2S_DC (GPIO2)	10	O	SS Mode I2S Data Output (function programmed through register) It is a multifunction pin (shared with GPIO2). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
I2S_DD (GPIO3)	9	O	SS Mode I2S Data Output (function programmed through register) It is a multifunction pin (shared with GPIO3). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
AUXILIARY AUDIO (AA) MODE LOCAL I2S CHANNEL PINS			
SWC (GPIO1)	8	O	AA Mode I2S Word Clock Output pin (function is programmed through registers) (Pin is shared with GPIO1) It is a multifunction pin (shared with GPIO1). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
SDOUT (GPIO0)	7	O	AA Mode I2S Data Output pin (function is programmed through registers) (Pin is shared with GPIO0) It is a multifunction pin (shared with GPIO0). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
MCLK (GPIO9)	15	O	AA Mode I2S System Clock Output pin (function is programmed through registers) (Pin is shared with GPIO9) It is a multifunction pin (shared with GPIO9). Pin function is programmed through registers. See *セクション 7.3.13*. If unused, tie to an external pulldown.
STATUS PINS			
LOCK	1	O	Lock Status Output pin LOCK = 1: PLL acquired lock to the reference clock input LOCK = 0: PLL is unlocked
PASS	7	O	BIST mode status output pin (BISTEN = 1) PASS = 1: No error detected PASS = 0: Error detected
POWER and GROUND			
VDD33_A, VDD33_B	56 31	P	3.3-V (±10%) supply. Power to on-chip regulator. Requires 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND.
VDDIO	3	P	LVCMOS I/O power supply: 1.8 V (±5%) OR 3.3 V (±10%). Requires 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND.
VDD12_LVDS VDDP12_LVDS VDDL12_0 VDDL12_1 VDDP12_CH0 VDDR12_CH0 VDDP12_CH1 VDDR12_CH1	20 32 6 44 51 52 60 57	P	1.2-V (±5%) supply. Requires 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND at each VDD pin.
CAP_I2S VDD25_CAP	2 33	D	Decoupling capacitor connection for on-chip regulator. Recommend to connect with a 0.1-µF decoupling capacitor to GND.
VSS	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 32 vias.
OTHER PINS			
CMLOUTP CMLOUTN	62 63	O	Channel Monitor Loop-through Driver differential output pins Route to a test point or a pad with 100-Ω termination resistor between pins for channel monitoring (recommended). See 図 8-1 or 図 8-2.
RES0 RES1	49 64	-	Reserved pins. 0.1-µF decoupling capacitor could be placed to GND. May be left floating as No Connect pins.

The following definitions define the functionality of the I/O cells for each pin. I/O TYPE:

- P = Power supply
- G = Ground
- D = Decoupling for an internal linear regulator
- S = Configuration/Strap Input (All strap pins have internal pulldowns determined by IOZ specification. If the default strap value is needed to be changed then an external resistor should be used.
- I = Input
- O = Output
- I/O = Input/Output
- PD = Internal pulldown

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[2] [1]

		MIN	MAX	UNIT
Supply voltage	VDD33 (VDD33_A, VDD33_B)	–0.3	3.96	V
	VDD12 (VDDL_0, VDDL_1, VDDP12_CH0, VDDR12_CH0, VDDP12_CH1, , VDDR12_CH1, VDD12_LVDS, VDDP12_LVDS)	-0.3	1.44	V
	VDDIO	–0.3	3.96	V
Configuration input voltage	IDX, MODE_SEL0, MODE_SEL1	–0.3	3.96	V
LVCMOS I/O voltage	PDB, BIST_EN	-0.3	3.96	V
	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, LOCK, PASS, INTB_IN, MCLK	–0.3	$V_{(VDDIO)}$ + 0.3	V
Open-Drain voltage	I2C_SDA, I2C_SCL	–0.3	3.96	V
CML output voltage	CMLOUTP, CMLOUTN	-0.3	2.75	V
FPD-Link III input voltage	RIN0+, RIN0-, RIN1+, RIN1-	–0.3	2.75	V
Junction temperature, T_J			150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.

(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±8000	V
		Charged-device model (CDM), per AEC Q100-011		±1250	
		ESD Ratings (IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±8000	
			Air-gap Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±15000	
		ESD Ratings (ISO10605) R_D = 330 Ω, C_S = 150 and 330 pF R_D = 2 kΩ, C_S = 150 and 330 pF	Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±8000	
			Air-gap Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±15000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD33)}$	3	3.3	3.6	V
	$V_{(VDD12)}$	1.14	1.2	1.26	V
LVCMOS I/O supply voltage	$V_{(VDDIO)}$ = 3.3 V	3	3.3	3.6	V
	OR $V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
Open-drain voltage	I2C pins = $V_{(I2C)}$	1.71		3.6	V
Operating free air temperature, T_A		−40	25	105	°C
Open LDI clock frequency (single link)		25		96	MHz

6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Open LDI clock frequency (dual link)		50		192	MHz
Local I^2C frequency, f_{I2C}				1	MHz
Supply noise(1)	$V_{(VDD33)}$			100	mV_{P-P}
	$V_{(VDDIO)}$ = 3.3 V			100	mV_{P-P}
	$V_{(VDDIO)}$ = 1.8 V			50	mV_{P-P}
	$V_{(VDD12)}$			25	mV_{P-P}

(1) DC to 50 MHz.

6.4 Thermal Information

THERMAL METRIC(1)		DS90UH948-Q1 NKD (WQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
P_T	Total power consumption, normal operation	PCLK = 170 MHz. 2-lane FPD-Link III input, dual-link OLDI output	VDD		858	1146	mW
P_Z	Total power consumption, power-down mode	PDB = 0 V	VDD		40	70	mW
SUPPLY CURRENT							
IDD12	Supply current, normal operation	PCLK = 170 MHz. 2-lane FPD-Link III input, dual-link OLDI output	VDD12 = 1.2 V		169	223	mA
IDD33	Supply current, normal operation	PCLK = 170 MHz. 2-lane FPD-Link III input, dual-link OLDI output	VDD33 = 3.6 V		168	222	mA
IDDIO	Supply current, normal operation	PCLK = 170 MHz. 2-lane FPD-Link III input, dual-link OLDI output	VDDIO = 1.89 V or 3.6 V		14	19	mA
IDD12	Supply current, normal operation	PCLK = 192 MHz 2-lane FPD-Link III input, dual link OLDI Output	VDD12 = 1.2 V		189		mA
IDD33	Supply current, normal operation	PCLK = 192 MHz 2-lane FPD-Link III input, dual link OLDI Output	VDD33 = 3.6 V		188		mA
IDDIO	Supply current, normal operation	PCLK = 192 MHz 2-lane FPD-Link III input, dual link OLDI Output	VDDIO = 1.89 V or 3.6 V		16		mA
IDD12Z	Supply current, power-down mode	PDB = 0 V	VDD12 = 1.2 V		2	30	mA
IDD33Z	Supply current, power-down mode	PDB = 0 V	VDD33 = 3.6 V		2	8	mA
IDDIOZ	Supply current, power-down mode	PDB = 0 V	VDDIO = 1.89 V or 3.6 V		0.1	1	mA
3.3-V LVCMOS I/O ($V_{(VDDIO)}$ = 3.3 V ± 10%)							

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6.5 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage		PDB, BISTEN	2		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.8	V
V_{IH}	High level input voltage		BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	2		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or $V_{(VDDIO)}$		–10		10	µA
$I_{IN-STRAP}$	Strap pin input current	V_{IN} = 0V or $V_{(VDD33)}$	IDX, MODE_SEL0, MODE_SEL1	-1		1	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA	BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	2.4		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		0		0.4	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			–55		mA
I_{OZ}	Tri-state output current	PDB = 0 V V_{OUT} = 0 V or $V_{(VDDIO)}$		–20		20	µA
C_{IN}	Input capacitance					10	pF
1.8-V LVCMOS I/O ($V_{(VDDIO)}$ = 1.8 V ± 5%)							
V_{IH}	High level input voltage		PDB, BISTEN	1.5		$V_{(VDDIO)}$	V
V_{IL}	High level input voltage			0		0.35 × $V_{(VDDIO)}$	V
V_{IH}	High level input voltage		BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	0.65 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.35 × $V_{(VDDIO)}$	V
I_{IN}	Input current	V_{IN} = 0V or $V_{(VDDIO)}$		–10		10	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA		$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		0		0.45	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			–35		mA
I_{OZ}	Tri-state output current	PDB = 0 V V_{OUT} = 0 V or $V_{(VDDIO)}$		–20		20	µA
C_{IN}	Input capacitance					10	pF
SERIAL CONTROL BUS ($V_{(VDDIO)}$ = 1.8 V ± 5% OR 3.3V ±10%)							
V_{IH}	Input high level	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	I2C_SDA, I2C_SCL	2		$V_{(VDDIO)}$	V
V_{IL}	Input low level			0		0.9	V
V_{IH}	Input high level	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		1.58		$V_{(VDDIO)}$	V
V_{IL}	Input low level			GND		0.9	V
V_{HYS}	Input hysteresis				50		mV
V_{OL}	Output low level	I_{OL} = 4 mA		0		0.4	V
I_{IN}	Input current	V_{IN} = 0 V or $V_{(VDDIO)}$		–10		10	µA

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6.5 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III INPUT							
V_{TH}	Differential threshold high voltage	V_{CM} = 2.1 V	RIN0+, RIN0– RIN1+, RIN1–			50	mV
V_{TL}	Differential threshold low voltage			–50			mV
V_{ID}	Input differential threshold			100			mV
V_{CM}	Differential common-mode voltage				2.1		V
R_T	Internal termination resistor - differential			80	100	120	Ω
LVDS DRIVER							
V_{OD}	Output voltage swing (differential)	R_L =100 Ω, VOD Setting 1. See 図 6-9. See セクション 7.7 Register 0x4B for configuration details.	D0±, D1±, D2±, D3±, D4±, D5±, D6±, D7±, CLK1±, CLK2±	220	380	540	mV_{P-P}
		R_L =100 Ω, VOD Setting 2. See 図 6-9. See セクション 7.7 Register 0x4B for configuration details.		370	550	730	mV_{P-P}
		R_L = 100 Ω, VOD Setting 3. See 図 6-9. See セクション 7.7 Register 0x4B for configuration details.		460	650	840	mV_{P-P}
		R_L = 100 Ω, VOD Setting 4. See 図 6-9. See セクション 7.7 Register 0x4B for configuration details.		530	750	970	mV_{P-P}
ΔV_{OD}	Change in V_{OD} between complementary output states	R_L = 100 Ω			1	50	mV
V_{OS}	Offset voltage	R_L = 100 Ω. See 図 6-9.		1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary Output States	R_L = 100 Ω			1	50	mV
I_{OS}	Output short-circuit current				-20		mA
I_{OZ}	Output tri-state LVDS driver current	PDB = 0 V		–500		500	µA
LOOP-THROUGH MONITOR OUTPUT							
V_{OD}	Differential output voltage	R_L = 100 Ω	CMLOUTP, CMLOUTN		360		mV

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6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO BIT RATE							
$R_{b,FC}$	Forward channel bit rate	Single OLDI output, OLDI Clock = 25 to 96 MHz	GPIO[3:0]		0.25 × OLDI Clock		Mbps
		Dual OLDI output, OLDI Clock = 25 to 85 MHz			0.25 × OLDI Clock		Mbps
$R_{b,BC}$	Back channel bit rate				133		kbps
$R_{b,BC}$	Back channel bit rate	High speed (2-lane mode), 1 D_GPIO active See 表 7-3	D_GPIO[3:0]		2		Mbps
		High speed (2-lane mode), 2 D_GPIOs active See 表 7-3.			1.33		Mbps
		High speed (2-lane mode), 4 D_GPIOs active See 表 7-3			800		kbps
		Normal mode — see 表 7-3			133		kbps
$t_{GPIO,FC}$	GPIO pulse width, forward channel		GPIO[3:0]	> 2 / OLDI Clock			s
$t_{GPIO,BC}$	GPIO pulse width, back channel		GPIO[3:0]	20			µs
RESET							
t_{LRST}	PDB reset low pulse		PDB	2			ms
LOOP-THROUGH MONITOR OUTPUT							
E_W	Differential output eye opening width	R_L = 100 Ω, jitter frequency >OLDI Clock / 40 See 図 6-2	CMLOUTP, CMLOUTN		0.4		UI(3)
E_H	Differential output eye height				300		mV
I2S TRANSMITTER							
$t_{J,I2S}$	Clock output jitter		I2S_CLK		2		ns
t_{I2S}	I2S clock period(1)	See 図 6-12			>2 / OLDI Clock or >77		ns
$t_{HC,I2S}$	I2S clock high time(1)	See 図 6-12			0.48		t_{I2S}
$t_{LC,I2S}$	I2S clock low time(1)	See 図 6-12			0.48		t_{I2S}
$t_{SR,I2S}$	I2S set-up time	See 図 6-12	I2S_DA, I2S_DB, I2S_DC, I2S_DD		0.4		t_{I2S}
$t_{HR,I2S}$	I2S hold time	See 図 6-12			0.4		t_{I2S}

(1) I2S specifications for $t_{LC,I2S}$ and $t_{HC,I2S}$ pulses must each be greater than 1 OLDI clock period to ensure sampling and supersedes the 0.35 × t_{I2S} requirement. $t_{LC,I2S}$ and $t_{HC,I2S}$ must be longer than the greater of either 0.35 × t_{I2S} or 2 × OLDI Clock.
(2) PCLK refers to the equivalent pixel clock frequency, which is equal to the FPD-Link III line rate / 35.
(3) UI – Unit Interval is equivalent to one serialized data bit width. For Single Lane mode 1UI = 1 / (35 × PCLK). For Dual Lane mode, 1UI = 1 / (35 × PCLK / 2). The UI scales with PCLK frequency.

6.7 Timing Requirements for the Serial Control Bus

Over I²C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	> 0	100	kHz
		Fast mode	> 0	400	kHz
		Fast plus mode	> 0	1	MHz
t_{LOW}	SCL low period	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast plus mode	0.5		µs
t_{HIGH}	SCL high period	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition 図 6-11	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{SU;STA}$	Set-up time for a start or a repeated start condition 図 6-11	Standard mode	4.7		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{HD;DAT}$	Data hold time 図 6-11	Standard mode	0		µs
		Fast mode	0		µs
		Fast plus mode	0		µs
$t_{SU;DAT}$	Data set-up time 図 6-11	Standard mode	250		ns
		Fast mode	100		ns
		Fast plus mode	50		ns
$t_{SU;STO}$	Set-up time for STOP condition 図 6-11	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
t_{BUF}	Bus free time between STOP and START 図 6-11	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast plus mode	0.5		µs
t_r	SCL and SDA rise time, 図 6-11	Standard mode		1000	ns
		Fast mode		300	ns
		Fast plus mode		120	ns
t_f	SCL and SDA fall time, 図 6-11	Standard mode		300	ns
		Fast mode		300	ns
		Fast plus mode		120	ns
C_b	Capacitive load for each bus line	Standard mode		400	pF
		Fast mode		400	pF
		Fast plus mode		200	pF
t_{SP}	Input filter	Fast mode		50	ns
		Fast plus mode		50	ns

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6.8 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
LVDS DRIVER SWITCHING CHARACTERISTICS							
t_{LVLHT}	LVDS low-to-high transition time	20% to 80% transition, 5-pF load See 図 6-8	D0±, D1±, D2±, D3±, D4±, D5±, D6±, D7±, CLK1±, CLK2±		0.15	0.25	ns
t_{LVHLT}	LVDS high-to-low transition time	80% to 20% transition, 5-pF load See 図 6-8			0.15	0.25	ns
t_{BIT}	Transmitter output bit width	T = 1 / OLDI clock frequency. See 図 6-10			1/7 × T		ns
t_{PPOS0}	Transmitter output pulse positions normalized for Bit 0				1		UI(1)
t_{PPOS1}	Transmitter output pulse positions normalized for Bit 1				2		UI(1)
t_{PPOS2}	Transmitter output pulse positions normalized for Bit 2				3		UI(1)
t_{PPOS3}	Transmitter output pulse positions normalized for Bit 3				4		UI(1)
t_{PPOS4}	Transmitter output pulse positions normalized for Bit 4				5		UI(1)
t_{PPOS5}	Transmitter output pulse positions normalized for Bit 5				6		UI(1)
t_{PPOS6}	Transmitter output pulse positions normalized for Bit 6				7		UI(1)
t_{PPOS}	Transmitter output pulse positions (Bit 6 - Bit 0) normalized				< 0.1		UI(1)
t_{CCS}	Channel-to-channel skew				100		ps
t_{JCC}	Transmitter jitter cycle-to-cycle	2-lane FPD-Link III input, dual openLDI output			0.16		UI(1)
		2-lane FPD-Link III input, single OpenLDI Output			0.18		UI(1)
		1-lane FPD-Link III input, dual openLDI output			0.04		UI(1)
		1-lane FPD-Link III input, single openLDI output			0.04		UI(1)
t_{PDD}	Transmitter power-down delay	See 図 6-5			100		ns
t_{DD}	Deserializer propagation delay	T = 1 / OLDI Clock frequency. See 図 6-4			147 × T		ns

(1) UI - Unit Interval is equal to 1 / (7 × OLDI clock).

6.9 Timing Diagrams and Test Circuits

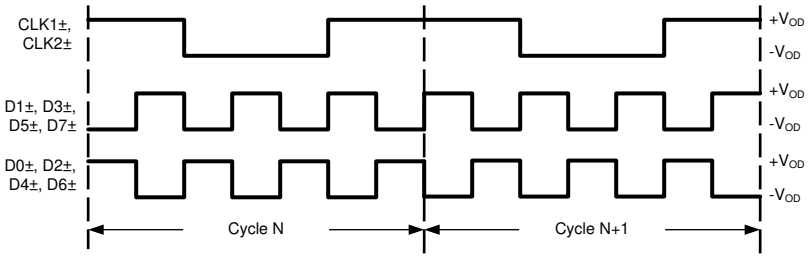

図 6-1. Checkerboard Data Pattern

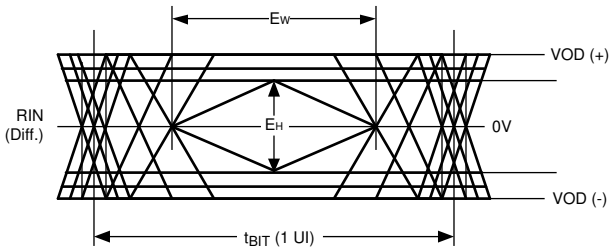

図 6-2. CML Output Driver

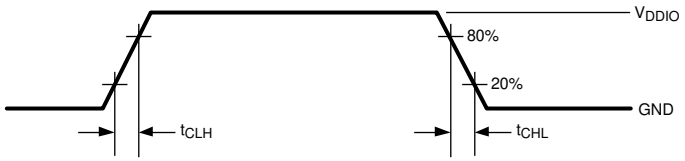

図 6-3. LVCMOS Transition Times

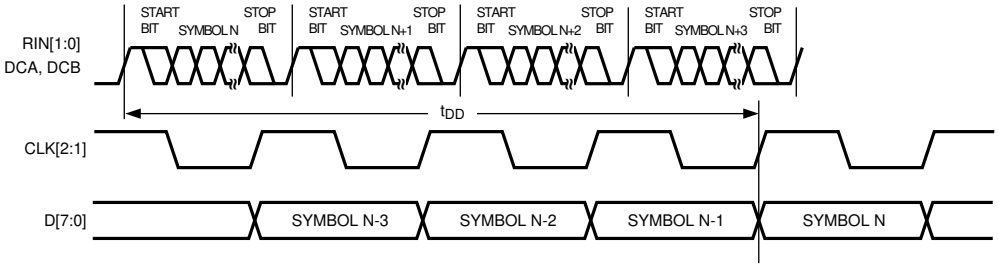

図 6-4. Latency Delay

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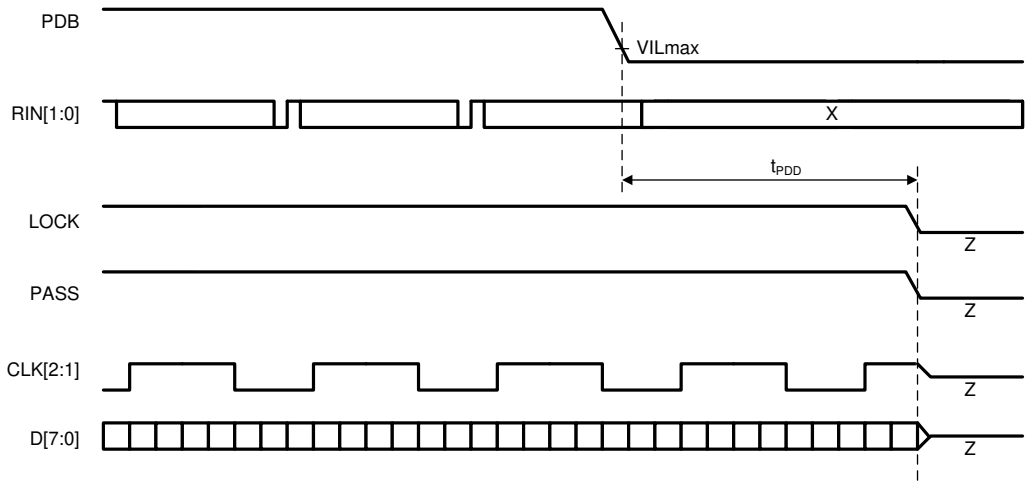

図 6-5. FPD-Link and LVCMOS Power Down Delay

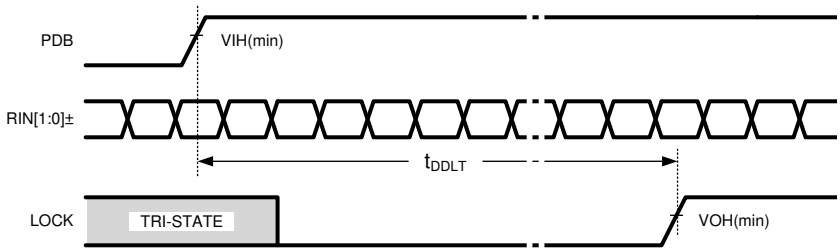

図 6-6. CML PLL Lock Time

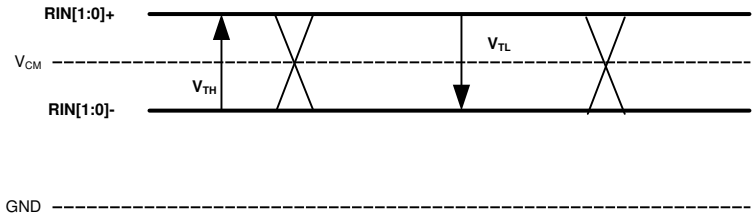

図 6-7. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

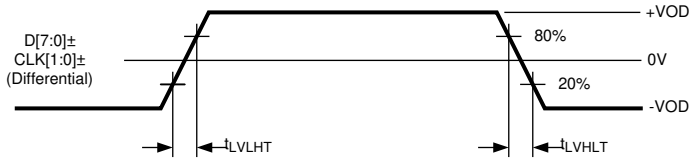

図 6-8. Input Transition Times

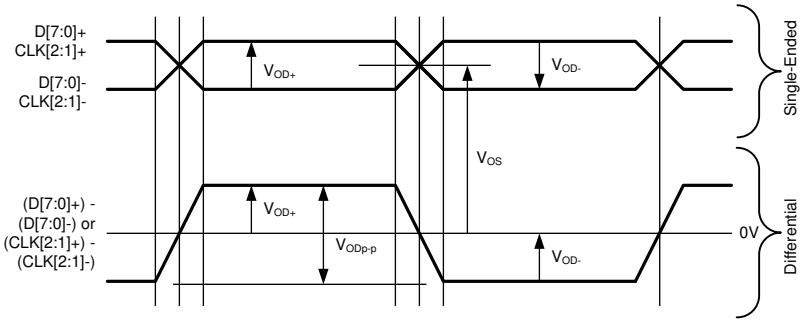

図 6-9. FPD-Link Single-Ended and Differential Waveforms

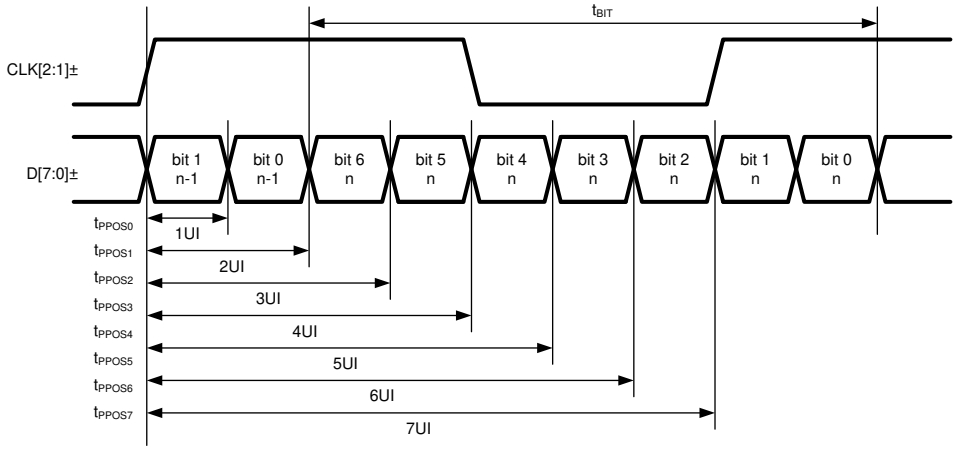

図 6-10. FPD-Link Transmitter Pulse Positions

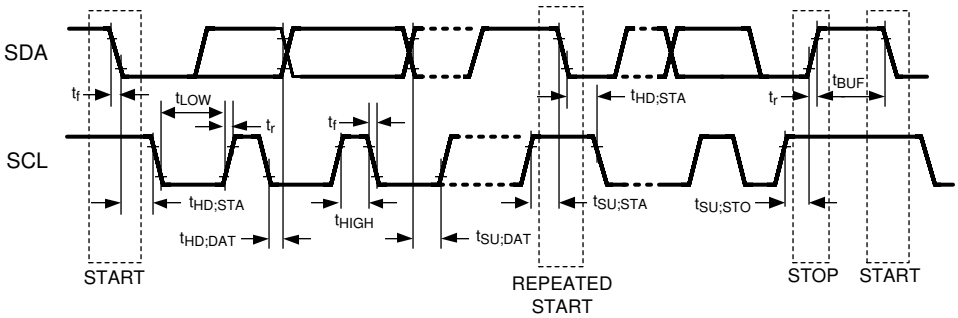

図 6-11. Serial Control Bus Timing Diagram

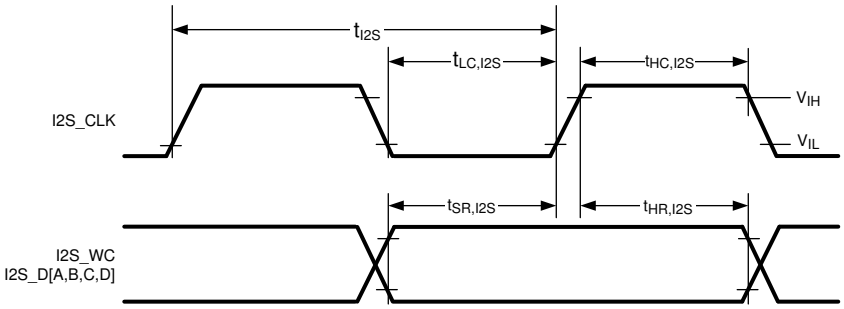

図 6-12. I2S Timing

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6.10 Typical Characteristics

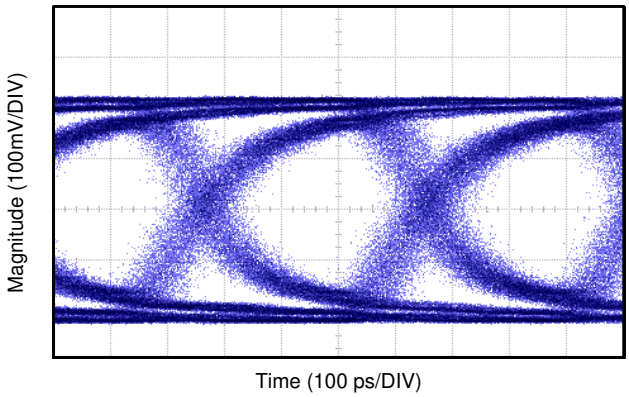

図 6-13. Deserializer Eye Diagram With 2.6-Gbps FPD-Link III Rate

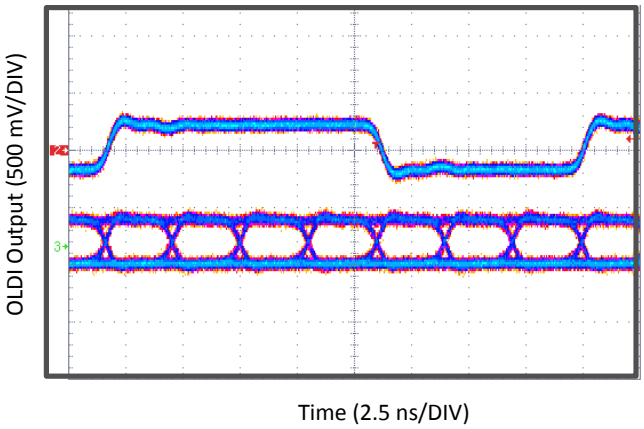

図 6-14. OpenLDI Output With 96-MHz Clock

7 Detailed Description

7.1 Overview

The DS90UH948-Q1 receives a 35-bit symbol over single or dual serial FPD-Link III pairs operating at up to 3.36 Gbps line rate in 1-lane FPD-Link III mode and 2.975 Gbps per lane in 2-lane FPD-Link III mode. The DS90UH948-Q1 converts this stream into a single or dual FPD-Link Interface (4 LVDS data channels + 1 LVDS clock, or 8 LVDS data channels + 2 LVDS clocks). The FPD-Link III serial stream contains an embedded clock, video control signals, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

The DS90UH948-Q1 is compatible with the following serializers: DS90UH949-Q1, DS90UH949A-Q1, DS90UH947-Q1, DS90UH941AS-Q1, DS90UH925Q-Q1, DS90UH927Q-Q1, DS90UH929-Q1, DS90UB921-Q1

The DS90UH948-Q1 deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. It also applies decryption through a high-bandwidth digital content protection (HDCP) Cipher to this video and audio data stream following reception of the data from the FPD-Link III decoder. On-chip non-volatile memory stores the HDCP keys. All key exchange is done through the FPD-Link III bidirectional control interface. The decrypted OpenLDI LVDS video interface is provided to the display.

The DS90UH948-Q1 deserializer incorporates an I2C-compatible interface. The I2C-compatible interface allows programming of serializer or deserializer devices from a local host controller. The devices also incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C Target devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C-compatible Controllers at either side of the serial link.

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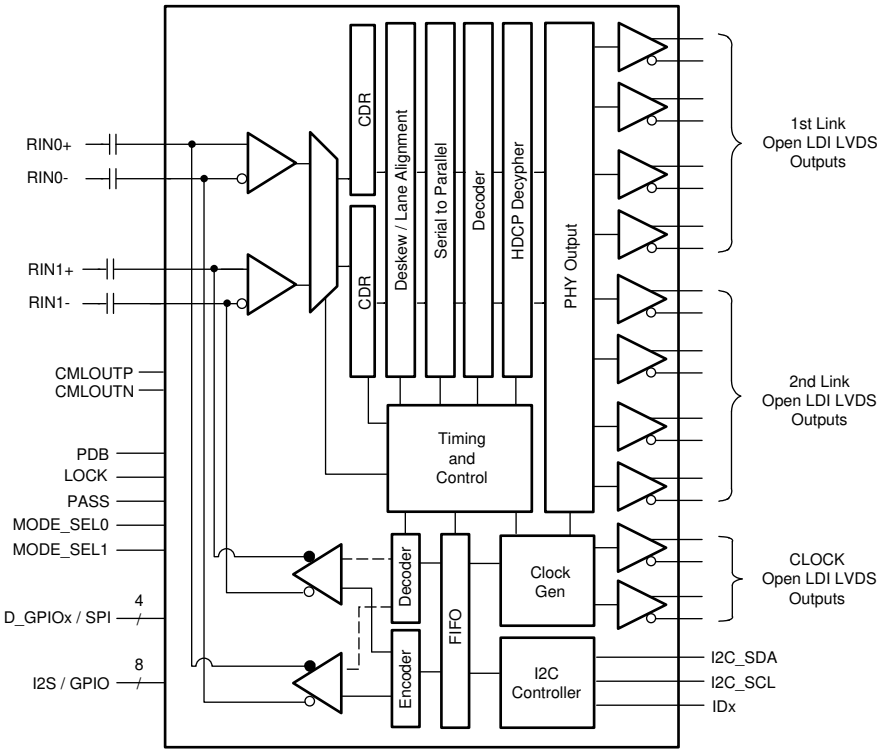
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Speed Forward Channel Data Transfer

The high-speed forward channel is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. 図 7-1 shows the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced, and scrambled.

図 7-1. FPD-Link III Serial Stream

The DS90UH948-Q1 supports clocks in the range of 25 MHz to 96 MHz over 1 lane, or 50 MHz to 192 MHz over 2 lanes. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum).

7.3.2 Low-Speed Back Channel Data Transfer

The Low-Speed Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, HDCP, CRC and 4 bits of standard GPIO information with 5-Mbps, 10Mbps, or 20-Mbps line rate (configured by MODE_SEL1 and/or register 0x23).

7.3.3 FPD-Link III Port Register Access

Because the DS90UH948-Q1 contains two ports, some registers must be duplicated to allow control and monitoring of the two ports. To facilitate this, PORT1_SEL and PORT0_SEL bits (0x34[1:0]) register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) are available independent of the settings in the PORT_SEL register.

Setting the PORT1_SEL and PORT0_SEL bit allows a read of the register for the selected port. If both bits are set, port1 registers are returned. Writes occur to ports for which the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

7.3.4 Oscillator Output

The deserializer provides an optional CLK[2:1]± output when the input clock (serial stream) has been lost. This is based on an internal oscillator and may be controlled from register 0x02, bit 5 (OSC Clock Output Enable). See *セクション 7.7*.

7.3.5 Clock and Output Status

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is tri-state or LOW (depending on the value of the OUTPUT ENABLE setting). After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVCMOS and LVDS outputs. The state of the outputs is based on the OUTPUT ENABLE and OUTPUT SLEEP STATE SELECT register settings. See register 0x02 in *セクション 7.7*.

表 7-1. Output State Table

INPUTS				OUTPUTS		
Serial INPUT	PDB	OUTPUT ENABLE Reg 0x02 [7]	OUTPUT SLEEP STATE SELECT Reg 0x02 [4]	LOCK	Data GPIO / D_GPIO I2S	D[7:0] / CLK[2:1]
X	L	X	X	Z	Z	Z
X	H	L	L	L	L	L
X	H	L	H	L or H	Z	Z
Static	H	H	L	L	L	L/OSC (Register EN)
Static	H	H	H	L	L	L
Active	H	H	L	L	L	L
Active	H	H	H	H	Valid	Valid

7.3.6 LVCMOS VDDIO Option

The 1.8-V or 3.3-V inputs and outputs are powered from a separate VDDIO supply to offer compatibility with external system interface signals.

注

When configuring the VDDIO power supplies, all the single-ended data and control input pins for device must scale together with the same operating VDDIO levels.

7.3.7 Power Down (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the VDDIO, where VDDIO = 3 V to 3.6 V or VDD33. To save power, disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after VDD33 and VDDIO have reached final levels; no external components are required. This pin is preferred to drive PDB pin through microcontroller where the RC filter is optional. In the case of driven by the VDDIO = 3 V to 3.6 V or VDD33 directly, a 10-kΩ resistor to the VDDIO = 3 V to 3.6 V or VDD33 and a > 10-µF capacitor to the GND, are required (see 図 8-1).

7.3.8 Interrupt Pin — Functional Description and Usage (INTB_IN)

The INTB_IN pin is an active low interrupt input pin. The INTB_IN pin may act as an output driver and pull low when PDB is low. This interrupt signal, when configured, propagates to the paired serializer. Consult the appropriate serializer data sheet for details of how to configure this interrupt functionality.

1. On the serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN (pin 4) is set *LOW* by some downstream device.

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3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register.
5. A read to HDCP_ ISR clears the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the deserializer INTB_IN. This would be when the downstream device releases the INTB_IN (pin 4) on the deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

7.3.9 General-Purpose I/O (GPIO)

7.3.9.1 GPIO[3:0] and D_GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as GPIOs in either forward channel (outputs) or back channel (inputs) mode. GPIO and D_GPIO modes may be configured from the registers (表 7-11). The same registers configure either GPIO or D_GPIO, depending on the status of PORT1_SEL and PORT0_SEL bits (0x34[1:0]). D_GPIO operation requires 2-lane FPD-Link III mode. Consult the appropriate serializer data sheet for details on D_GPIO configuration. Note: if paired with a DS90UH925Q-Q1 serializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the serializer. To enable 18-bit mode, set serializer register 0x12[2] = 1. 18-bit mode is auto-loaded into the deserializer from the serializer. See 表 7-2 for GPIO enable and configuration.

表 7-2. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3 / D_GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2 / D_GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1 / D_GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0 / D_GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

The input value present on GPIO[3:0] or D_GPIO[3:0] may also be read from register or configured to local output mode (表 7-11).

7.3.9.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. The mode is controlled by register 0x43 (表 7-11). The back channel frequency can be controlled several ways:

1. Register 0x23[6] sets the divider that controls the back channel frequency based on the internal oscillator. 0x23[6] = 0 sets the divider to 4 and 0x23[6] = 1 sets the divider to 2. As long as BC_HS_CTL (0x23[4]) is set to 0, the back channel frequency is either 5 Mbps or 10 Mbps, based on this bit.
2. Register 0x23[4] enables the high-speed back channel. This can also be pin-strapped through MODE_SEL1 (see 表 7-3). This bit overrides 0x23[6] and sets the divider for the back channel frequency to 1. Setting this bit to 1 sets the back channel frequency to 20 Mbps.

The back channel frequency has variation of ±20%. Note: The back channel frequency must be set to 5 Mbps when paired with a DS90UH925Q-Q1, DS90UH921-Q1, DS90UH929-Q1, or DS90UH927Q-Q1. See 表 7-3 for details about configuring the D_GPIOs in various modes.

The HSCC modes replace normal back-channel signaling with dedicated GPIOs or SPI data, allowing greater bandwidth for those functions. The HSCC Modes are enabled by setting the HSCC_MODE field in the HSCC_CONTROL register 0x43[2:0] in the DS90UH948-Q1. The HSCC modes eliminate the normal signaling such as Device ID, Capabilities, and RX Lock detect. It is intended to be turned on after obtaining RX Lock in normal back channel mode. Hence, the serializer properly determines capabilities prior to HSCC mode initiation. HSCC mode prevents loading capabilities, and it should only be enabled after RX Lock is established.

表 7-3. Back Channel D_GPIO Effective Frequency

HSCC_MODE (0x43[2:0])	MODE	NUMBER OF D_GPIOs	SAMPLES PER FRAME	D_GPIO EFFECTIVE FREQUENCY(1) (kHz)			D_GPIOs ALLOWED
				5 Mbps BC(2)	10 Mbps BC(3)	20 Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst-case back channel frequency (–20%) and a 4×sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 & BC_HS_CTL = 0.
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 & BC_HS_CTL = 0.
(4) 20 Mbps corresponds to BC FREQ SELECT = X & BC_HS_CTL = 1.

7.3.9.3 GPIO Register Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See 表 7-4 for GPIO enable and configuration.

注

Local GPIO value may be configured and read either through local register access, or remote register access through the low-speed bidirectional control channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

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表 7-4. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO9	0x1A[3:0] = 0x1	Output, L
	0x1A[3:0] = 0x9	Output, H
	0x1A[3:0] = 0x3	Input, Read: 0x6F[1]
GPIO_REG8	0x21[7:4] = 0x1	Output, L
	0x21[7:4] = 0x9	Output, H
	0x21[7:4] = 0x3	Input, Read: 0x6F[0]
GPIO_REG7	0x21[3:0] = 0x1	Output, L
	0x21[3:0] = 0x9	Output, H
	0x21[3:0] = 0x3	Input, Read: 0x6E[7]
GPIO_REG6	0x20[7:4] = 0x1	Output, L
	0x20[7:4] = 0x9	Output, H
	0x20[7:4] = 0x3	Input, Read: 0x6E[6]
GPIO_REG5	0x20[3:0] = 0x1	Output, L
	0x20[3:0] = 0x9	Output, H
	0x20[3:0] = 0x3	Input, Read: 0x6E[5]
GPIO3	0x1F[3:0] = 0x1	Output, L
	0x1F[3:0] = 0x9	Output, H
	0x1F[3:0] = 0x3	Input, Read: 0x6E[3]
GPIO2	0x1E[7:4] = 0x1	Output, L
	0x1E[7:4] = 0x9	Output, H
	0x1E[7:4] = 0x3	Input, Read: 0x6E[2]
GPIO1	0x1E[3:0] = 0x1	Output, L
	0x1E[3:0] = 0x9	Output, H
	0x1E[3:0] = 0x3	Input, Read: 0x6E[1]
GPIO0	0x1D[3:0] = 0x1	Output, L
	0x1D[3:0] = 0x9	Output, H
	0x1D[3:0] = 0x3	Input, Read: 0x6E[0]

7.3.10 SPI Communication

The SPI control channel uses the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available: forward channel and reverse channel modes. In forward channel mode, the SPI Controller is located at the serializer, such that the direction of sending SPI data is in the same direction as the video data. In reverse channel mode, the SPI Controller is located at the deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI control channel can operate in a high-speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the Peripheral to the Controller on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the POCI pin can be ignored by the Controller.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

注

SPI cannot be used to access serializer or deserializer registers.

7.3.10.1 SPI Mode Configuration

SPI is configured over I2C using the high-speed control channel configuration (HSCC_CONTROL) register, 0x43 (*セクション 7.7*). HSCC_MODE (0x43[2:0]) must be configured for either high-speed, forward channel SPI mode (110) or high-speed, reverse channel SPI mode (111).

7.3.10.2 Forward Channel SPI Operation

In forward channel SPI operation, the SPI Controller located at the serializer generates the SPI clock (SPLK), Controller out / Peripheral in data (PICO), and active low Peripheral select (CS). The serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, PICO, and CS are each sent on data bits in the forward channel frame. At the deserializer, the SPI signals are regenerated using the pixel clock. To preserve setup and hold time, the deserializer holds POCI data while the SPLK signal is high. The deserializer also delays SPLK by one pixel clock relative to the PICO data, increasing setup by one pixel clock.

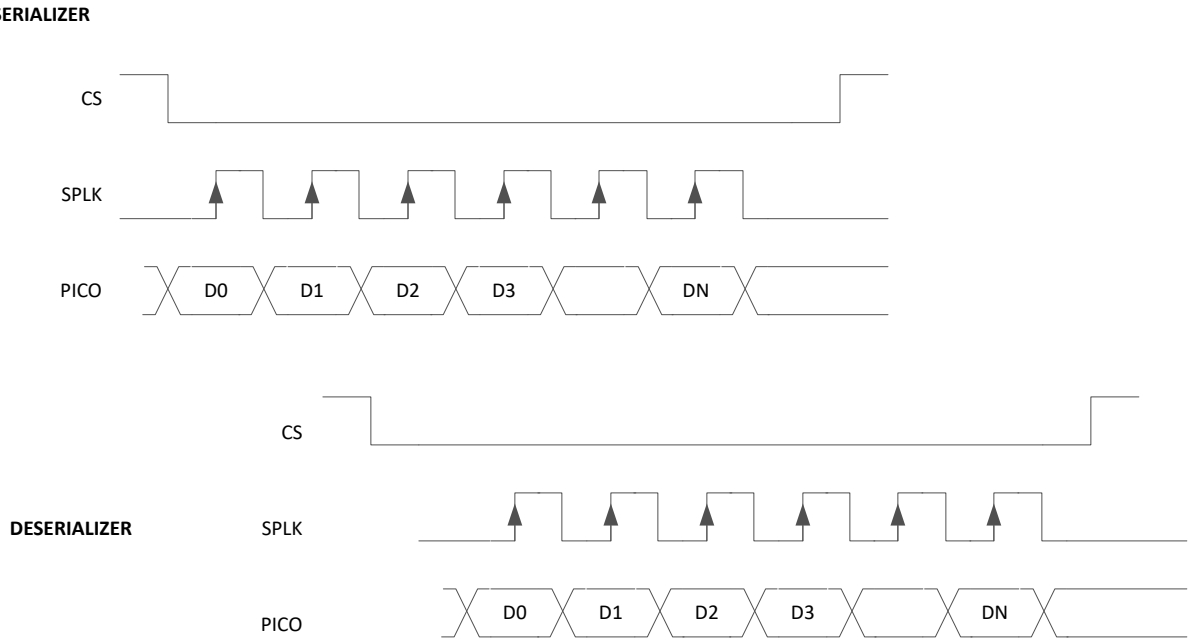

図 7-2. Forward Channel SPI Write

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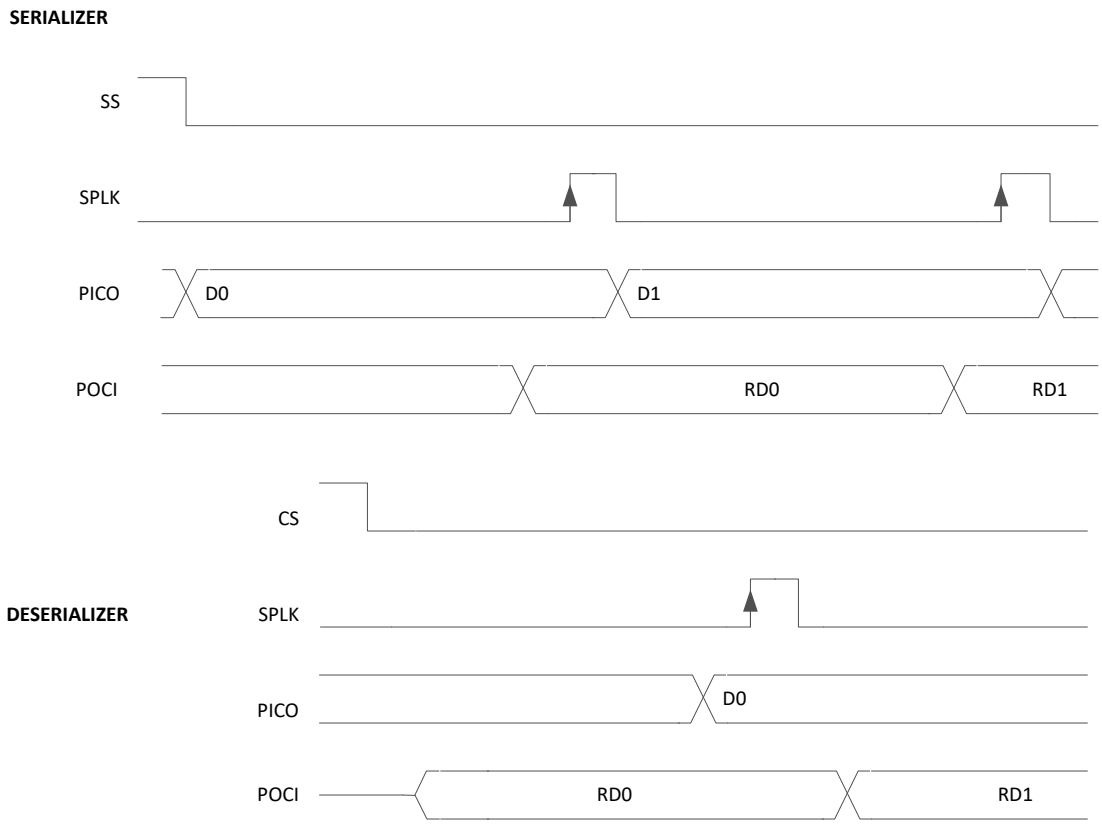

図 7-3. Forward Channel SPI Read

7.3.10.3 Reverse Channel SPI Operation

In reverse channel SPI operation, the deserializer samples the Peripheral select (CS), SPI clock (SCLK) into the internal oscillator clock domain. Upon detection of the active SPI clock edge, the deserializer also samples the SPI data (PICO). The SPI data samples are stored in a buffer to be passed to the serializer over the back channel. The deserializer sends SPI information in a back channel frame to the serializer. In each back channel frame, the deserializer sends an indication of the CS value. The CS must be inactive (high) for at least one back-channel frame period to ensure propagation to the serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. 図 7-4 shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the CS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

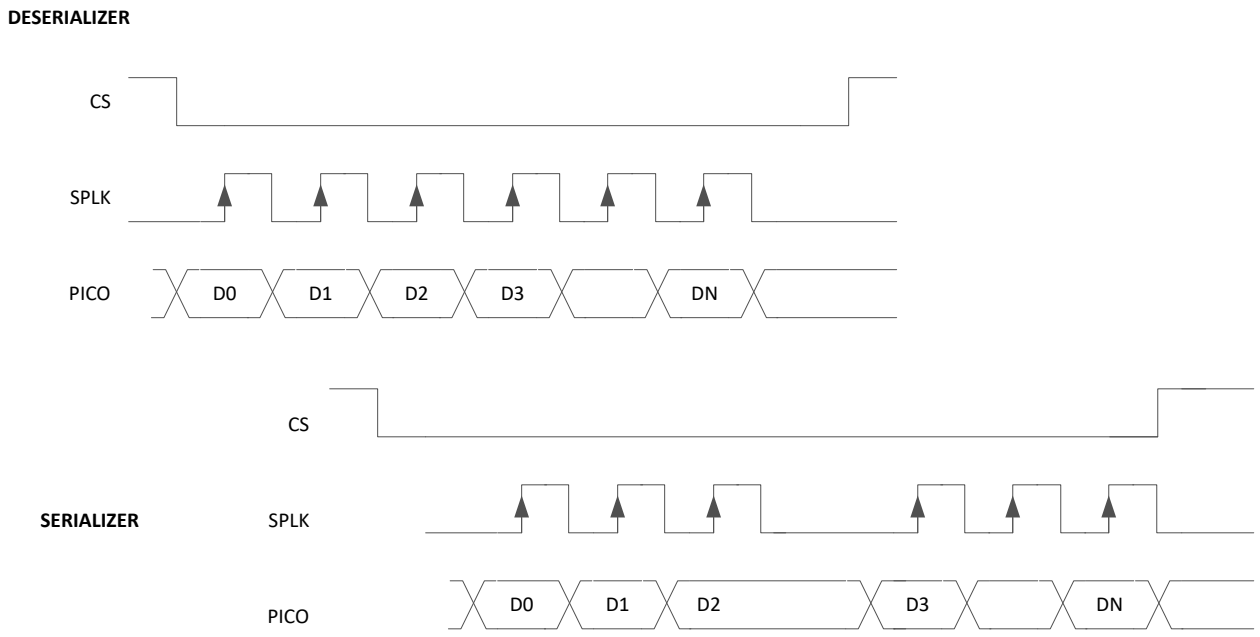

図 7-4. Reverse Channel SPI Write

For reverse channel SPI reads, the SPI Controller must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in forward channel mode. Note that at most one data/clock sample is sent per back channel frame.

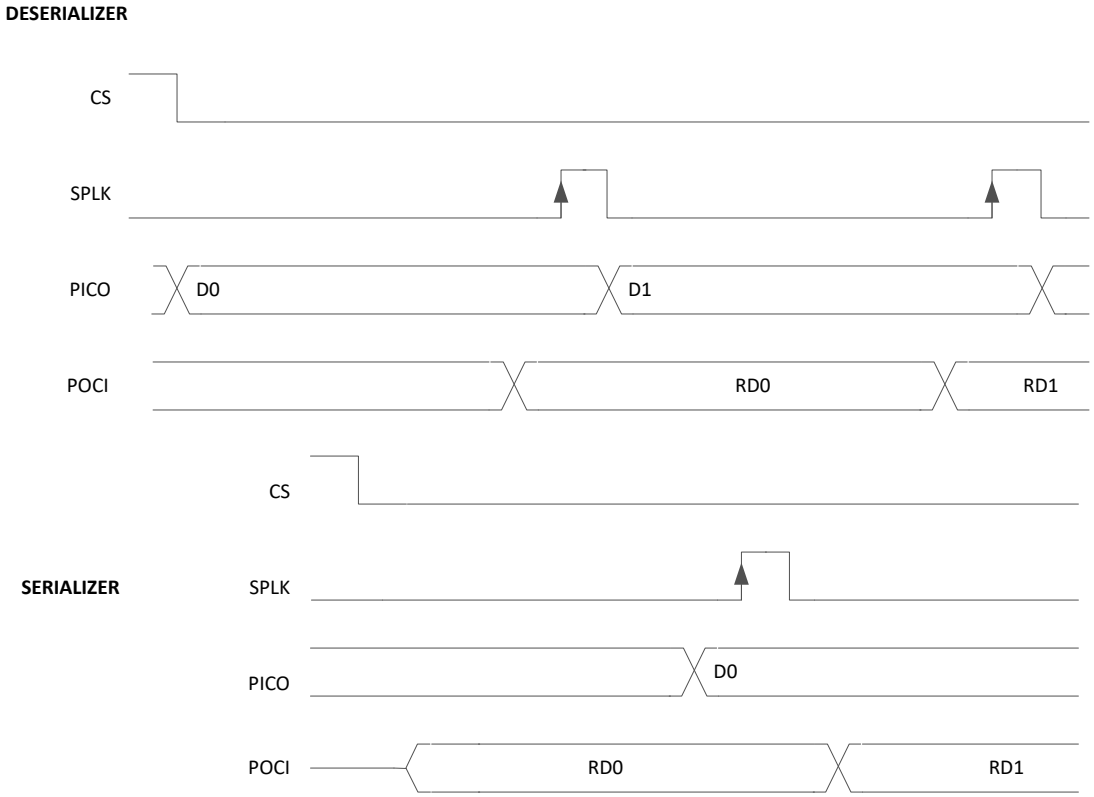

図 7-5. Reverse Channel SPI Read

For both reverse-channel SPI writes and reads, the SPI_CS signal must be deasserted for at least one back-channel frame period.

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表 7-5. SPI CS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

7.3.11 Backward Compatibility

The DS90UH948-Q1 is also backward compatible to the DS90UH925Q-Q1 and DS90UH927Q-Q1 for PCLK frequencies ranging from 25 MHz to 85 MHz or 25 MHz to 96 MHz when paired with DS90UB921-Q1 and DS90UH929-Q1. Backward compatibility does not need to be enabled. When paired with a backward-compatible device, the deserializer auto-detects to 1-lane FPD-Link III on the primary channel (RIN0±).

7.3.12 Adaptive Equalizer

The FPD-Link III receiver inputs incorporate an adaptive equalizer (AEQ) to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI), crosstalk, and so forth, must also be considered. The equalization configuration programmed in registers 0x35 (AEQ_CTL1) and 0x45 (AEQ_CTL2).

7.3.12.1 Transmission Distance

When designing the transmission channel, consider the total insertion loss of all components in the signal path between a serializer and a deserializer. An example of the transmission channel connects from a FPD-Link serializer (SER) to a deserializer would consist of a serializer PCB, two or more connectors, one or more cables, and a deserializer PCB as shown in 図 7-6

図 7-6. Typical Transmission Channel Components With Coaxial Cables

表 7-6 depicts the maximum attenuation using DS90UH948-Q1. The PCLK is the maximum frequency based on the channel attenuation. The attenuation increases with cable length and frequency. The trace length of the PCB has very small contribution to the differential insertion loss of the transmission channel. 表 7-6 shows the maximum attenuation that the AEQ can compensate for at the given PCLK and resultant Nuyquist frequency.

表 7-6. Insertion Loss

PCLK (MHz)	FPD-LINK LINE RATE (Gbps)	NYQUIST FREQUENCY (GHz)	CHANNEL ATTENUATION (dB)	TYP CABLE LENGTH (m)
170	2.97	1.48	-15	10
188	3.29	1.64	-12	7
192	3.36	1.68	-9	5

7.3.12.2 Adaptive Equalizer Algorithm

The AEQ process steps through allowed values of the equalizer controls find a value that allows the Clock Data Recovery (CDR) circuit to maintain valid lock condition. For each EQ setting, the circuit waits for a programmed re-lock time period, then checks results for valid lock. If valid lock is detected, the circuit will stop at the current EQ setting and maintain constant value as long as lock state persists. If the deserializer loses LOCK, the adaptive equalizer will resume the LOCK algorithm and the EQ setting is incremented to the next valid state.

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Once lock is lost, the circuit will continue searching EQ settings to find a valid setting to reacquire the serial data stream sent by the serializer that remains locked.

7.3.12.3 AEQ Settings

7.3.12.3.1 AEQ Start-Up and Initialization

The AEQ circuit can be restarted at any time by setting the AEQ_RESTART bit in the AEQ_CTL1 register 0x35. Once the deserializer is powered on, the AEQ is continually searching through EQ settings and could be at any setting when signal is supplied from the serializer. If the Rx Port CDR locks to the signal, it may be good enough for low bit errors, but could be not optimized or over-equalized. For a consistent initial EQ setting, TI recommends that the user applies AEQ_RESTART or DIGITAL_RESET0 when the serializer input signal frequency is stable to restart adaption from the minimum EQ gain value.

7.3.12.3.2 AEQ Range

The user can program the AEQ circuit with the minimum AEQ level setting used during the EQ adaption. Using the full AEQ range will provide the most flexible solution, however, if the channel conditions are known and an improved deserializer lock time can be achieved by narrowing the search window for allowable EQ gain settings. For example, in a system use case with a longer cable and multiple interconnects creating a higher channel attenuation, the AEQ would not adapt to the minimum EQ gain settings. In this case, starting the adaptation from a higher AEQ level would improve lock time. The AEQ range is determined by the AEQ_CTL2 register 0x45 where the ADAPTIVE_EQ_FLOOR_VALUE determines the starting value for EQ gain adaption. The maximum AEQ limit is not adjustable. To enable the minimum AEQ limit, OVERRIDE_AEQ_FLOOR and SET_AEQ_FLOOR bits in the AEQ_CTL1 register must also be set. The setting for the AEQ after adaption can be readback from the AEQ_STATUS register 0x3B.

7.3.12.3.3 AEQ Timing

The dwell time for AEQ to wait for either the lock or error-free status is also programmable. When checking each EQ setting, the AEQ will wait for a time interval, controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register (see *セクション 7.7*) before incrementing to the next allowable EQ gain setting. The default wait time is set to 2.62 ms. Once the maximum setting is reached, if there is no lock acquired during the programmed relock time, the AEQ will restart adaption at the minimum setting or AEQ_FLOOR value.

7.3.13 I2S Audio Interface

This deserializer features six I2S output pins that, when paired with a compatible serializer, support surround-sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the smaller of < PCLK/2 or < 13 MHz. Four I2S data outputs carry two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input.

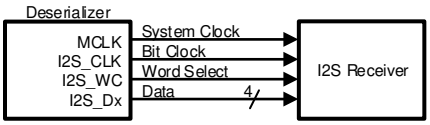

図 7-7. I2S Connection Diagram

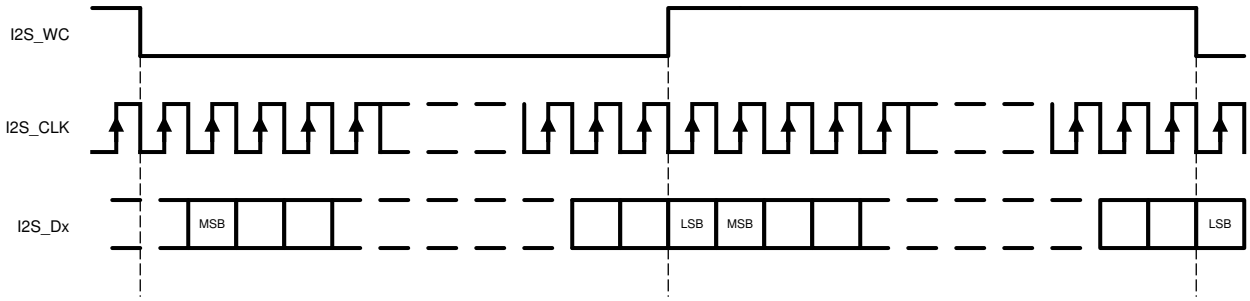

図 7-8. I2S Frame Timing Diagram

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When paired with a DS90UH925Q , the deserializer I2S interface supports a single I2S data output through I2S_DA (24-bit video mode) or two I2S data outputs through I2S_DA and I2S_DB (18-bit video mode).

7.3.13.1 I2S Transport Modes

By default, packetized audio is received during video blanking periods in dedicated data island transport frames. The transport mode is set in the serializer and auto-loaded into the deserializer by default. The audio configuration may be disabled from control registers if forward channel frame transport of I2S data is desired. In frame transport, only I2S_DA is received to the deserializer. Surround sound mode, which transmits all four I2S data inputs (I2S_D[D:A]), may only be operated in data island transport mode. This mode is only available when connected to a DS90UH927Q, DS90UH949-Q1, DS90UH947-Q1, or DS90UH929-Q1 serializer. If connected to a DS90UH925Q serializer, only I2S_DA and I2S_DB may be received.

There are two I2S transport modes:

Surround Sound (SS) Mode which is the standard 8-channel audio. In this case Audio source is on the Serializer side and uses I2S_DA/DB/DC/ DD pins to drive Audio into the serializer which show up on the Deserializer I2S_DA/DB/DC/DD outputs.

Auxiliary Audio (AA) Mode which is only relevant when the DS90UH948-Q1 is paired with DS90UH949-Q1 Serializer and Audio is send through AUX input of this Serializer.

7.3.13.2 I2S Repeater

I2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via data island transport on the FPD-Link interface during the video blanking periods. If frame transport is desired, connect the I2S pins from the deserializer to all serializers. Activating surround sound at the top-level serializer automatically configures downstream serializers and deserializers for surround-sound transport utilizing data island transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (*セクション 7.7*).

A DS90UH948-Q1 deserializer configured in repeater mode may also regenerate I2S audio from its I2S input pins in lieu of data island frames. See 図 7-11 and the I2C Control Registers (*セクション 7.7*) for additional details.

7.3.13.3 I2S Jitter Cleaning

This device features a standalone PLL to clean the I2S data jitter, supporting high-end car audio systems. If I2S_CLK frequency is less than 1MHz, this feature must be disabled through register 0x2B[7]. See the *セクション 7.7* section.

7.3.13.4 MCLK

The deserializer has an I2S MCLK output. It supports x1, x2, or x4 of I2S CLK frequency. When the I2S PLL is disabled, the MCLK output is off. 表 7-7 covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bits 0x3A[6:4] (I2S DIVSEL), shown in *セクション 7.7*. To select desired MCLK frequency, write 0x3A[7], then write to bit [6:4] accordingly.

表 7-7. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	16	1.024	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		1.4112	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
48		1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
96		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
192		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
32	24	1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		2.117	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		2.304	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		4.608	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		9.216	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	101

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表 7-7. Audio Interface Frequencies (continued)

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	32	2.048	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
44.1		2.8224	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		12.288	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	110

7.3.14 HDCP Repeater

The supported repeater application provides a mechanism to extend transmission over multiple links to multiple display devices.

7.3.14.1 HDCP

The HDCP cipher function is implemented in the deserializer per HDCP v1.4 specification. The DS90UH948-Q1 provides HDCP decryption of audiovisual content when connected to an HDCP capable FPD-Link III serializer. HDCP authentication and shared key generation is performed using the HDCP control channel, which is embedded in the forward and backward channels of the serial link. On-chip non-volatile memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

7.3.14.2 HDCP Repeater

The supported HDCP repeater application provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. It authenticates all HDCP devices in the system and distributes protected content to the HDCP receivers using the encryption mechanisms provided in the HDCP specification.

7.3.14.2.1 Repeater Configuration

In the HDCP repeater application, this document refers to the DS90UH947-Q1 as the HDCP transmitter (TX), and refers to the DS90UH948-Q1 as the HDCP receiver (RX). 図 7-9 shows the maximum configuration supported for HDCP repeater implementations. Two levels of HDCP repeaters are supported with a maximum of three HDCP Transmitters per HDCP receiver.

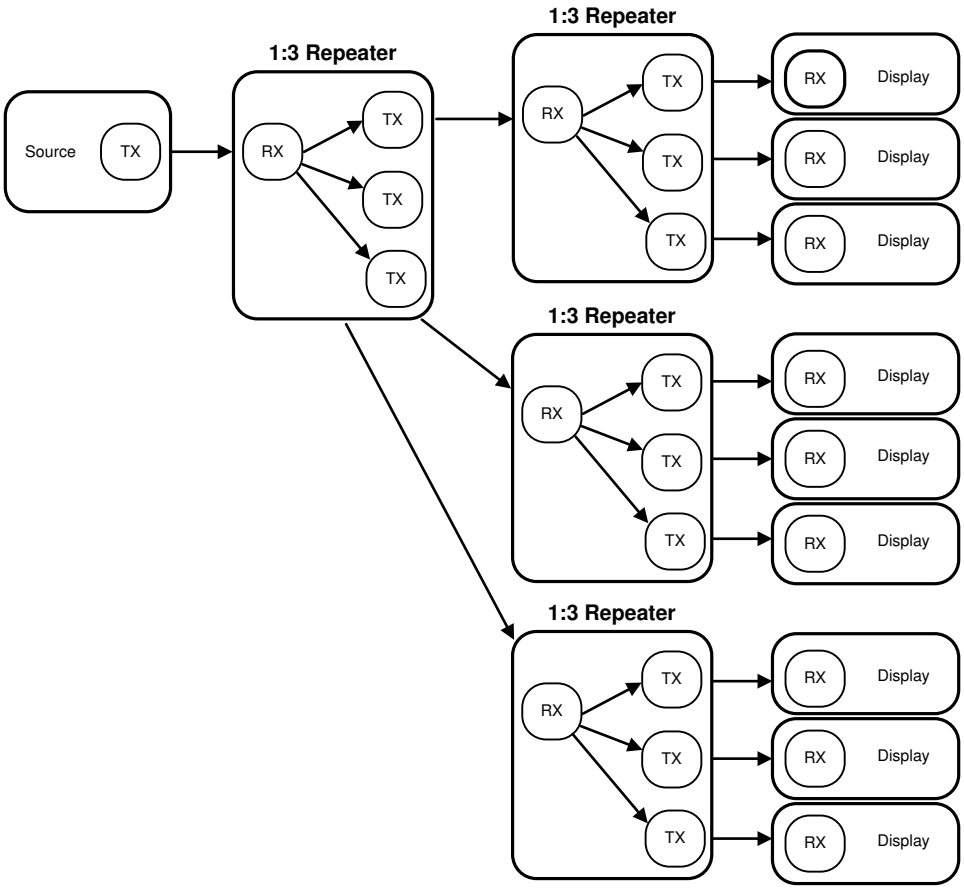

図 7-9. HDCP Maximum Repeater Application

In a repeater application, the I2C interface at each TX and RX is configured to transparently pass I2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Target Aliases) to downstream devices in the case of duplicate addresses.

To support HDCP repeater operation, the RX includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP receivers, and pass the KSV list to the upstream HDCP transmitter. An I2C Controller within the RX communicates with the I2C Target within the TX. The TX handles authenticating with a downstream HDCP Receiver and makes status available through the I2C interface. The RX monitors the transmit port status for each TX and reads downstream KSV and KSV list values from the TX.

In addition to the I2C interface used to control the authentication process, the HDCP repeater implementation includes two other interfaces. The FPD-Link LVDS interface outputs the unencrypted video data. In addition to providing the video data, the LVDS interface communicates control information and packetized audio data. All audio and video data is decrypted at the output of the HDCP receiver and is re-encrypted by the HDCP transmitter. 図 7-10 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

If the repeater node includes a local output to a display, white-balancing and Hi-FRC dithering functions must not be used as they will block encrypted I2S audio and HDCP authentication.

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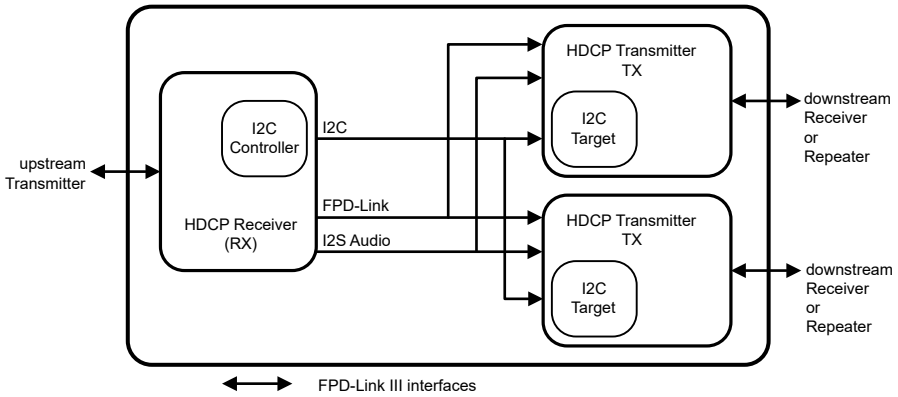

図 7-10. HDCP 1:2 Repeater Configuration

7.3.14.2.2 Repeater Connections

The HDCP repeater requires the following connections between the HDCP receiver and each HDCP Transmitter 図 7-11.

1. Video Data – Connect all FPD-Link data and clock pairs. Single FPD-Link (D[3:0]) or Dual FPD-Link (D[7:0]) are both possible, provided the Deserializer and all Serializers are configured in the same mode.
2. I2C – Connect SCL and SDA signals. Both signals must be pulled up to VDD33 or VDDIO = 3 V to 3.6 V with 4.7-kΩ resistors.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals. Audio is normally transported on the FPD-Link interface.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. MODE_SEL pins — All transmitters and receivers must be set into repeater mode. FPD-Link settings (single vs. dual) must also match.
6. Interrupt pin – Connect DS90UH948-Q1 INTB_IN pin to the DS90UH947-Q1 INTB pin. The signal must be pulled up to VDDIO with a 10-kΩ resistor.

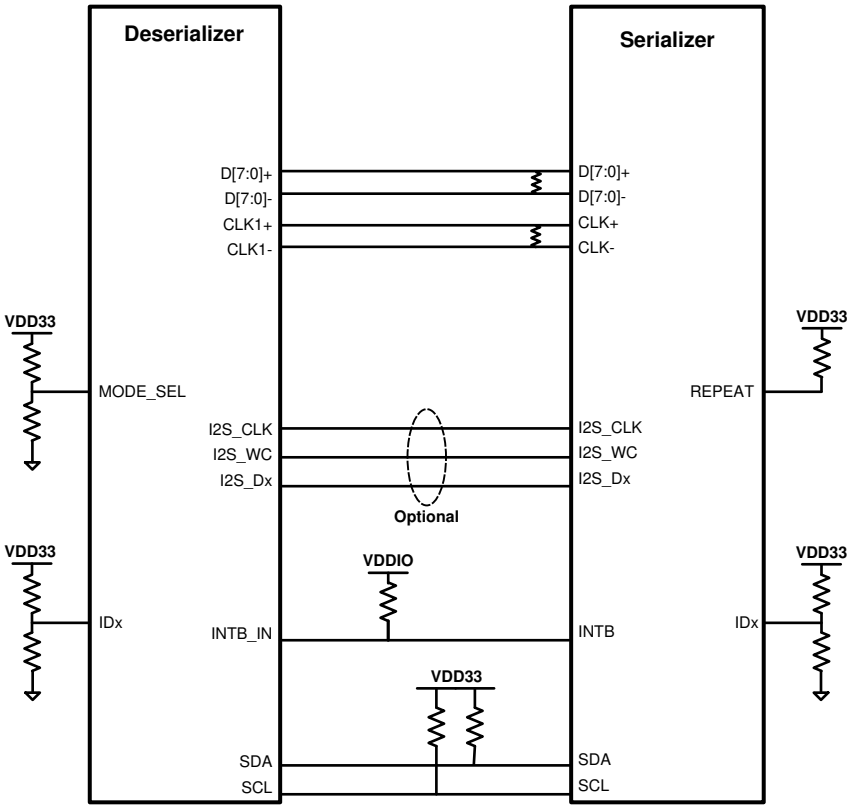

図 7-11. HDCP Repeater Connection Diagram

7.3.14.2.2.1 Repeater Fan-Out Electrical Requirements

Repeater applications requiring fan-out from one DS90UH948-Q1 deserializer to up to three DS90UH947-Q1 serializers requires special considerations for routing and termination of the FPD-Link differential traces. 図 7-12 details the requirements that must be met for each signal pair:

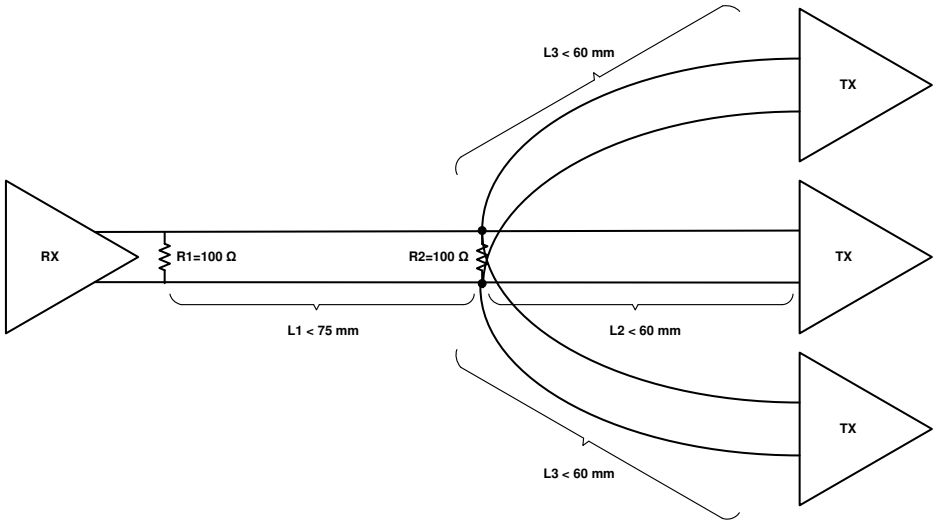

図 7-12. FPD-Link Fan-Out Electrical Requirements

7.3.14.2.2.2 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized data island transport audio is also encrypted along with the video

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data per HDCP v1.4. I2S audio transmitted in forward channel frame transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

7.3.15 Built-In Self Test (BIST)

An optional at-speed built-in self test (BIST) feature supports testing of the high-speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.15.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33-MHz internal oscillator clock (OSC) frequency in the serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

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If there is a loss of lock, then BIST error count will be reset.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or power down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See 図 7-13 for the BIST mode flow diagram.

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When BIST is disabled, AEQ will automatically increment to the next value. After BIST is complete it is suggested to perform an AEQ reset.

7.3.15.1.1 Sample BIST Sequence

Note: Before BIST can be enabled, D_GPIO0 (pin 19) must be strapped HIGH and D_GPIO[3:1] (pins 16, 17, and 18) must be strapped LOW.

1. BIST Mode is enabled through the BISTEN pin of deserializer. The desired clock source is selected through the deserializer BISTC pin.
2. The serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires LOCK, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin switches low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate per 35 bits.
3. To stop BIST mode, set the BISTEN pin LOW. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. 図 7-14 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, and so forth). Errors may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx equalization).

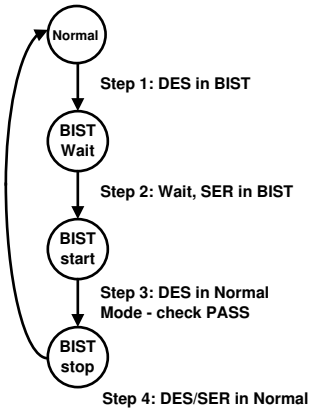

図 7-13. BIST Mode Flow Diagram

7.3.15.2 Forward Channel and Back Channel Error Checking

The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer. Forward channel errors may also be read from register 0x25 (*セクション 7.7*).

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - *セクション 7.7*). CRC errors are recorded in an 8-bit register in the serializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until either the error is cleared or the serializer enters BIST mode again.

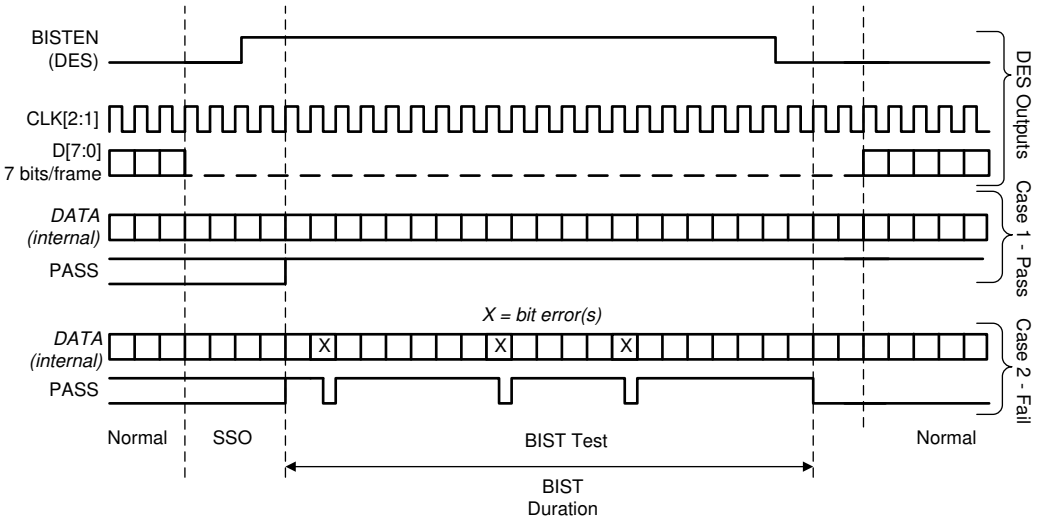

図 7-14. BIST Waveforms

7.3.16 Internal Pattern Generation

The deserializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern is displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to *Exploring the Int Test Pattern Generation Feature of FPDLink III IVI Devices* (SNLA132).

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Enabling PATGEN on the DS90UH948-Q1, using the internal clock, will cause loss of communication between the serializer and deserializer, so internal PATGEN from the DS90UH948-Q1 should only be enabled via local I2C access.

7.4 Device Functional Modes

7.4.1 Configuration Select MODE_SEL[1:0]

The DS90UH948-Q1 can be configured for several different operating modes via the MODE_SEL[1:0] input pins, or via the register bits 0x23 [4:2] (MODE_SEL1) and 0x49 (MODE_SEL0).

The DS90UH948-Q1 is capable of operating in either in 1-lane or 2-lane mode for FPD-Link III. By default, the FPD-Link III receiver automatically configures the input based on 1- or 2-lane mode operation. Programming register 0x34 [4:3] settings will override the automatic detection. For each FPD-Link III pair, the serial datastream is composed of a 35-bit symbol.

The DS90UH948-Q1 recovers the FPD-Link III serial datastream(s) and produces video data driven to the OpenLDI (LVDS) interface. OpenLDI single link and dual link are supported with color depths of 18 bits per pixel or 24 bits per pixel. There are 8 differential data pairs (D0 through D7) and two clock pairs (CLK1 and CLK2) on the OpenLDI interface. The number of data lines may vary, depending on the pixel formats supported. For single-link output the pixel clock is limited to 96 MHz. In the case of dual link, the pixel clock is limited to 192 MHz (or 96 MHz per LVDS port). When in a dual-link configuration, LVDS channels D0 to D3 carry ODD pixel data, and LVDS channels D4 to D7 carry EVEN pixel data.

The device can be configured in following modes:

- 1-lane FPD-Link III input, single-link OpenLDI output
- 1-lane FPD-Link III Input, Dual Link OpenLDI output
- 2-lane FPD-Link III Input, dual-link OpenLDI output
- 2-lane FPD-Link III Input, single-link OpenLDI output
- 2-lane FPD-Link III Input, single-link OpenLDI output (replicate)

7.4.1.1 1-Lane FPD-Link III Input, Single Link OpenLDI Output

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each LVDS data lane operates at a speed of 7 bits per LVDS clock cycle; resulting in a serial line rate of 175 Mbps to 672 Mbps. CLK1 operates at the same rate as PCLK with a duty cycle ratio of 57:43.

7.4.1.2 1-Lane FPD-Link III Input, Dual Link OpenLDI Output

The input RGB data is split into odd and even pixels starting with the ODD (first) pixel outputs D0 to D3 and then the EVEN (second) pixel outputs D4 to D7. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data.

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 50 MHz to 96 MHz, resulting in a link rate of 1.75 Gbps (35 bit × 50 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each LVDS data lane operates at a speed of 7 bits per 2 LVDS clock cycles, resulting in a serial line rate of 175 Mbps to 336 Mbps. CLK1 and CLK2 operate at half the rate as PCLK with a duty cycle ratio of 57:43.

7.4.1.3 2-Lane FPD-Link III Input, Dual Link OpenLDI Output

The input RGB data is split into odd and even pixels starting with the ODD (first) pixel outputs D0 to D3 and then the EVEN (second) pixel outputs D4 to D7. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data.

In this configuration the PCLK rate embedded within 2-lane FPD-Link III frame can range from 50 MHz to 192 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each LVDS data lane will operate at a speed of 7 bits per 2 LVDS clock cycles, resulting in a serial line rate of 175 Mbps to 672 Mbps. CLK1 and CLK2 operate at half the rate as PCLK with a duty cycle ratio of 57:43.

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7.4.1.4 2-Lane FPD-Link III Input, Single Link OpenLDI Output

In this configuration the PCLK rate embedded within 2-lane FPD-Link III frame can range from 50 MHz to 192 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each LVDS data lane will operate at a speed of 7 bits per LVDS clock cycle; resulting in a serial line rate of 350 Mbps to 1344 Mbps. CLK1 operates at the twice the rate as PCLK with a duty cycle ratio of 57:43.

7.4.1.5 1-Lane FPD-Link III Input, Single Link OpenLDI Output (Replicate)

Same as 1-lane FPD-Link III input, single-link OpenLDI output mode, and duplicates the LVDS signal on D4 to D7 outputs.

7.4.2 MODE_SEL[1:0]

Possible configurations are shown in 図 7-15. These are described above (*セクション 7.4.1*).

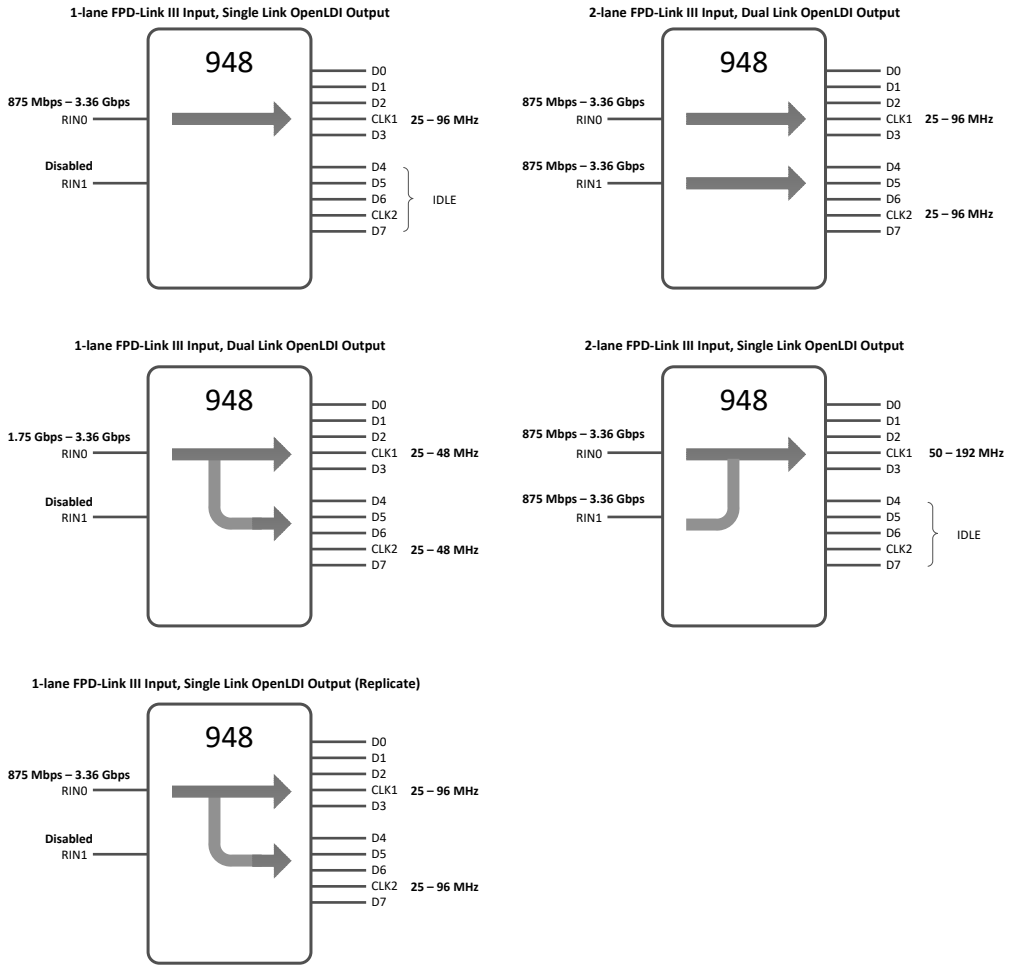

図 7-15. Data-Path Configurations

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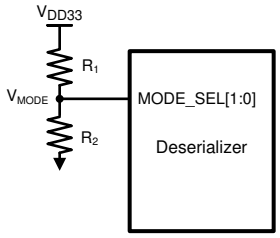

図 7-16. MODE_SEL[1:0] Connection Diagram

表 7-8. Configuration Select (MODE_SEL0)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% tolerance)		MAP_SEL	OUTPUT_MODE [1:0]	OUTPUT MODE
	V (TYP)	VDD33 = 3.3 V	R1 (kΩ)	R2 (kΩ)			
0	0	0	Open	10	0	00	Dual OLDI output
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	0	01	Dual SWAP output
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	0	10	Single OLDI output
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	0	11	Replicate
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	1	00	Dual OLDI output
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	1	01	Dual SWAP output
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	1	10	Single OLDI output
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	1	11	Replicate

表 7-9. Configuration Select (MODE_SEL1)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% tolerance)		REPEATER	MODE	HIGH-SPEED BACK CHANNEL	INPUT MODE
	V (TYP)	VDD33 = 3.3 V	R1 (kΩ)	R2 (kΩ)				
0	0	0	Open	10	0	00	5 Mbps	STP
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	0	01	5 Mbps	Coax
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	0	10	20 Mbps	STP
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	0	11	20 Mbps	Coax
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	1	00	5 Mbps	STP
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	1	01	5 Mbps	Coax
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	1	10	20 Mbps	STP
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	1	11	20 Mbps	Coax

7.4.2.1 Dual Swap

When operated in Dual OLDI output mode, the odd and even output channels (D0-3 and D4-7 respectively) can be swapped. This is configurable through MODE_SEL0 pin strapping (see table 7-8) and can be overridden via I2C using the FPD_TX_MODE register.

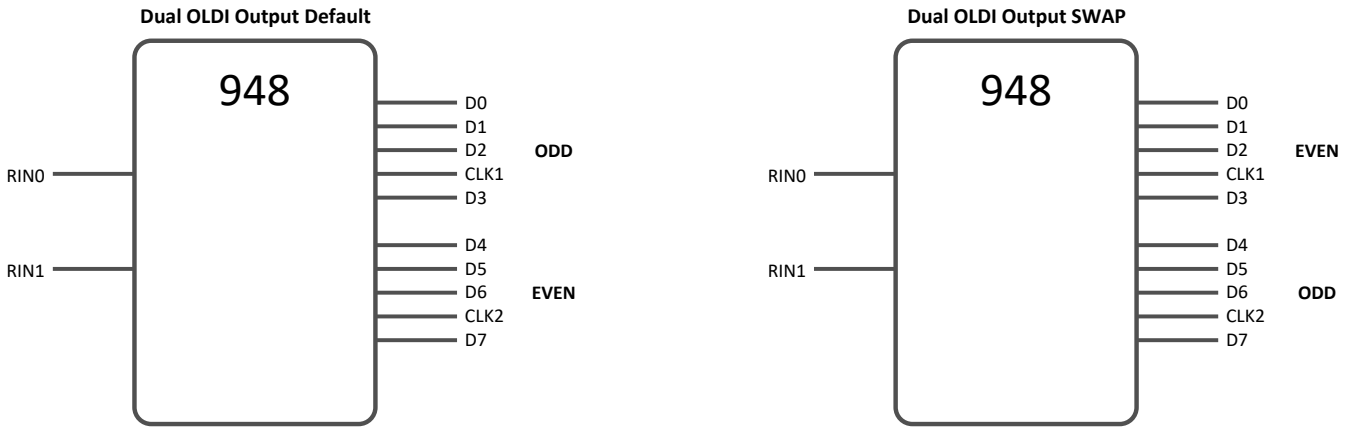

図 7-17. Dual oLDI Output SWAP

7.4.3 OpenLDI Output Frame and Color Bit Mapping Select

DS90UH948-Q1 can be configured to output 24-bit color (RGB888) or 18-bit color (RGB666) with 2 different mapping schemes, shown in 図 7-18 and 図 7-19. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock output from CLK1± and CLK2± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MODE_SEL0 pin or by Register (*セクション 7.7*).

表 7-10 lists common industry standard naming conventions for these LVDS bit mapping schemes.

表 7-10. LVDS Formats

	24 Bit Mode	18 Bit Mode
MAPSEL = H	OLDI/SPWG/VESA	4 Lane 18 Bit Mode
MAPSEL = L	JEIDA	Standard 18 bit

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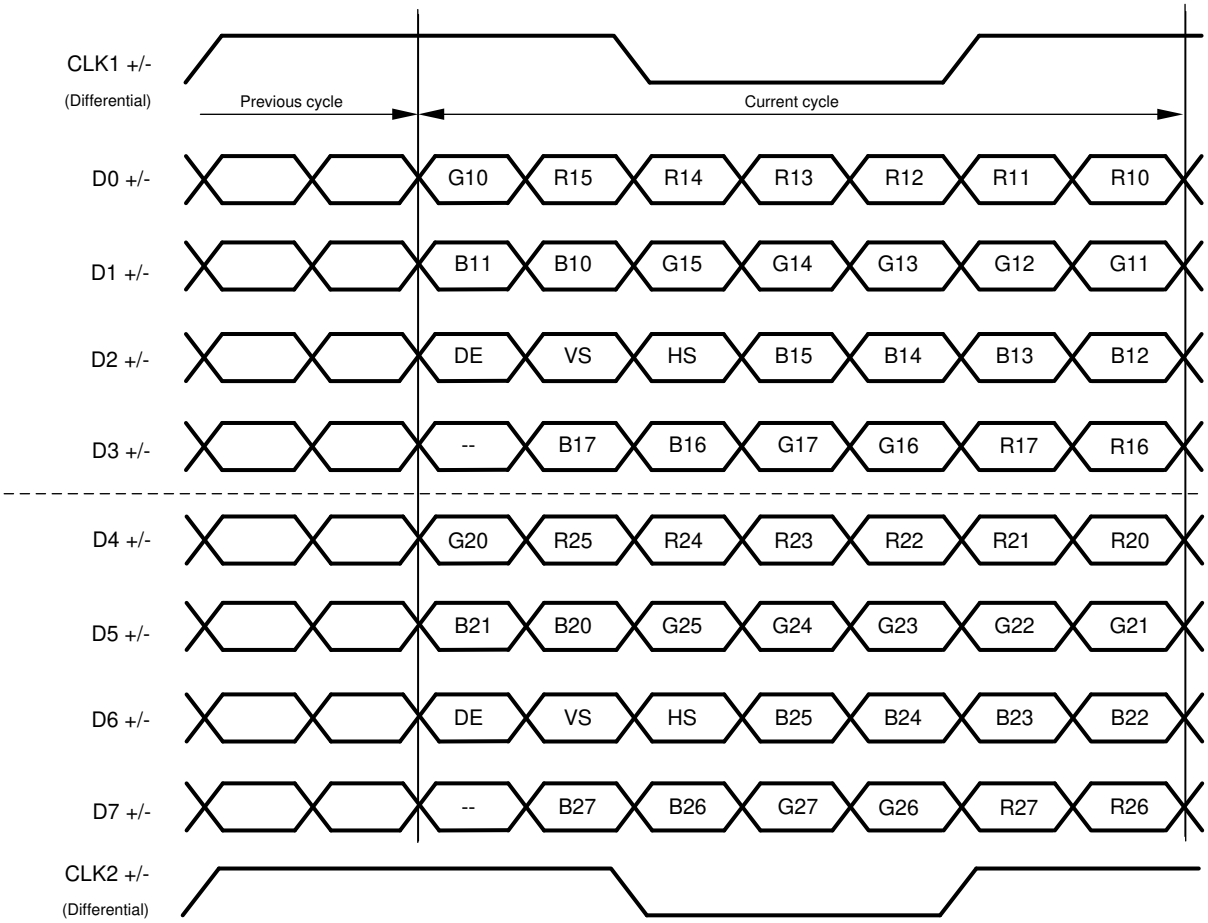

図 7-18. 24-Bit Color Dual FPD-Link Mapping: MSBs on D3/D7,"OLDI/SPWG/VESA" (MAPSEL = H)

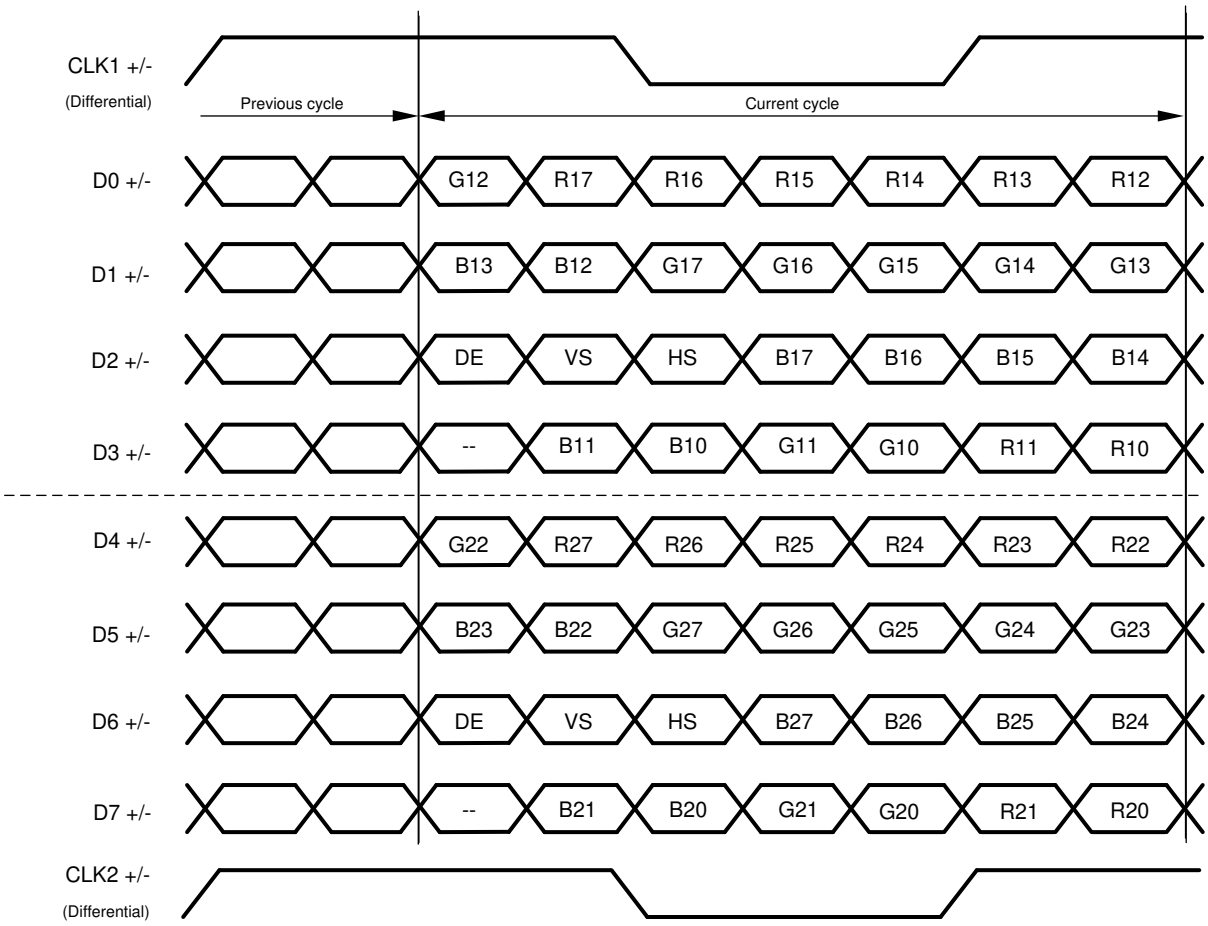

図 7-19. 24-Bit Color Dual FPD-Link Mapping: LSBs on D3/D7, "JEIDA" (MAPSEL = L)

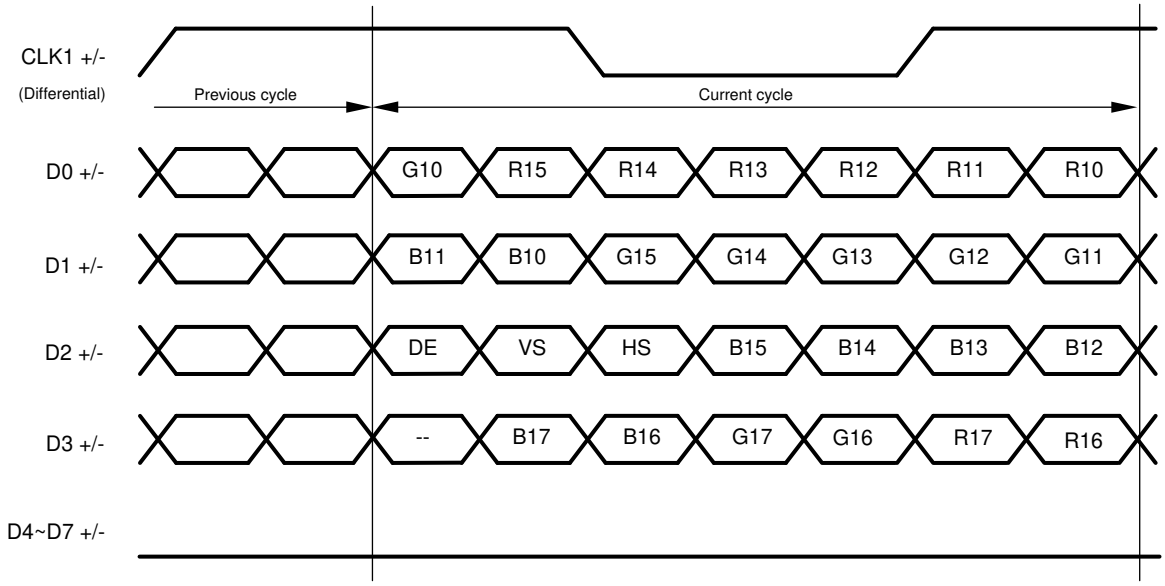

図 7-20. 24-Bit Color Single FPD-Link Mapping: MSBs on D3, "OLDI/SPWG/VESA" (MAPSEL = H)

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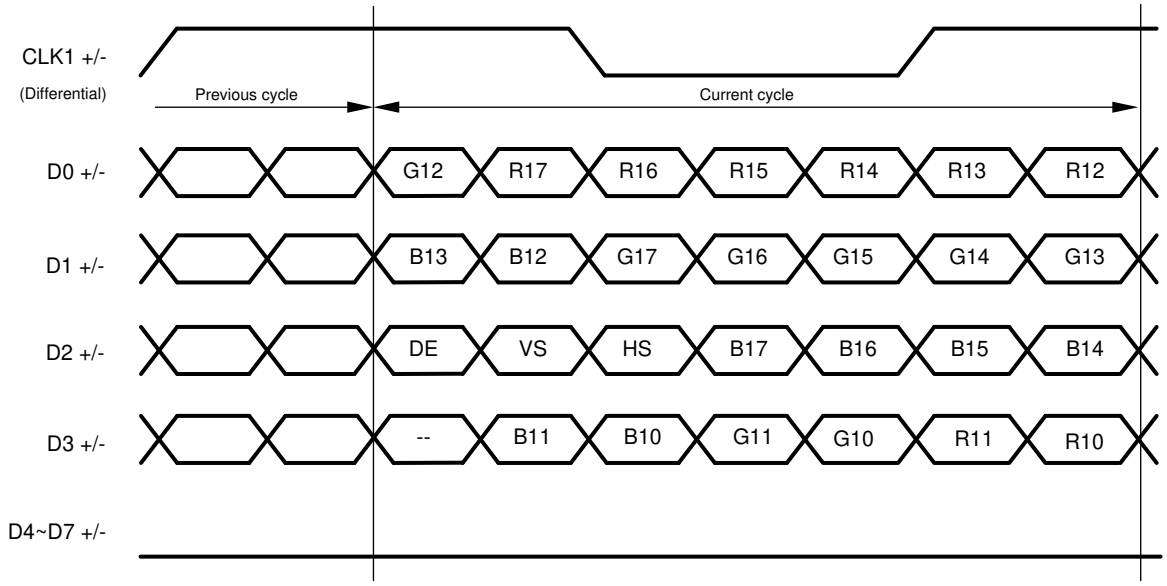

図 7-21. 24-Bit Color Single FPD-Link Mapping: LSBs on D3, "JEIDA" (MAPSEL = L)

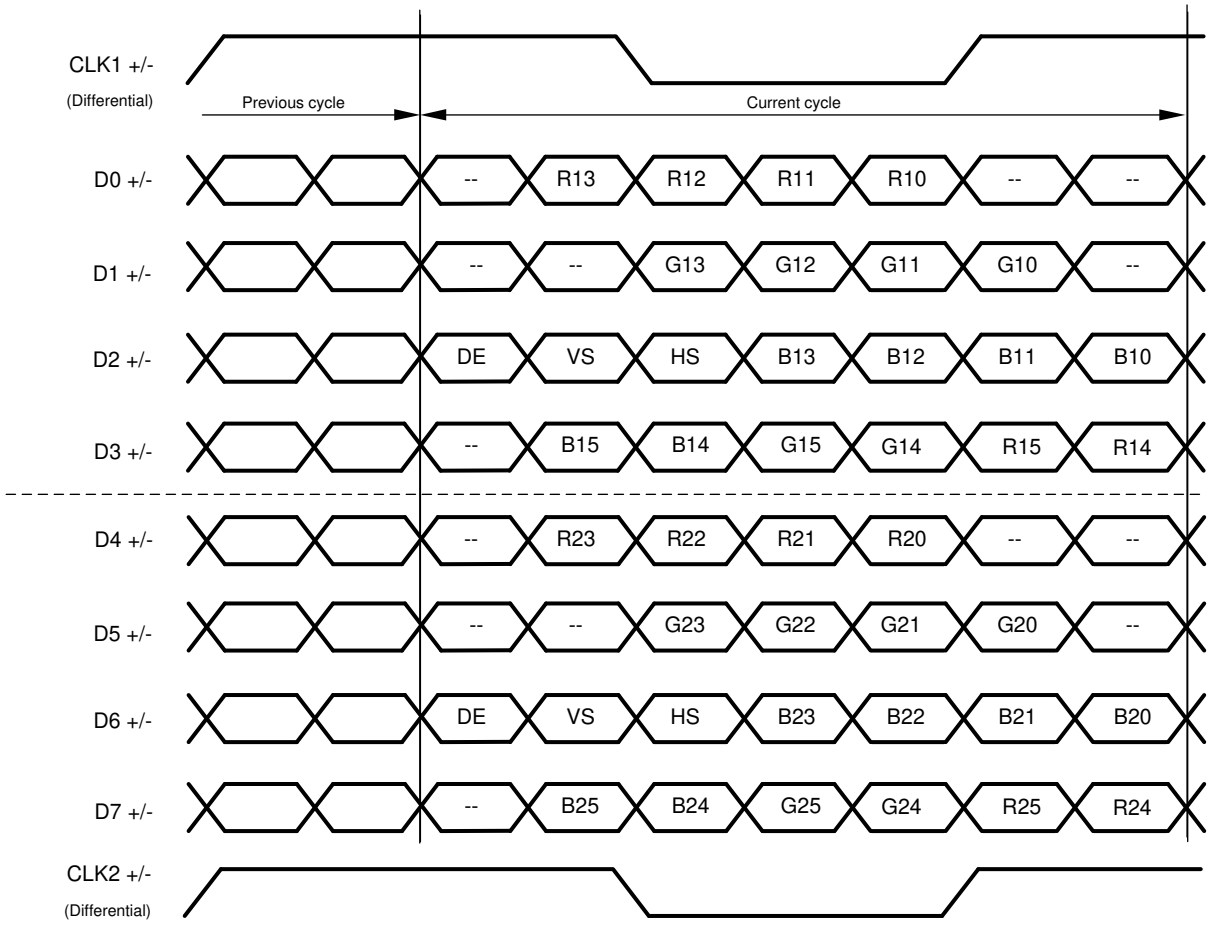

図 7-22. 18-Bit Color Dual FPD-Link Mapping, "4 Lane 18 Bit Mode" (MAPSEL = H)

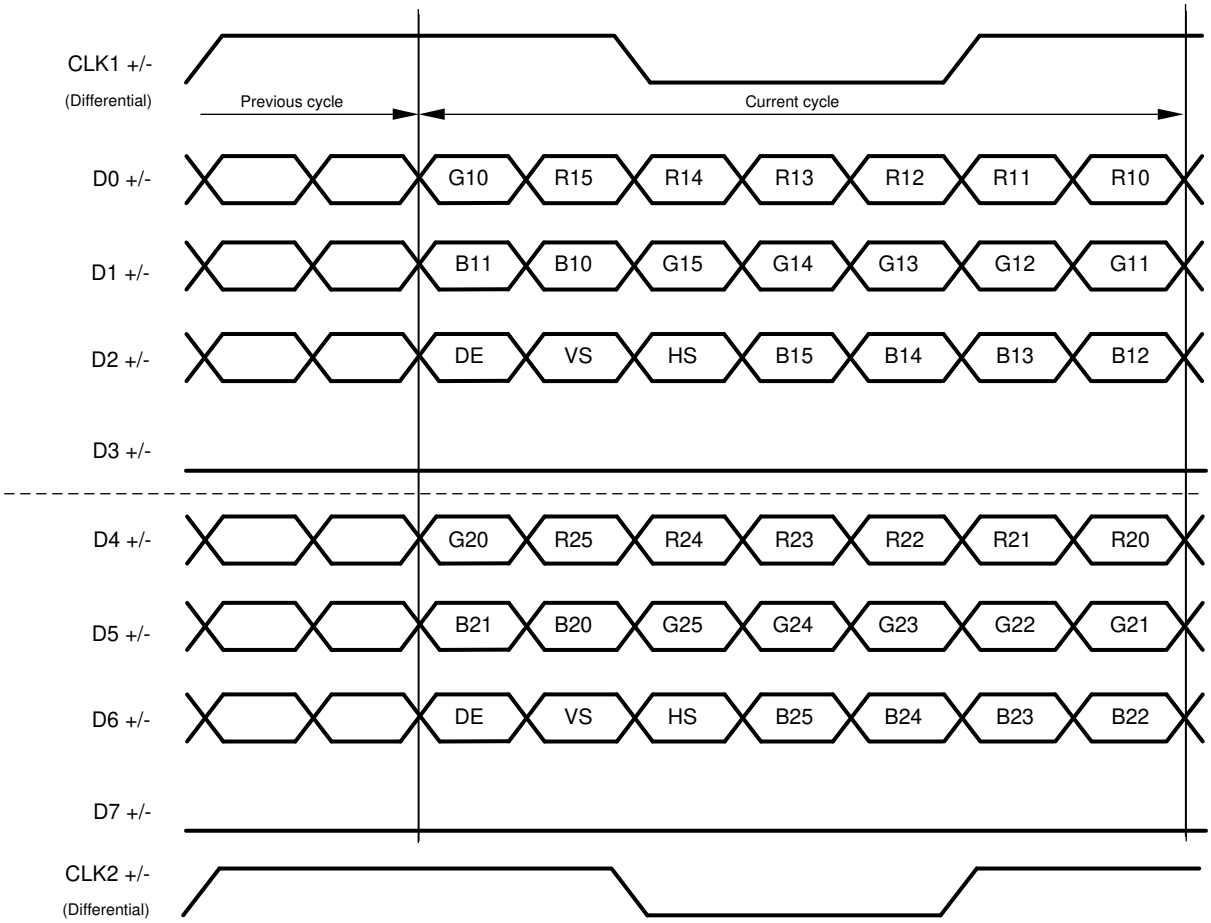

図 7-23. 18-Bit Color Dual FPD-Link Mapping, Standard 18 Bit (MAPSEL = L)

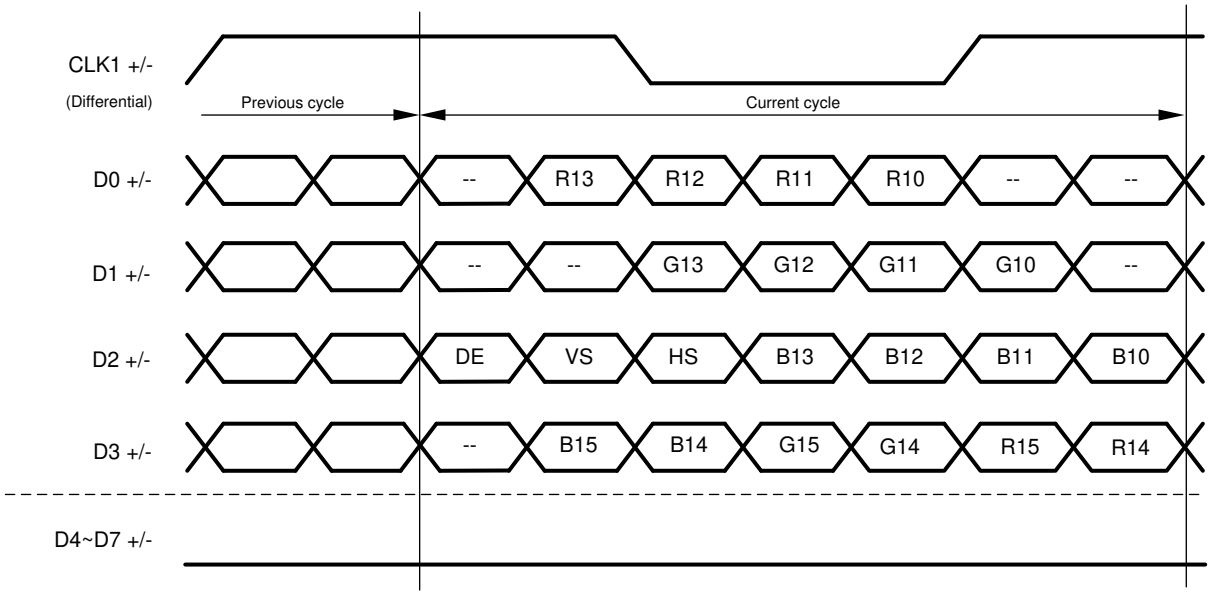

図 7-24. 18-Bit Color Single FPD-Link Mapping, "4 Lane 18 Bit Mode" (MAPSEL = H)

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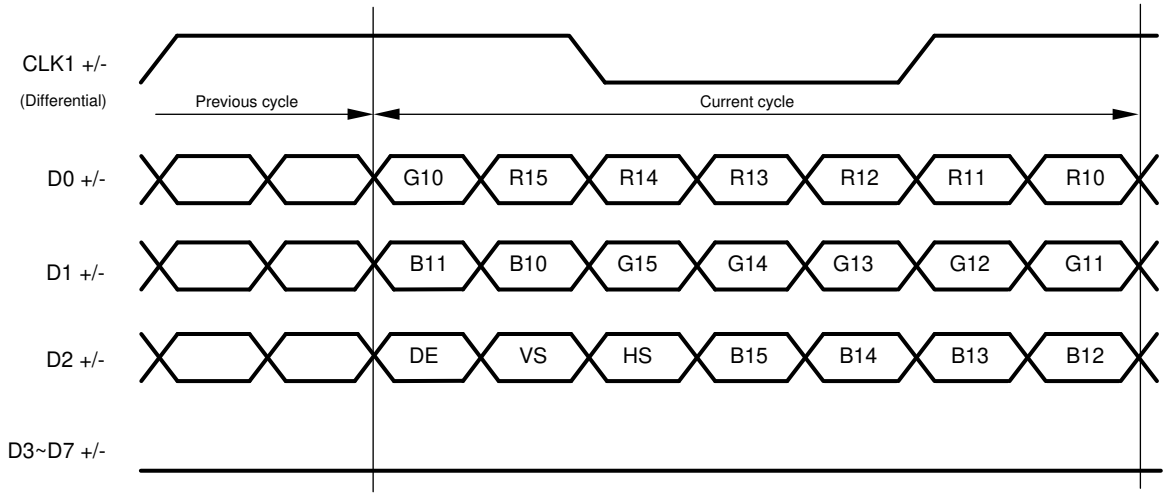

図 7-25. 18-Bit Color Single FPD-Link Mapping, Standard 18 Bit (MAPSEL = L)

7.5 Image Enhancement Features

Several image enhancement features are provided. The white-balance LUTs allow the user to define and map the color profile of the display. Adaptive Hi-FRC dithering enables the presentation of 'true color' images on an 18-bit display.

7.5.1 White Balance

The white-balance feature enables similar display appearance when using LCD's from different vendors. It compensates for native color temperature of the display, and adjusts relative intensities of R, G, and B to maintain specified color temperature. Programmable control registers are used to define the contents of three LUTs (8-bit color value for Red, Green and Blue) for the white-balance feature. The LUTs map input RGB values to new output RGB values. There are three LUTs, one LUT for each color. Each LUT contains 256 entries, 8-bits per entry with a total size of 6144 bits (3 × 256 x 8). All entries are readable and writable. Calibrated values are loaded into registers through the I2C interface (deserializer is a Target device). This feature may also be applied to lower color depth applications such as 18-bit (666) and 16-bit (565). White balance is enabled and configured via serial control bus register.

7.5.2 LUT Contents

The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs: 256 colors × 8 bits × 3 tables. Unused bits – LSBs – shall be set to 0 by the user. When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the deserializer, and driven to the display.

Alternatively, with 6-bit input data the user may choose to load complete 8-bit values into each LUT. This mode of operation provides the user with finer resolution at the LUT output to more closely achieve the desired white point of the calibrated display. Although 8-bit data is loaded, only 64 unique 8-bit white balance output values are available for each color (R, G and B). The result is 8-bit white balanced data. Before driving to the output of the deserializer, the 8-bit data must be reduced to 6-bit with an FRC dithering function. To operate in this mode, the user must configure the deserializer to enable the FRC2 function.

Examples of the three types of LUT configurations described are shown in 図 7-26.

注

When the LUT programming is active, register access to the main page is restricted.

注

If the LUT programming page is accidentally entered, it can be exited by writing anything to register 0xFF

7.5.3 Enabling White Balance

The user must load all 3 LUTs prior to enabling the white balance feature. The following sequence must be followed by the user to initialize white balance after power-on:

1. Load contents of all 3 LUTs . This requires a sequential loading of LUTs - first RED, second GREEN, third BLUE. 256, 8-bit entries must be loaded to each LUT. Page registers must be set to select each LUT.
2. Enable white balance. By default, the LUT data may not be reloaded after initialization at power-on.

An option does exist to allow LUT reloading after power-on and initial LUT loading (as previously described). This option may only be used after enabling the white-balance reload feature via the associated serial control bus register. In this mode the LUTs may be reloaded by the host controller via I2C. This provides the user with the flexibility to refresh LUTs periodically, or upon system requirements, to change to a new set of LUT values. The host controller loads the updated LUT values via the serial bus interface. There is no need to disable the white balance feature while reloading the LUT data. Refreshing the white balance to the new set of LUT data is seamless — no interruption of displayed data. Please refer to the programming example in the next section.

Note that initial loading of LUT values requires that all 3 LUTs be loaded sequentially. When reloading, partial LUT updates may be made; the LUT cannot be read.

8-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	00000001b
2	00000011b
3	00000011b
4	00000110b
5	00000110b
6	00000111b
7	00000111b
8	00001000b
9	00001010b
10	00001001b
11	00001011b
⋮	⋮
248	11111010b
249	11111010b
250	11111011b
251	11111011b
252	11111110b
253	11111101b
254	11111101b
255	11111111b

6-bit in / 6 bit out

Gray level Entry	Data Out (8-bits)
0	00000**00**b
1	N/A
2	N/A
3	N/A
4	00000**100**b
5	N/A
6	N/A
7	N/A
8	00001**000**b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111**000**b
249	N/A
250	N/A
251	N/A
252	11111**100**b
253	N/A
254	N/A
255	N/A

6-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000001b
1	N/A
2	N/A
3	N/A
4	00000110b
5	N/A
6	N/A
7	N/A
8	00001011b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111010b
249	N/A
250	N/A
251	N/A
252	11111111b
253	N/A
254	N/A
255	N/A

図 7-26. White-Balance LUT Configuration

7.5.3.1 LUT Programming Example

```
# Example DS90UH948-Q1 White Balance RGB LUT loading:

board.devAddr = 0x58

board.WriteReg(0x2A, 0x70) # Red LUT

board.WriteReg(0x00, 0x00)

board.WriteReg(0x01, 0x01)

board.WriteReg(0x02, 0x02)

...

board.WriteReg(0x98, 0x98)
```


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```
board.WriteReg(0x99, 0x99)
board.WriteReg(0x9A, 0x9A)
...
board.WriteReg(0xFD, 0xFD)
board.WriteReg(0xFE, 0xFE)
board.WriteReg(0xFF, 0xFF)

board.WriteReg(0x2A, 0xB0) # Green LUT
board.WriteReg(0x00, 0x00)
board.WriteReg(0x01, 0x01)
board.WriteReg(0x02, 0x02)
...
board.WriteReg(0x98, 0x98)
board.WriteReg(0x99, 0x99)
board.WriteReg(0x9A, 0x9A)
...
board.WriteReg(0xFD, 0xFD)
board.WriteReg(0xFE, 0xFE)
board.WriteReg(0xFF, 0xFF)

board.WriteReg(0x2A, 0xF0) # Blue LUT
board.WriteReg(0x00, 0x00)
board.WriteReg(0x01, 0x01)
board.WriteReg(0x02, 0x02)
...
board.WriteReg(0x98, 0x98)
board.WriteReg(0x99, 0x99)
board.WriteReg(0x9A, 0x9A)
...
board.WriteReg(0xFD, 0xFD)
board.WriteReg(0xFE, 0xFE)
board.WriteReg(0xFF, 0xFF)
board.WriteReg(0x2A, 0x20) # Enable WB
```

7.5.4 Adaptive Hi-FRC Dithering

The adaptive frame rate control FRC dithering feature delivers product-differentiating image quality. It reduces 24-bit RGB (8 bits per sub-pixel) to 18-bit RGB (6 bits per sub-pixel), smoothing color gradients, and allowing the flexibility to use lower cost 18-bit displays. FRC dithering is a method to emulate *missing* colors on a lower color depth LCD display by changing the pixel color slightly with every frame. FRC is achieved by controlling on and off pixels over multiple frames (temporal). Static dithering regulates the number of on and off pixels in a small defined pixel group (spatial). The FRC module includes both temporal and spatial methods and also Hi-FRC.

Conventional FRC can display only 16,194,277 colors with 6-bit RGB source. Hi-FRC enables full (16,777,216) color on an 18-bit LCD panel. The *adaptive* FRC module also includes input pixel detection to apply specific Spatial dithering methods for smoother gray level transitions. When enabled, the lower LSBs of each RGB output are not active; only 18-bit data (6 bits per R,G and B) are driven to the display. This feature is enabled via serial control bus register. Two FRC functional blocks are available, and may be independently enabled. FRC1 precedes the white-balance LUT, and is intended to be used when 24-bit data is being driven to an 18-bit display with a white-balance LUT that is calibrated for an 18-bit data source. The second FRC block, RC2, follows the white balance block and is intended to be used when fine adjustment of color temperature is required on an 18-bit color display, or when a 24-bit source drives an 18-bit display with a white-balance LUT calibrated for 24-bit source data.

For proper operation of the FRC dithering feature, the user must provide a description of the display timing control signals. The timing mode, sync mode (HS, VS) or *DE only* must be specified, along with the active polarity of the timing control signals. All this information is entered to device control registers via the serial bus interface.

Adaptive Hi-FRC dithering consists of several components. Initially, the incoming 8-bit data is expanded to 9-bit data. This allows the effective dithered result to support a total of 16.7 million colors. The incoming 9-bit data is evaluated, and one of four possible algorithms is selected. The majority of incoming data sequences are supported by the default dithering algorithm. Certain incoming data patterns (black/white pixel, full on/off sub-pixel) require special algorithms designed to eliminate visual artifacts associated with these specific gray level transitions. Three algorithms are defined to support these critical transitions.

An example of the default dithering algorithm is shown in 図 7-27. The 1 or 0 value shown in 図 7-27

図 7-27 describes whether the 6-bit value is increased by 1 (“1”) or left unchanged (“0”). In this case, the 3 truncated LSBs are 001.

F0L0	Frame = 0, Line = 0
PD1	Pixel Data one
Cell Value 010	R[7:2]+0, G[7:2]+1, B[7:2]+0
LSB=001	three lsb of 9 bit data (8 to 9 for Hi-Frc)

Pixel Index	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**	**PD8**	
LSB = 001									
F0L0	010	000	000	000	000	000	010	000	R = 4/32 G = 4/32 B = 4/32
F0L1	101	000	000	000	101	000	000	000	
F0L2	000	000	010	000	010	000	000	000	
F0L3	000	000	101	000	000	000	101	000	
F1L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F1L1	000	111	000	000	000	111	000	000	
F1L2	000	000	000	000	000	000	000	000	
F1L3	000	000	000	111	000	000	000	111	
F2L0	000	000	010	000	010	000	000	000	R = 4/32 G = 4/32 B = 4/32
F2L1	000	000	101	000	000	000	101	000	
F2L2	010	000	000	000	000	000	010	000	
F2L3	101	000	000	000	101	000	000	000	
F3L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F3L1	000	000	000	111	000	000	000	111	
F3L2	000	000	000	000	000	000	000	000	
F3L3	000	111	000	000	000	111	000	000	

図 7-27. Default FRC Algorithm

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7.6 Programming

7.6.1 Serial Control Bus

The device may also be configured by the use of a I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to eight device addresses supported). The device address is set through a resistor divider (R_{HIGH} and R_{LOW} — see 図 7-28 below) connected to the IDx pin.

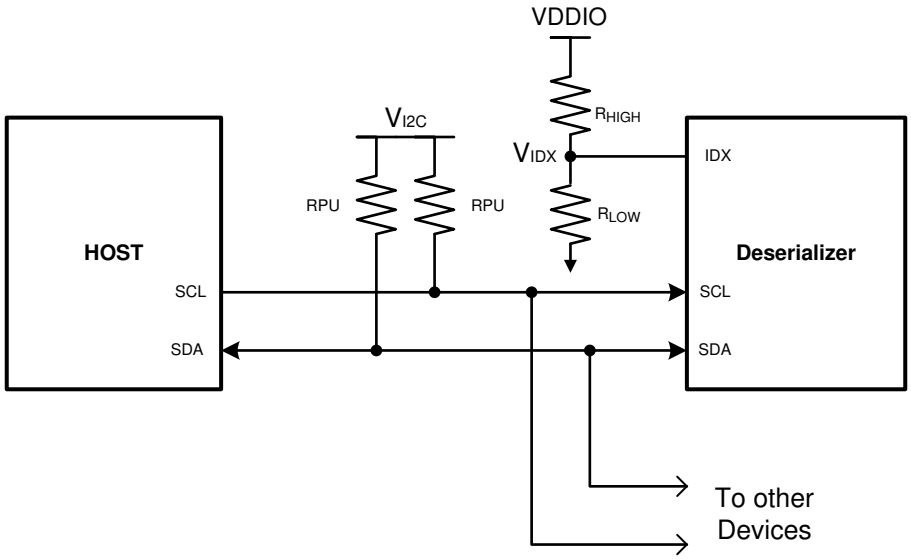

図 7-28. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a serial bus clock input. SDA is the serial bus data input / output signal. Both SCL and SDA signals require an external pullup resistor to 1.8-V or 3.3-V V_{I2C}. For most applications, TI recommends that the user adds a 4.7-kΩ pullup resistor to the VDD33 or 2.2 kΩ resistor to the VDD18. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled high or driven low. For more details information on how to calculate the pullup resistor, see *I2C Bus Pullup Resistor Calculation* (SLVA689).

The IDx pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{LOW}) and VDD33, each ratio corresponding to a specific device address. See 表 7-11 for more information.

表 7-11. Serial Control Bus Addresses for IDx

NO.	V_{IDX} VOLTAGE	V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% tolerance)		PRIMARY ASSIGNED I_2C ADDRESS	
	V (TYP)	VDD = 3.3 V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	Open	10	0x2C	0x58
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	0x2E	0x5C
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	0x30	0x60
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	0x32	0x64
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	0x34	0x68
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	0x36	0x6C
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	0x38	0x70
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	0x3C	0x78

The serial bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions low while SCL is high. A STOP occurs when SCL transitions high while SDA is also HIGH. See 図 7-29.

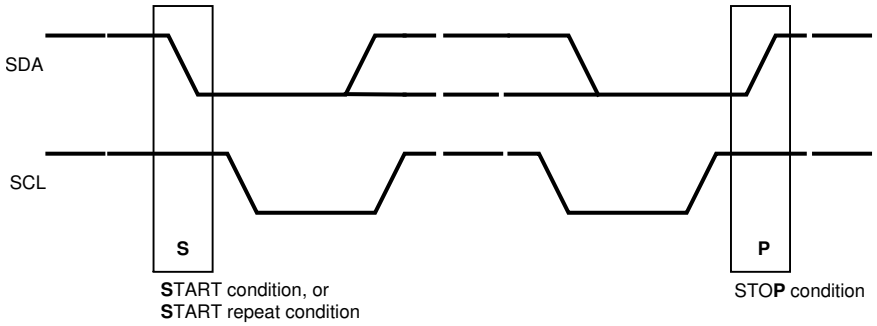

図 7-29. START and STOP Conditions

To communicate with a remote device, the host controller sends the Target address and listens for a response from the Target. This response is referred to as an acknowledge bit (ACK). If a Target on the bus is addressed correctly, it acknowledges (ACKs) the Controller by driving the SDA bus low. If the address does not match the Target address of a device, the Target not-acknowledges (NACKs) the Controller by letting the SDA be pulled High. ACKs also occur on the bus when data is transmitted. When the Controller writes data, the Target sends an ACK after every data byte is successfully received. When the Controller reads data, the Controller sends an ACK after every data byte is received to let the Target know that the Controller is ready to receive another data byte. When the Controller wants to stop reading, the Controller sends a NACK after the last data byte to create a stop condition on the bus. All communication on the bus begins with either a start condition or a repeated Start condition. All communication on the bus ends with a stop condition. A READ is shown in 図 7-30 and a WRITE is shown in 図 7-31.

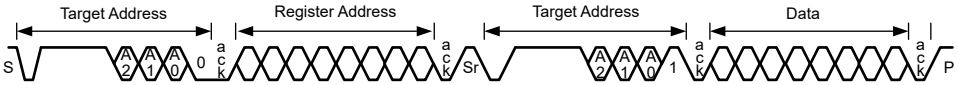

図 7-30. Serial Control Bus — READ

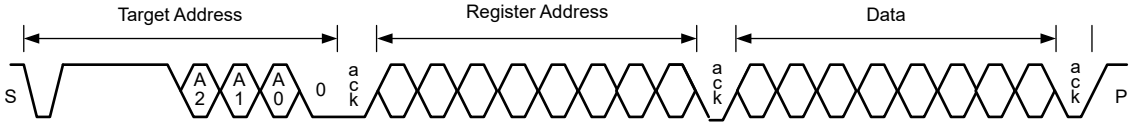

図 7-31. Serial Control Bus — WRITE

The I2C Controller located in the deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to the *I2C Communication Over FPD-Link III with Bidirectional Control Channel* (SNLA131).

注

I2C access over the BCC requires each transaction be terminated with a STOP rather than a repeated START.

注

Serial Control Bus does not spport short format read over the BCC

7.6.2 Multi-Controller Arbitration Support

The bidirectional control channel in the FPD-Link III devices implements I2C-compatible bus arbitration in the proxy I2C Controller implementation. When sending a data bit, each I2C Controller senses the value on the SDA line. If the Controller sends a logic 1 but senses a logic 0, the Controller loses arbitration. The Controller will stop driving SDA and retry the transaction when the bus becomes idle. Thus, multiple I2C Controllers may be implemented in the system.

For example, there might also be a local I2C Controller at each camera. The local I2C Controller could access the image sensor and EEPROM. The only restriction would be that the remote I2C Controller at the camera

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should not attempt to access a remote Target through the BCC that is located at the host controller side of the link. In other words, the control channel should only operate in camera mode for accessing remote Target devices to avoid issues with arbitration across the link. The remote I2C Controller should also not attempt to access the deserializer registers to avoid a conflict in register access with the Host controller.

If the system does require Controller-Target operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available R/W registers in the deserializer to allow Controllers to communicate with each other to pass control between the two Controllers. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one Controller to another.

7.6.3 I2C Restrictions on Multi-Controller Operation

The I2C specification does not provide for arbitration between Controllers under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I2C bus:

- One Controller generates a repeated start while another Controller is sending a data bit.
- One Controller generates a stop while another Controller is sending a data bit.
- One Controller generates a repeated start while another Controller sends a stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C Target.

7.6.4 Multi-Controller Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices (DS90UH94x-Q1), serializers or deserializer registers may be accessed simultaneously from both local and remote I2C Controllers. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I2C Targets is still be allowed in only one direction at a time (camera or display mode).

7.6.5 Multi-Controller Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices (in backward compatible mode), simultaneous access to serializer or deserializer registers from both local and remote I2C Controllers may cause incorrect operation. Thus, restrictions must be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in a read or write error.

TI recommends two basic options:

- Allow device register access only from one controller.

  In a display mode system, this would allow only the host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer (local to the display) would not be allowed to access the deserializer or serializer registers.
- Allow local register access only with no access to remote serializer or deserializer registers.

  The host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I2C Targets would still be allowed in one direction (camera or display mode).

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access is ensured to work correctly if both local and remote Controllers are accessing the same deserializer register. This allows a simple method of passing control of the bidirectional control channel from one Controller to another.

7.6.6 Restrictions on Control Channel Direction for Multi-Controller Operation

Only display or camera mode operation should be active at any time across the bidirectional control channel. If both directions are required, some method of transferring control between I2C Controllers should be implemented.

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7.7 Register Maps

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at start-up
- LL = Latched Low and held until read
- LH = Latched High and held until read
- S = Set based on strap pin configuration at start-up

7.7.1 DS90UH948-Q1 Registers

表 7-12 lists the memory-mapped registers for the DS90UH948-Q1 registers. All register offset addresses not listed in 表 7-12 should be considered as reserved locations and the register contents should not be modified.

表 7-12. DS90UH948-Q1 Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID		Go
0x1	RESET		Go
0x2	GENERAL_CONFIGURATION_0		Go
0x3	GENERAL_CONFIGURATION_1		Go
0x4	BCC_WATCHDOG_CONTROL		Go
0x5	I2C_CONTROL_1		Go
0x6	I2C_CONTROL_2		Go
0x7	REMOTE_ID		Go
0x8	TargetID_0		Go
0x9	TargetID_1		Go
0xA	TargetID_2		Go
0xB	TargetID_3		Go
0xC	TargetID_4		Go
0xD	TargetID_5		Go
0xE	TargetID_6		Go
0xF	TargetID_7		Go
0x10	TargetALIAS_0		Go
0x11	TargetALIAS_1		Go
0x12	TargetALIAS_2		Go
0x13	TargetALIAS_3		Go
0x14	TargetALIAS_4		Go
0x15	TargetALIAS_5		Go
0x16	TargetALIAS_6		Go
0x17	TargetALIAS_7		Go
0x18	MAILBOX_18		Go
0x19	MAILBOX_19		Go
0x1A	GPIO_9_and_GLOBAL_GPIO_CONFIG		Go
0x1B	FREQUENCY_COUNTER		Go
0x1C	GENERAL_STATUS		Go
0x1D	GPIO0_CONFIG		Go
0x1E	GPIO1_2_CONFIG		Go
0x1F	GPIO3_CONFIG		Go

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表 7-12. DS90UH948-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x20	GPIO5_6_CONFIG		Go
0x21	GPIO7_8_CONFIG		Go
0x22	DATAPATH_CONTROL		Go
0x23	RX_MODE_STATUS		Go
0x24	BIST_CONTROL		Go
0x25	BIST_ERROR_COUNT		Go
0x26	SCL_HIGH_TIME		Go
0x27	SCL_LOW_TIME		Go
0x28	DATAPATH_CONTROL_2		Go
0x29	FRC_CONTROL		Go
0x2A	WHITE_BALANCE_CONTROL		Go
0x2B	I2S_CONTROL		Go
0x2E	PCLK_TEST_MODE		Go
0x34	DUAL_RX_CTL		Go
0x35	AEQ_TEST		Go
0x37	MODE_SEL		Go
0x3A	I2S_DIVSEL		Go
0x3B	EQ_STATUS		Go
0x41	LINK_ERROR_COUNT		Go
0x43	HSCC_CONTROL		Go
0x44	ADAPTIVE_EQ_BYPASS		Go
0x45	ADAPTIVE_EQ_MIN_MAX		Go
0x49	FPD_TX_MODE		Go
0x4B	LVDS_CONTROL		Go
0x52	CML_OUTPUT_CTL1		Go
0x56	CML_OUTPUT_ENABLE		Go
0x57	CML_OUTPUT_CTL2		Go
0x63	CML_OUTPUT_CTL3		Go
0x64	PGCTL		Go
0x65	PGCFG		Go
0x66	PGIA		Go
0x67	PGID		Go
0x68	PGDBG		Go
0x69	PGTSTDAT		Go
0x6E	GPI_PIN_STATUS_1		Go
0x6F	GPI_PIN_STATUS_2		Go
0x80	RX_BKSV0		Go
0x81	RX_BKSV1		Go
0x82	RX_BKSV2		Go
0x83	RX_BKSV3		Go
0x84	RX_BKSV4		Go
0x90	TX_KSV0		Go
0x91	TX_KSV1		Go
0x92	TX_KSV2		Go
0x93	TX_KSV3		Go

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表 7-12. DS90UH948-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x94	TX_KSV4		Go
0xC0	HDCP_DBG		Go
0xC1	HDCP_DBG2		Go
0xC4	HDCP_STS		Go
0xC9	KSV_FIFO__DATA		Go
0xCA	KSV_FIFO_A_DDR0		Go
0xCB	KSV_FIFO_ADDR1		Go
0xE0	RPTR_TX0		Go
0xE1	RPTR_TX1		Go
0xE2	RPTR_TX2		Go
0xE3	RPTR_TX3		Go
0xE8	XRPTR_STS		Go
0xE9	XRPTR_CTL		Go
0xEA	XRPTR_BSTS0		Go
0xEB	XRPTR_BSTS1		Go
0xF0	HDCP_RX_ID0		Go
0xF1	HDCP_RX_ID1		Go
0xF2	HDCP_RX_ID2		Go
0xF3	HDCP_RX_ID3		Go
0xF4	HDCP_RX_ID4		Go
0xF5	HDCP_RX_ID5		Go

7.7.1.1 I2C_DEVICE_ID Register (Address = 0x0) [reset = STRAP]

I2C_DEVICE_ID is described in 表 7-13.

Return to Summary Table.

表 7-13. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DEVICE_ID	R/W	STRAP	7-bit address of Deserializer Defaults to address configured by the IDX strap pin
0	DES_ID	R/W	0x0	0: Device ID is from IDX strap 1: Register I2C Device ID overrides IDX strap

7.7.1.2 RESET Register (Address = 0x1) [reset = 0x0]

RESET is described in 表 7-14.

Return to Summary Table.

表 7-14. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

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表 7-14. RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BC_ENABLE	R/W	0x1	Back Channel enable. Note: This bit can not be set to 0 through the control channel, it is only writable via local I2C at the DES. Note: Setting this bit to 0 will disable the back channel only if both I2C pass through bits, 0x03[3] and 0x05[7], are also set to low.
1	DIGITAL_RESET0	R/W	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap ' as their default value in this table.
0	DIGITAL_RESET1	R/W	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

注

After a digital reset, the following registers are not reset:

0x00, 0x01[4:3, 1:0], 0x23[4:3], 0x2A[7:6], 0x32[0], 0x34[4:0], 0x49[1:0], 0x71[5]

7.7.1.3 GENERAL_CONFIGURATION_0 Register (Address = 0x2) [reset = 0x0]

GENERAL_CONFIGURATION_0 is described in 表 7-15.

Return to Summary Table.

表 7-15. GENERAL_CONFIGURATION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUTPUT_ENABLE	R/W	0x0	Output Enable Override Value (in conjunction with Output Sleep State Select) If the Override control is not set, the Output Enable will be set to 1. A Digital reset 0x01[0] should be asserted after toggling Output Enable bit LOW to HIGH
6	OUTPUT_ENABLE_OVERRIDE	R/W	0x0	Overrides Output Enable and Output Sleep State default 0: Disable override 1: Enable override
5	OSC_CLOCK_OUTPUT_ENABLE__AUTO_CLOCK_EN	R/W	0x0	OSC clock output enable If loss of lock OSC clock is output onto PCLK. The frequency is selected in register 0x24. 1: Enable 0: Disable
4	OUTPUT_SLEEP_STATE_SELECT	R/W	0x0	OSS Select Override value to control output state when LOCK is low (used in conjunction with Output Enable) If the Override control is not set, the Output Sleep State Select will be set to 1.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.7.1.4 GENERAL_CONFIGURATION_1 Register (Address = 0x3) [reset = 0xF0]

GENERAL_CONFIGURATION_1 is described in 表 7-16.

Return to Summary Table.

表 7-16. GENERAL_CONFIGURATION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Reserved
6	BC_CRC_GENERATOR_ENABLE	R/W	0x1	Back Channel CRC Generator Enable 0: Disable 1: Enable
5	FAILSAFE_LOW	R/W	0x1	Controls the pull direction for undriven LVCMOS inputs 1: Pull down 0: Pull up
4	FILTER_ENABLE	R/W	0x1	HS,VS,DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected. For HS, It is a 2-clock filter for single FPD3 mode and a 4-clock filter for dual FPD3 mode. 1: Filtering enable 0: Filtering disable
3	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
2	AUTO_ACK	R/W	0x0	Automatically Acknowledge I2C writes independent of the forward channel lock state 1: Enable 0: Disable
1	DE_GATE_RGB	R/W	0x0	Gate RGB data with DE signal. RGB data is gated with DE in order to allow packetized audio and block unencrypted data when paired with a serializer that supports HDCP. When paired with a serializer that does not support HDCP, RGB data is not gated with DE by default. However, to enable packetized autio this bit must be set. 1: Gate RGB data with DE (has no effect when paired with a serializer that supports HDCP) 0: Pass RGB data independent of DE (has no effect when paired with a serializer that does not support HDCP)
0	RESERVED	R	0x0	Reserved

7.7.1.5 BCC_WATCHDOG_CONTROL Register (Address = 0x4) [reset = 0xFE]

BCC_WATCHDOG_CONTROL is described in 表 7-17.

Return to Summary Table.

表 7-17. BCC_WATCHDOG_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

7.7.1.6 I2C_CONTROL_1 Register (Address = 0x5) [reset = 0x1E]

I2C_CONTROL_1 is described in 表 7-18.

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表 7-18. I2C_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_PASS_THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6-4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3-0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

7.7.1.7 I2C_CONTROL_2 Register (Address = 0x6) [reset = 0x0]

I2C_CONTROL_2 is described in 表 7-19.

Return to Summary Table.

表 7-19. I2C_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FORWARD_CHANNEL_SEQUENCE_ERROR	R	0x0	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. If this bit is set, an error may have occurred in the control channel operation.
6	CLEAR_SEQUENCE_ERROR	R/W	0x0	Clears the Sequence Error Detect bit
5	RESERVED	R	0x0	Reserved
4-3	SDA_Output_Delay	R/W	0x0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00: 250ns 01: 300ns 10: 350ns 11: 400ns
2	LOCAL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C Controller attached to the Serializer. Setting this bit does not affect remote access to I2C Targets at the Deserializer.
1	I2C_BUS_TIMER_SPEED UP	R/W	0x0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISABLE	R/W	0x0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

7.7.1.8 REMOTE_ID Register (Address = 0x7) [reset = 0x0]

REMOTE_ID is described in 表 7-20.

Return to Summary Table.

表 7-20. REMOTE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	REMOTE_ID	R/W	0x0	7-bit Serializer Device ID Configures the I2C Target ID of the remote Serializer. A value of 0 in this field disables I2C access to the remote Serializer. This field is automatically loaded from the Serializer once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.

7.7.1.9 TargetID_0 Register (Address = 0x8) [reset = 0x0]

TargetID_0 is described in 表 7-21.

Return to Summary Table.

表 7-21. TargetID_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.10 TargetID_1 Register (Address = 0x9) [reset = 0x0]

TargetID_1 is described in 表 7-22.

Return to Summary Table.

表 7-22. TargetID_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.11 TargetID_2 Register (Address = 0xA) [reset = 0x0]

TargetID_2 is described in 表 7-23.

Return to Summary Table.

表 7-23. TargetID_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

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表 7-23. TargetID_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0x0	Reserved

7.7.1.12 TargetID_3 Register (Address = 0xB) [reset = 0x0]

TargetID_3 is described in 表 7-24.

Return to Summary Table.

表 7-24. TargetID_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.13 TargetID_4 Register (Address = 0xC) [reset = 0x0]

TargetID_4 is described in 表 7-25.

Return to Summary Table.

表 7-25. TargetID_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID4	R/W	0x0	7-bit Remote Target Device ID 4v Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.14 TargetID_5 Register (Address = 0xD) [reset = 0x0]

TargetID_5 is described in 表 7-26.

Return to Summary Table.

表 7-26. TargetID_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.15 TargetID_6 Register (Address = 0xE) [reset = 0x0]

TargetID_6 is described in 表 7-27.

Return to Summary Table.

表 7-27. TargetID_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.16 TargetID_7 Register (Address = 0xF) [reset = 0x0]

TargetID_7 is described in 表 7-28.

Return to Summary Table.

表 7-28. TargetID_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved

7.7.1.17 TargetALIAS_0 Register (Address = 0x10) [reset = 0x0]

TargetALIAS_0 is described in 表 7-29.

Return to Summary Table.

表 7-29. TargetALIAS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.18 TargetALIAS_1 Register (Address = 0x11) [reset = 0x0]

TargetALIAS_1 is described in 表 7-30.

Return to Summary Table.

表 7-30. TargetALIAS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

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7.7.1.19 TargetALIAS_2 Register (Address = 0x12) [reset = 0x0]

TargetALIAS_2 is described in 表 7-31.

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表 7-31. TargetALIAS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.20 TargetALIAS_3 Register (Address = 0x13) [reset = 0x0]

TargetALIAS_3 is described in 表 7-32.

Return to Summary Table.

表 7-32. TargetALIAS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.21 TargetALIAS_4 Register (Address = 0x14) [reset = 0x0]

TargetALIAS_4 is described in 表 7-33.

Return to Summary Table.

表 7-33. TargetALIAS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.22 TargetALIAS_5 Register (Address = 0x15) [reset = 0x0]

TargetALIAS_5 is described in 表 7-34.

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表 7-34. TargetALIAS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.

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表 7-34. TargetALIAS_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0x0	Reserved

7.7.1.23 TargetALIAS_6 Register (Address = 0x16) [reset = 0x0]

TargetALIAS_6 is described in 表 7-35.

Return to Summary Table.

表 7-35. TargetALIAS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.24 TargetALIAS_7 Register (Address = 0x17) [reset = 0x0]

TargetALIAS_7 is described in 表 7-36.

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表 7-36. TargetALIAS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Target_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	RESERVED	R	0x0	Reserved

7.7.1.25 MAILBOX_18 Register (Address = 0x18) [reset = 0x0]

MAILBOX_18 is described in 表 7-37.

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表 7-37. MAILBOX_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_18	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C Controllers on opposite ends of the link.

7.7.1.26 MAILBOX_19 Register (Address = 0x19) [reset = 0x1]

MAILBOX_19 is described in 表 7-38.

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表 7-38. MAILBOX_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_19	R/W	0x1	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C Controllers on opposite ends of the link.

7.7.1.27 GPIO_9_and_GLOBAL_GPIO_CONFIG Register (Address = 0x1A) [reset = 0x0]

GPIO_9_and_GLOBAL_GPIO_CONFIG is described in 表 7-39.

Return to Summary Table.

表 7-39. GPIO_9_and_GLOBAL_GPIO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL_GPIO_OUTPUT_VALUE	R/W	0x0	Global GPIO Output Value This value is output on each GPIO pin when the individual pin is not otherwise enabled as a GPIO and the global GPIO direction is Output
6	RESERVED	R	0x0	Reserved
5	GLOBAL_GPIO_FORCE_DIR	R/W	0x0	The GLOBAL GPIO DIR and GLOBAL GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. The GLOBAL bits are overridden by the individual GPIO DIR and GPIO EN bits. {GLOBAL GPIO DIR, GLOBAL GPIO EN} 00: Functional mode; output 10: Tri-state 01: Force mode; output 11: Force mode; input
4	GLOBAL_GPIO_FORCE_EN	R/W	0x0	This bit grouped together with bit 5 to form the configuration of GPIO DIR and GPIO EN.
3	GPIO9_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	RESERVED	R	0x0	Reserved
1	GPIO9_DIR	R/W	0x0	The GPIO DIR and GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO9_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.28 FREQUENCY_COUNTER Register (Address = 0x1B) [reset = 0x0]

FREQUENCY_COUNTER is described in 表 7-40.

Return to Summary Table.

表 7-40. FREQUENCY_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Frequency_Count	R/W	0x0	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 50ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

7.7.1.29 GENERAL_STATUS Register (Address = 0x1C) [reset = 0x0]

GENERAL_STATUS is described in 表 7-41.

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表 7-41. GENERAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	DUAL_TX_STS	R	0x0	Transmitter Dual Link Status: This bit indicates the current operating mode of the FPD-Link Transmit port 1: Dual-link mode active 0: Single-link mode active
4	DUAL_RX_STS	R	0x0	Receiver Dual Link Status: This bit indicates the current operating mode of the FPD-Link III Receive port 1: Dual-link mode active 0: Single-link mode active
3	I2S_LOCKED	R	0x0	I2S LOCK STATUS 0: I2S PLL controller not locked 1: I2S PLL controller locked to input i2s clock
2	RESERVED	R	0x0	Reserved
1	SIGNAL_DETECT	R	0x0	1: Serial input detected 0: Serial input not detected
0	LOCK	R	0x0	De-Serializer CDR, PLL's clock to recovered clock frequency 1: De-Serializer locked to recovered clock 0: De-Serializer not locked In Dual-link mode, this indicates both channels are locked.

7.7.1.30 GPIO0_CONFIG Register (Address = 0x1D) [reset = 0x10]

GPIO0_CONFIG is described in 表 7-42.

Return to Summary Table.

GPIO0 and D_GPIO0 Configuration: If PORT1_SEL is set, this register controls the D_GPIO0 pin

表 7-42. GPIO0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Rev_ID	R	0x1	Revision ID 0001: B1
3	GPIO0_OUTPUT_VALUE_D_GPIO0_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.

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表 7-42. GPIO0_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	GPIO0_REMOTE_ENABLE _D_GPIO0_REMOTE_ENABLE	R/W	0x0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO0_DIR _D_GPIO0_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO0_EN _D_GPIO0_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.31 GPIO1_2_CONFIG Register (Address = 0x1E) [reset = 0x00]

GPIO1_2_CONFIG is described in 表 7-43.

Return to Summary Table.

GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration: If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins

表 7-43. GPIO1_2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO2_OUTPUT_VALUE _D_GPIO2_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
6	GPIO2_REMOTE_ENABLE _D_GPIO2_REMOTE_ENABLE	R/W	0x0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
5	GPIO2_DIR _D_GPIO2_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO2_EN _D_GPIO2_EN	R/W	0x0	This bit grouped together with bit 5 to form the configuration of GPIO DIR and GPIO EN.
3	GPIO1_OUTPUT_VALUE _D_GPIO1_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO1_REMOTE_ENABLE _D_GPIO1_REMOTE_ENABLE	R/W	0x0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO1_DIR _D_GPIO1_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

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表 7-43. GPIO1_2_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GPIO1_EN _D_GPIO1_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.32 GPIO3_CONFIG Register (Address = 0x1F) [reset = 0x00]

GPIO3_CONFIG is described in 表 7-44.

Return to Summary Table.

GPIO3 and D_GPIO3 Configuration: If PORT1_SEL is set, this register controls the D_GPIO3 pin

表 7-44. GPIO3_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	GPIO3_OUTPUT_VALUE _D_GPIO3_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO3_REMOTE_ENABLE _D_GPIO3_REMOTE_ENABLE	R/W	0x0	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO3_DIR _D_GPIO3_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO3_EN _D_GPIO3_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.33 GPIO5_6_CONFIG Register (Address = 0x20) [reset = 0x0]

GPIO5_6_CONFIG is described in 表 7-45.

Return to Summary Table.

表 7-45. GPIO5_6_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO6_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
6	Reserved	R/W	0x0	Reserved
5	GPIO6_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO6_EN	R/W	0x0	This bit grouped together with bit 5 to form the configuration of GPIO DIR and GPIO EN.
3	GPIO5_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.

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表 7-45. GPIO5_6_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	Reserved	R/W	0x0	Reserved
1	GPIO5_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO5_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.34 GPIO7_8_CONFIG Register (Address = 0x21) [reset = 0x0]

GPIO7_8_CONFIG is described in 表 7-46.

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表 7-46. GPIO7_8_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
6	Reserved	R/W	0x0	Reserved
5	GPIO8_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO8_EN	R/W	0x0	This bit grouped together with bit 5 to form the configuration of GPIO DIR and GPIO EN.
3	GPIO7_OUTPUT_VALUE	R/W	0x0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	Reserved	R/W	0x0	Reserved
1	GPIO7_DIR	R/W	0x0	The GPIO DIR and GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO7_EN	R/W	0x0	This bit grouped together with bit 1 to form the configuration of GPIO DIR and GPIO EN.

7.7.1.35 DATAPATH_CONTROL Register (Address = 0x22) [reset = 0x0]

DATAPATH_CONTROL is described in 表 7-47.

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表 7-47. DATAPATH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register
6	PASS_RGB	R/W	0x0	Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in DS90UB928 or in Backward Compatibility mode. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
5	DE_POLARITY	R/W	0x0	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
4	I2S_RPTR_REGEN	R/W	0x0	This bit controls whether the HDCP Receiver outputs packetized Auxiliary/Audio data on the RGB video output pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins. Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
3	I2S_4_CHANNEL_ENABLE_OVERRIDE	R/W	0x0	1: Set I2S 4-Channel Enable from bit of of this register 0: Set I2S 4-Channel disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
2	18_BIT_VIDEO_SELECT	R/W	0x0	1: Select 18-bit video mode 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.Note: Surround audio is not supported in repeater mode when 18-bit video mode is enabled.
1	I2S_TRANSPORT_SELECT	R/W	0x0	1: Enable I2S In-Band Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
0	I2S_4_CHANNEL_ENABLE	R/W	0x0	I2S 4-Channel Enable 1: Enable I2S 4-Channel 0: Disable I2S 4-Channel Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.

7.7.1.36 RX_MODE_STATUS Register (Address = 0x23) [reset = X]

RX_MODE_STATUS is described in 表 7-48.

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表 7-48. RX_MODE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

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表 7-48. RX_MODE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BC_FREQ_SELECT	R/W	0x0	Back Channel Frequency Select Used in conjunction with BC_HIGH_SPEED to set the back channel frequency. If BC_HIGH_SPEED = 0 then: 0: 5Mbps Back Channel 1: 10Mbps Back Channel If BC_HIGH_SPEED = 1 then BC_FREQ_SELECT is ignored and the back channel frequency is set to 20Mbps (not available when paired with 92x serializers) Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer.
5	AUTO_I2S	R/W	0x1	Auto I2S Determine I2S mode from the AUX data codes.
4	BC_HIGH_SPEED	R/W	X	Back-Channel High-Speed control Enables high-speed back-channel at 20Mbps This bit will override the BC_FREQ_SELECT setting Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer. BC_HIGH_SPEED is loaded from the MODE_SEL1 pin strap options.
3	COAX_MODE	R/W	X	Coax Mode Configures the FPD3 Receiver for operation over Coax or STP cabling: 0 : Shielded Twisted pair (STP) 1 : Coax Coax Mode is loaded from the MODE_SEL1 pin strap options.
2	REPEATER_MODE	R	X	Repeater Mode Indicates device is strapped to repeater mode. Repeater Mode is loaded from the MODE_SEL1 pin strap options.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.7.1.37 BIST_CONTROL Register (Address = 0x24) [reset = 0x8]

BIST_CONTROL is described in 表 7-49.

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表 7-49. BIST_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00 : No toggling 01 : Alternating 1/0 toggling 1x : Toggle based on BIST data
5-4	AUTO_OSC_FREQ	R/W	0x0	When register 0x02 bit 5 (AUTO)CLOCK_EN) is set, this field controls the nominal frequency of the oscillator-based receive clock. 00: 50 MHz 01: 25 MHz 10: 10 MHz 11: Reserved (selects analog 25 MHz, but not for customer use)
3	BIST_PIN_CONFIG	R/W	0x1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register

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表 7-49. BIST_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	BIST_CLOCK_SOURCE	R/W	0x0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details.
0	BIST_EN	R/W	0x0	BIST Control 1: Enabled 0: Disabled

7.7.1.38 BIST_ERROR_COUNT Register (Address = 0x25) [reset = 0x0]

BIST_ERROR_COUNT is described in 表 7-50.

Return to Summary Table.

表 7-50. BIST_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIST_ERROR_COUNT	R	0x0	Bist Error Count Returns BIST error count for selected port. Port selected is based on the PORT1_SEL control in the DUAL_RX_CTL register.

7.7.1.39 SCL_HIGH_TIME Register (Address = 0x26) [reset = 0x83]

SCL_HIGH_TIME is described in 表 7-51.

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表 7-51. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCL_HIGH_TIME	R/W	0x83	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Controller on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz. Note: Minimum allowed value for this register is 0x07.

7.7.1.40 SCL_LOW_TIME Register (Address = 0x27) [reset = 0x84]

SCL_LOW_TIME is described in 表 7-52.

Return to Summary Table.

表 7-52. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCL_LOW_TIME	R/W	0x84	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.

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7.7.1.41 DATAPATH_CONTROL_2 Register (Address = 0x28) [reset = 0x20]

DATAPATH_CONTROL_2 is described in 表 7-53.

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表 7-53. DATAPATH_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	1: Disable loading of this register from the forward channel, keeping locally witten values intact 0: Allow forward channel loading of this register
6	RESERVED	R	0x0	Reserved
5	VIDEO_DISABLED	R/W	0x1	Forward channel video disabled 0 : Normal operation 1 : Video is disabled, control channel is enabled This is a status bit indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled.
4	DUAL_LINK	R/W	0x0	1: Dual-Link mode enabled 0: Single-Link mode enabled This bit indicates whether the FPD3 serializer is in single link or dual link mode. This control is used for recovering forward channel data when the FPD3 Reciever is in auto-detect mode. To force DUAL_LINK receive mode, use the RX_PORT_SEL register (address 0x34).
3	ALTERNATE_I2S_ENABLE	R/W	0x0	1: Enable alternate I2S output on GPIO1 (word clock) and GPIO0 (data) 0: Normal Operation
2	I2S_DISABLED	R/W	0x0	1: I2S DISABLED 0: Normal Operation
1	28_BIT_VIDEO	R/W	0x0	1: 28 bit Video enable. i.e. HS, VS, DE are present in forward channel. 0: Normal Operation
0	I2S_SURROUND	R/W	0x0	1: I2S Surround enabled 0: I2S Surround disabled

7.7.1.42 FRC_CONTROL Register (Address = 0x29) [reset = 0x0]

FRC_CONTROL is described in 表 7-54.

Return to Summary Table.

表 7-54. FRC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Timing_Mode_Select	R/W	0x0	Select display timing mode 0: DE only Mode 1: Sync Mode (VS,HS)
6	HS_Polarity	R/W	0x0	0: Active High 1: Active Low
5	VS_Polarity	R/W	0x0	0: Active High 1: Active Low
4	DE_Polarity	R/W	0x0	0: Active High 1: Active Low
3	FRC2_Enable	R/W	0x0	0: FRC2 disable 1: FRC2 enable
2	FRC1_Enable	R/W	0x0	0: FRC1 disable 1: FRC1 enable
1	Hi-FRC2_Disable	R/W	0x0	0: Hi-FRC2 enable 1: Hi-FRC2 disable

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表 7-54. FRC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Hi-FRC1_Disable	R/W	0x0	0: Hi-FRC1 enable 1: Hi-FRC1 disable

7.7.1.43 WHITE_BALANCE_CONTROL Register (Address = 0x2A) [reset = 0x0]

WHITE_BALANCE_CONTROL is described in 表 7-55.

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表 7-55. WHITE_BALANCE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Page_Setting	R/W	0x0	Page setting 00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
5	White_Balance_Enable	R/W	0x0	0: White Balance Disable 1: White Balance Enable
4	LUT_Reload_Enable	R/W	0x0	0: Reload Disable 1: Reload Enable
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

7.7.1.44 I2S_CONTROL Register (Address = 0x2B) [reset = 0x0]

I2S_CONTROL is described in 表 7-56.

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表 7-56. I2S_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5-4	RESERVED	R	0x0	Reserved
3	I2S_FIFO_OVERRUN_STATUS	R	0x0	I2S FIFO Overrun Status
2	I2S_FIFO_UNDERRUN_STATUS	R	0x0	I2S FIFO Underrun Status
1	I2S_FIFO_ERROR_RESET	R/W	0x0	I2S Fifo Error Reset 1: Clears FIFO Error
0	I2S_DATA_FALLING_EDGE	R/W	0x0	I2S Clock Edge Select 1: I2S Data is strobed on the Rising Clock Edge. 0: I2S Data is strobed on the Falling Clock Edge.

7.7.1.45 PCLK_TEST_MODE Register (Address = 0x2E) [reset = 0x0]

PCLK_TEST_MODE is described in 表 7-57.

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表 7-57. PCLK_TEST_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EXTERNAL_PCLK	R/W	0x0	Select pixel clock from BISTC input

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表 7-57. PCLK_TEST_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	RESERVED	R	0x0	Reserved

7.7.1.46 DUAL_RX_CTL Register (Address = 0x34) [reset = 0x1]

DUAL_RX_CTL is described in 表 7-58.

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表 7-58. DUAL_RX_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RX_LOCK_MODE	R/W	0x0	RX Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0 : RX_LOCK asserted only when receiving active video (Forward channel VIDEO_DISABLED bit is 0) 1 : RX_LOCK asserted when device is linked to a Serializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but Deserializer is not receiving Audio/Video data.
5	RAW_2ND_BC	R/W	0x0	Enable Raw Secondary Back channel if this bit is set to a 1, the secondary back channel will operate in a raw mode, passing D_GPIO0 from the Deserializer to the Serializer, without any oversampling or filtering.
4-3	FPD3_INPUT_MODE	R/W	0x0	FPD-Link III Input Mode Determines operating mode of dual FPD-Link III Receive interface 00: Auto-detect based on received data 01: Forced Mode: Dual link 10: Forced Mode: Single link, primary input 11: Forced Mode: Single link, secondary input
2	RESERVED	R	0x0	Reserved
1	PORT1_SEL	R/W	0x0	Selects Port 1 for Register Access from primary I2C Address For writes, port1 registers and shared registers will both be written. For reads, port1 registers and shared registers will be read. This bit must be cleared to read port0 registers.
0	PORT0_SEL	R/W	0x1	Selects Port 0 for Register Access from primary I2C Address For writes, port0 registers and shared registers will both be written. For reads, port0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then port1 registers will be read.

7.7.1.47 AEQ_TEST Register (Address = 0x35) [reset = 0x0]

AEQ_TEST is described in 表 7-59.

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AEQ Test register: If PORT1_SEL is set, this register sets port1 AEQ controls.

表 7-59. AEQ_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	AEQ_RESTART	R/W	0x0	Set high to restart AEQ adaptation from initial value. Method is write HIGH then write LOW - not self clearing. Adaption will be restarted on both ports.
5	OVERRIDE_AEQ_FLOOR	R/W	0x0	Enable operation of SET_AEQ_FLOOR

表 7-59. AEQ_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SET_AEQ_FLOOR	R/W	0x0	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
3-1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.7.1.48 MODE_SEL Register (Address = 0x37) [reset = 0x0]

MODE_SEL is described in 表 7-60.

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表 7-60. MODE_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MODE_SEL1_DONE	R	0x0	MODE_SEL1 Done: 0: indicates the MODE_SEL1 decode has not been latched into the MODE_SEL1 status bits. 1: indicates the MODE_SEL1 decode has completed and latched into the MODE_SEL1 status bits. If set, indicates the MODE_SEL1 decode has completed and latched into the MODE_SEL1 status bits.
6-4	MODE_SEL1	R	0x0	MODE_SEL1 Decode 3-bit decode from MODE_SEL1 pin, see MODE_SEL1 Table 9 first column "#" for mode selection: 000: 5 Mbps/STP (#1 on MODE_SEL1) 001: 5 Mbps/Coax (#2 on MODE_SEL1) 010: 20 Mbps/STP (#3 on MODE_SEL1) 011: 20 Mbps/Coax (#4 on MODE_SEL1) 100: 5 Mbps/STP (#5 on MODE_SEL1) 101: 5 Mbps/Coax (#6 on MODE_SEL1) 110: 20 Mbps/STP (#7 on MODE_SEL1) 111: 20 Mbps/Coax (#8 on MODE_SEL1) Note: 0x37[6] is the MSB; 0x37[4] is the LSB
3	MODE_SEL0_DONE	R	0x0	MODE_SEL0 Done: 0: indicates the MODE_SEL0 decode has not been latched into the MODE_SEL0 status bits. 1: indicates the MODE_SEL0 decode has completed and latched into the MODE_SEL0 status bits. If set, indicates the MODE_SEL0 decode has completed and latched into the MODE_SEL0 status bits.
2-0	MODE_SEL0	R	0x0	MODE_SEL0 Decode 3-bit decode from MODE_SEL0 pin, see MODE_SEL0 in Table 8 first column "#" for mode selection: 000: Dual OLDI output (#1 on MODE_SEL0) 001: Dual SWAP output (#2 on MODE_SEL0) 010: Single OLDI output (#3 on MODE_SEL0) 011: Replicate (#4 on MODE_SEL0) 100: Dual OLDI output (#5 on MODE_SEL0) 101: Dual SWAP output (#6 on MODE_SEL0) 110: Single OLDI output (#7 on MODE_SEL0) 111: Replicate (#8 on MODE_SEL0) Note: 0x37[2] is the MSB; 0x37[0] is the LSB

7.7.1.49 I2S_DIVSEL Register (Address = 0x3A) [reset = 0x0]

I2S_DIVSEL is described in 表 7-61.

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表 7-61. I2S_DIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_ov_mdiv	R/W	0x0	0: No override for MCLK divider 1: Override divider select for MCLK
6-4	reg_mdiv	R/W	0x0	Divide ratio select for VCO output (32*REF/M) 000: Divide by 32 (=REF/M) 001: Divide by 16 (=2*REF/M) 010: Divide by 8 (=4*REF/M) 011: Divide by 4 (=8*REF/M) 100, 101: Divide by 2 (=16*REF/M) 110, 111: Divide by 1 (32*REF/M)
3	RESERVED	R	0x0	Reserved
2	reg_ov_mselect	R/W	0x0	0: Divide ratio of reference clock VCO selected by PLL-SM 1: Override divide ratio of clock to VCO
1-0	reg_mselect	R/W	0x0	Divide ratio select for VCO input (M) 00: Divide by 1 01: Divide by 2 10: Divide by 4 11: Divide by 8

7.7.1.50 EQ_STATUS Register (Address = 0x3B) [reset = 0x0]

EQ_STATUS is described in 表 7-62.

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Equalizer Status register: If PORT1_SEL is set, this register returns port1 status.

表 7-62. EQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5-0	EQ_status	R	0x0	EQ Status - setting direct to analog If Adaptive EQ is bypassed, these values are the {EQ2, EQ1} settings from the ADAPTIVE EQ BYPASS register (0x44). If Adaptive EQ is enabled, the EQ status is determined by the adaptive Equalizer.

7.7.1.51 LINK_ERROR_COUNT Register (Address = 0x41) [reset = 0x3]

LINK_ERROR_COUNT is described in 表 7-63.

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表 7-63. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R	0x0	Reserved
4	LINK_ERROR_COUNT_ENABLE	R/W	0x0	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
3-0	LINK_ERROR_COUNT	R/W	0x3	Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserializer loose lock once error count reaches threshold. If disabled deserilizer loose lock with one error.

7.7.1.52 HSCC_CONTROL Register (Address = 0x43) [reset = 0x0]

HSCC_CONTROL is described in 表 7-64.

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表 7-64. HSCC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	SPI_POCI_MODE	R/W	0x0	SPI POCI pin mode during Reverse SPI mode During Reverse SPI mode, SPI_POCI is typically an output signal. For bused SPI applications, it may be necessary to tri-state the SPI_POCI output if the device is not selected (SPI_CS = 0). 0 : Always enable SPI_POCI output driver 1 : Tri-state SPI_POCI output if SPI_CS is not asserted (low)
3	SPI_CPOL	R/W	0x0	SPI Clock Polarity Control 0 : SPI Data driven on Falling clock edge, sampled on Rising clock edge 1 : SPI Data driven on Rising clock edge, sampled on Falling clock edge
2-0	HSCC_MODE	R/W	0x0	High-Speed Control Channel Mode Enables high-speed modes for the secondary link back-channel, allowing higher speed signaling of GPIOs or SPI interface: These bits indicates the High Speed Control Channel mode of operation: 000: Normal frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode

7.7.1.53 ADAPTIVE_EQ_BYPASS Register (Address = 0x44) [reset = 0x60]

ADAPTIVE_EQ_BYPASS is described in 表 7-65.

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Adaptive Equalizer Bypass register: If PORT1_SEL is set, this register sets port1 AEQ controls.

表 7-65. ADAPTIVE_EQ_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	EQ_STAGE_1_SELECT_VALUE	R/W	0x3	EQ select value[2:0] - Used if adaptive EQ is bypassed. When ADAPTIVE_EQ_BYPASS is set to 1, these bits will be reflected in EQ Status[2:0] (register 0x3B)
4	RESERVED	R	0x0	Reserved
3-1	EQ_STAGE_2_SELECT_VALUE	R/W	0x0	EQ select value[5:3] - Used if adaptive EQ is bypassed. When ADAPTIVE_EQ_BYPASS is set to 1, these bits will be reflected in EQ Status[5:3] (register 0x3B)
0	ADAPTIVE_EQ_BYPASS	R/W	0x0	1: Disable adaptive EQ 0: Enable adaptive EQ

7.7.1.54 ADAPTIVE_EQ_MIN_MAX Register (Address = 0x45) [reset = 0x8]

ADAPTIVE_EQ_MIN_MAX is described in 表 7-66.

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If PORT1_SEL is set, this register sets port1 AEQ_FLOOR value. AEQ_FLOOR readback is only available on port0, that means writes to the port1 setting will still work but the written value can not be read back.

表 7-66. ADAPTIVE_EQ_MIN_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	100	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	ADAPTIVE_EQ_FLOOR_VALUE	R/W	0x8	When AEQ floor is enabled byregister {reg_35[5:4]} the starting setting is given by this register.

7.7.1.55 FPD_TX_MODE Register (Address = 0x49) [reset = X]

FPD_TX_MODE is described in 表 7-67.

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表 7-67. FPD_TX_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MAPSEL_MODE	R	X	Mapsel Pin Status Strap option on the MODE_SEL0 pin
6	MAPSEL_OVER_WRITE	R/W	0x0	Mapsel Over Write enable from register configuration
5	MAPSEL_REG_BIT	R/W	0x0	Register setting of MAPSEL mode if MAPSEL OVER WRITE is set
4-2	RESERVED	R	0x0	Reserved
1-0	FPD_OUT_MODE	R/W	X	FPD/OLDI output mode Controls single/dual operation of the FPD Transmit ports 00 : Dual FPD/OLDI output 01 : Dual SWAP FPD/OLDI output 10 : Single FPD/OLDI output 11 : Replicate FPD/OLDI output The FPD_OUT_MODE register bits are loaded at reset from the MODE_SEL0 pin strap options.

7.7.1.56 LVDS_CONTROL Register (Address = 0x4B) [reset = 0x8]

LVDS_CONTROL is described in 表 7-68.

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表 7-68. LVDS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R/W	0x10	Reserved
1-0	LVDS_VOD_Control	R/W	0x0	FPD/OLDI Output VOD Setting 00: Setting 1 - 190mV typical voltage swing (single-ended) 01: Setting 2 - 275mV typical voltage swing (single-ended) 10: Setting 3 - 325mV typical voltage swing (single-ended) 11: Setting 4 - 375mV typical voltage swing (single-ended). Note: Changing this value for Port1 requires selecting Port1 in reg 0x34.

7.7.1.57 CML_OUTPUT_CTL1 Register (Address = 0x52) [reset = 0x0]

CML_OUTPUT_CTL1 is described in 表 7-69.

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表 7-69. CML_OUTPUT_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CML_Channel_Select_1	R/W	0x0	Selects between PORT0 and PORT1 to output onto CMLOUT±. 0: Recovered forward channel data from RIN0± is output on CMLOUT± 1: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This bit must match 0x57[2:1] setting for PORT0 or PORT1.
6	RESERVED	R	0x0	Reserved
5-2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

7.7.1.58 CML_OUTPUT_ENABLE Register (Address = 0x56) [reset = 0x0]

CML_OUTPUT_ENABLE is described in 表 7-70.

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表 7-70. CML_OUTPUT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	CML_Output_Enable	R/W	0x0	Enable CMLOUT± Loop-through Driver 0: Disabled (Default) 1: Enabled
2-1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.7.1.59 CML_OUTPUT_CTL2 Register (Address = 0x57) [reset = 0x0]

CML_OUTPUT_CTL2 is described in 表 7-71.

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表 7-71. CML_OUTPUT_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2-1	CML_CHANNEL_SELECT_2	R/W	0x0	Selects between PORT0 and PORT1 to output onto CMLOUT±. 01: Recovered forward channel data from RIN0± is output on CMLOUT± 10: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This must match 0x52[7] setting for PORT0 or PORT1.Note: Due to internal routing differences between CMLOUT0 and CMLOUT1 inside the device, CMLOUT1 monitor may show significantly degraded performance when compared to CMLOUT0, especially at high PCLK frequency. This does not necessarily indicate an issue with the true channel performance.
0	RESERVED	R	0x0	Reserved

7.7.1.60 CML_OUTPUT_CTL3 Register (Address = 0x63) [reset = 0x0]

CML_OUTPUT_CTL3 is described in 表 7-72.

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表 7-72. CML_OUTPUT_CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	CML_TX_PWDN	R/W	0x0	Powerdown CML TX 0: CML TX powered up 1: CML TX powered down NOTE: CML TX must be powered down prior to enabling Pattern Generator.

7.7.1.61 PGCTL Register (Address = 0x64) [reset = 0x10]

PGCTL is described in 表 7-73.

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表 7-73. PGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode: 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/White to Cyan 1000: Horizontally Scaled Black to Green/White to Magenta 1001: Horizontally Scaled Black to Blue/White to Yellow 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertically Scaled Black to Green/White to Magenta 1101: Vertically Scaled Black to Blue/White to Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved
3	PATGEN_UNH	R/W	0x0	Enables the UNH-IOL compliance test pattern: 0: Pattern type selected by PATGEN_SEL 1: Compliance test pattern is selected. Value of PATGEN_SEL is ignored.
2	PATGEN_COLOR_BARS	R/W	0x0	Enable Color Bars: 0: Color Bars disabled 1: Color Bars enabled (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)
1	PATGEN_VCOM_REV	R/W	0x0	Reverse order of color bands in VCOM pattern: 0: Color sequence from top left is (Yellow, Cyan, Blue, Red) 1: Color sequence from top left is (Blue, Cyan, Yellow, Red)

表 7-73. PGCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PATGEN_EN	R/W	0x0	Pattern Generator Enable: 1: Enable Pattern Generator 0: Disable Pattern Generator NOTE: CML TX must be powered down prior to enabling Pattern Generator by setting register bit 0x63[0]=1.

7.7.1.62 PGCFG Register (Address = 0x65) [reset = 0x0]

PGCFG is described in 表 7-74.

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表 7-74. PGCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	PATGEN_18B	R/W	0x0	18-bit Mode Select: 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
3	PATGEN_EXTCLK	R/W	0x0	Select External Clock Source: 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

7.7.1.63 PGIA Register (Address = 0x66) [reset = 0x0]

PGIA is described in 表 7-75.

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表 7-75. PGIA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_IA	R/W	0x0	Indirect Address: This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register.

7.7.1.64 PGID Register (Address = 0x67) [reset = 0x0]

PGID is described in 表 7-76.

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表 7-76. PGID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

7.7.1.65 PGDBG Register (Address = 0x68) [reset = 0x0]

PGDBG is described in 表 7-77.

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表 7-77. PGDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	PATGEN_BIST_EN	R/W	0x0	Pattern Generator BIST Enable: Enables Pattern Generator in BIST mode. Pattern Generator will compare received video data with local generated pattern. Upstream device must be programmed to the same pattern.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.7.1.66 PGTSTDAT Register (Address = 0x69) [reset = 0x0]

PGTSTDAT is described in 表 7-78.

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表 7-78. PGTSTDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PATGEN_BIST_ERR	R	0x0	Pattern Generator BIST Error Flag During Pattern Generator BIST mode, this bit indicates if the BIST engine has detected errors. If the BIST Error Count (available in the Pattern Generator indirect registers) is non-zero, this flag will be set.
6	RESERVED	R	0x0	Reserved
5-0	RESERVED	R	0x0	Reserved

7.7.1.67 GPI_PIN_STATUS_1 Register (Address = 0x6E) [reset = 0x0]

GPI_PIN_STATUS_1 is described in 表 7-79.

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表 7-79. GPI_PIN_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI7_Pin_Status	R	0x0	GPI7/I2S_WC pin status
6	GPI6_Pin_Status	R	0x0	GPI6/I2S_DA pin status
5	GPI5_Pin_Status	R	0x0	GPI5/I2S_DB pin status
4	RESERVED	R	0x0	Reserved
3	GPI3_Pin_Status	R	0x0	GPI3 / I2S_DD pin status
2	GPI2_Pin_Status	R	0x0	GPI2 / I2S_DC pin status
1	GPI1_Pin_Status	R	0x0	GPI1 pin status

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表 7-79. GPI_PIN_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GPI0_Pin_Status	R	0x0	GPI0 pin status

7.7.1.68 GPI_PIN_STATUS_2 Register (Address = 0x6F) [reset = 0x0]

GPI_PIN_STATUS_2 is described in 表 7-80.

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表 7-80. GPI_PIN_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved
0	GPI8_Pin_Status	R	0x0	GPI8/I2S_CLK pin status

7.7.1.69 RX_BKSV0 Register (Address = 0x80) [reset = 0x0]

RX_BKSV0 is described in 表 7-81.

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表 7-81. RX_BKSV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV0	R	0x0	BKSV0: Value of byte0 of the Receiver KSV.

7.7.1.70 RX_BKSV1 Register (Address = 0x81) [reset = 0x0]

RX_BKSV1 is described in 表 7-82.

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表 7-82. RX_BKSV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV1	R	0x0	BKSV1: Value of byte1 of the Receiver KSV.

7.7.1.71 RX_BKSV2 Register (Address = 0x82) [reset = 0x0]

RX_BKSV2 is described in 表 7-83.

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表 7-83. RX_BKSV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV2	R	0x0	BKSV2: Value of byte2 of the Receiver KSV.

7.7.1.72 RX_BKSV3 Register (Address = 0x83) [reset = 0x0]

RX_BKSV3 is described in 表 7-84.

Return to Summary Table.

表 7-84. RX_BKSV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV3	R	0x0	BKSV3: Value of byte3 of the Receiver KSV.

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7.7.1.73 RX_BKSV4 Register (Address = 0x84) [reset = 0x0]

RX_BKSV4 is described in 表 7-85.

Return to Summary Table.

表 7-85. RX_BKSV4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV4	R	0x0	BKSV4: Value of byte4 of the Receiver KSV.

7.7.1.74 TX_KSV0 Register (Address = 0x90) [reset = 0x0]

TX_KSV0 is described in 表 7-86.

Return to Summary Table.

表 7-86. TX_KSV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV0	R	0x0	TX_KSV0: Value of byte0 of the Transmitter KSV.

7.7.1.75 TX_KSV1 Register (Address = 0x91) [reset = 0x0]

TX_KSV1 is described in 表 7-87.

Return to Summary Table.

表 7-87. TX_KSV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV1	R	0x0	TX_KSV1: Value of byte1 of the Transmitter KSV.

7.7.1.76 TX_KSV2 Register (Address = 0x92) [reset = 0x0]

TX_KSV2 is described in 表 7-88.

Return to Summary Table.

表 7-88. TX_KSV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV2	R	0x0	TX_KSV2: Value of byte2 of the Transmitter KSV.

7.7.1.77 TX_KSV3 Register (Address = 0x93) [reset = 0x0]

TX_KSV3 is described in 表 7-89.

Return to Summary Table.

表 7-89. TX_KSV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV3	R	0x0	TX_KSV3: Value of byte3 of the Transmitter KSV.

7.7.1.78 TX_KSV4 Register (Address = 0x94) [reset = 0x0]

TX_KSV4 is described in 表 7-90.

Return to Summary Table.

表 7-90. TX_KSV4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV4	R	0x0	TX_KSV4: Value of byte4 of the Transmitter KSV.

7.7.1.79 HDCP_DBG Register (Address = 0xC0) [reset = X]

HDCP_DBG is described in 表 7-91.

Return to Summary Table.

表 7-91. HDCP_DBG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	HDCP_I2C_TO_DIS	R	X	HDCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C Controller. When enabled, the bus timeout function allows the I2C Controller to assume the bus is free if no signaling occurs for more than 1 second. Set via the HDCP_DBG register in the HDCP Transmitter.
5-4	RESERVED	R	0x0	Reserved
3	RGB_CHKSUM_EN	R	0x0	Enable RGB video line checksum: Enables sending of ones-complement checksum for each 8-bit RGB data channel following end of each video data line. Set via the HDCP_DBG register in the HDCP Transmitter.
2	FAST_LV	R	0x0	Fast Link Verification: HDCP periodically verifies that the HDCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames. Set via the HDCP_DBG register in the HDCP Transmitter.
1	TMR_SPEEDUP	R	0x0	Timer Speedup: Speed up HDCP authentication timers. Set via the HDCP_DBG register in the HDCP Transmitter.
0	HDCP_I2C_FAST	R	0x0	HDCP I2C Fast mode Enable: Setting this bit to a 1 will enable the HDCP I2C Controller in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Controller will operation with Standard mode timing. Set via the HDCP_DBG register in the HDCP Transmitter.

7.7.1.80 HDCP_DBG2 Register (Address = 0xC1) [reset = 0x0]

HDCP_DBG2 is described in 表 7-92.

Return to Summary Table.

表 7-92. HDCP_DBG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	NO_DECRYPT	R/W	0x0	No Decrypt: When set to a 1, the HDCP Receiver will output the encrypted data on the RGB pins. All other functions will work normally. This provides a simple way of showing that the link is encrypted.

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表 7-92. HDCP_DBG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HDCP_EN_MODE	R/W	0x0	HDCP Enable Mode: This bit controls whether the HDCP Repeater function will enable HDCP in attached HDCP Transmitters if it detects HDCP is already enabled 1 : Don't re-enable HDCP if already enabled 0 : Re-enable HDCP at start of authentication, even if HDCP Transmitter already has HDCP enabled

7.7.1.81 HDCP_STS Register (Address = 0xC4) [reset = 0x0]

HDCP_STS is described in 表 7-93.

Return to Summary Table.

表 7-93. HDCP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	RGB_CHKSUM_ERR	R	0x0	RGB Checksum Error Detected: If RGB Checksum in enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register
0	AUTHED	R	0x0	HDCP Authenticated: Indicates the HDCP authentication has completed suc-cessfully. The controller may now send video data re-quiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authen-tication.

7.7.1.82 KSV_FIFO__DATA Register (Address = 0xC9) [reset = 0x0]

KSV_FIFO__DATA is described in 表 7-94.

Return to Summary Table.

表 7-94. KSV_FIFO__DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KSV_FIFO__DATA	R/W	0x0	NVM Data: Texas Instruments Use Only Writing a value to this register will write the data into the NVM SRAM at the address currently selected by the NVM_ADDR0 and NVM_ADDR1 registers. In NVM Parallel load operation, the lowest bit of this register acts as a Memory Enable for the clock and data. Setting NVM_DATA[0] to a one will enable NVM SRAM writes. Setting to a zero will disable NVM SRAM writes. KSV_FIFO_DATA: During External Repeater Control mode, the External HDCP controller writes KSV data to the KSV FIFO through this register. A byte written to this register location will write one byte of KSV data to the KSV FIFO at the location indicated by the KSV_FIFO_ADDR registers.

7.7.1.83 KSV_FIFO_A_DDR0 Register (Address = 0xCA) [reset = 0x0]

KSV_FIFO_A_DDR0 is described in 表 7-95.

Return to Summary Table.

表 7-95. KSV_FIFO_A_DDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KSV_FIFO__ADDR0	R/W	0x0	NVM Address Register 0: Texas Instruments Use Only This register contains the lower 8 bits of the NVM SRAM address. KSV FIFO Address Register 0: This register contains the lower 8 bits of the KSF FIFO Address. This value should be set to 0 before writing the first byte of KSV data to the KSV FIFO. The KSV FIFO Address will automatically increment for each write to the KSV_FIFO_DATA register.

7.7.1.84 KSV_FIFO_ADDR1 Register (Address = 0xCB) [reset = 0x0]

KSV_FIFO_ADDR1 is described in 表 7-96.

Return to Summary Table.

表 7-96. KSV_FIFO_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description

7.7.1.85 RPTR_TX0 Register (Address = 0xE0) [reset = 0x0]

RPTR_TX0 is described in 表 7-97.

Return to Summary Table.

表 7-97. RPTR_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT0_ADDR	R	0x0	Transmit Port 0 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT0_VALID	R	0x0	Transmit Port 0 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

7.7.1.86 RPTR_TX1 Register (Address = 0xE1) [reset = 0x0]

RPTR_TX1 is described in 表 7-98.

Return to Summary Table.

表 7-98. RPTR_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT1_ADDR	R	0x0	Transmit Port 1 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT1_VALID	R	0x0	Transmit Port 1 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

7.7.1.87 RPTR_TX2 Register (Address = 0xE2) [reset = 0x0]

RPTR_TX2 is described in 表 7-99.

Return to Summary Table.

表 7-99. RPTR_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT2_ADDR	R	0x0	Transmit Port 2 I2C Address Indicates the I2C address for the Repeater Transmit Port.

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表 7-99. RPTR_TX2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PORT2_VALID	R	0x0	Transmit Port 2 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

7.7.1.88 RPTR_TX3 Register (Address = 0xE3) [reset = 0x0]

RPTR_TX3 is described in 表 7-100.

Return to Summary Table.

表 7-100. RPTR_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT3_ADDR	R	0x0	Transmit Port 3 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT3_VALID	R	0x0	Transmit Port 3 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

7.7.1.89 XRPTR_STS Register (Address = 0xE8) [reset = 0x0]

XRPTR_STS is described in 表 7-101.

Return to Summary Table.

表 7-101. XRPTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1	RX_ENCRYPTED	R	0x0	RX Encrypted: Indicates Repeater is receiving encrypted data
0	KSV_WRITTEN	R	0x0	KSV Written: This flag will be set after the upstream device has written the Aksv value to the HDCP Repeater. This bit will be cleared once Ready has been asserted following setting of the XRPTR_LIST_RDY flag in the XRPTR_CTL register.

7.7.1.90 XRPTR_CTL Register (Address = 0xE9) [reset = 0x0]

XRPTR_CTL is described in 表 7-102.

Return to Summary Table.

表 7-102. XRPTR_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	XRPTR_NO_INBAND	R/W	0x0	External Control Inband Signaling disable: This bit controls whether the Repeater will send inband encryption and AVMUTE controls to the attached HDCP Transmitters 0 : Send Encryption/AVMUTE controls inband with video data 1 : Don't send Encryption/AVMUTE controls inband with video data
2	XRPTR_HPD	R/W	0x0	External Control Hot-Plug Detect This bit should be set following detection of a new downstream HDCP Receiver. This signal should remain high for a short period of time and then cleared.

表 7-102. XRPTR_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XRPTR_LIST_RDY	R/W	0x0	Repeater KSV List Ready: This register bit indicates to the device that the BStatus and KSV List data have been loaded for the HDCP Repeater. Following setting of this bit, the device will compute the SHA-1 checksum and indicate Ready to the upstream device. This flag will read-back a 1 after computing the SHA-1 value. The value will be cleared if a new KSV is written by the upstream device.
0	XRPTR_ENABLE	R/W	0x0	Repeater External Control Enable: Setting this bit will disable the internal HDCP Repeater controller and allow use of an external controller for HDCP Repeater operations. This mode is useful in devices that may include multiple upstream HDCP capable video sources.

7.7.1.91 XRPTR_BSTS0 Register (Address = 0xEA) [reset = 0x0]

XRPTR_BSTS0 is described in 表 7-103.

Return to Summary Table.

表 7-103. XRPTR_BSTS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	XRPTR_MAX_DEVS	R/W	0x0	External Control Max Devices Exceeded Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater 's KSV FIFO.
6-0	XRPTR_DEV_CNT	R/W	0x0	External Control Device Count Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0.

7.7.1.92 XRPTR_BSTS1 Register (Address = 0xEB) [reset = 0x0]

XRPTR_BSTS1 is described in 表 7-104.

Return to Summary Table.

表 7-104. XRPTR_BSTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	XRPTR_MAX_CASCADE	R/W	0x0	External Control Max Cascade Exceeded Indicates a topology error was detected. Indicates that more than seven levels of repeaters have been cascaded together.
2-0	XRPTR_DEPTH	R/W	0x0	External Control Cascade Depth Indicates the number of attached levels of devices for the Repeater.

7.7.1.93 HDCP_RX_ID0 Register (Address = 0xF0) [reset = 0x5F]

HDCP_RX_ID0 is described in 表 7-105.

Return to Summary Table.

表 7-105. HDCP_RX_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID0	R	0x5F	HDCP_RX_ID0: First byte ID code, '_ '

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7.7.1.94 HDCP_RX_ID1 Register (Address = 0xF1) [reset = 0x55]

HDCP_RX_ID1 is described in 表 7-106.

Return to Summary Table.

表 7-106. HDCP_RX_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID1	R	0x55	HDCP_RX_ID1: 2nd byte of ID code, 'U '

7.7.1.95 HDCP_RX_ID2 Register (Address = 0xF2) [reset = 0x48]

HDCP_RX_ID2 is described in 表 7-107.

Return to Summary Table.

表 7-107. HDCP_RX_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID2	R	0x48	HDCP_RX_ID2: 3rd byte of ID code. Value will be either 'B ' or 'H '. 'H ' indicates an HDCP capable device.

7.7.1.96 HDCP_RX_ID3 Register (Address = 0xF3) [reset = 0x39]

HDCP_RX_ID3 is described in 表 7-108.

Return to Summary Table.

表 7-108. HDCP_RX_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID3	R	0x39	HDCP_RX_ID3: 4th byte of ID code: '9 '

7.7.1.97 HDCP_RX_ID4 Register (Address = 0xF4) [reset = 0x34]

HDCP_RX_ID4 is described in 表 7-109.

Return to Summary Table.

表 7-109. HDCP_RX_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID4	R	0x34	HDCP_RX_ID4: 5th byte of ID code.

7.7.1.98 HDCP_RX_ID5 Register (Address = 0xF5) [reset = 0x38]

HDCP_RX_ID5 is described in 表 7-110.

Return to Summary Table.

表 7-110. HDCP_RX_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID5	R	0x38	HDCP_RX_ID5: 6th byte of ID code.

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8 Application and Implementation

注

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8.1 Application Information

The DS90UH948-Q1 is a FPD-Link III deserializer which, in conjunction with the DS90UH949/947-Q1 serializers, converts 1-lane or 2-lane FPD-Link III streams into a FPD-Link (OpenLDI) interface. The deserializer is capable of operating over cost-effective 50-Ω single-ended coaxial or 100-Ω differential shielded twisted-pair (STP) cables. It recovers the data from two FPD-Link III serial streams and translates it into dual pixel FPD-Link (data lanes + clock) supporting video resolutions up to WUXGA and 2K with 24-bit color depth. This provides a bridge between HDMI enabled sources such as GPUs to connect to existing LVDS displays or application processors.

8.2 Typical Applications

Bypass capacitors must be placed near the power supply pins. At a minimum, use four (4) 10-µF capacitors for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3 V or 1.8 V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See 図 8-1 for a typical STP connection diagram and 図 8-2 for a typical coax connection diagram.

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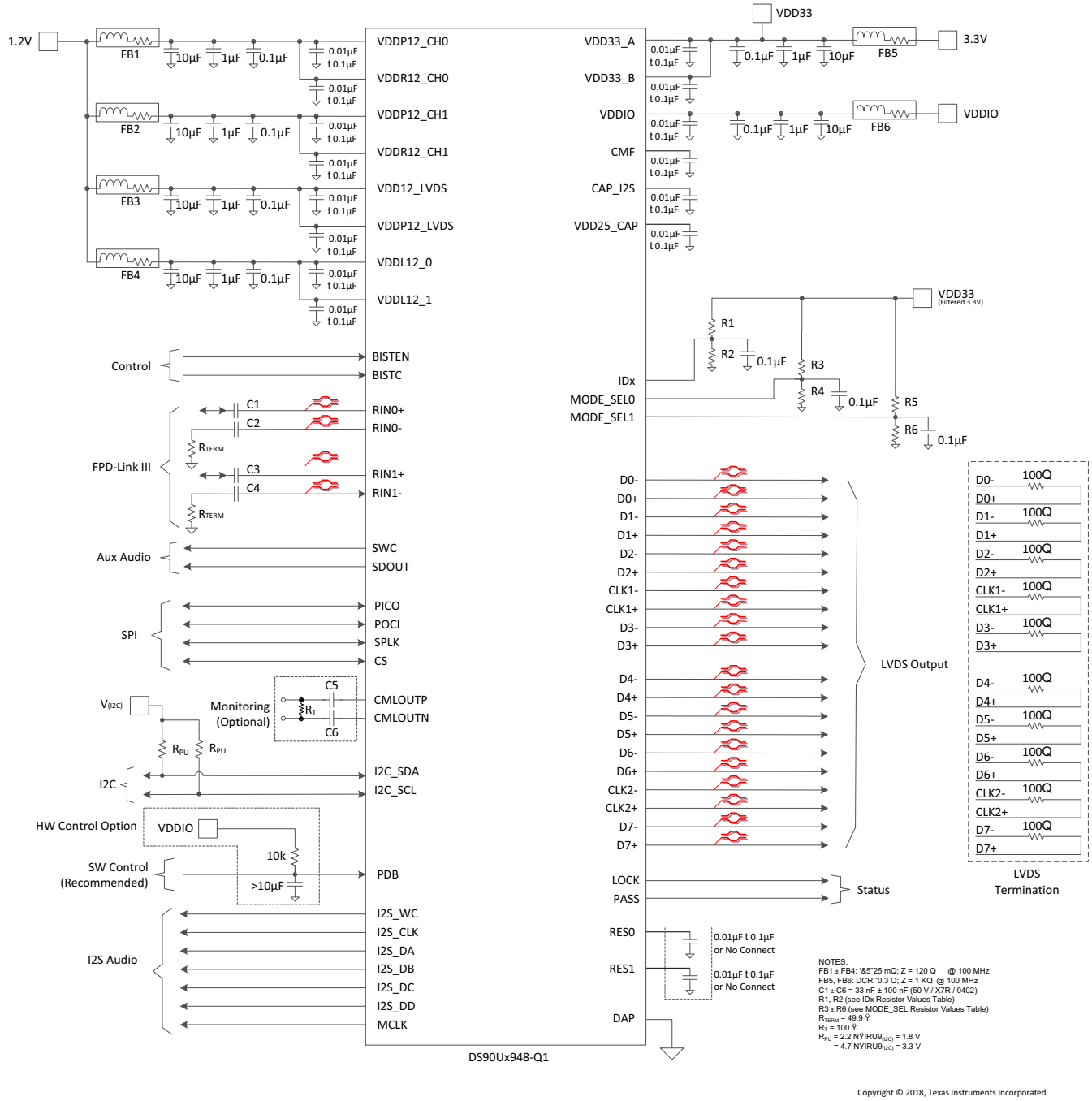

図 8-1. Typical Connection Diagram (Coax)

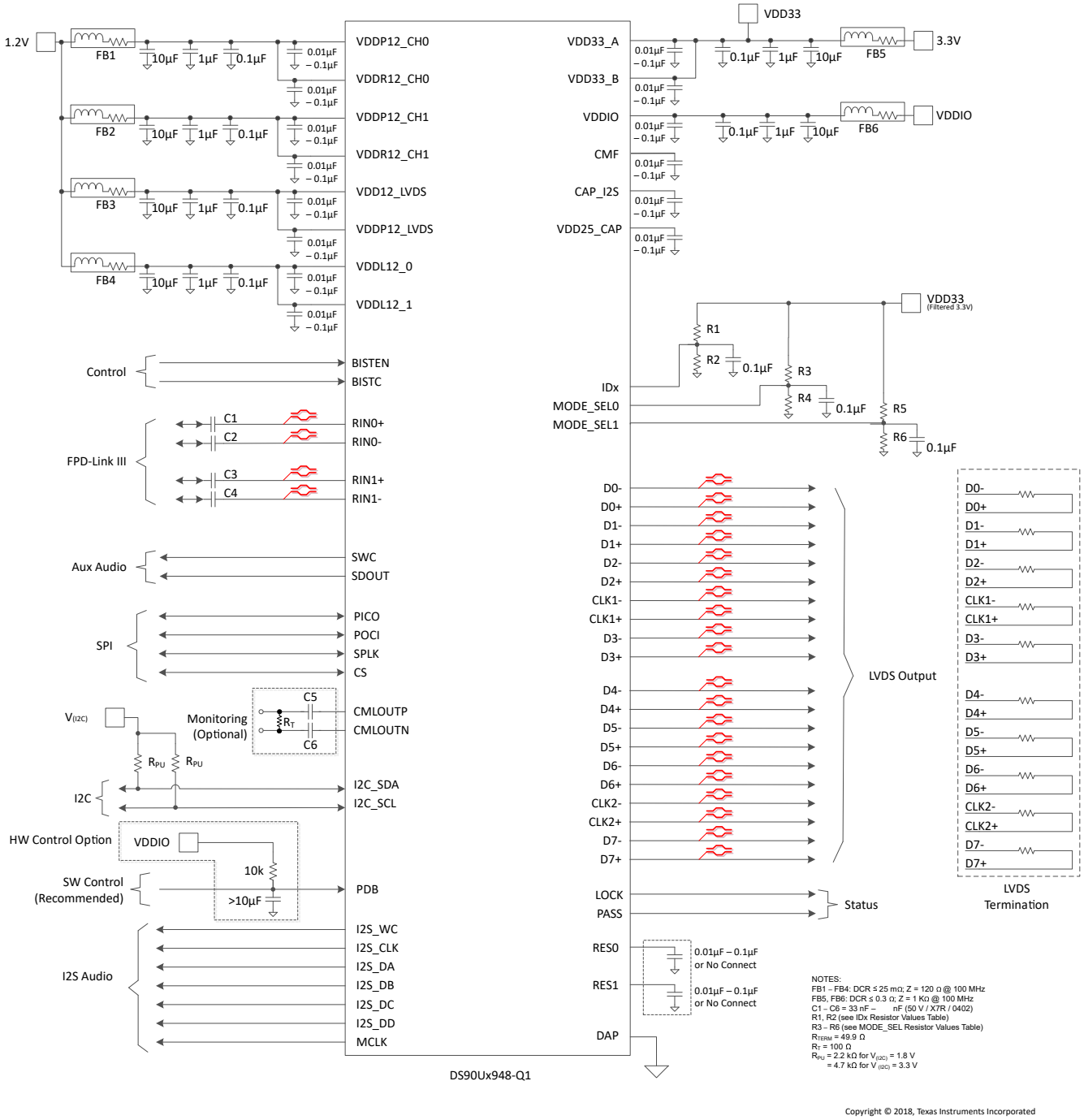

図 8-2. Typical Connection Diagram (STP)

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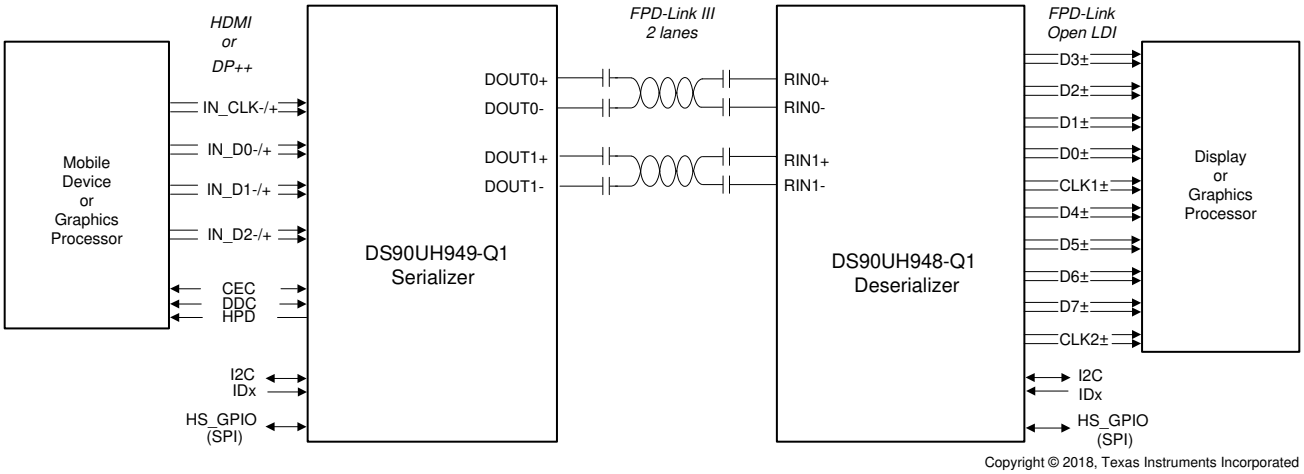

図 8-3. Typical Display System Diagram

8.2.1 Design Requirements

For the typical design application, use the following as input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD33	3.3 V
VDDIO	1.8 or 3.3 V
VDD12	1.2 V
AC-coupling capacitor for STP with 925/927: RIN[1:0]±	100 nF
AC-coupling capacitor for STP with 929/947/949: RIN[1:0]±	33 nF - 100 nF
AC-coupling capacitor for Coax with 921: RIN[1:0]+	100 nF
AC-coupling capacitor for Coax with 921: RIN[1:0]-	47 nF
AC-coupling capacitor for Coax with 929/947/949: RIN[1:0]+	33 nF - 100 nF
AC-coupling capacitor for Coax with 929/947/949: RIN[1:0]+	15 nF - 47 nF

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in 図 8-4. For applications using single-ended 50-Ω coaxial cable, the unused data pins (RIN0– and RIN1–) must use a 15-nF to 47-nF capacitor and must be terminated with a 50-Ω resistor.

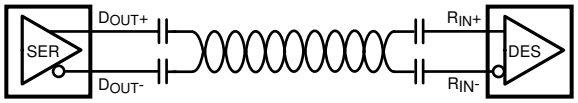

図 8-4. AC-Coupled Connection (STP)

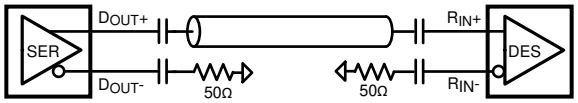

図 8-5. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor. This minimizes degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

8.2.2.1 FPD-Link III Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER Operation and Application Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187) available in PDF format from the Texas Instruments web site.

8.2.2.2 AV Mute Prevention

The DS90UH948Q-Q1 supports AV MUTE functionality when receiving the specifically defined data pattern (0x666666) during the blanking period (DE = LOW). Once the device enters the AV MUTE state, the device mutes both audio and video outputs resulting in a black display screen.

Be advised if the video source continues sending random data during blanking interval, the deserializer may inadvertently enter the AV MUTE state upon receiving random data matching the AV MUTE command pattern. When paired with a UB version FPD-Link compatible serializer, setting the gate DE Register 0x04[4] will prevent video signals from being sent during the blanking interval. This will ensure AV MUTE mode is not entered during normal operation. By default the Data Enable (DE) signal is assumed to be active high. If DE is active low, then setting DE_POLARITY register bit 0x12 bit[5] = 1 is also required. With the DE permanently LOW, deserializers do not check for the AV Mute conditions, so the AV Mute is not an issue when operating with HSYNC/VSYNC only mode displays.

If unexpected AV MUTE state is seen, it is recommended to verify checking the data path control setting of the paired Serializer. This setting is not accessible from DS90UH948Q-Q1.

When the DS90UH948Q-Q1 is paired with a compatible "UH" Serializer, inadvertently entering the AVMUTE state is not possible as the "UH" Serializers do not send video data during the blanking interval. Setting the register 0x12 bit 6, PASS_RGB is not recommended as it will make the "UH" Serializers function as "UB" Serializers and induce the possibility of inadvertently entering the AVMUTE state.

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8.2.2.3 Prevention of I2C Errors During Abrupt System Faults

In rare instances, FPD-Link III bi-directional control channel data errors caused by system fault conditions (e.g. abrupt power downs of the remote serializer or cable disconnects) may result in the DS90UH948Q-Q1 sending inadvertent I2C transactions on the local I2C bus prior to determining loss of valid signal.

For minimizing impact of these types of events, TI suggests the following precautions:

- Set DS90UH948Q-Q1 register 0x04 = 0x02 to minimize the duration of inadvertent I2C events
- Ensure all I2C Controllers on the bus support multi-Controller arbitration
- Assign I2C addresses with more than a single bit set to 1 for all devices on the I2C bus
  - 0x6A, 0x7B, and 0x37 are examples of good choices for an I2C address
  - 0x40 and 0x20 are examples of bad choices for an I2C address

8.2.3 Application Curves

The plots below correspond to 1080p60 video application with a 2-lane FPD-Link III input and dual OpenLDI output.

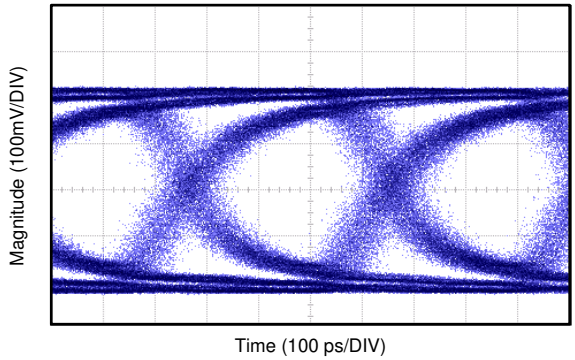


図 8-6. Loop-Through CML Output at 2.6-Gbps Serial Line Rate

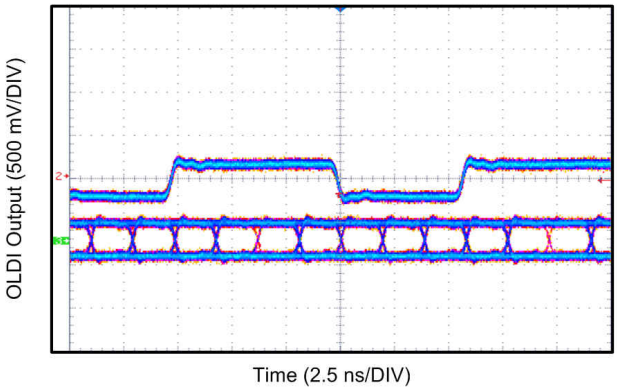


図 8-7. OpenLDI Clock and Data Output at 74.25-MHz Pixel Clock

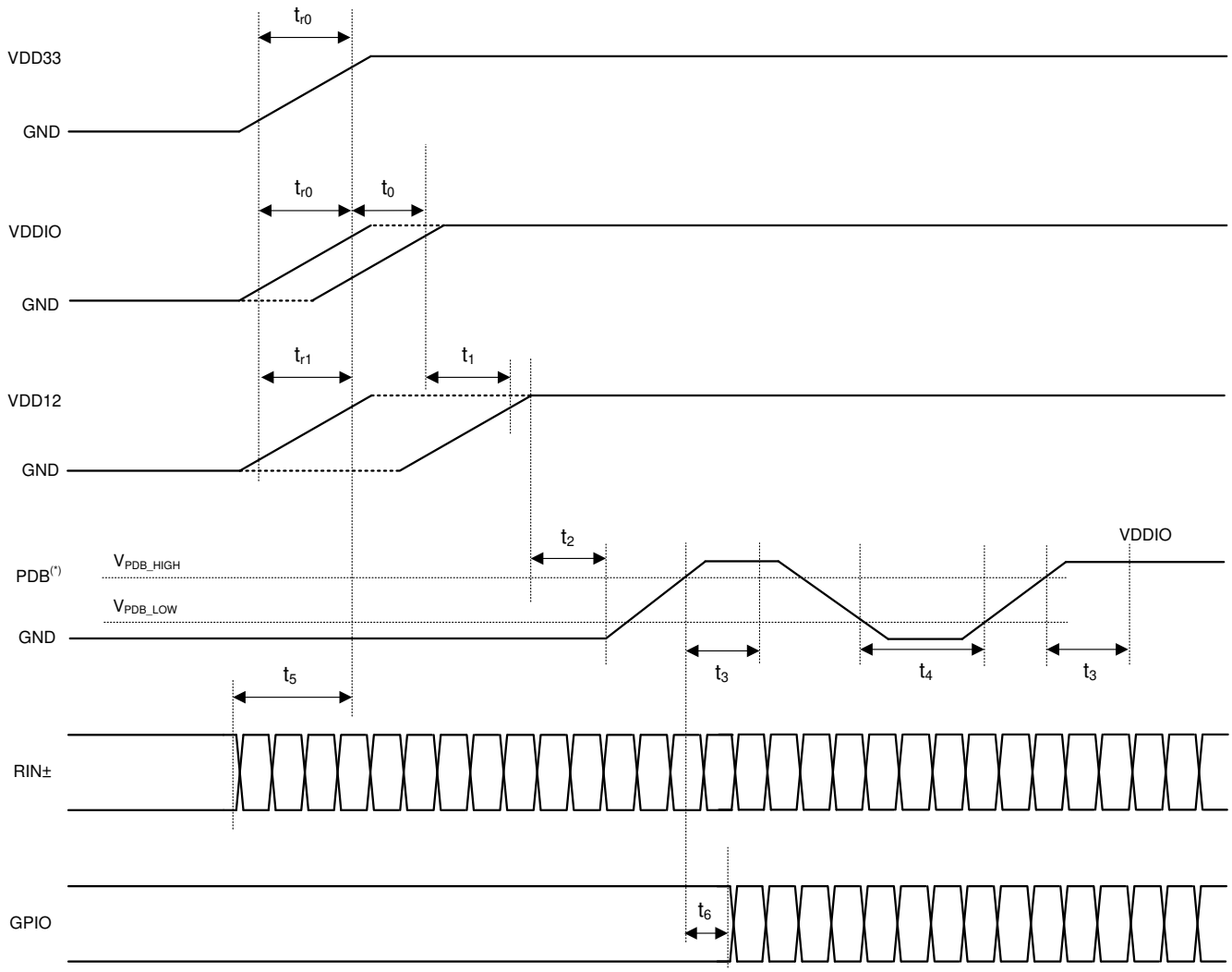
9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. *表 5-1* provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 Power-Up Requirements and PDB Pin

When power is applied, power from the highest voltage rail to the lowest voltage rail on any of the supply pins. For 3.3-V IO operation, VDDIO and VDD33 can be powered by the same supply and ramped simultaneously. Use a large capacitor on the PDB pin to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD33, a 10-kΩ pullup and a > 10–µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both VDD33 and VDDIO has reached steady state. Pins VDD33_A and VDD33_B must both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

9.2 Power Sequence



(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

図 9-1. Power Sequence

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表 9-1. Power-Up Sequencing Constraints

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
t_{r0}	VDD33 / VDDIO rise time	0.2			ms	@10/90%
t_{r1}	VDD12 rise time	0.05			ms	@10/90%
t_0	VDD33 to VDDIO delay	0			ms	
t_1	VDD33 / VDDIO to VDD12 delay	0			ms	
t_2	VDDx to PDB delay	0			ms	Release PDB after all supplies are up and stable.
t_3	PDB to I2C ready delay	2			ms	
t_4	PDB pulse width	2			ms	Hard reset
t_5	Valid data on RIN± to VDDx delay	0			ms	Provide valid data from a compatible Serializer before power-up . (1)
t_6	PDB to GPIO delay	2			ms	Keep GPIOs low or high until PDB is high.

(1) Note that the DS90UH948Q-Q1 should be powered up after a compatible Serializer has started sending valid video data. If this condition is not satisfied, then a digital (software) reset or hard reset (toggling PDB pin) is required after receiving the input data. This requirement prevents the DS90UH948Q-Q1 from locking to any random or noise signal, ensures DS90UH948Q-Q1 has a deterministic startup behavior, specified lock time, and optimal adaptive equalizer setting.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pick-up, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Ceramic capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the ceramic capacitors must be at least 5× the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from power and ground pins to the planes to reduce the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coaxial interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Information on the WQFN package is provided *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

10.2 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the device to this plane with vias.

At least 32 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the WQFN style package, including PCB design and manufacturing requirements, is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNLU165).

10.3 Routing FPD-Link III Signal Traces

Routing the FPD-Link III signal traces between the R_{IN} pins and the connector is the most critical pieces of a successful PCB layout. 図 10-2 shows an example PCB layout. For additional PCB layout details of the example, refer to the *DS90UH948-Q1EVM User's Guide* (SNLU162).

The following list provides essential recommendations for routing the FPD-Link III signal traces between the receiver input pins (R_{IN}) and the connector.

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- The routing of the FPD-Link III traces may be all on the top layer or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors should be on the top layer and very close to the receiver input pins.
- Route the RIN traces between the AC-coupling capacitor and the connector as a 100-Ω differential micro-strip with tight impedance control (±10%). Calculate the proper width of the traces for a 100-Ω differential impedance based on the PCB stack-up.
- When choosing to implement a common mode choke for common mode noise reduction, minimize the effects of any impedance mismatch.
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the thru-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.

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10.4 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in 図 10-1:

表 10-1. No Pullback WQFN Stencil Aperture Summary

DEVICE	PIN COUNT	MKT DWG	PCB I/O Pad SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE(mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UH948-Q1	64	NKD	0.25 × 0.6	0.5	7.2 x 7.2	0.25 x 0.6	1.16 × 1.16	25	0.2

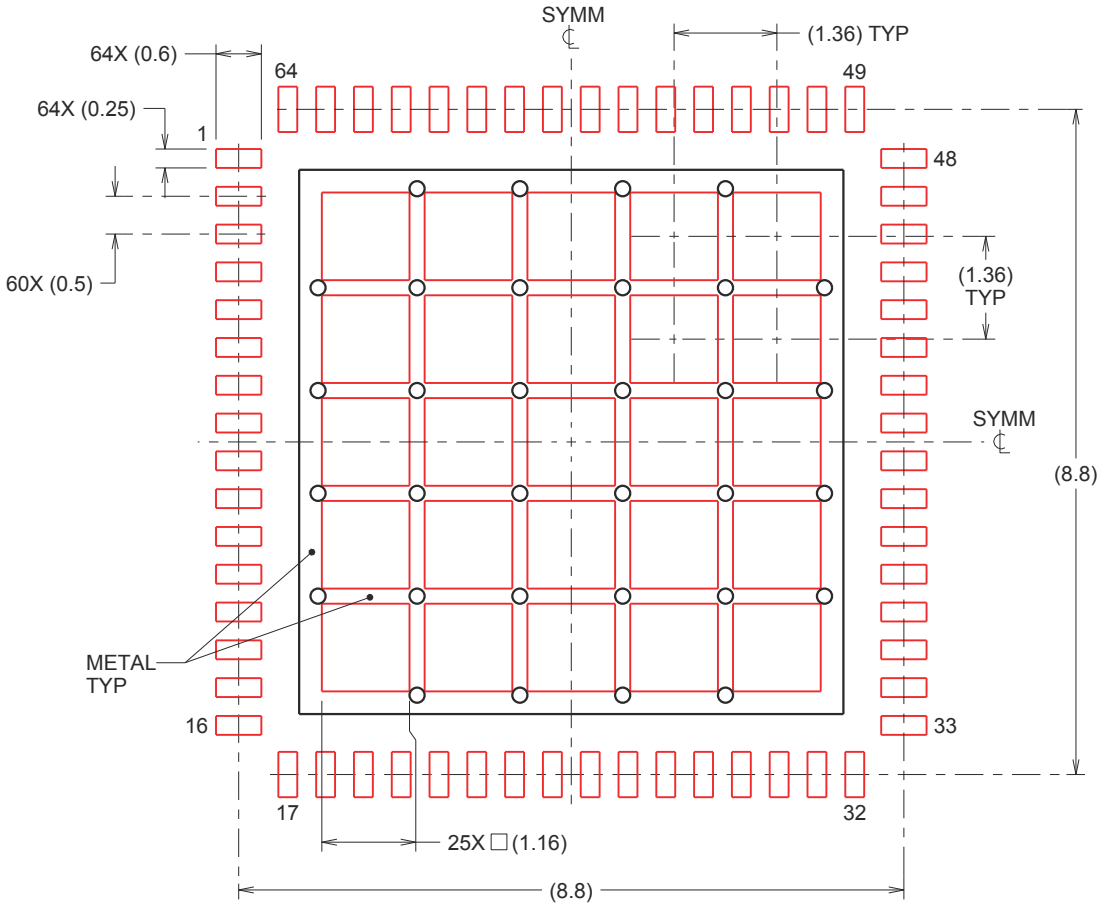

図 10-1. 64-Pin WQFN Stencil Example of Via and Opening Placement (Dimensions in mm)

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図 10-2 (PCB layout example) is derived from a layout design of the DS90UH948-Q1. This graphic and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

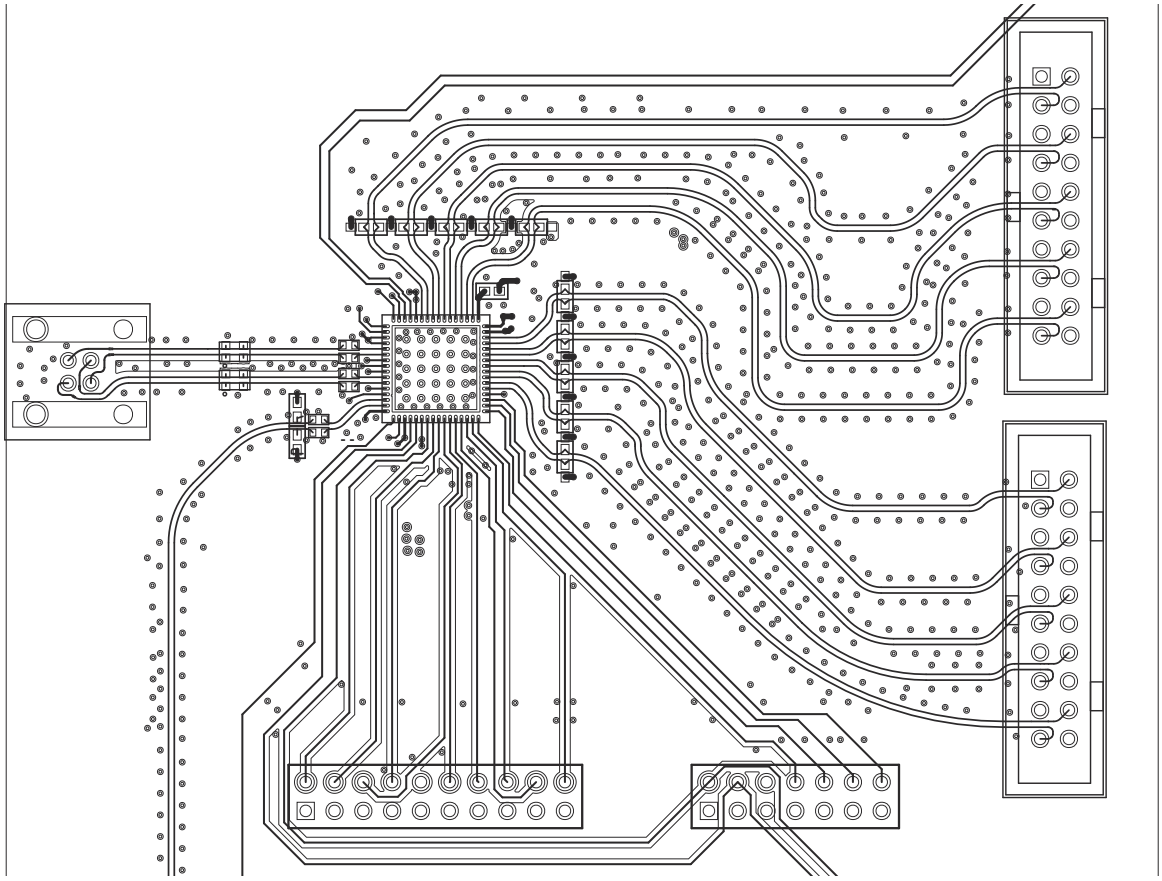

図 10-2. DS90UH948-Q1 Deserializer Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Soldering Specifications Application Report* (SNOA549)
- *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953)
- *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008)
- *AN-905 Transmission Line RAPIDESIGNER Operation and Application Guide* (SNLA035)
- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *LVDS Owner's Manual* (SNLA187)
- *AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel* (SNLA131)
- *Using the I2S Audio Interface of DS90Ux92x FPD-Link III Devices* (SNLA221)
- *AN-Exploring the Int Test Pattern Generation Feature of FPDLink III IVI Devices* (SNLA132)
- *I2C Bus Pullup Resistor Calculation* (SLVA689)
- *FPD-Link™ Learning Center*
- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719)
- *Ten Tips for Successfully Designing With Automotive EMC/EMI Requirements* (SLYT636)

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11.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UH948TNKDRQ1	ACTIVE	WQFN	NKD	64	2000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	90UH948Q1	Samples
DS90UH948TNKDTQ1	ACTIVE	WQFN	NKD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	90UH948Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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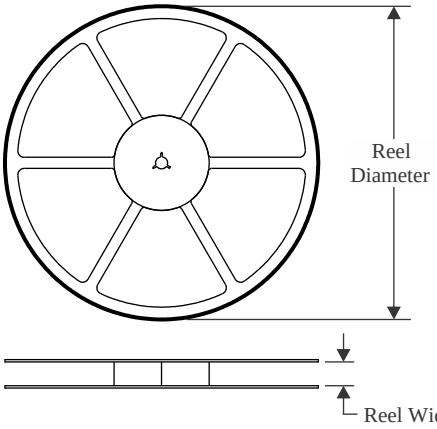
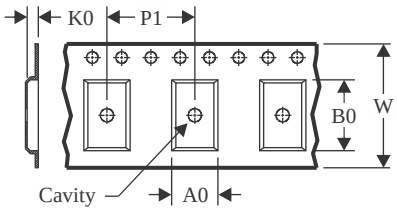
TAPE AND REEL INFORMATION

REEL DIMENSIONS

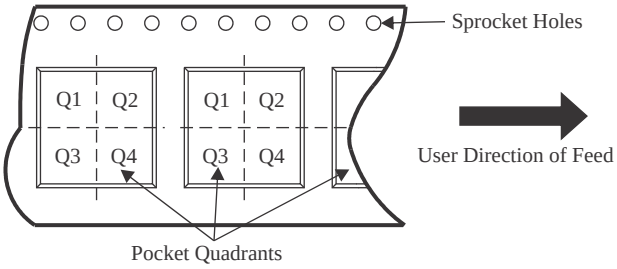


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

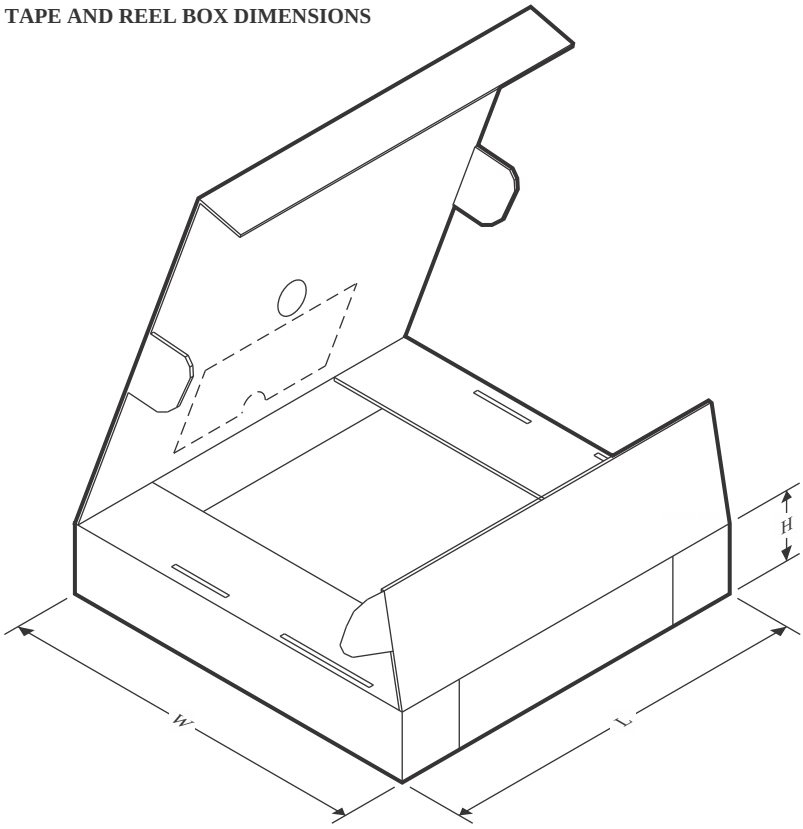
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH948TNKDRQ1	WQFN	NKD	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UH948TNKDTQ1	WQFN	NKD	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH948TNKDRQ1	WQFN	NKD	64	2000	356.0	356.0	35.0
DS90UH948TNKDTQ1	WQFN	NKD	64	250	208.0	191.0	35.0

GENERIC PACKAGE VIEW

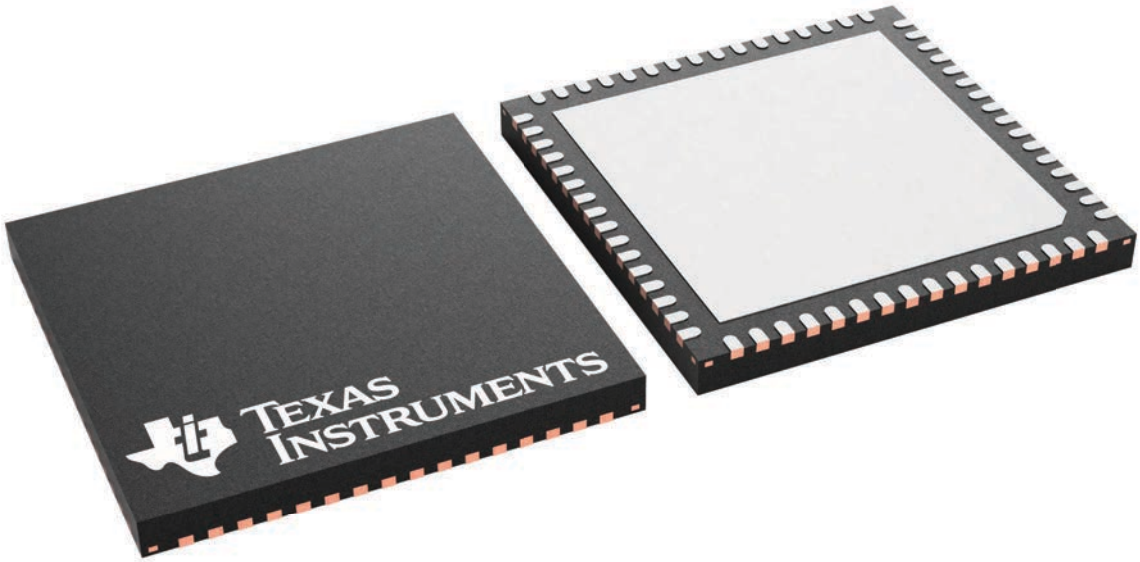
NKD 64

WQFN - 0.8 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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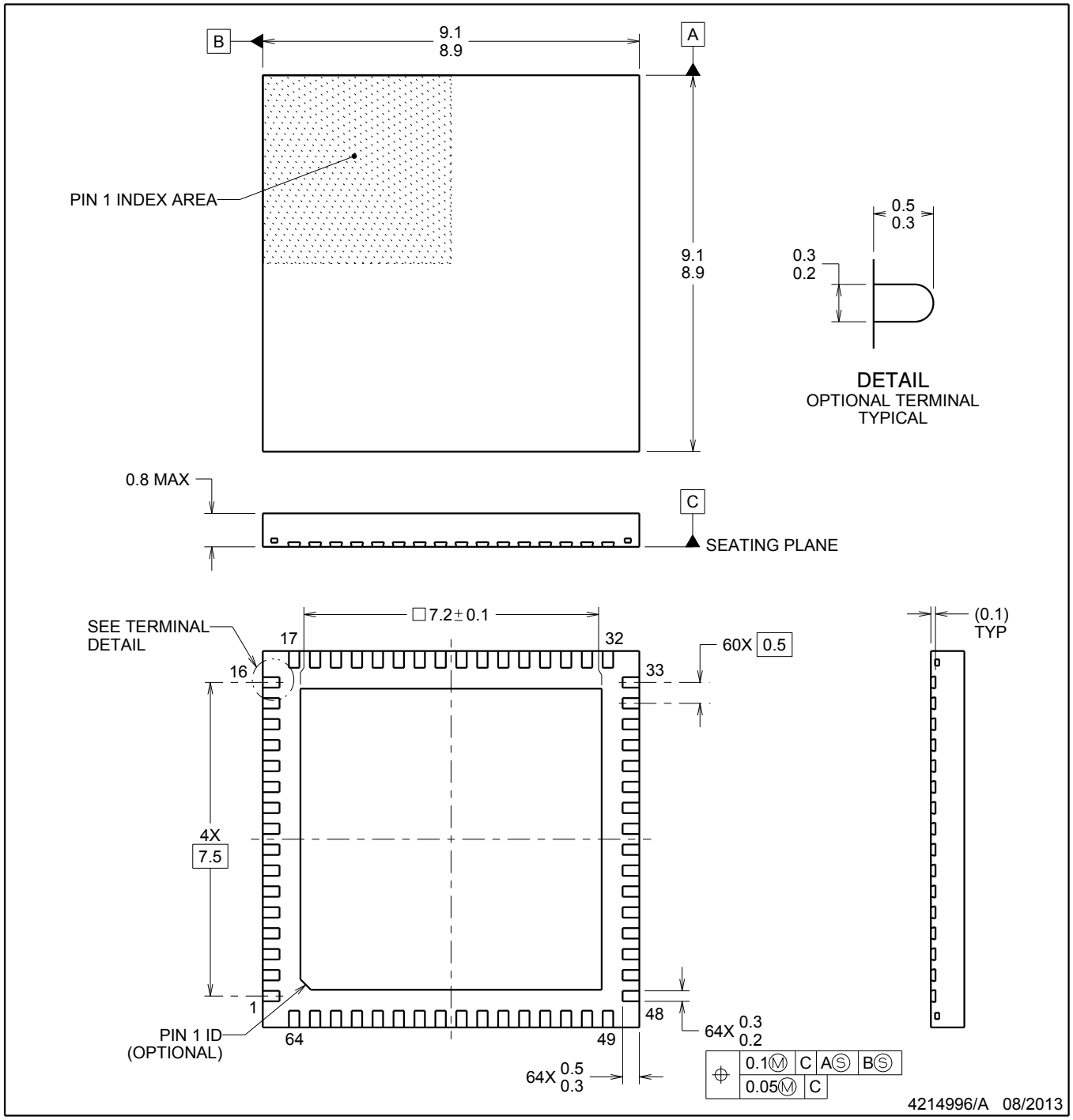
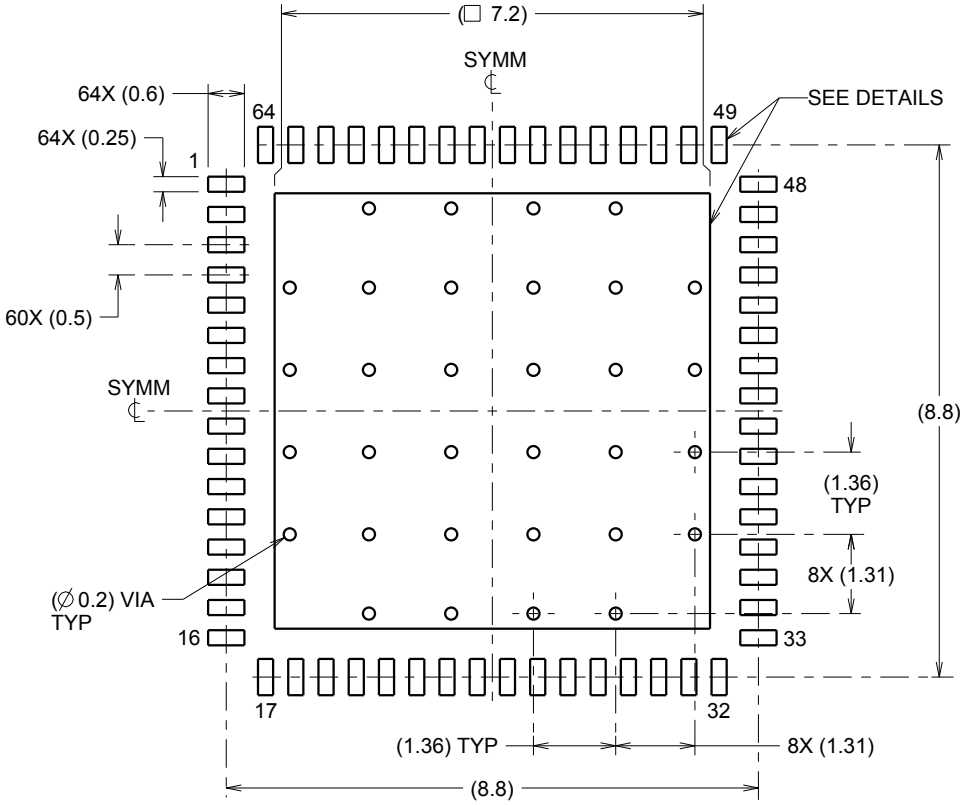
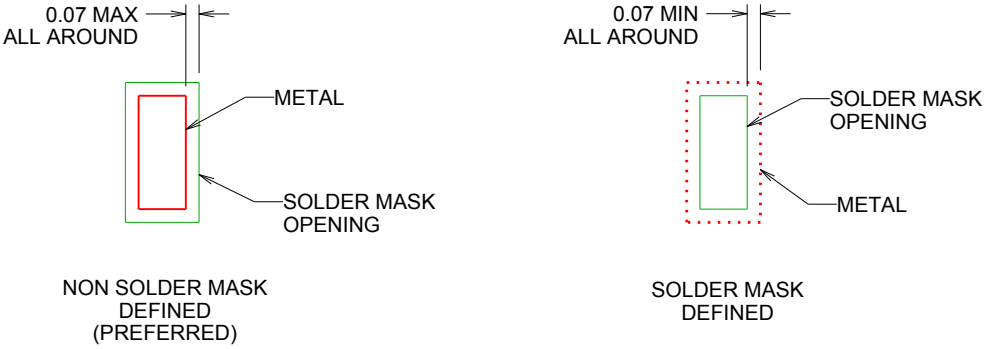


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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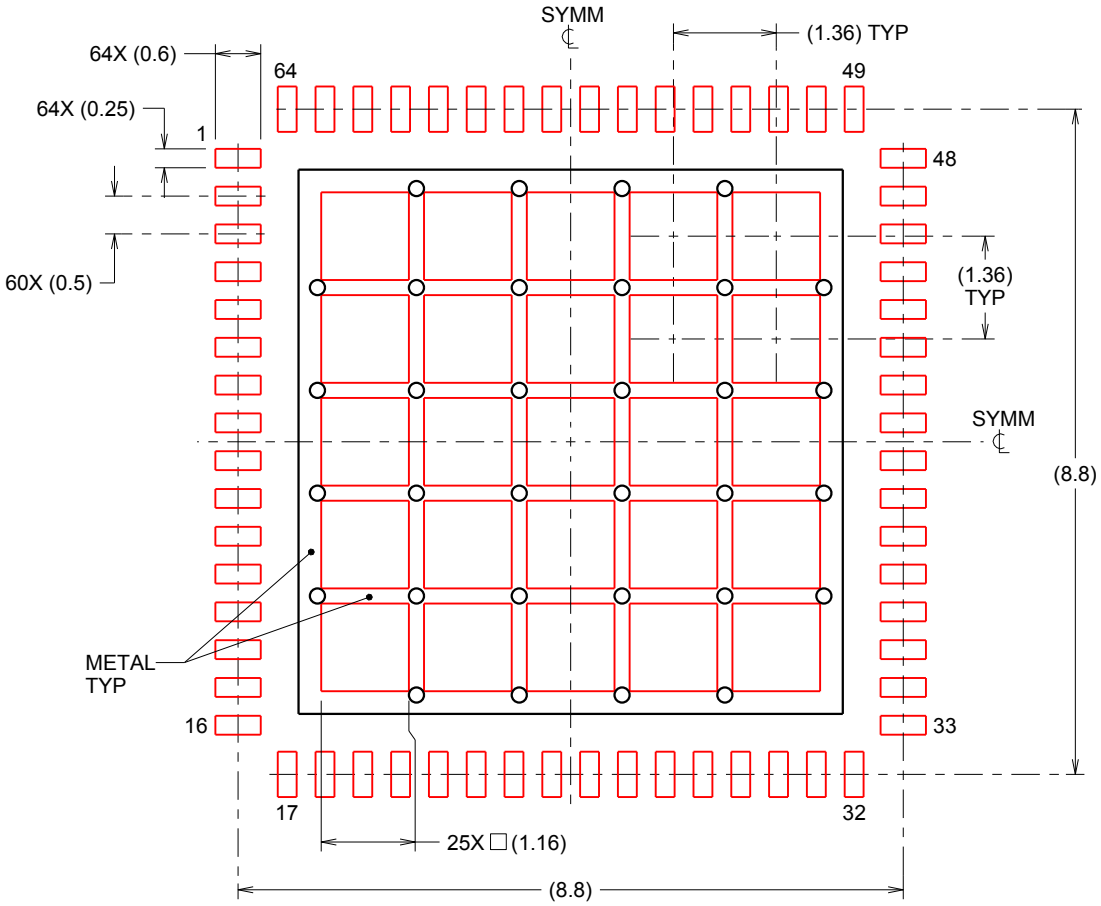
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214996/A 08/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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