ISO72x シングル チャネル高速デジタル アイソレータ

1 特長

- 100Mbps および 150Mbps の信号速度オプション
- 伝搬遅延は 12ns (標準値) です。
- パルス スキューは 0.5ns (標準値) です。
- 低消費電力スリープ モード
- 定格動作電圧で 28 年の標準寿命 (「絶縁寿命予測」を参照)
- 高い電磁界耐性 (アプリケーションノート『ISO72x デジタル アイソレータの磁界耐性』を参照)
- フェイルセーフ出力
- 大半の光・磁気アイソレータに対しドロップイン代替可能
- 3.3V および 5V 電源で動作
- –40℃～+125℃の動作温度範囲
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1 認定、IEC 62368-1 認定
-

2 アプリケーション

- ファクトリ オートメーション
  - Modbus
  - Profibus™
  - DeviceNet™ データバス
- コンピュータ ペリフェラル インターフェイス
- サーボ制御インターフェイス
- データ アクイジション

3 概要

ISO721、ISO721M、ISO722、ISO722M デバイスは、ロジック入力および出力バッファが二酸化ケイ素 (SiO_2) の絶縁膜によって分離されたデジタル アイソレータです。この絶縁膜は、VDE 0884-17 に準拠した、最大 4000V_{PK} のガルバニック絶縁を提供します。これらのデバイスを絶縁型電源と組み合わせて使用すると、データ バスや他の回路上のノイズ電流がローカル グランドに入り込んでノイズに敏感な回路に干渉または損傷を与えることを防止できます。

バイナリ入力信号がコンディショニングされ、平衡信号に変換されてから、絶縁バリアによって差動化されます。絶縁バリアを通過して、差動コンパレータがロジック変換情報を受け取り、それに応じてフリップフロップおよび出力回路を設定またはリセットします。バリアを通して周期的に更新パルスが送信され、適切な DC 出力レベルを実現します。

この DC 更新パルスが 4μs を超えて受信されない場合、入力に電力が供給されていない、または入力がアクティブに駆動されていないと見なされ、フェイルセーフ回路により出力が論理 HIGH 状態に駆動されます。

これらのデバイスは、3.3V、5V、または任意の組み合わせの 2 つの電源電圧を必要とします。3.3V 電源で動作するとき、すべての入力は 5V 許容で、すべての出力は 4mA CMOS です。

ISO722 および ISO722M デバイスは、アクティブ LOW 出力イネーブルを備えており、HIGH ロジック レベルに駆動すると出力が高インピーダンス状態になり、内部バイアス回路をオフにして消費電力を節約します。

ISO721 および ISO722 デバイスは、TTL 入力しきい値とノイズ フィルタが入力に存在し、パルス幅 2ns までの遷移パルスがデバイスの出力に渡されることを防止します。

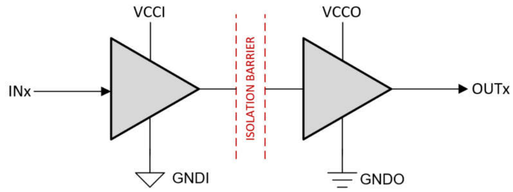
ISO721M および ISO722M デバイスには CMOS $V_{CC}/2$ 入力しきい値が存在しますが、入力ノイズ フィルタがなく追加の伝搬遅延はありません。ISO721M デバイスのこれらの機能は、ジッタ低減の動作も実現しています。

IISO721 、ISO721M 、ISO722 、ISO722M デバイスは、-40℃～+125℃ の周囲温度範囲で動作することが特徴です。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO721	D (SOIC、8)	4.90mm × 3.91mm	4.9mm × 6mm
ISO721M			
ISO722			
ISO722M			

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Device Comparison Table

PART NUMBER	SIGNALING RATE	OUTPUT ENABLED	INPUT THRESHOLDS	NOISE FILTER
ISO721	100 Mbps	NO	TTL	YES
ISO721M	150 Mbps	NO	CMOS	NO
ISO722	100 Mbps	YES	TTL	YES
ISO722M	150 Mbps	YES	CMOS	NO

5 Pin Configuration and Functions

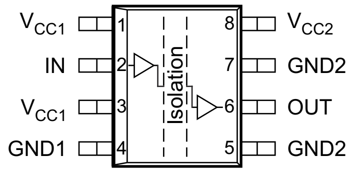


図 5-1. ISO721 and ISO721M D Package 8-Pin SOIC Top View

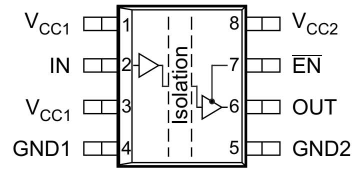


図 5-2. ISO722 and ISO722M D Package 8-Pin SOIC Top View

図 5-3. I

表 5-1. Pin Functions

PIN NAME	PIN NO. ISO721x	PIN NO. ISO722x	Type[1]	DESCRIPTION
V_{CC1}	1	1	—	Power supply, V_{CC1}
	3	3		
V_{CC2}	8	8	—	Power supply, V_{CC2}
IN	2	2	I	Input
OUT	6	6	O	Output
$\overline{EN}$	—	7	I	Output enable. OUT is enabled when $\overline{EN}$ is low or disconnected and disabled when $\overline{EN}$ is high.
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
	7			

(1) I = Input; O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Input voltage	IN, OUT, or $\overline{EN}$	–0.5	V_{CC} + 0.5[(2)]	V
I_O	Output current			±15	mA
T_J	Maximum junction temperature			170	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage[(1)], V_{CC1}, V_{CC2}		3		5.5	V
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse duration	ISO72x	10			ns
		ISO72xM	6.67			
1 / t_{ui}	Signaling rate	ISO72x	0		100	Mbps
		ISO72xM	0		150	
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	ISO72x	2		5.5	V
		IOS72xM	0.7 x V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)	ISO72x	0		0.8	V
		IOS72xM	0		0.3 x V_{CC}	
T_A	Ambient temperature		–40	25	125	°C
T_J	Junction temperature, see the Thermal Information				150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

6.4 Thermal Information

THERMAL METRIC[1]			ISO72x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K Board	114.7	°C/W
		Low-K Board	263	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		63	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		54.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		18.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150C, C_L = 15 pF, Input a 100-Mbps 50% duty-cycle square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO721 AND ISO722 IN D PACKAGE						
P_D	Power dissipation				159	mW
ISO721M AND ISO722M IN D PACKAGE						
P_D	Power dissipation				195	mW

6.6 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 263°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see 図 9-6			100	mA
		$R_{\theta JA}$ = 263°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see 図 9-6			153	
T_S	Safety temperature				150	°C

6.7 Insulation Specifications

PARAMETER		TEST CONDITIONS		VALUE	UNIT
GENERAL					
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	D package	4	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	D package	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)		0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112		400	V
	Material group			II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}		I-IV	
		Rated mains voltage ≤ 300 V_{RMS}		I-III	
DIN EN IEC 60747-17 (VDE 0884-17):[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)		560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1 s (100% production)		4000	V_{PK}
q_{pd}	Apparent charge[3]	Method a: After I/O safety test subgroup 2/3. V_{ini} = V_{IOTM}, tini = 60 s; Vpd(m) = 1.2 × V_{IORM} , tm = 10 s,		672	V_{PK}
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, tini = 60 s; Vpd(m) = 1.3 × V_{IORM} , tm = 10 s,		896	
		Method b1: At routine test (100% production) V_{ini} = V_{IOTM}, tini = 1 s; Vpd(m) = 1.5 × V_{IORM} , tm = 1 s,		1050	
C_{IO}	Barrier capacitance, input to output[4]	VI = 0.4 sin (2πft), f = 1 MHz		1	pF
R_{IO}	Isolation resistance, input to output[4]	V_{IO} = 500 V, T_A = 25°C; all pins on each side of the barrier tied together, creating a two-terminal device		10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ $T_A$max		10^{11}	
		V_{IO} = 500 V at T_S = 150°C		> 10^{9}	
	Pollution degree			2	
	Climatic category			40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification); VTEST = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)		2500	VRMS

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.8 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

6.9 Electrical Characteristics, 5 V, 3.3 V

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent, $V_I = V_{CC}$ or 0 V, no load		0.5	1	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		2	4	
I_{CC2}	V_{CC2} supply current	ISO722 and ISO722M, Sleep mode, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at V_{CC}			150	μA
		Quiescent, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at 0 V or ISO721 and ISO721M		4	6.5	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		5	7.5	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See 図 7-1	V_{CC} – 0.4	3		V
		I_{OH} = –20 μA, See 図 7-1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See 図 7-1		0.2	0.4	V
		I_{OL} = 20 μA, See 図 7-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	$\overline{EN}$, IN at 2 V			10	μA
I_{IL}	Low-level input current	$\overline{EN}$, IN at 0.8 V	–10			μA
I_{OZ}	High-impedance output current, ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}			1	μA
C_I	Input capacitance to ground	IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See 図 7-5	25	40		kV/μs

6.10 Electrical Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent, $V_I = V_{CC}$ or 0 V, no load		0.5	1	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		2	4	
I_{CC2}	V_{CC2} supply current	ISO722 and ISO 722M Sleep Mode, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at V_{CC}			200	μA
		Quiescent, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at 0 V or ISO721 and ISO721M		8	12	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		10	14	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See 図 7-1	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 μA, See 図 7-1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See 図 7-1		0.2	0.4	V
		I_{OL} = 20 μA, See 図 7-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	$\overline{EN}$, IN at 2 V			10	μA
I_{IL}	Low-level input current	$\overline{EN}$, IN at 0.8 V	–10			
I_{OZ}	High-impedance output current, ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}			1	μA
C_I	Input capacitance to ground	IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See 図 7-5	25	50		kV/μs

6.11 Switching Characteristics, 3.3 V, 5 V

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1	12	17	30	ns
t_{PHL}	Propagation delay , high-to-low-level output	ISO72x		12	17	30	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$	ISO72x			0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		10	12	21	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM		10	12	21	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$	ISO72xM			0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See 図 7-1		2.3		ns
t_f	Output signal fall time				2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722 ISO722M	See 図 7-2	5.4	9	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M		4.5	5	15	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See 図 7-3	5.4	9	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M		4.5	5	15	μs
t_{fs}	Failsafe output delay time from input power loss		See 図 7-4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See 図 7-6		2		ns
		ISO72x	100-Mbps unrestricted bit run length data input, See 図 7-6		3		ns
		ISO72xM	150-Mbps NRZ data input, See 図 7-6		1		ns
		ISO72xM	150-Mbps unrestricted bit run length data input, See 図 7-6		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.12 Electrical Characteristics, 3.3 V, 5 V

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent, V_I = V_{CC} or 0 V, no load		0.3	0.6	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load		1	2	
I_{CC2}	V_{CC2} supply current	ISO722 and ISO722M, Sleep mode, V_I = V_{CC} or 0 V, No load, $\overline{EN}$ at V_{CC}			200	µA
		Quiescent, V_I = V_{CC} or 0 V, No load, $\overline{EN}$ at 0 V or ISO721 and ISO721M		8	12	mA
		25 Mbps, V_I = V_{CC} or 0 V, No load		10	14	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See 図 7-1	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See 図 7-1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See 図 7-1		0.2	0.4	V
		I_{OL} = 20 µA, See 図 7-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	$\overline{EN}$, IN at 2 V			10	µA
I_{IL}	Low-level input current	$\overline{EN}$, IN at 0.8 V	–10			µA
I_{OZ}	High-impedance output current, ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}			1	µA
C_I	Input capacitance to ground	IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See 図 7-5	25	40		kV/µs

6.13 Electrical Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent, $V_I = V_{CC}$ or 0 V, no load		0.3	0.6	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		1	2	
I_{CC2}	V_{CC2} supply current	ISO722 and ISO722M Sleep Mode, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at V_{CC}			150	µA
		Quiescent, $V_I = V_{CC}$ or 0 V, No load, $\overline{EN}$ at 0 V or ISO721 and ISO721M		4	6.5	mA
		25 Mbps, $V_I = V_{CC}$ or 0 V, no load		5	7.5	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See 図 7-1	V_{CC} – 0.4	3		V
		I_{OH} = –20 µA, See 図 7-1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See 図 7-1		0.2	0.4	V
		I_{OL} = 20 µA, See 図 7-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	$\overline{EN}$, IN at 2 V			10	µA
I_{IL}	Low-level input current	$\overline{EN}$, IN at 0.8 V	–10			µA
I_{OZ}	High-impedance output current, ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}			1	µA
C_I	Input capacitance to ground	IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See 図 7-5	25	40		kV/µs

6.14 Switching Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1	12	20	34	ns
t_{PHL}	Propagation delay , high-to-low-level output			12	20	34	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$				0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		10	12	25	ns
t_{PHL}	Propagation delay, high-to-low-level output			10	12	25	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$				0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See 図 7-1		2.3		ns
t_f	Output signal fall time				2.3		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722 ISO722M	See 図 7-2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			5	6	15	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See 図 7-3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			5	6	15	μs
t_{fs}	Failsafe output delay time from input power loss		See 図 7-4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See 図 7-6		2		ns
			100-Mbps unrestricted bit run length data input, See 図 7-6		3		
		ISO72xM	150-Mbps NRZ data input, See 図 7-6		1		
			150-Mbps unrestricted bit run length data input, See 図 7-6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.15 Switching Characteristics, 5 V, 3.3 V

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1	10	19	30	ns
t_{PHL}	Propagation delay , high-to-low-level output	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1	10	19	30	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1		0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM	$\overline{EN}$ at 0 V, See 図 7-1	10	12	20	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM	$\overline{EN}$ at 0 V, See 図 7-1	10	12	20	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} – t_{PLH}\|$	ISO72xM	$\overline{EN}$ at 0 V, See 図 7-1		0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See 図 7-1		2.3		ns
t_f	Output signal fall time		$\overline{EN}$ at 0 V, See 図 7-1		2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722 ISO722M	See 図 7-2	7	11	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M	See 図 7-2	4.5	6	15	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See 図 7-3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M	See 図 7-3	4.5	6	15	μs
t_{fs}	Failsafe output delay time from input power loss		See 図 7-4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See 図 7-6		2		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps unrestricted bit run length data input, See 図 7-6		3		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps NRZ data input, See 図 7-6		1		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps unrestricted bit run length data input, See 図 7-6		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.16 Switching Characteristics, 5 V

V_{CC1} and V_{CC2}at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See 図 7-1	10	17	24	ns
t_{PHL}	Propagation delay, high-to-low-level output			10	17	24	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} – t_{PLH} \rvert$				0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM		8	10	16	ns
t_{PHL}	Propagation delay, high-to-low-level output			8	10	16	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} – t_{PLH} \rvert$				0.5	1	ns
$t_{sk(pp)}$ [(1)]	Part-to-part skew				0	3	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See 図 7-1		2.3		ns
t_f	Output signal fall time				2.3		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722 ISO722M	See 図 7-2	6	8	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			3.5	4	15	μs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See 図 7-3	5.5	8	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4	5	15	μs
t_{fs}	Failsafe output delay time from input power loss		See 図 7-4		3		μs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See 図 7-6		2		ns
			100-Mbps unrestricted bit run length data input, See 図 7-6		3		
		ISO72xM	150-Mbps NRZ data input, See 図 7-6		1		
			150-Mbps unrestricted bit run length data input, See 図 7-6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.17 Typical Characteristics

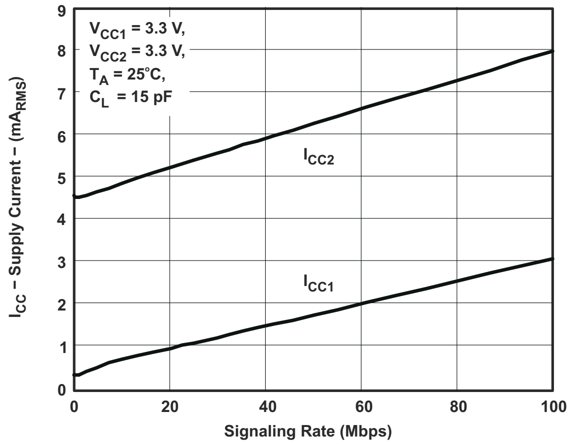


図 6-1. RMS Supply Current vs Signaling Rate

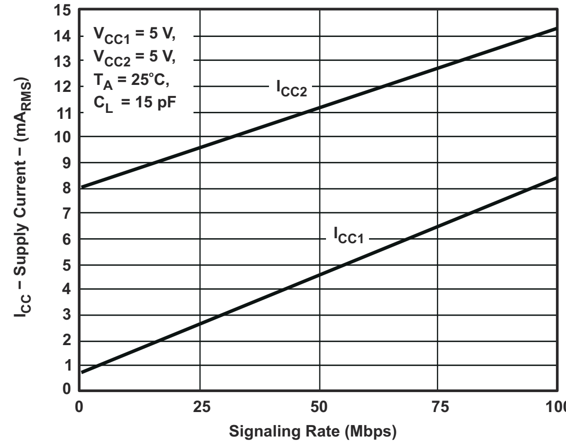


図 6-2. RMS Supply Current vs Signaling Rate

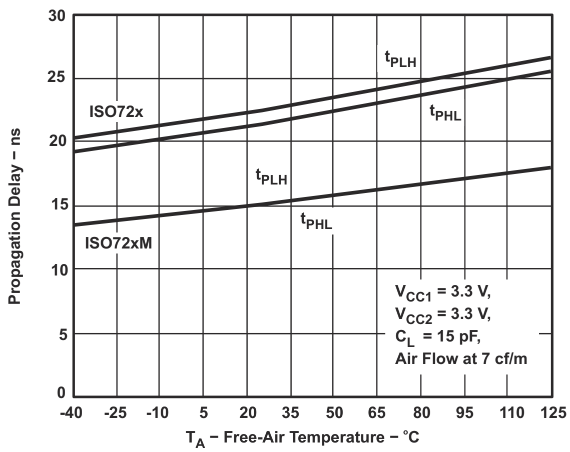


図 6-3. Propagation Delay vs Free-Air Temperature

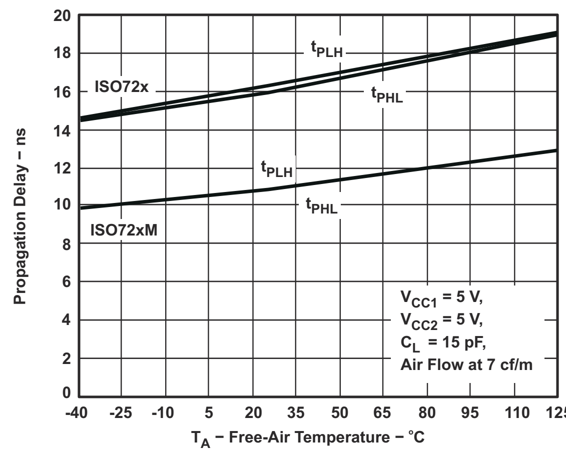


図 6-4. Propagation Delay vs Free-Air Temperature

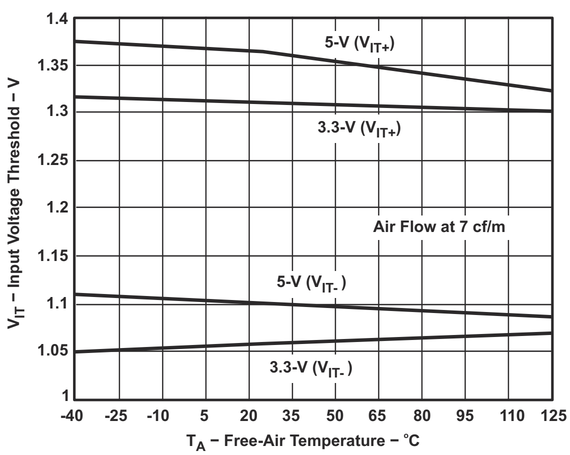


図 6-5. ISO72x Input Threshold Voltage vs Free-Air Temperature

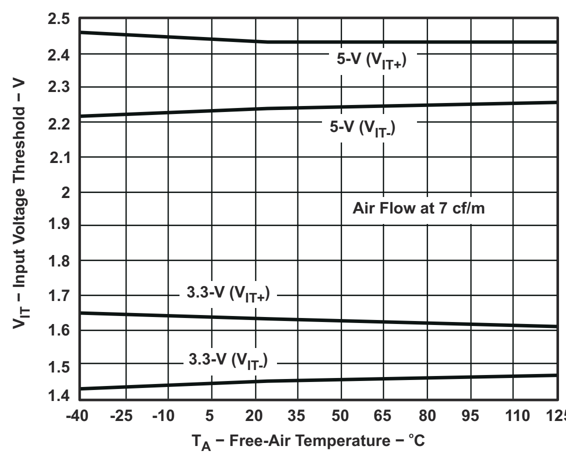


図 6-6. ISO72xM Input Threshold Voltage vs Free-Air Temperature

6.17 Typical Characteristics (continued)

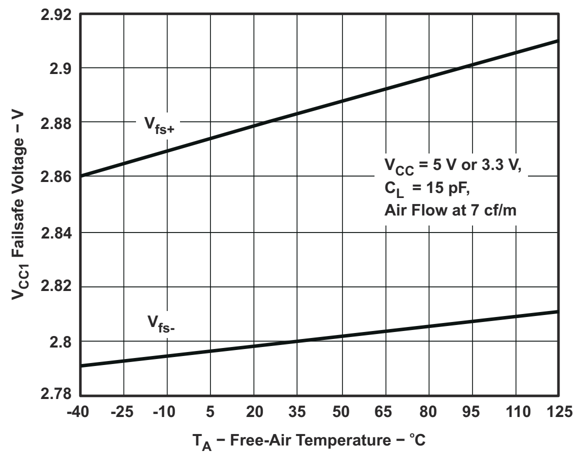


図 6-7. V_{CC1} Failsafe Threshold Voltage vs Free-Air Temperature

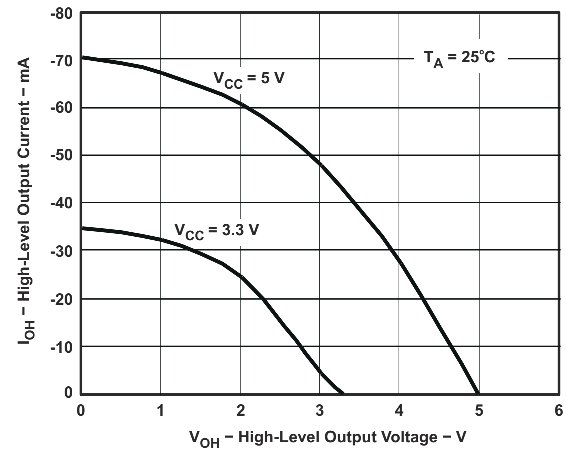


図 6-8. High-Level Output Current vs High-Level Output Voltage

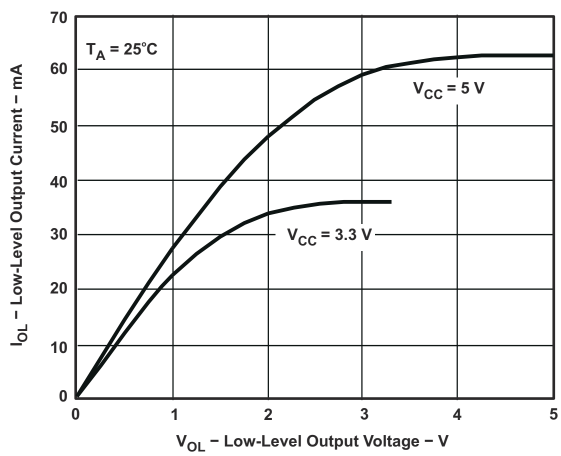


図 6-9. Low-Level Output Current vs Low-Level Output Voltage

7 Parameter Measurement Information

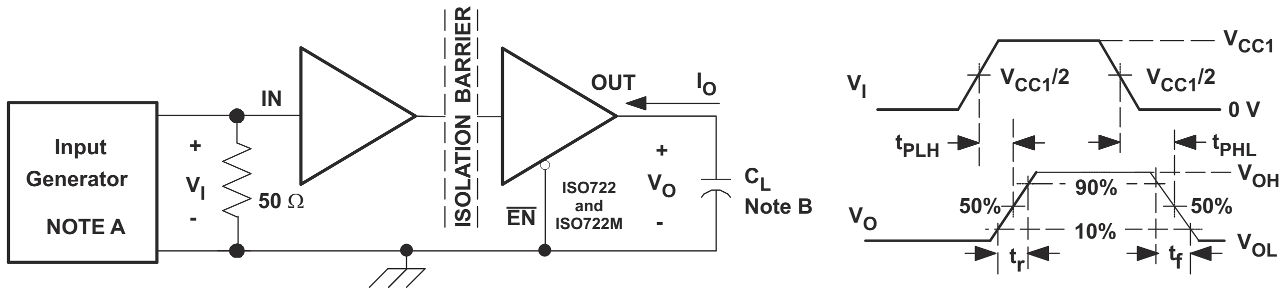


図 7-1. Switching Characteristic Test Circuit and Voltage Waveforms

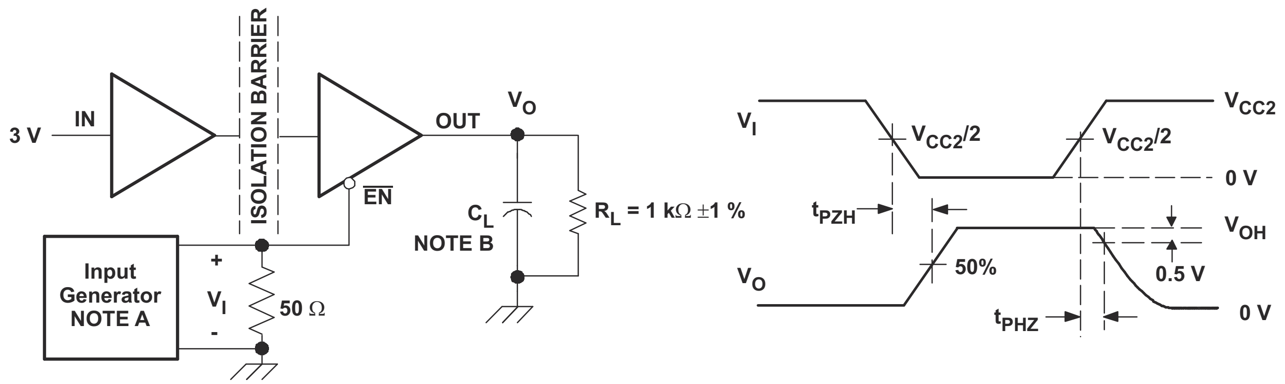


図 7-2. ISO722 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

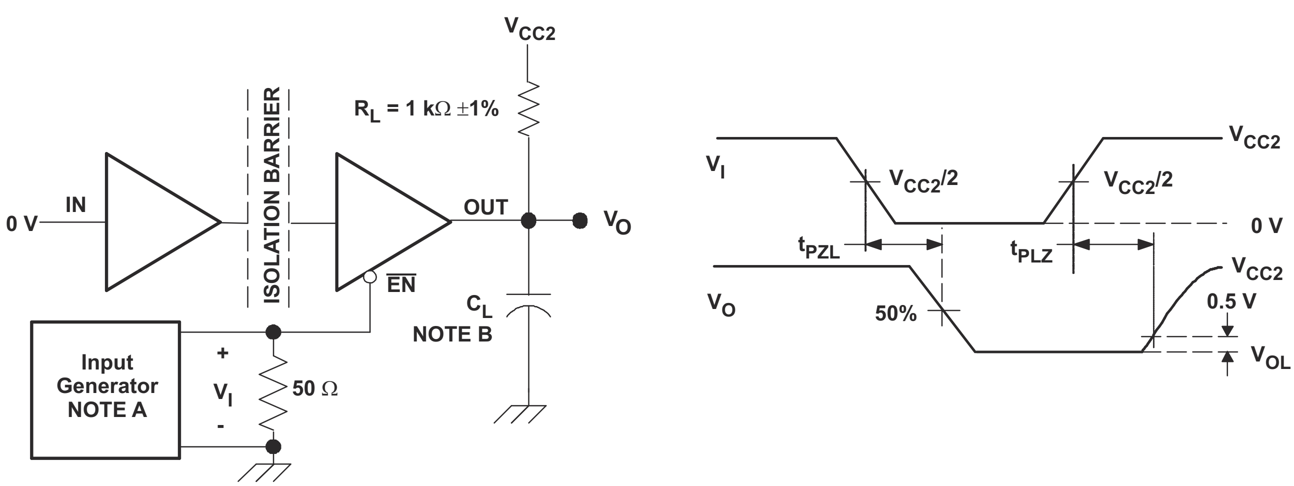


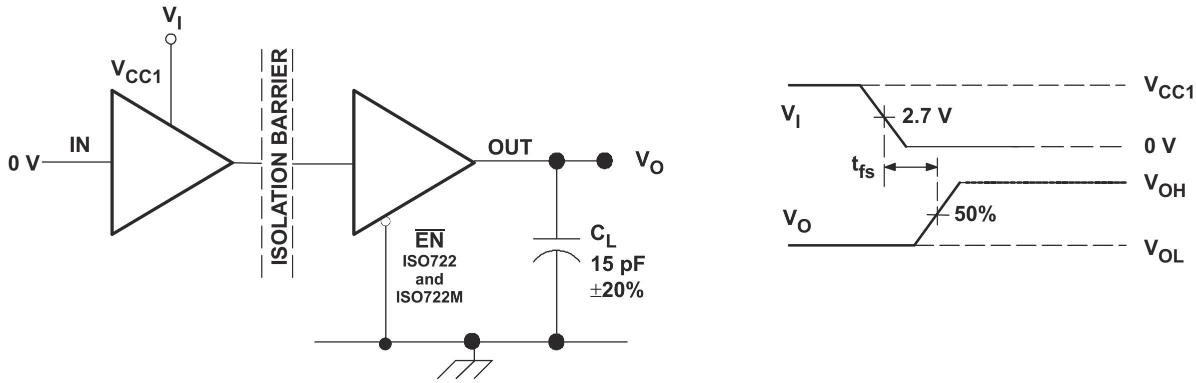
図 7-3. ISO722 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

注

A: The input pulse is supplied by a generator having the following characteristics:

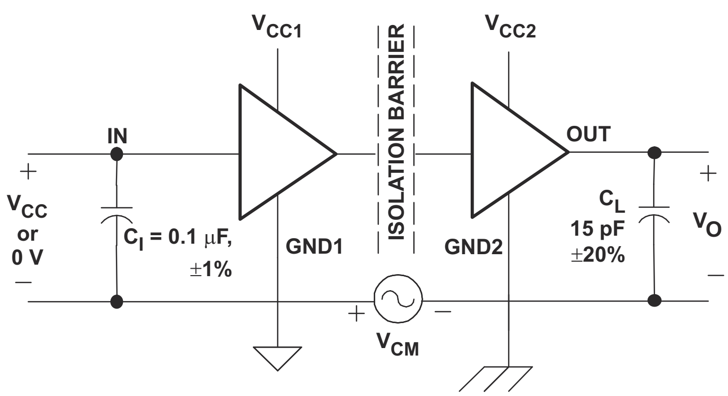
PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B: C_L = 15 pF ± 20% and includes instrumentation and fixture capacitance.



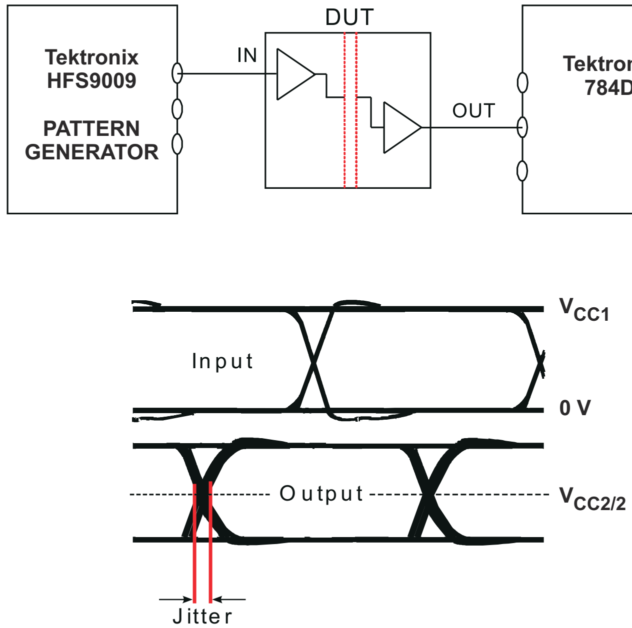
NOTE: V_I transition time is 100 ns.

図 7-4. Failsafe Delay Time Test Circuit and Voltage Waveforms



NOTE: Pass/fail criterion is no change in V_O.

図 7-5. Common-Mode Transient-Immunity Test Circuit and Voltage Waveform



NOTE: Bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

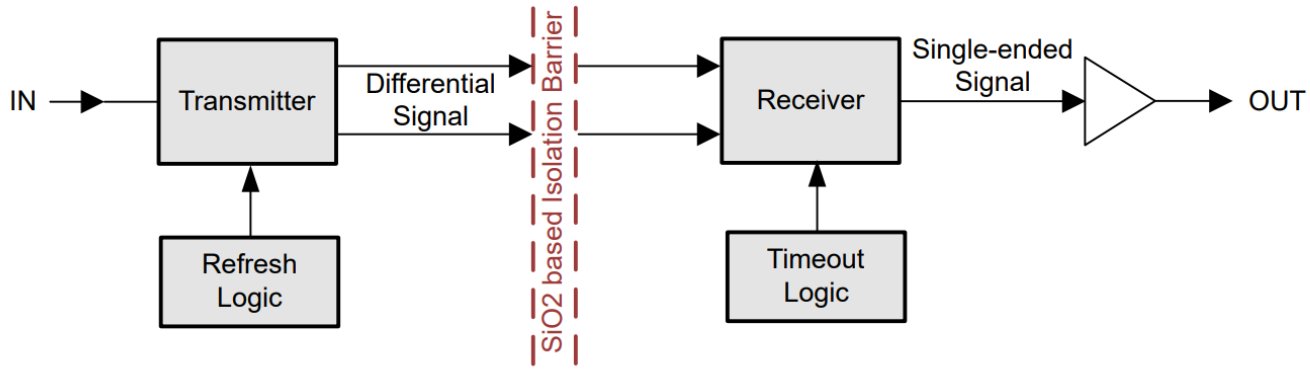
図 7-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

8 Detailed Description

8.1 Overview

The ISO72x family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

8.2 Functional Block Diagram



8.3 Device Functional Modes

表 8-1 and 表 8-2 list the functional modes for the ISO72x family of devices.

表 8-1. ISO721 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

表 8-2. ISO722 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or open	H
		L	L or open	L
		X	H	Z
		Open	L or open	H
PD	PU	X	L or open	H
PD	PU	X	H	Z
X	PD	X	X	Undetermined

8.3.1 Device I/O Schematic

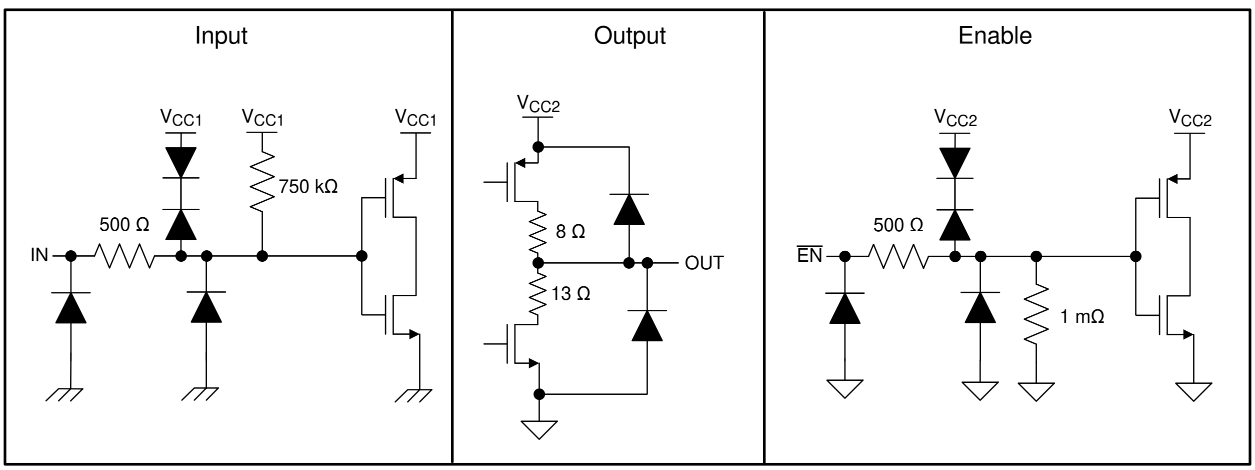


図 8-1. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

注

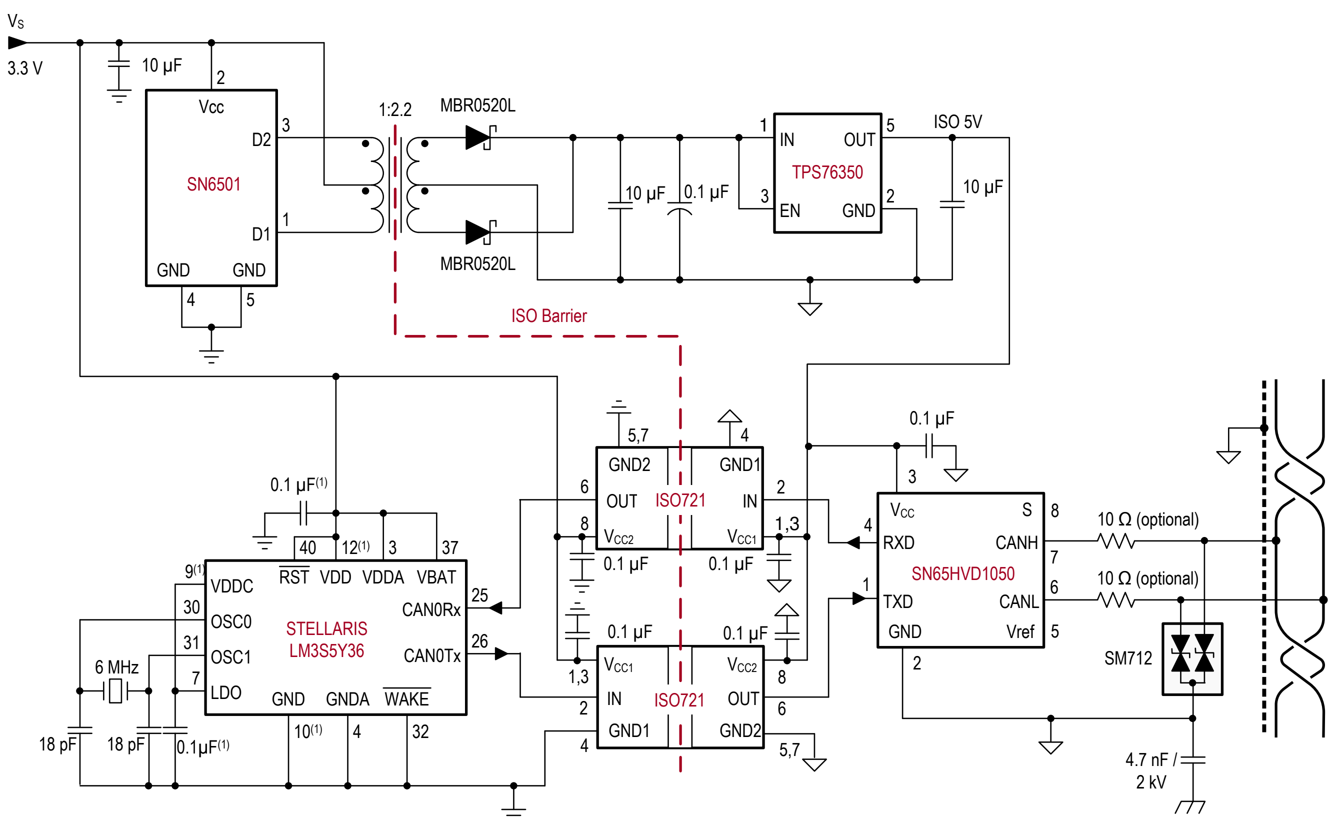
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The ISO72x devices use single-ended TTL or CMOS-logic-switching technology. The supply voltage range of the devices is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, because the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO721 device can be used with Texas Instruments' microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown in 図 9-1.



A. Multiple pins and capacitors omitted for clarity purpose.

図 9-1. Isolated CAN Interface

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO72x devices only require two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

図 9-2 shows a typical circuit hook-up for the ISO721 device.

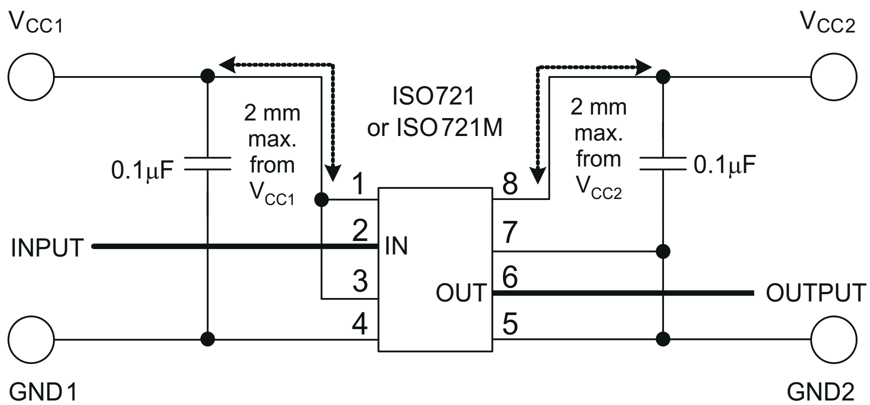


図 9-2. Typical ISO721 Circuit Hook-up

The ISO72x isolators have the same functional pinout as those of most other vendors as shown in 図 9-3, and are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. 表 9-1 is used as a guide for replacing other isolators with the ISO72x family of single-channel isolators.

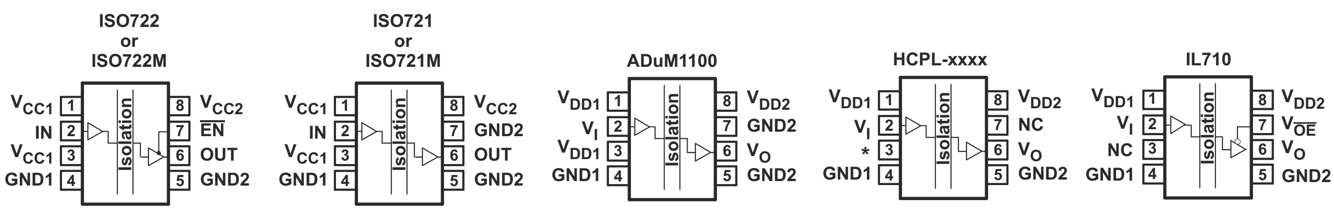


図 9-3. Pin Cross Reference

表 9-1. Cross Reference

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7: ISO721 OR ISO721M	PIN 7: ISO722 OR ISO722M	PIN 8
ISO721[(1)] [(2)]	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100[(1)] [(2)]	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	*Leave Open[(3)]	GND1	GND2	V_O	NC[(5)]		V_{DD2}
IL710	V_{DD1}	V_I	NC[(4)]	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) Pin 1 must be used as V_{CC1}. Pin 3 can also be used as V_{CC1} or left open, as long as pin 1 is connected to V_{CC1}.
(2) Pin 5 must be used as GND2. Pin 7 can also be used as GND2 or left open, as long as pin 5 is connected to GND2.
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO72x device, because the extra V_{CC1} on pin 3 can be left an open circuit as well.
(4) Pin 3 of the IL710 must not be tied to ground on the circuit board because this shorts the ISO72x V_{CC1} to ground. The IL710 pin 3 can only be tied to V_{CC} or left open to drop in an ISO72x device.
(5) An HCPL device pin 7 must be left floating (open) or grounded when an ISO722 or ISO722M device is to be used as a drop-in replacement. If pin 7 of the ISO722 or ISO722M device is placed in a high logic state, the output of the device is disabled.

9.2.3 Application Curves

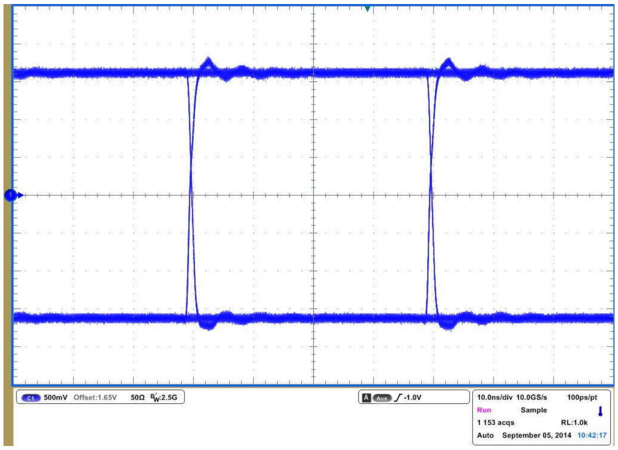


図 9-4. ISO721M Eye Diagram at 25 Mbps, 3.3 V, and 25°C

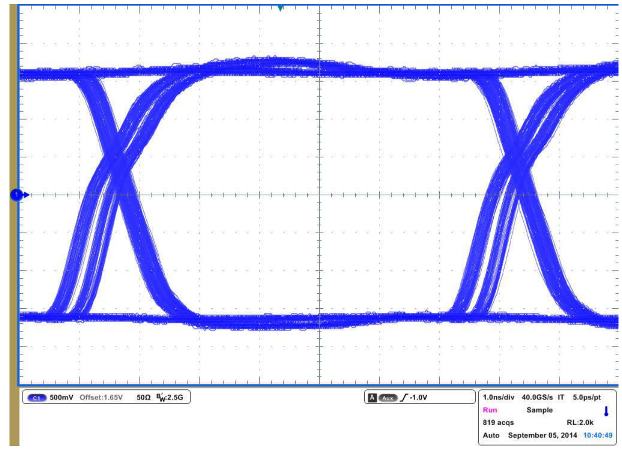


図 9-5. ISO721M Eye Diagram at 150 Mbps, 3.3 V, and 25°C

9.2.3.1 Insulation Characteristics Curves

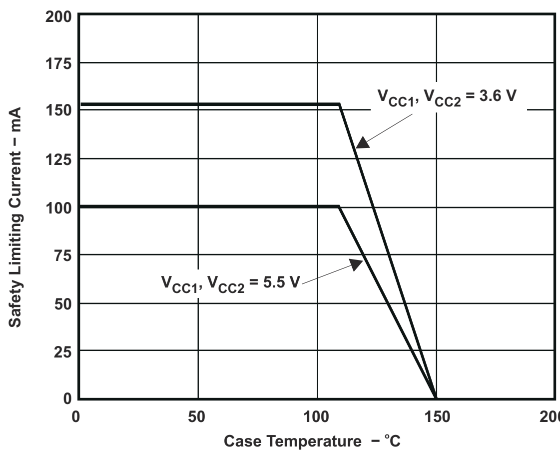


図 9-6. Thermal Derating Curve for Limiting Current per VDE

9.2.3.2 Insulation Lifetime

At maximum working voltage, the isolation barrier of the ISO72x and ISO72xM family of devices has more than 28 years of life.

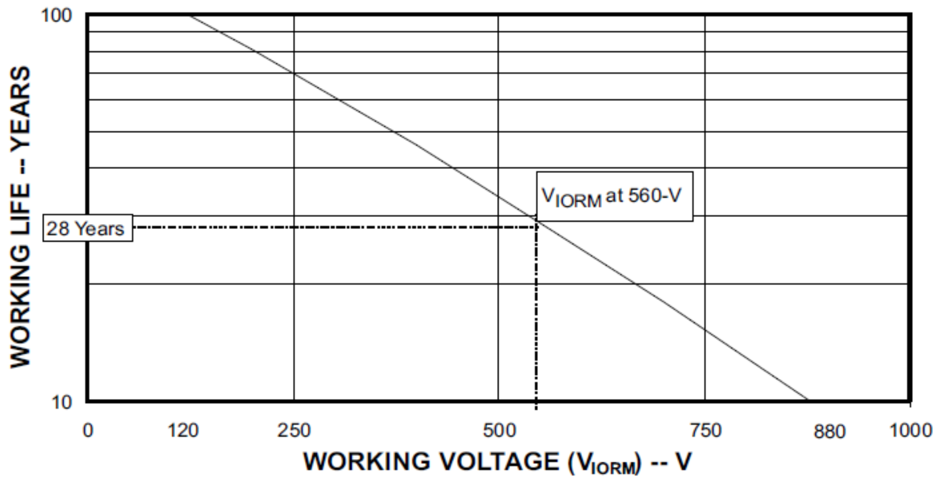


図 9-7. Insulation Lifetime Projection

9.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor must be placed at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet.

9.4 Layout

9.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 9-8). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

9.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

9.4.2 Layout Example

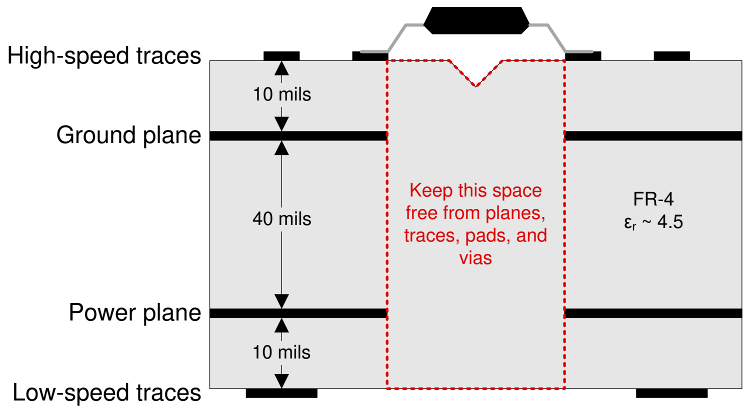


図 9-8. Recommended Layer Stack

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

For development support, see the following:

- Texas Instruments, *36Vdc-75Vdc Input, 20V @ 4A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *18Vdc-54Vdc Input, 24V @ 5A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *36Vdc-75Vdc Input, 6V @ 20A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *ISO72x IBIS Model*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *Isolated RS-485 Reference Design* application report
- Texas Instruments, *ISO721EVM* user's guide

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (July 2021) to Revision N (February 2025) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新......1
- ドキュメント全体で VDE V 0884-11 を DIN VDE 0884-17 に更新......1

Changes from Revision L (October 2015) to Revision M (October 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新......1
- Updated reference from capacitive isolation to isolation barrier throughout the document......1
- Changed the *Power Dissipation* table to *Power Ratings*. Combined the *Package Insulation Characteristics* table, *IEC 60664-1 Ratings Table* table, and *Insulation Characteristics* table in the *Insulation Specifications* table. Changed the *Regulatory Information* table to the *Safety-Related Certifications* table......6
- Changed the L(I01) parameter name to external clearance (CLR) and L(I02) to external creepage (CPG). Also changed the input-to-output test voltage (V_{PR}) parameter name to apparent charge (q_{pd})......7
- Changed Vpeak to V_{PK} throughout the data sheet......7
- Changed the CSA information in the *Safety-Related Certifications* table......7
- Moved the *Insulation Characteristics Curves* section to the *Application Curves* section......24
- Changed the name of the *Application Curve* section to *Insulation Lifetime* and moved to the *Application Curves* section......24

Changes from Revision K (February 2012) to Revision L (September 2015) **Page**

- Moved Power Dissipation metric into new table, called *Power Dissipation* 6
- Added header row above "V_{IORM}" row with the text "DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" in the *Insulation Characteristics* table......7
- Deleted "per UL" in "Isolation voltage" in the *Insulation Characteristics* table......7
- Changed Test Condition "DIN IEC 60112/VDE 0303 Part 1" to "DIN EN 60112 (VDE 0303-11); IEC 60112" in the *Package Insulation Characteristics* table......7
- Changed the D-8 MIN value of L(102) from "4.3" to "4" in the *Package Insulation Characteristics* table......7
- Deleted bottom row of the *Package Insulation Characteristics* table......7
- Moved "V_{ISO}" row to the bottom of the *Insulation Characteristics* table......7
- Changed the D-8 MIN value of L(101) from "4.8" to "4" in the *Package Insulation Characteristics* table......7
- Added "UL 1577" header row over "V_{ISO}" row in the *Insulation Characteristics* table......7

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO721D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	ISO721
ISO721DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721
ISO721DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721
ISO721DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721
ISO721MDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M
ISO721MDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M
ISO721MDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M
ISO722D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	ISO722
ISO722DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722
ISO722DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722
ISO722DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722
ISO722MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	IS722M
ISO722MDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M
ISO722MDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M
ISO722MDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M
ISO722MDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO721, ISO721M, ISO722 :

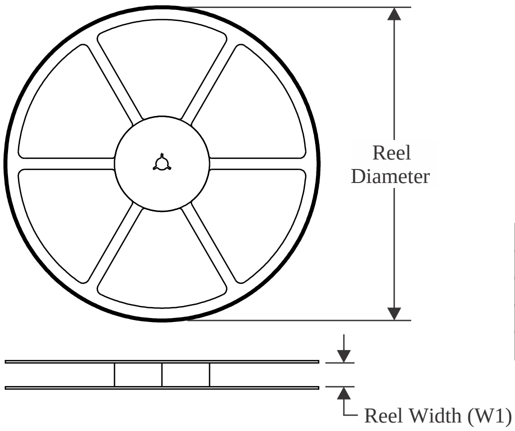
- Automotive : ISO721-Q1, ISO721-Q1, ISO722-Q1
- Enhanced Product : ISO721M-EP
- Military : ISO721M

NOTE: Qualified Version Definitions:

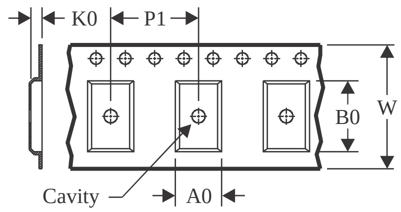
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

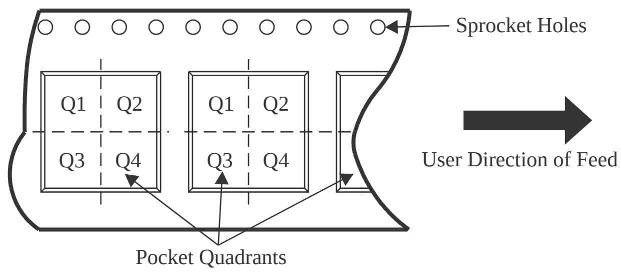


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

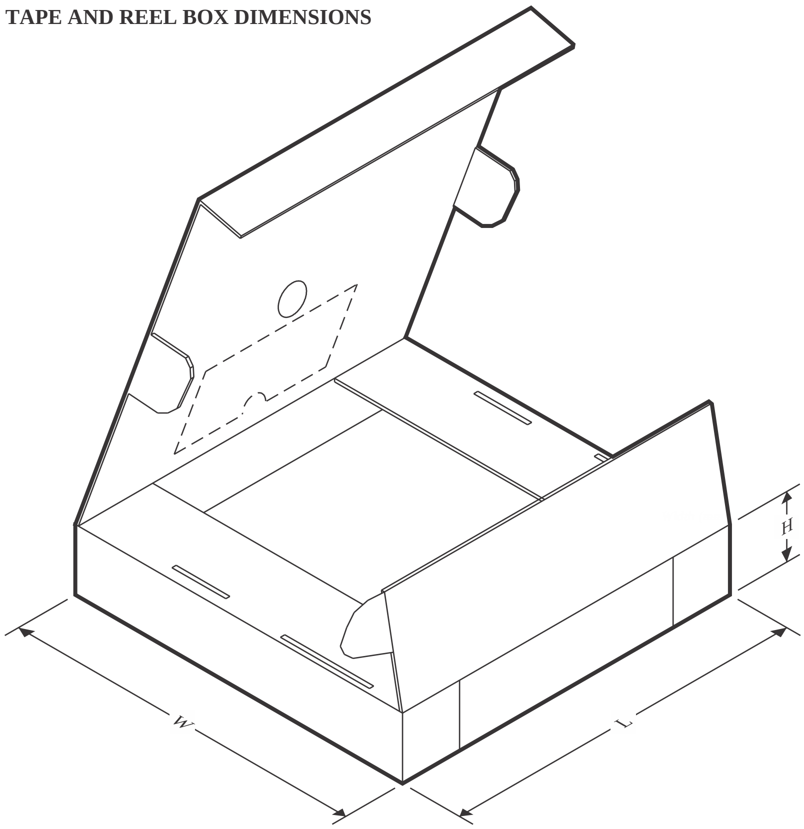
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

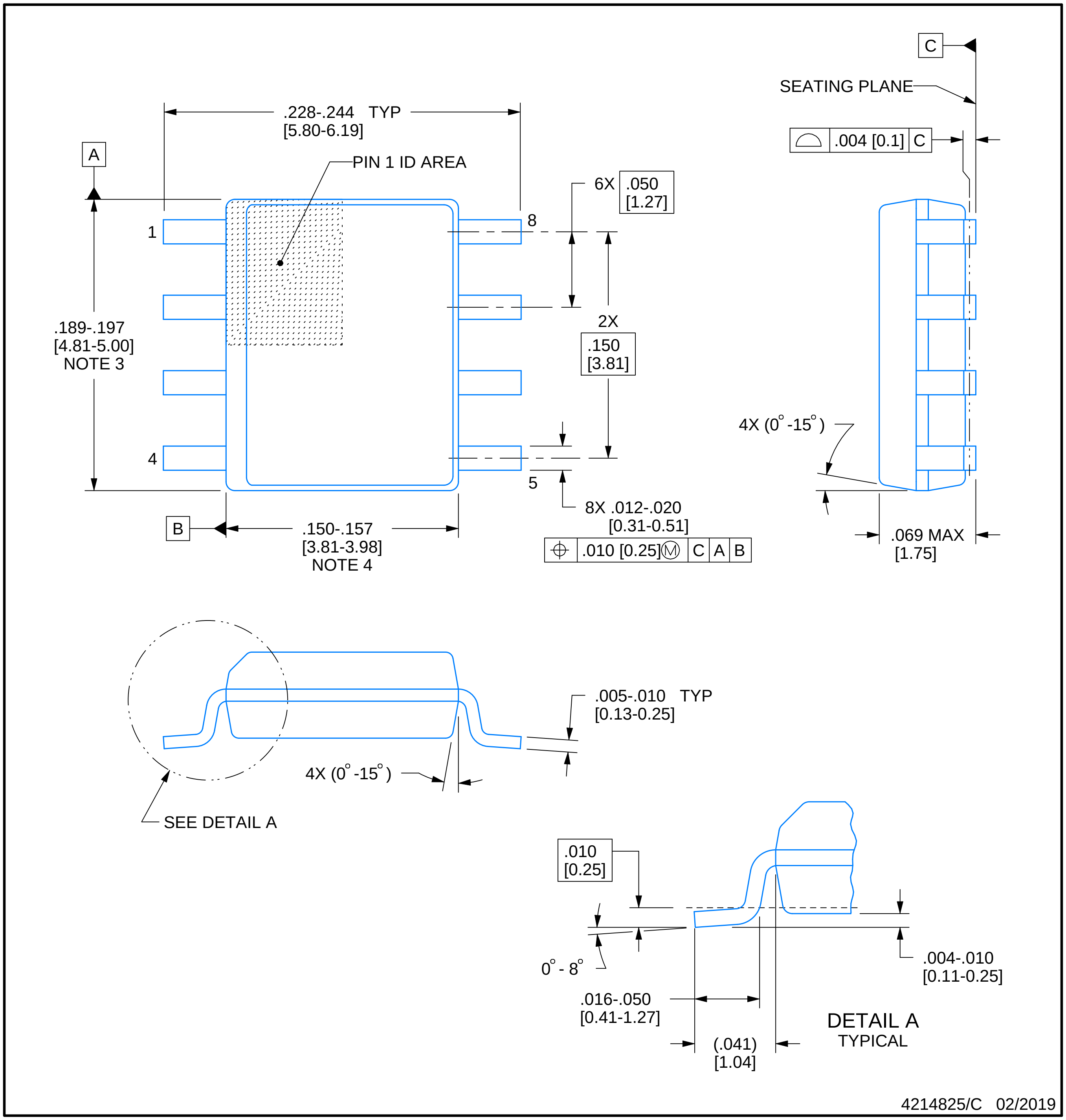
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO721MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



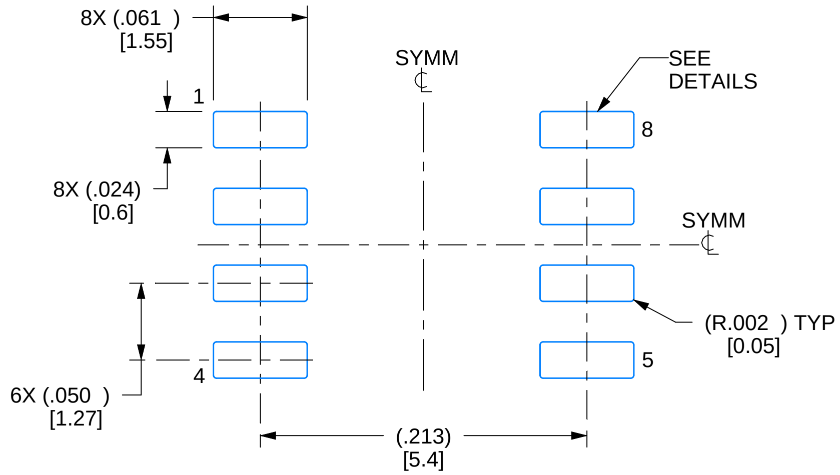
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO721MDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO722DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO722MDR	SOIC	D	8	2500	350.0	350.0	43.0

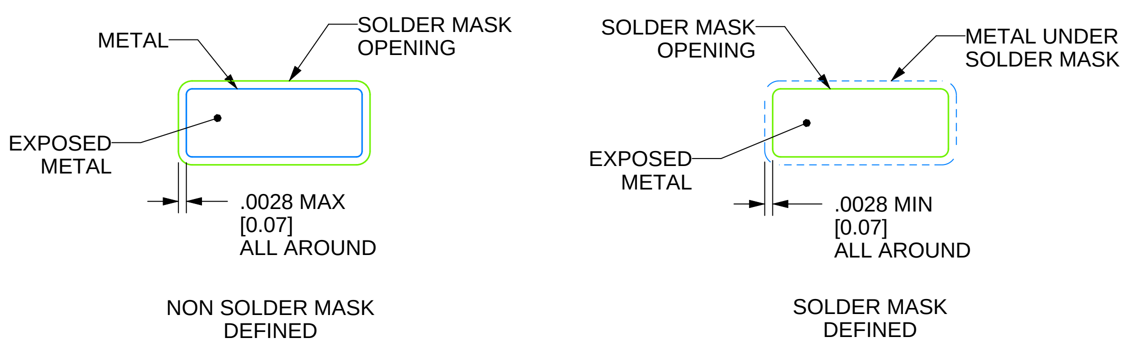


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

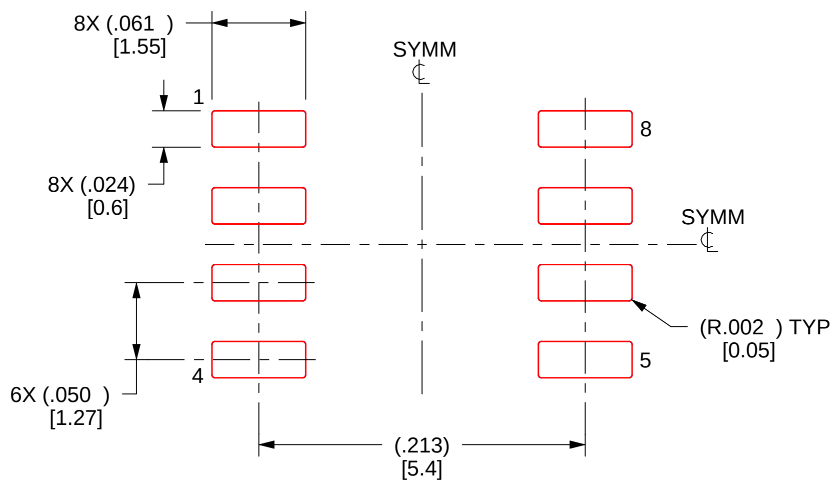


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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