



LM10-MIL オペアンプおよび基準電圧

1 特長

- 入力オフセット電圧: 2mV (最大値)
- 入力オフセット電流: 0.7nA (最大値)
- 入力バイアス電流: 20nA (最大値)
- 基準レギュレーション: 0.1% (最大値)
- オフセット電圧ドリフト係数: $2\mu\text{V}/^\circ\text{C}$
- 基準ドリフト係数: $0.002\%/^\circ\text{C}$

2 アプリケーション

- リモート・アンプ
- バッテリ残量インジケータ
- 熱電対トランスミッタ
- 電圧および電流レギュレータ

3 概要

LM10-MILはモノリシックなリニアICで、高精度の基準電圧、可変の基準バッファ、独立した高品質のオペアンプで構成されます。

このユニットは最低1.1V、最高40Vの合計電源電圧で動作でき、消費電流はわずか $270\mu\text{A}$ です。補完出力段は電源端子の15mV以内にシングするか、または $\pm 0.4\text{V}$ の飽和で $\pm 20\text{mA}$ の出力電流を供給します。基準電圧出力は最低200mVに設定できます。

この回路は携帯用機器向けに推奨され、単一の電源セルからの動作が完全に規定されています。一方で、電圧と電流の両方での高い出力駆動能力と、熱過負荷からの保護を備えているため、要求の厳しい汎用アプリケーションにも適しています。

このデバイスは、固定電源に依存しないフローティング・モードで動作できます。リモート・コンパレータ、信号コンディショナ、SCRコントローラまたはアナログ信号トランスミッタとして機能し、処理した信号を電源と同じラインで送出できます。このデバイスは、広範な電圧および電流レギュレータ・アプリケーションでの使用にも適しており、低電圧から数百ボルトまでに対応でき、既存のICよりも高い精度が得られます。

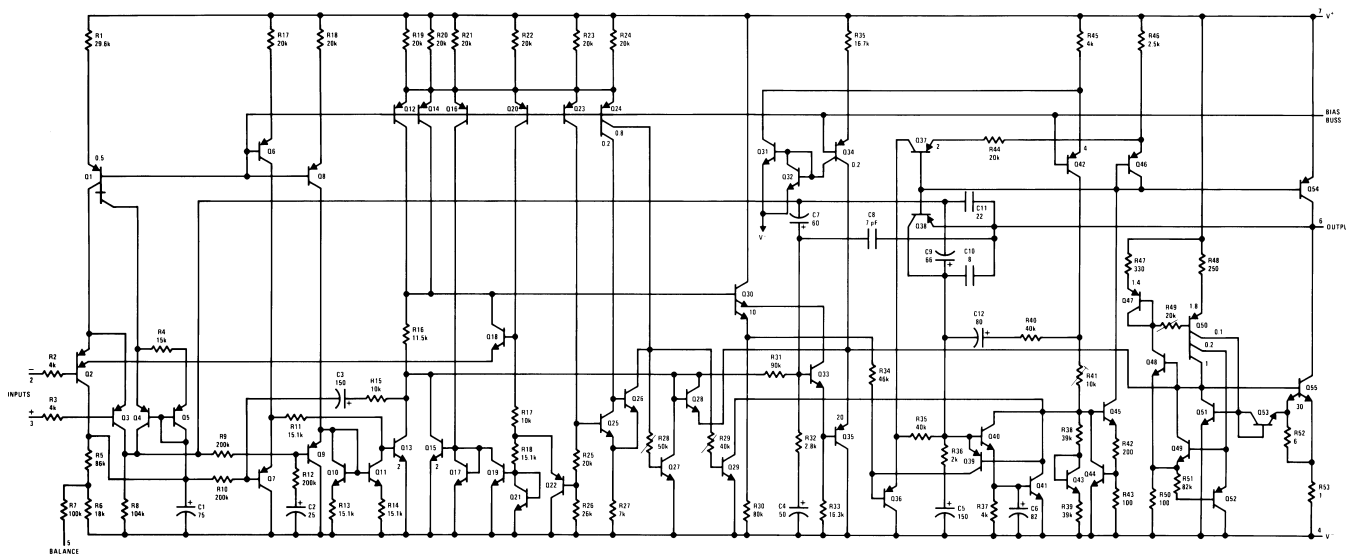
このシリーズは3つの標準温度範囲で利用可能で、商用部品では制限が緩和されています。さらに、低電圧仕様(接尾辞L)が用意されており、温度範囲が制限される代わりにコストを低減できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
LM10-MIL	SOIC (14)	8.992mm×7.498mm
	SDIP (8)	8.255mm×8.255mm
	PDIP (8)	9.81mm×6.35mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

オペアンプ回路図



(ピン番号は8ピン・パッケージのものです)



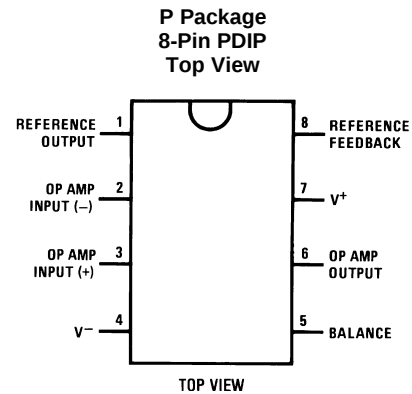
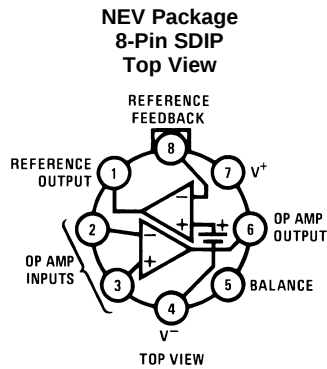
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4 改訂履歴

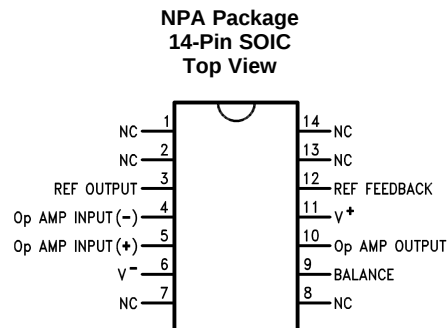
日付	改訂内容	注
2017年6月	*	初版

5 Pin Configuration and Functions



Pin Functions — 8-Pin SDIP or PDIP

PIN		I/O	DESCRIPTION
NAME	NO.		
Balance	5	I	Used for offset nulling
Op Amp Input (+)	3	I	Noninverting input of operational amplifier
Op Amp Input (-)	2	I	Inverting input of operational amplifier
Op Amp Output	6	O	Output terminal of operational amplifier
Reference Feedback	8	I	Feedback terminal of reference
Reference Output	1	O	Output terminal of reference
V+	7	I	Positive supply voltage
V-	4	I	Negative supply voltage



Pin Functions — 14-Pin SOIC

PIN		I/O	DESCRIPTION
NAME	NO.		
Balance	9	I	Used for offset nulling
NC	1, 2, 7, 8, 14, 13	—	No connection
Op Amp Input (-)	4	I	Inverting input of operational amplifier
Op Amp Input (+)	5	I	Noninverting input of operational amplifier
Op Amp Output	10	O	Output terminal of operational amplifier
Reference Feedback	12	I	Feedback terminal of reference
Reference Output	3	O	Output terminal of reference
V+	11	I	Positive supply voltage
V-	6	I	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

 See ⁽¹⁾⁽²⁾⁽³⁾

			MIN	MAX	UNIT
Total supply voltage			45		V
Differential input voltage ⁽⁴⁾			±40		V
Power dissipation ⁽⁵⁾			Internally limited		
Output short-circuit duration ⁽⁶⁾			Continuous		
Lead temperature	TO	Soldering (10 seconds)	300		°C
	DIP	Soldering (10 seconds)	260		°C
		Vapor phase (60 seconds)	215		°C
		Infrared (15 seconds)	220		°C
Maximum junction temperature			150		°C
Storage temperature, T _{stg}			-55	150	°C

- (1) Refer to RETS10X for LM10H military specifications.
- (2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.
- (5) The maximum, operating-junction temperature is 150°C for the LM10-MIL. At elevated temperatures, devices must be derated based on package thermal resistance.
- (6) Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply input voltage range (V ⁻) – (V ⁺)	1.2		40	V
V _{CM}	Common-mode voltage	(V ⁻)		(V ⁺) – 0.85	V
V _{REF}	Reference voltage		0.2		V
I _{REF}	Reference current	0		1	mA

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		LM10-MIL			UNIT
		NEV (SDIP)	NPA (SOIC)	P (PDIP)	
		8 PINS	14 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	150	90	87	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	45	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.4 Electrical Characteristics

 $T_J = 25^\circ\text{C}$ unless otherwise specified⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	$T_J = 25^\circ\text{C}$		0.3	2	mV
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			3	mV
Input offset current ⁽²⁾	$T_J = 25^\circ\text{C}$		0.25	0.7	nA
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			1.5	nA
Input bias current	$T_J = 25^\circ\text{C}$		10	20	nA
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			30	nA
Input resistance	$T_J = 25^\circ\text{C}$	250	500		k Ω
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	150			k Ω
Large signal voltage gain	$V_S = \pm 20\text{ V}$, $I_{\text{OUT}} = 0$	120	400		V/mV
	$V_{\text{OUT}} = \pm 19.95\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	80			V/mV
	$V_S = \pm 20\text{ V}$, $V_{\text{OUT}} = \pm 19.4\text{ V}$	50	130		V/mV
	$I_{\text{OUT}} = \pm 20\text{ mA}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	20			V/mV
	$I_{\text{OUT}} = \pm 15\text{ mA}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	20			V/mV
	$V_S = \pm 0.6\text{ V}$, $I_{\text{OUT}} = \pm 2\text{ mA}$	1.5	3		V/mV
	$V_S = \pm 0.65\text{ V}$, $I_{\text{OUT}} = \pm 2\text{ mA}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	1.5	3		V/mV
	$V_{\text{OUT}} = \pm 0.4\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	0.5			V/mV
	$V_{\text{OUT}} = \pm 0.3\text{ V}$, $V_{\text{CM}} = -0.4\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	0.5			V/mV
Shunt gain ⁽³⁾	$1.2\text{ V} \leq V_{\text{OUT}} \leq 40\text{ V}$, $R_L = 1.1\text{ k}\Omega$	14	33		V/mV
	$1.3\text{ V} \leq V_{\text{OUT}} \leq 40\text{ V}$, $R_L = 1.1\text{ k}\Omega$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	14	33		V/mV
	$0.1\text{ mA} \leq I_{\text{OUT}} \leq 5\text{ mA}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	6			V/mV
	$1.5\text{ V} \leq V^+ \leq 40\text{ V}$, $R_L = 250\text{ }\Omega$	8	25		V/mV
	$0.1\text{ mA} \leq I_{\text{OUT}} \leq 20\text{ mA}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	4			V/mV
Common-mode rejection	$-20\text{ V} \leq V_{\text{CM}} \leq 19.15\text{ V}$	93	102		dB
	$-20\text{ V} \leq V_{\text{CM}} \leq 19\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	93	102		dB
	$V_S = \pm 20\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	87			dB
Supply-voltage rejection	$-0.2\text{ V} \geq V^- \geq -39\text{ V}$	90	96		dB
	$V^+ = 1\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	84			dB
	$V^+ = 1.1\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	84			dB
	$1\text{ V} \leq V^+ \leq 39.8\text{ V}$	96	106		dB
	$1.1\text{ V} \leq V^+ \leq 39.8\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	96	106		dB
	$V^- = -0.2\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	90			dB
Offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
Offset current drift			2		pA/ $^\circ\text{C}$
Bias current drift	$T_C < 100^\circ\text{C}$		60		pA/ $^\circ\text{C}$
Line regulation	$1.2\text{ V} \leq V_S \leq 40\text{ V}$		0.001	0.003	%/V
	$1.3\text{ V} \leq V_S \leq 40\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)		0.001	0.003	%/V
	$0 \leq I_{\text{REF}} \leq 1\text{ mA}$, $V_{\text{REF}} = 200\text{ mV}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			0.006	%/V
Load regulation	$0 \leq I_{\text{REF}} \leq 1\text{ mA}$		0.01%	0.1%	
	$V^+ - V_{\text{REF}} \geq 1\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			0.15%	
	$V^+ - V_{\text{REF}} \geq 1.1\text{ V}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			0.15%	

(1) These specifications apply for $V^- \leq V_{\text{CM}} \leq V^+ - 0.85\text{ V}$, 1 V ($T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$), 1.2 V , 1.3 V ($T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$) $< V_S \leq V_{\text{MAX}}$, $V_{\text{REF}} = 0.2\text{ V}$ and $0 \leq I_{\text{REF}} \leq 1\text{ mA}$, unless otherwise specified: $V_{\text{MAX}} = 40\text{ V}$ for the standard part and 6.5 V for the low voltage part. The full-temperature-range operation is -55°C to 125°C for the LM10-MIL. The specifications do not include the effects of thermal gradients ($\tau_1 \approx 20\text{ ms}$), die heating ($\tau_2 \approx 0.2\text{ s}$) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

(2) For $T_J > 90^\circ\text{C}$, I_{OS} may exceed 1.5 nA for $V_{\text{CM}} = V^-$. With $T_J = 125^\circ\text{C}$ and $V^- \leq V_{\text{CM}} \leq V^- + 0.1\text{ V}$, $I_{\text{OS}} \leq 5\text{ nA}$.

(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see [System Examples](#)). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Electrical Characteristics (continued)
 $T_J = 25^\circ\text{C}$ unless otherwise specified⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Amplifier gain	$0.2\text{ V} \leq V_{\text{REF}} \leq 35\text{ V}$	$T_J = 25^\circ\text{C}$	50	75		V/mV
		$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)	23			V/mV
Feedback sense voltage	$T_J = 25^\circ\text{C}$		195	200	205	mV
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)		194		206	mV
Feedback current	$T_J = 25^\circ\text{C}$			20	50	nA
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)				65	nA
Reference drift				0.002		%/ $^\circ\text{C}$
Supply current	$T_J = 25^\circ\text{C}$			270	400	μA
	$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)				500	μA
Supply current change	$1.2\text{ V} \leq V_S \leq 40\text{ V}$	$T_J = 25^\circ\text{C}$		15		μA
		$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			75	
	$1.3\text{ V} \leq V_S \leq 40\text{ V}$	$T_J = 25^\circ\text{C}$		15		μA
		$T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$ (see ⁽¹⁾)			75	

6.5 Typical Characteristics

6.5.1 Typical Characteristics (Op Amp)

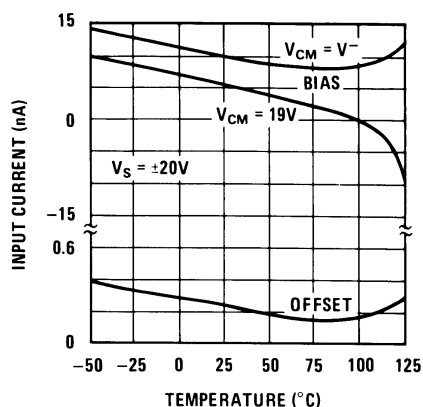


Figure 1. Input Current

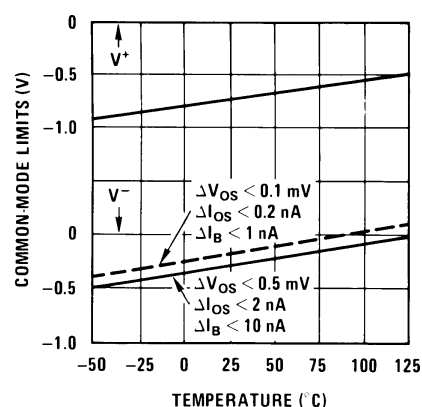


Figure 2. Common-Mode Limits

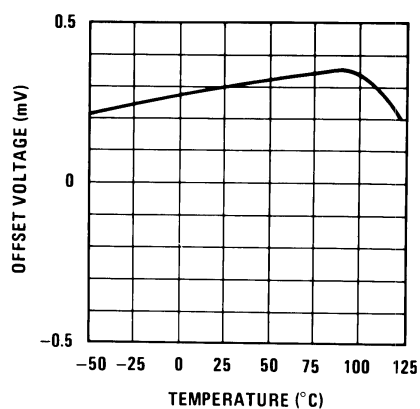


Figure 3. Output Voltage Drift

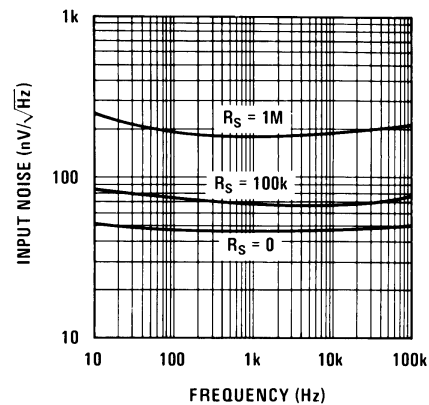


Figure 4. Input Noise Voltage

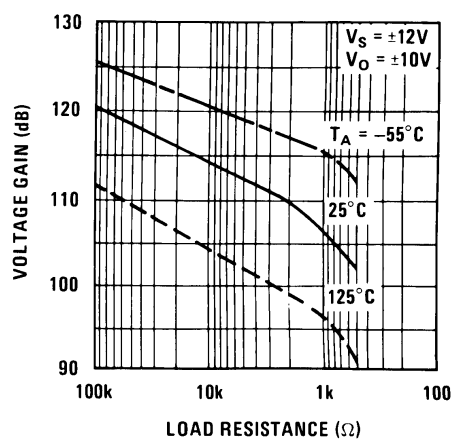


Figure 5. DC Voltage Gain

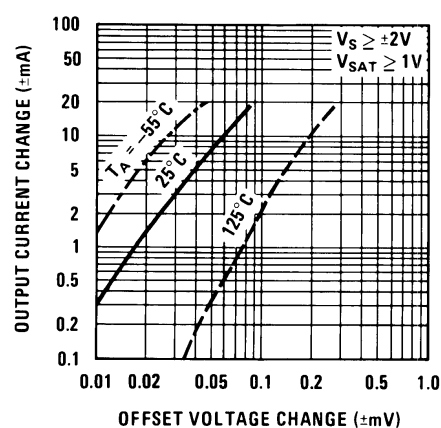


Figure 6. Transconductance

Typical Characteristics (Op Amp) (continued)

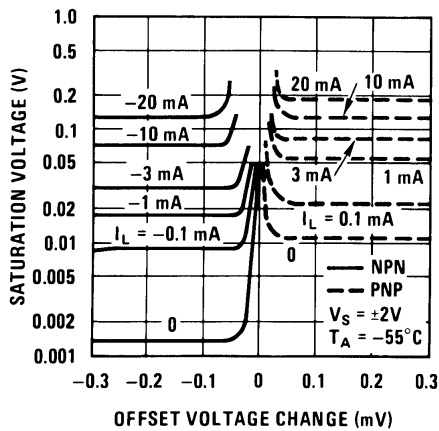


Figure 7. Output Saturation Characteristics

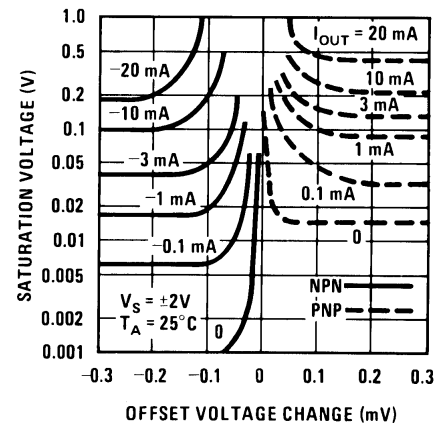


Figure 8. Output Saturation Characteristics

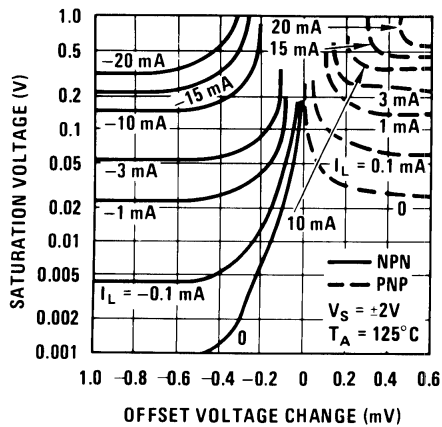


Figure 9. Output Saturation Characteristics

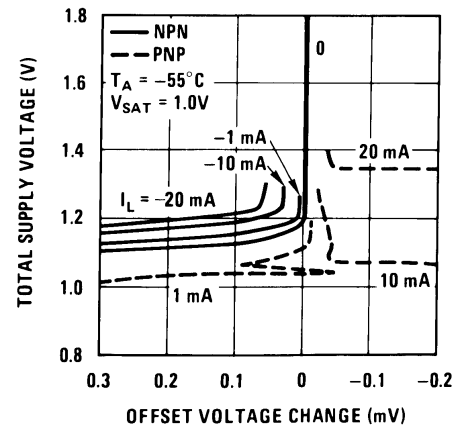


Figure 10. Minimum Supply Voltage

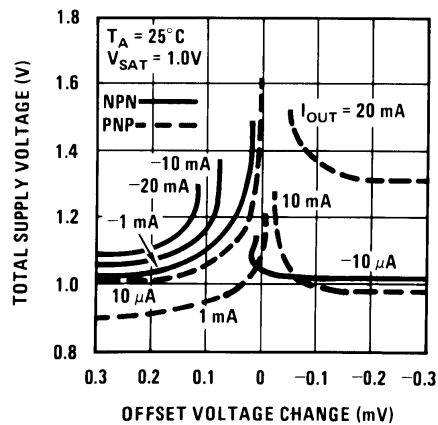


Figure 11. Minimum Supply Voltage

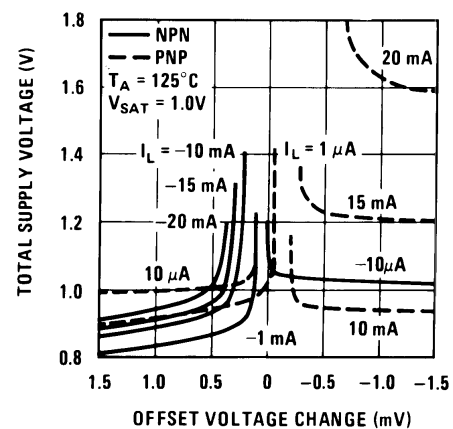


Figure 12. Minimum Supply Voltage

Typical Characteristics (Op Amp) (continued)

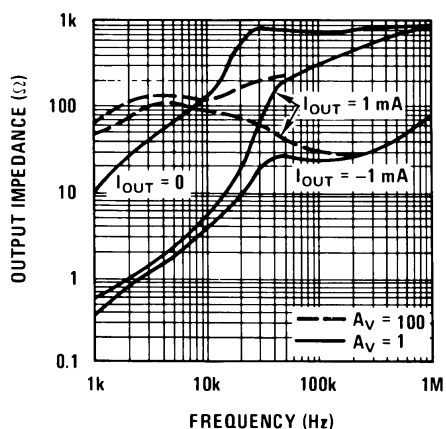


Figure 13. Output Impedance

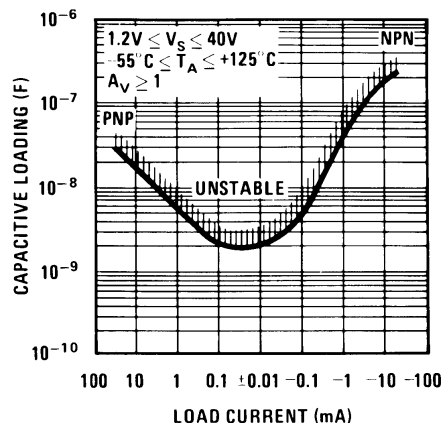


Figure 14. Typical Stability Range

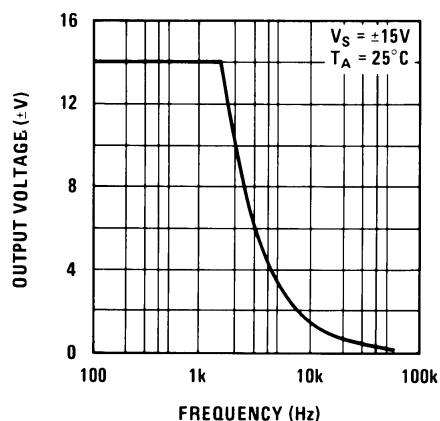


Figure 15. Large Signal Response

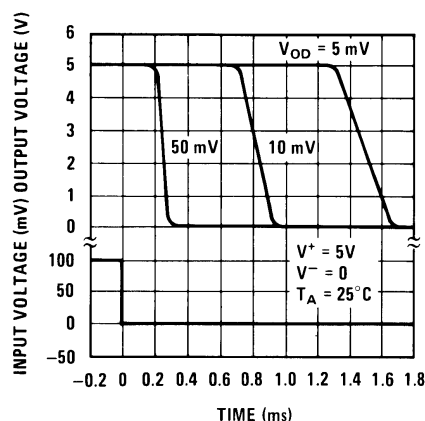


Figure 16. Comparator Response Time For Various Input Overdrives

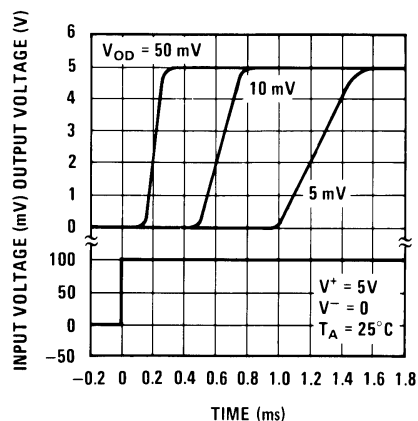


Figure 17. Comparator Response Time For Various Input Overdrives

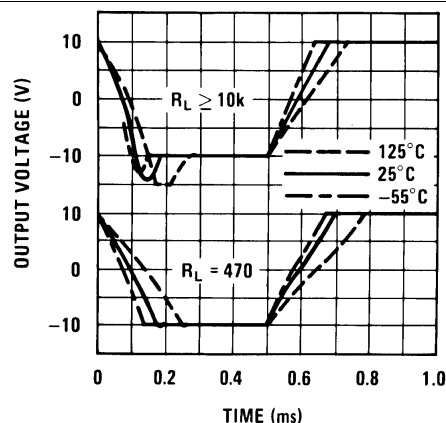


Figure 18. Follower Pulse Response

Typical Characteristics (Op Amp) (continued)

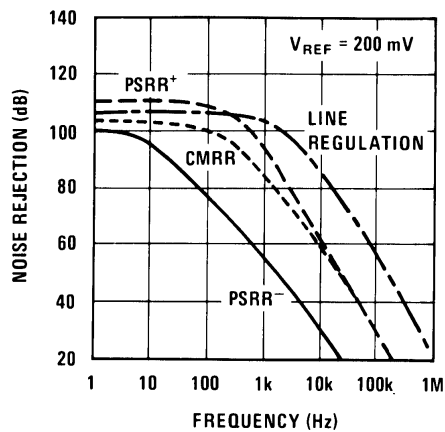


Figure 19. Noise Rejection

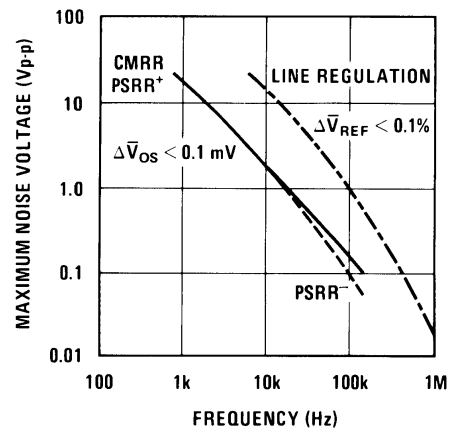


Figure 20. Rejection Slew Limiting

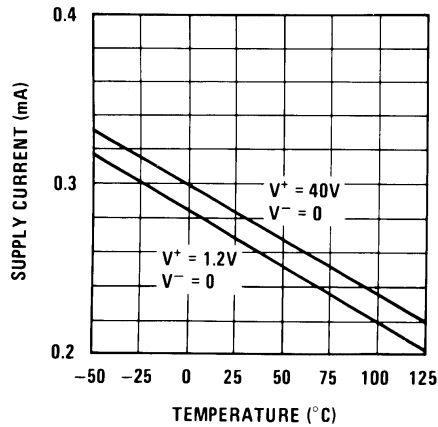


Figure 21. Supply Current

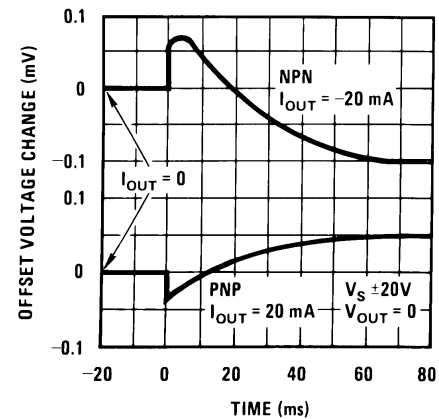


Figure 22. Thermal Gradient Feedback

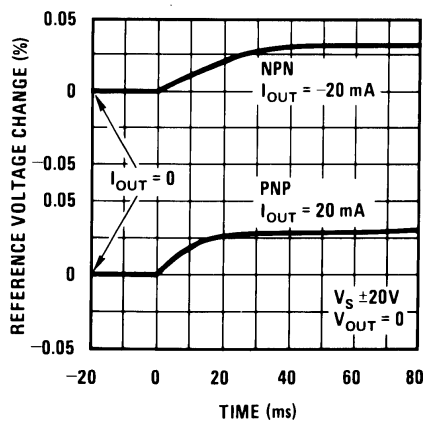


Figure 23. Thermal Gradient Cross-Coupling

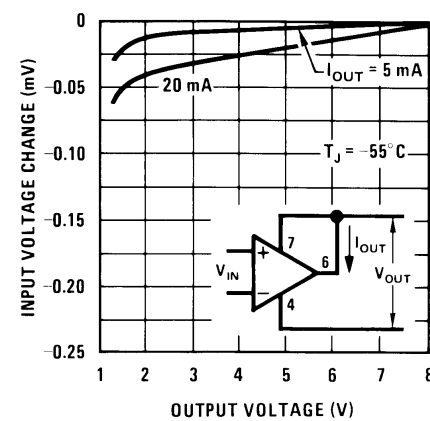


Figure 24. Shunt Gain

Typical Characteristics (Op Amp) (continued)

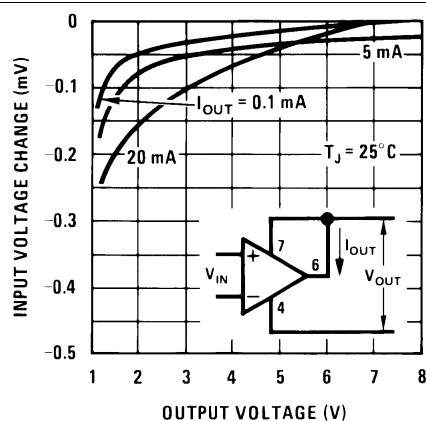


Figure 25. Shunt Gain

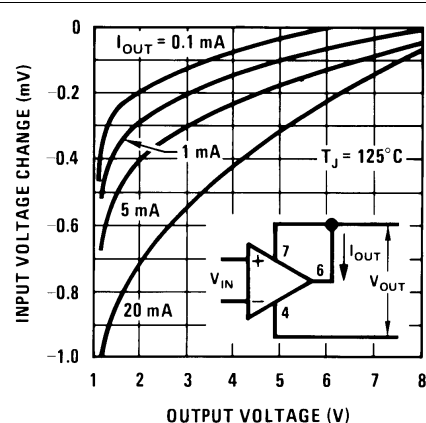


Figure 26. Shunt Gain

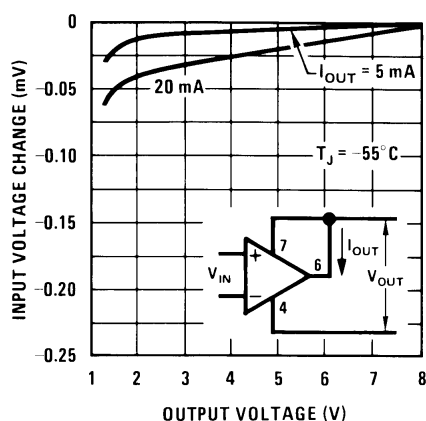


Figure 27. Shunt Gain

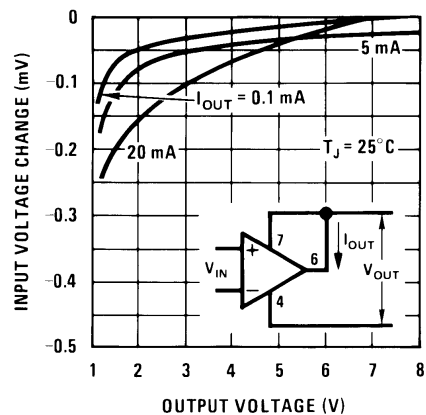


Figure 28. Shunt Gain

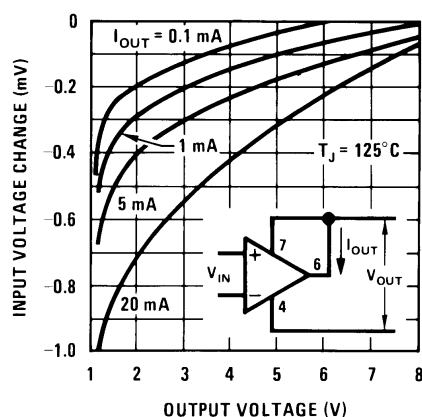


Figure 29. Shunt Gain

6.5.2 Typical Characteristics (Reference)

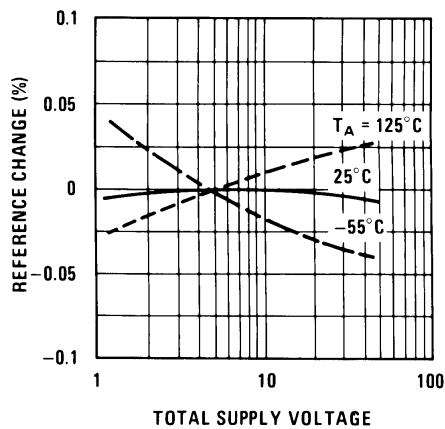


Figure 30. Line Regulation

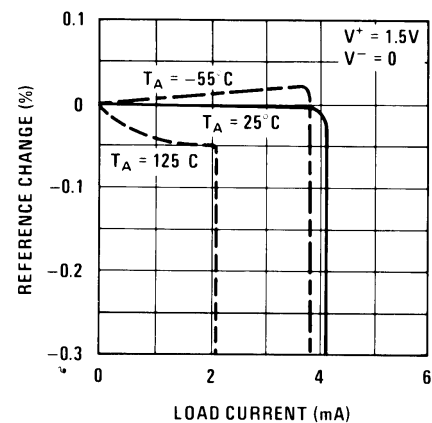


Figure 31. Load Regulation

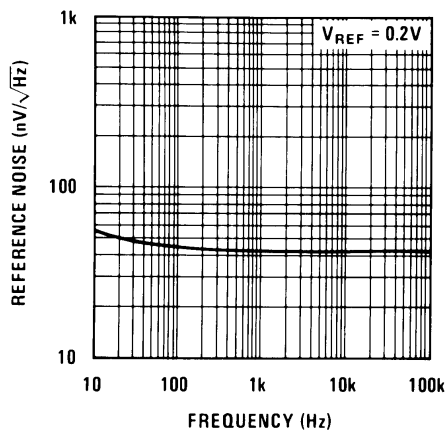


Figure 32. Reference Noise Voltage

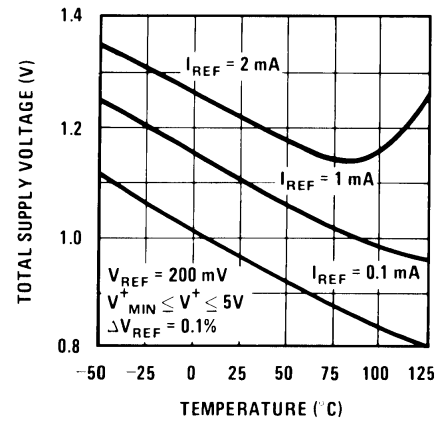


Figure 33. Minimum Supply Voltage

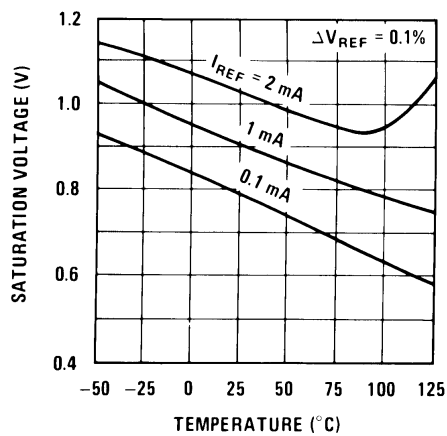


Figure 34. Output Saturation

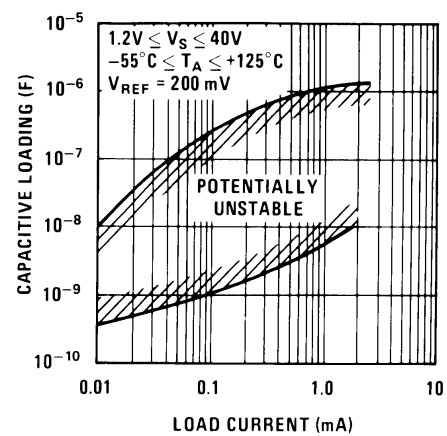


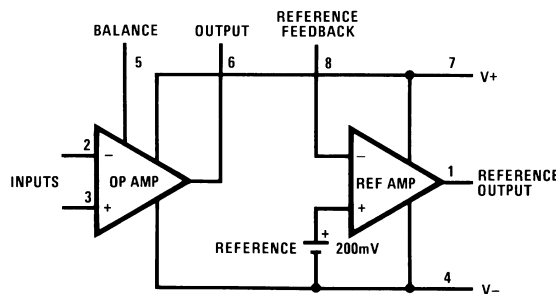
Figure 35. Typical Stability Range

7 Detailed Description

7.1 Overview

The LM10-MIL is a dual-operational amplifier combined with a voltage reference capable of a single-supply operation down to 1.1 V. It provides high overall performance, making it ideal for many general-purpose applications. The circuit can also operate in a floating mode, powered by residual voltage, independent of fixed supplies and it is well-protected from temperature drift.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The LM10-MIL is specified for operation from 1.2 V to 40 V. Many of the specifications apply from -55°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in electrical characteristics tables under [Specifications](#) and in the [Typical Characteristics](#) section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the LM10-MIL extends from the negative rail to 0.85 V less than the positive rail.

7.3.3 Operational Amplifier

The minimum operating voltage is reduced to nearly one volt and the current gain is less affected by temperature, resulting in a fairly flat bias current over temperature.

7.3.4 Voltage Reference

Second-order nonlinearities are compensated for which eliminates the bowed characteristics of conventional designs, resulting in better temperature stability.

7.4 Device Functional Modes

7.4.1 Floating Mode

To use the device in a floating mode, the operational amplifier output is shorted to $V+$ which disables the PNP portion of the output stage. Thus, with a positive input signal, neither halves of the output conducts and the current between the supply terminals is equal to the quiescent supply current. With negative input signals, the NPN portion of the output begins to turn on, reaching the short circuit current for a few hundred microvolts overdrive.

7.4.2 Linear Operation

This device can also operate linearly while in the floating mode. An example of this is shown in the [Typical Application](#) section.

8 Application and Implementation

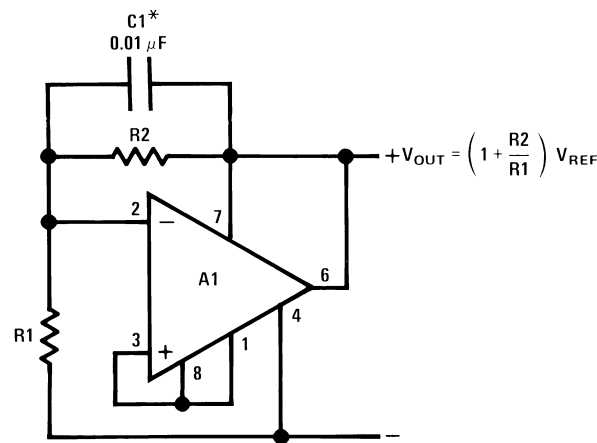
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

With heavy amplifier loading to V^- , resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach $1\ \Omega$. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

8.2 Typical Application



* required for capacitive loading

Figure 36. Shunt Voltage Regulator

8.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Ambient Temperature Range	–55°C to 125°C
Supply Voltage Range	1.2 V to 40 V
Common-Mode Input Range	(V^-) to (V^+) – 0.85 V

8.2.2 Detailed Design Procedure

Given that the transfer function of this circuit is:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) V_{REF} \quad (1)$$

the output can be set between 0.2 V and the breakdown voltage of the IC by selecting an appropriate value for R_2 . The circuit regulates for input voltages within a saturation drop of the output (typically 0.4 V at 20 mA and 0.15 V at 5 mA). The regulator is protected from shorts or overloads by current limiting and thermal shutdown.

Typical regulation is about 0.05% load and 0.003%/V line. A substantial improvement in regulation can be effected by connecting the operational amplifier as a follower and setting the reference to the desired output voltage. This has the disadvantage that the minimum input-output differential is increased to a little more than a diode drop. If the operational amplifier were connected for a gain of 2, the output could again saturate. But this requires an additional pair of precision resistors.

The regulator in [Figure 36](#) could be made adjustable to zero by connecting the operational amplifier to a potentiometer on the reference output. This has the disadvantage that the regulation at the lower voltage settings is not as good as it might otherwise be.

8.2.3 Application Curve

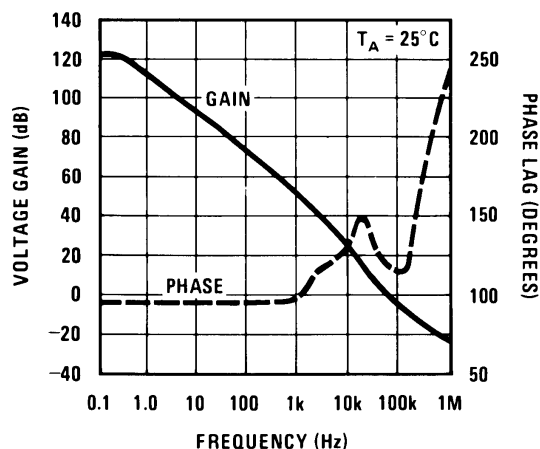


Figure 37. Frequency Response

8.3 System Examples

Circuit descriptions available in application note AN-211 ([SNOA638](#)).

8.3.1 Operational Amplifier Offset Adjustment

(Pin numbers are for 8-pin packages)

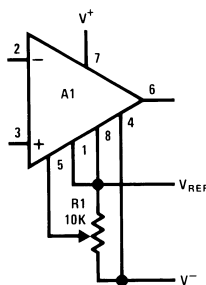


Figure 38. Standard

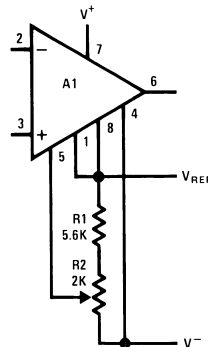


Figure 39. Limited Range

System Examples (continued)

(Pin numbers are for 8-pin packages)

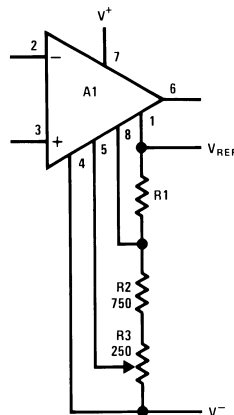


Figure 40. Limited Range With Boosted Reference

8.3.2 Positive Regulators

(Pin numbers are for 8-pin packages)

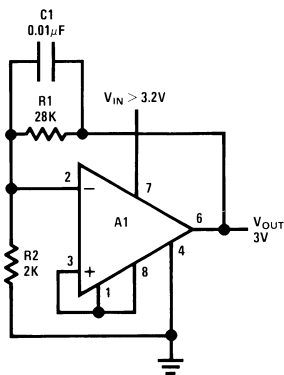


Figure 41. Low Voltage

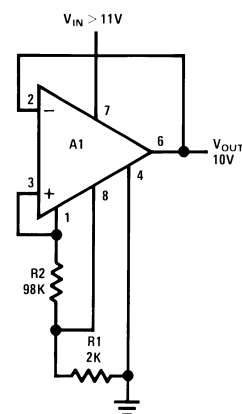
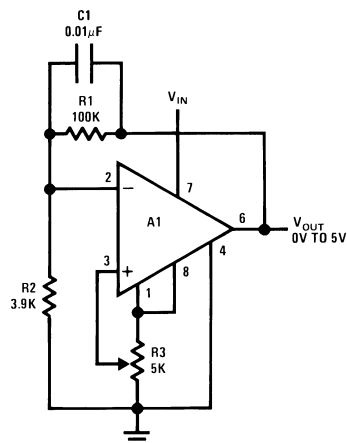


Figure 42. Best Regulation



Use only electrolytic output capacitors.

Figure 43. Zero Output

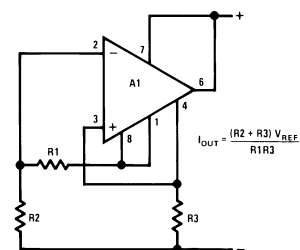
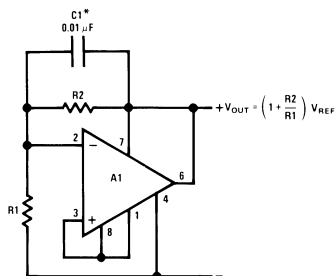


Figure 44. Current Regulator

System Examples (continued)

(Pin numbers are for 8-pin packages)



Required For Capacitive Loading

Figure 45. Shunt Regulator

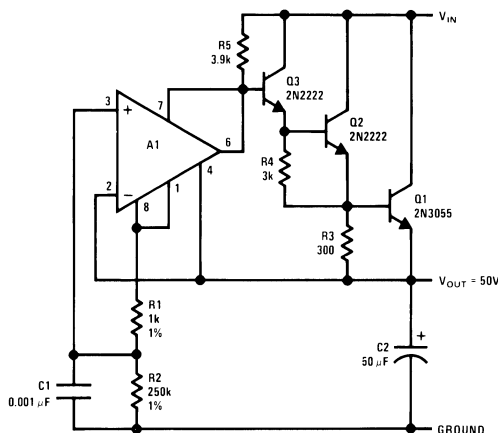
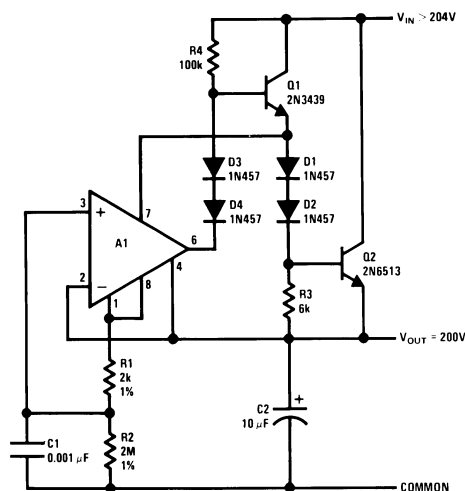
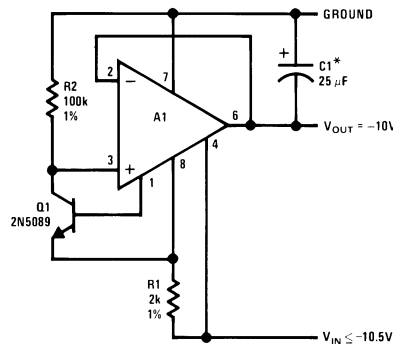


Figure 47. Precision Regulator



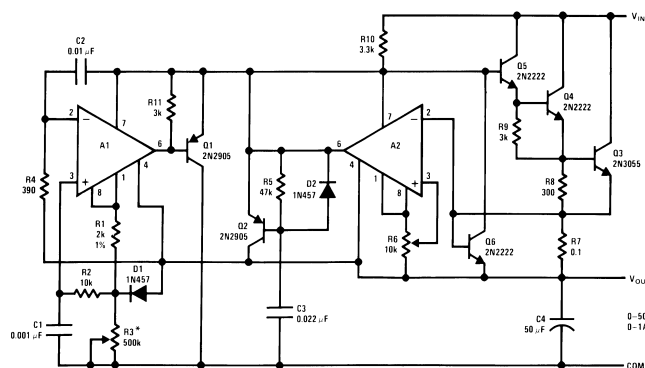
$$V_{OUT} = \frac{R_2}{R_1} V_{REF}$$

Figure 49. HV Regulator



*Electrolytic

Figure 46. Negative Regulator



$$*V_{OUT} = 10^{-4} R_3$$

Figure 48. Laboratory Power Supply

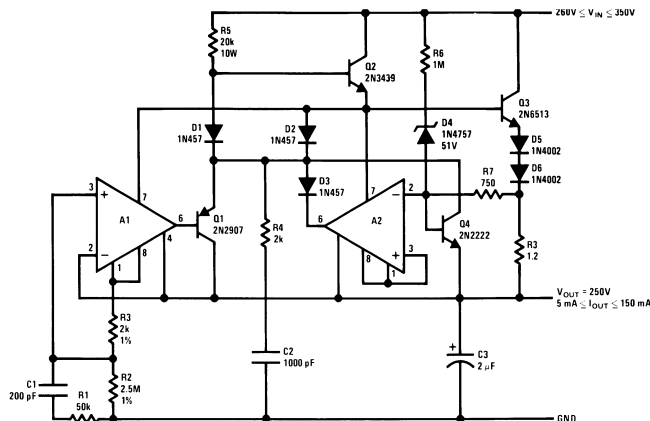
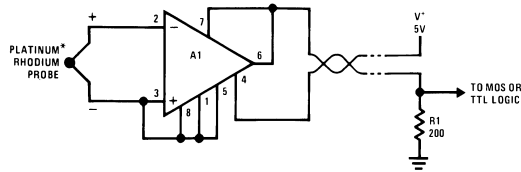


Figure 50. Protected HV Regulator

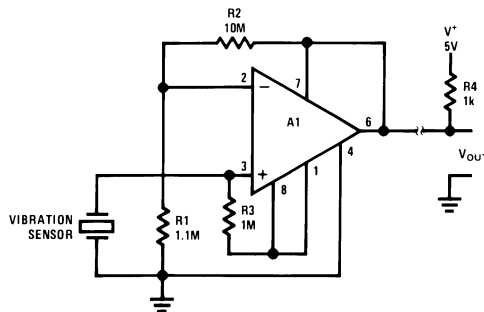
System Examples (continued)

(Pin numbers are for 8-pin packages)



*800°C Threshold Is Established By Connecting Balance To V_{REF} .

Figure 51. Flame Detector



*Provides Hysteresis

Figure 52. Light Level Sensor

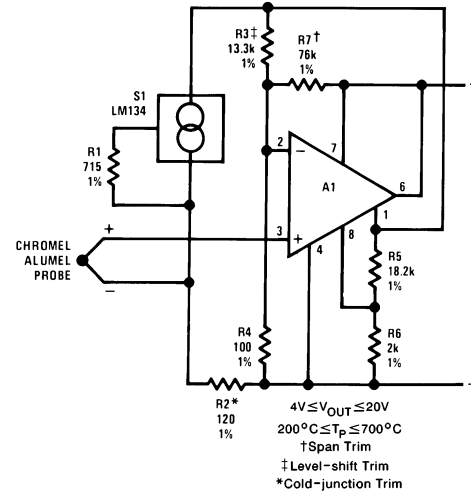


Figure 53. Remote Amplifier

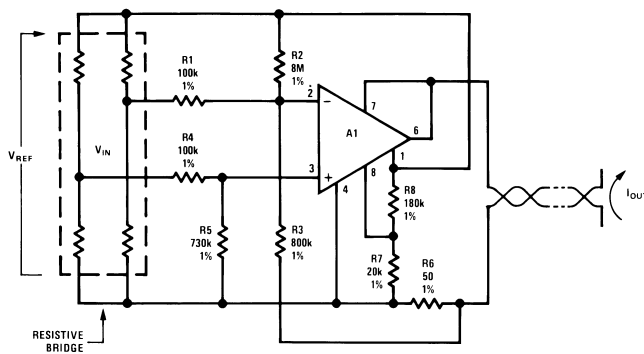


Figure 54. Remote Thermocouple Amplifier

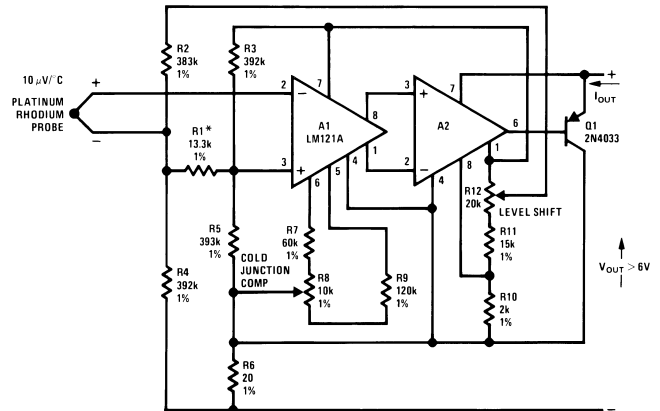


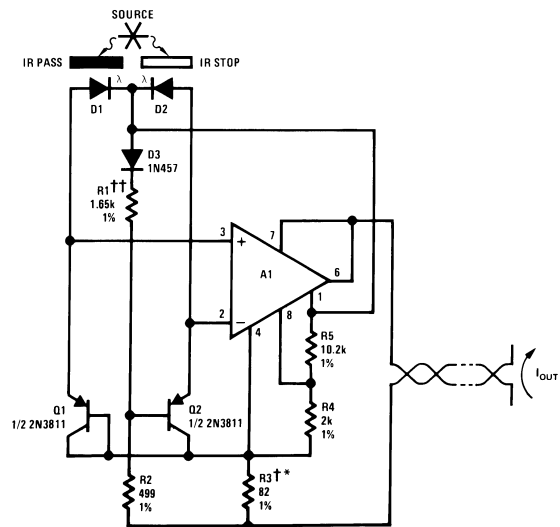
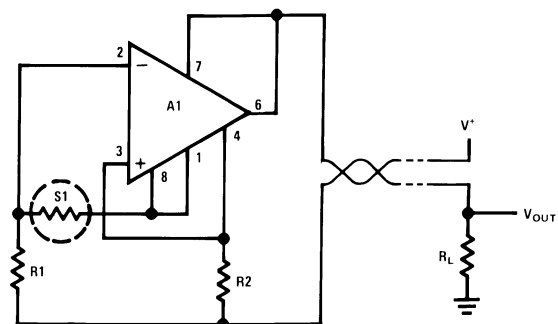
Figure 55. Transmitter for Bridge Sensor

$10 \mu V/^\circ C$
 $10 \text{ mA} \leq I_{OUT} \leq 50 \text{ mA}$
 $500^\circ C \leq T_P \leq 1500^\circ C$
 $*$ Gain Trim

Figure 56. Precision Thermocouple Transmitter

System Examples (continued)

(Pin numbers are for 8-pin packages)



††Level-shift Trim

*Scale Factor Trim

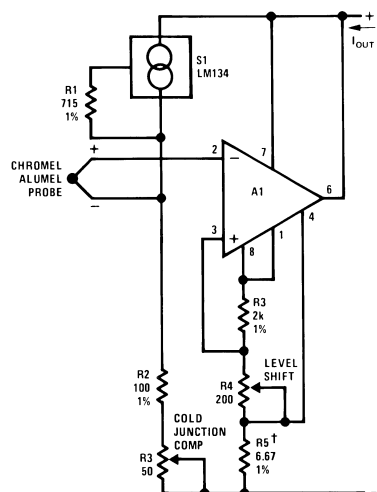
†Copper Wire Wound

$1 \text{ mA} \leq I_{OUT} \leq 5 \text{ mA}$

$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

Figure 57. Resistance Thermometer Transmitter

Figure 58. Optical Pyrometer

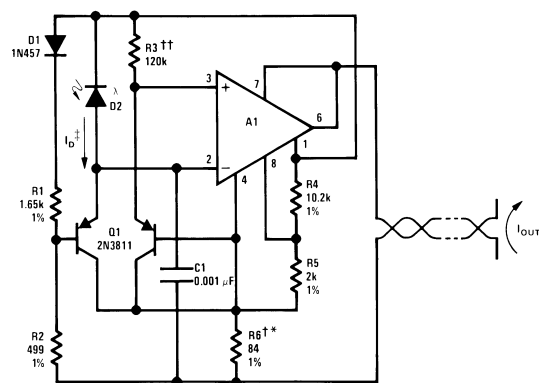


$200^{\circ}\text{C} \leq T_P \leq 700^{\circ}\text{C}$

$1 \text{ mA} \leq I_{OUT} \leq 5 \text{ mA}$

†Gain Trim

Figure 59. Thermocouple Transmitter



$1 \text{ mA} \leq I_{OUT} \leq 5 \text{ mA}$

$\pm 50 \mu\text{A} \leq I_D \leq 500 \mu\text{A}$

††Center Scale Trim

†Scale Factor Trim

*Copper Wire Wound

Figure 60. Logarithmic Light Sensor

System Examples (continued)

(Pin numbers are for 8-pin packages)

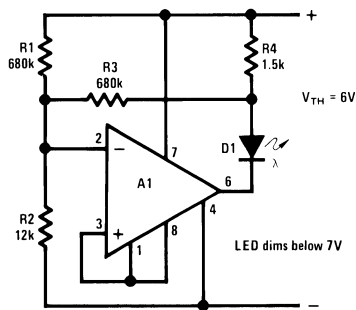


Figure 61. Battery-level Indicator

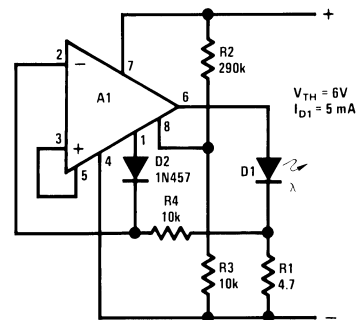
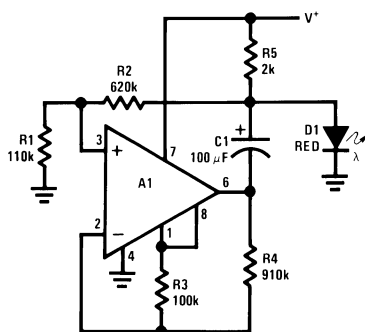
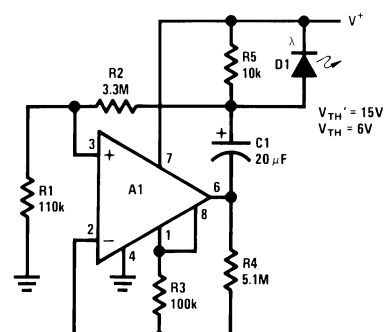


Figure 62. Battery-threshold Indicator



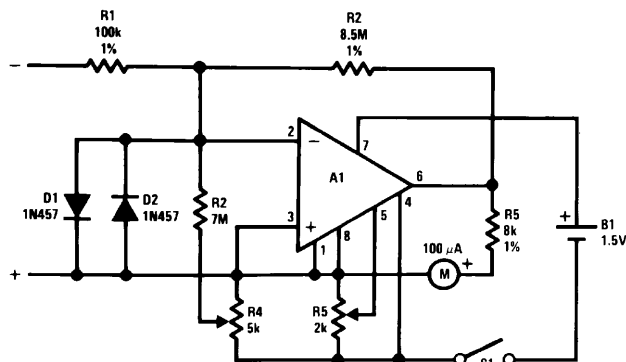
Flashes Above 1.2V
Rate Increases With
Voltage

Figure 63. Single-cell Voltage Monitor



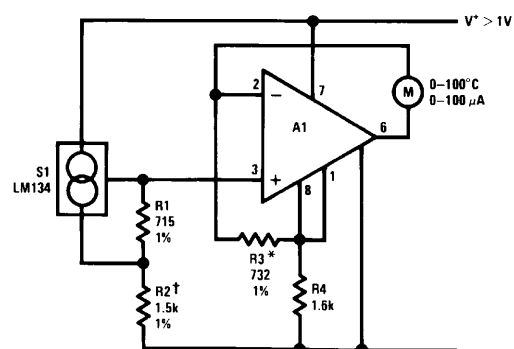
Flash Rate Increases
Above 6V and Below 15V

Figure 64. Double-ended Voltage Monitor



INPUT
10 mV, 100nA
FULL-SCALE

Figure 65. Meter Amplifier



*Trim For Span
†Trim For Zero

Figure 66. Thermometer

System Examples (continued)

(Pin numbers are for 8-pin packages)

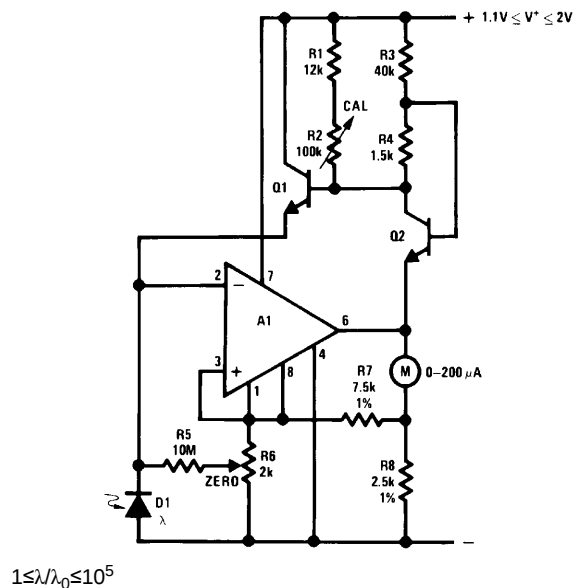
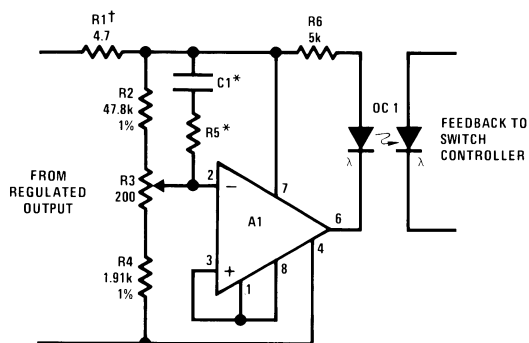


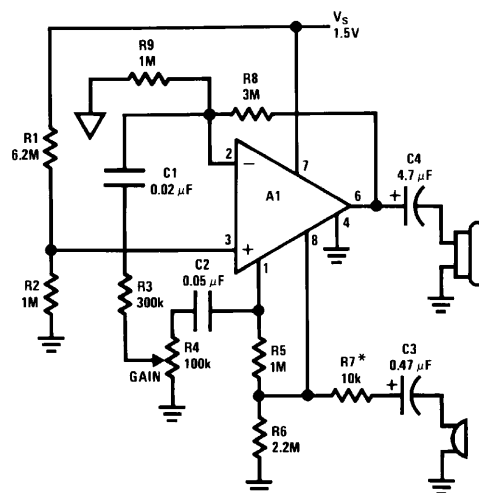
Figure 67. Light Meter



†Controls "Loop Gain"

*Optional Frequency Shaping

Figure 69. Isolated Voltage Sensor



$Z_{OUT} \sim 680\Omega @ 5 \text{ kHz}$

$A_V \leq 1k$

$f_1 \sim 100 \text{ Hz}$

$f_2 \sim 5 \text{ kHz}$

$R_L \sim 500$

*Max Gain Trim

Figure 68. Microphone Amplifier

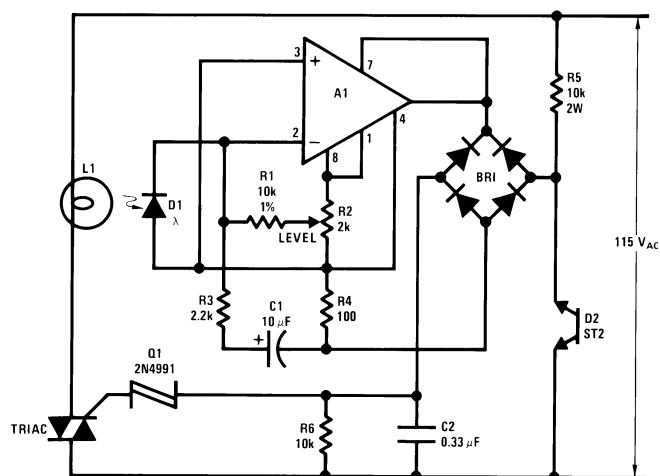


Figure 70. Light-Level Controller

System Examples (continued)

(Pin numbers are for 8-pin packages)

8.3.3 Reference and Internal Regulator

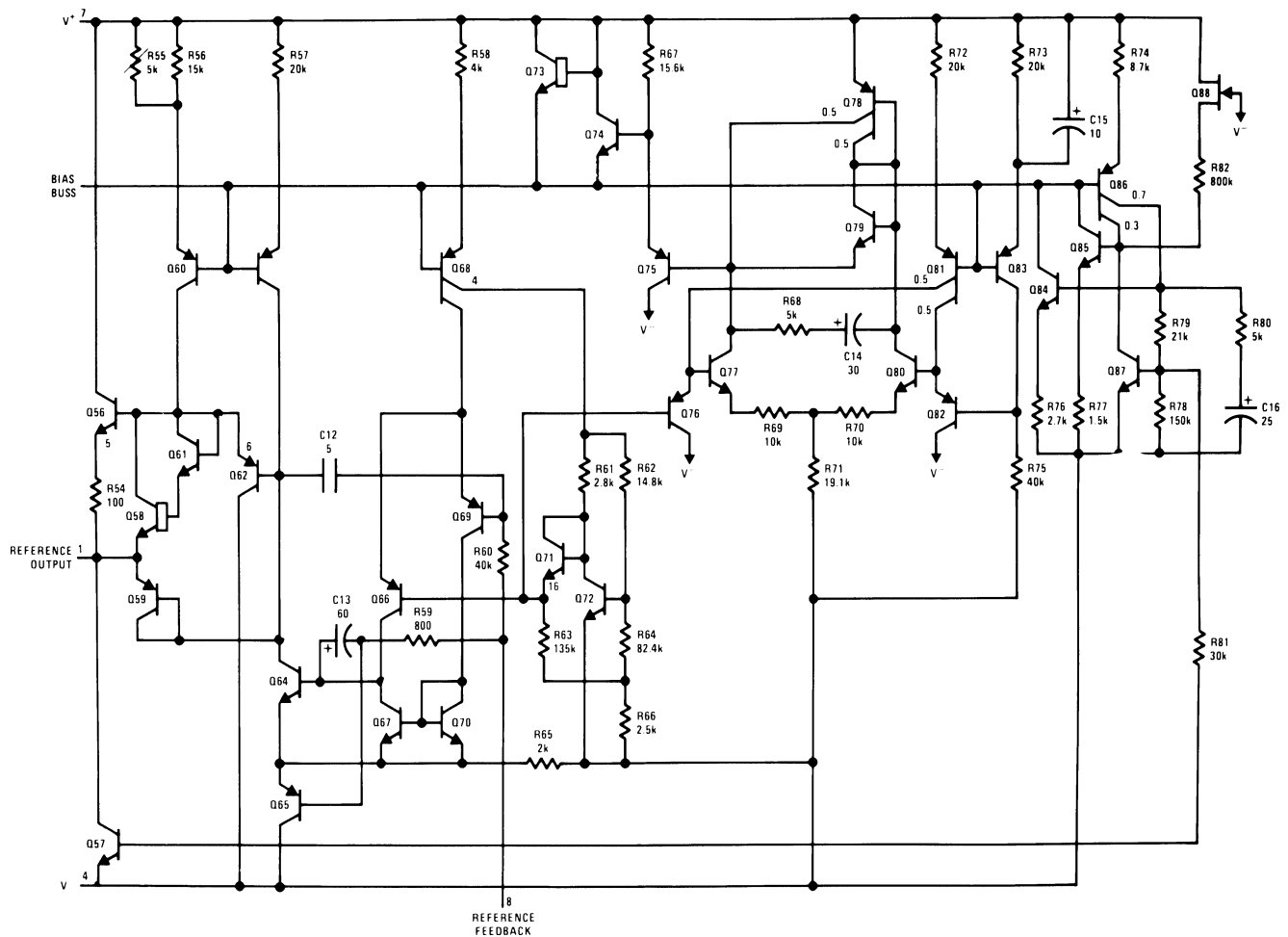


Figure 71. Reference and Internal Regulator

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの関連用語

11.1.1.1 用語の定義

入力オフセット電圧: 無負荷時の出力を線形領域内にバイアスするため、入力端子間に印加する必要がある電圧。

入力オフセット電流: 無負荷時の出力が線形領域内にあるとき、入力端子における電流の差分。

入力バイアス電流: 2つの入力電流の平均の絶対値。

入力抵抗: 一方の入力端子が接地しているとき、もう一方の入力における入力電圧の変化と、入力電流の変化との比率。

大信号電圧ゲイン: 指定された出力電圧スイングと、それを生成するため必要な差動入力電圧の変化との比率。

シャント・ゲイン: 出力がICの V^+ 端子に接続されているとき、指定された出力電圧スイングと、それを生成するため必要な差動入力電圧の変化との比率。負荷と電源は V^+ 端子と V^- 端子との間に接続され、入力同相モードは V^- 端子を基準とします。

同相除去: 入力電圧範囲と、両極間のオフセット電圧変化との比率。

電源電圧除去: 指定された電源電圧変化と、両極間のオフセット電圧変化との比率。

ライン・レギュレーション: 指定された電源電圧範囲全体にわたる基準出力電圧の平均変化量。

負荷レギュレーション: 無負荷から、指定された負荷までにわたる基準出力電圧の変化。

帰還検知電圧: レギュレーション動作中の基準帰還端子の電圧で、 V^- を基準とします。

基準アンプ・ゲイン: 指定された基準出力電圧変化と、それを生成するために必要な帰還検知電圧の変化との比率。

帰還電流: レギュレーション動作中の、帰還端子における電流の絶対値。

消費電流: アンプと基準電圧の出力が無負荷で、線形範囲内で動作しているとき、アンプと基準電圧が動作するため電源から供給する必要がある電流。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

『AN-211 新しいオペアンプのアイディア』、[SNOA638](#)

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項



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11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10BH	ACTIVE	TO-CAN	LMG	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85	(LM10BH, LM10BH)	Samples
LM10BH/NOPB	ACTIVE	TO-CAN	LMG	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85	(LM10BH, LM10BH)	Samples
LM10CH	ACTIVE	TO-CAN	LMG	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	(LM10CH, LM10CH)	Samples
LM10CH/NOPB	ACTIVE	TO-CAN	LMG	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	(LM10CH, LM10CH)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

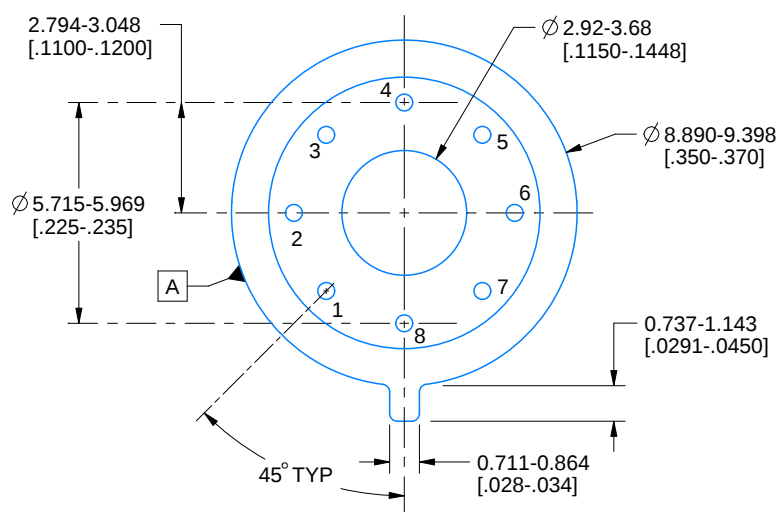
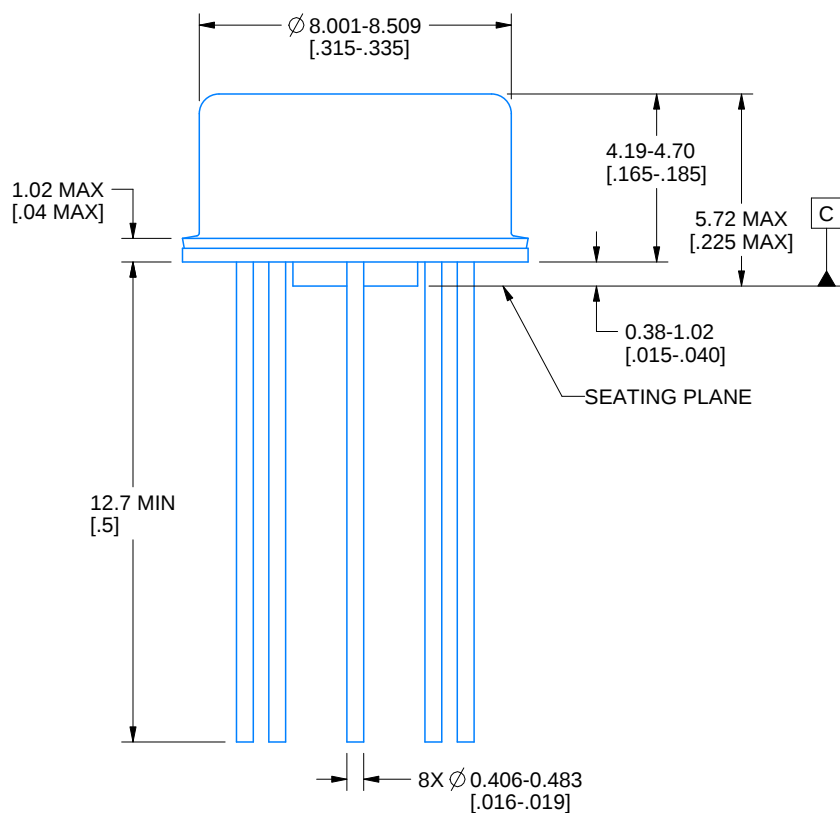
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PACKAGE OUTLINE

LMG0008A

TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



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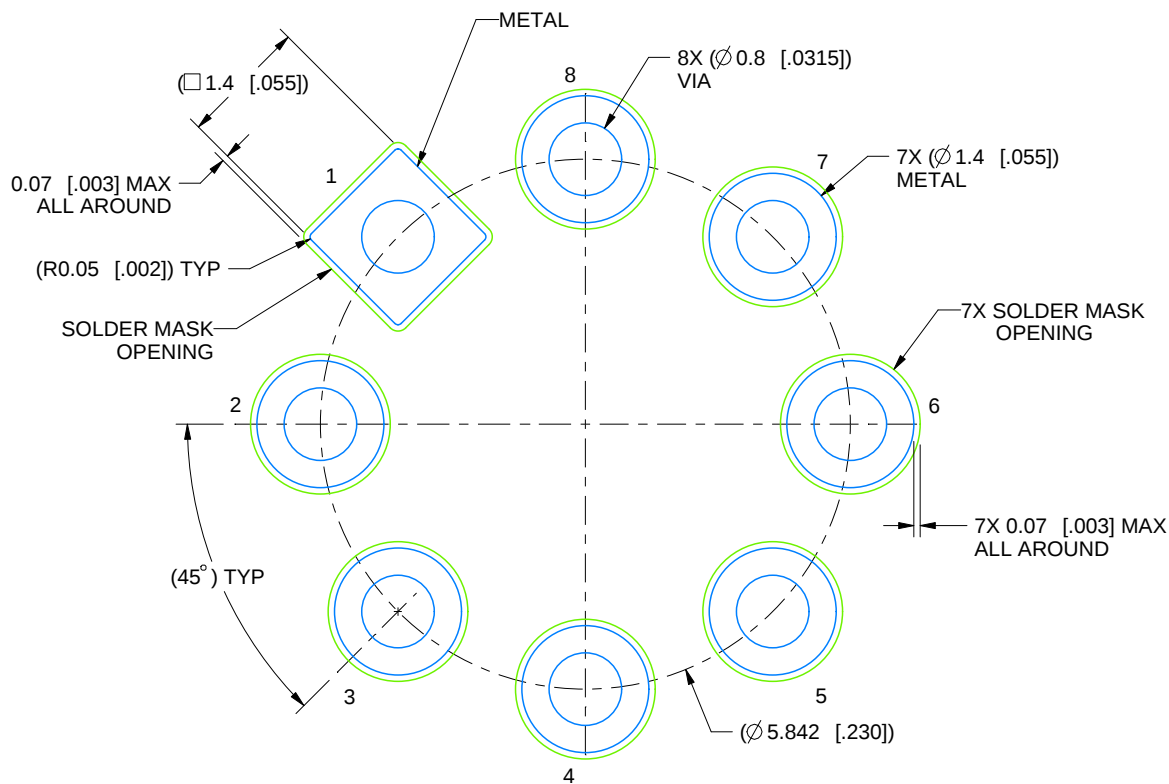
NOTES:

1. All linear dimensions are in millimeters [inches]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LMG0008A

TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

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REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2174627	07/10/2018	V. DASIKA / K. SINCERBOX
B	CHANGE TO DUAL DIMENSIONING MM [INCH] FORMAT	2175848	08/17/2018	V. DASIKA / K. SINCERBOX

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