LM5009A、100V、150mA、コンスタント・オンタイム、降圧スイッチング・レギュレータ

1 特長

- 動作入力電圧範囲(6V～95V)
- 100VのNチャネル降圧スイッチを内蔵
- スタートアップ用レギュレータを内蔵
- ループ補償が不要
- 超高速の過渡応答
- オン時間は入力電圧に反比例
- ライン電圧や負荷電流の変動に対して動作周波数を一定に維持
- 出力電圧を2.5V～の範囲で調整可能
- 高効率動作
- 高精度な内部リファレンス電圧
- 低いバイアス電流
- インテリジェントな電流制限機能
- サーマル・シャットダウン
- 8ピンVSSOP、8ピンWSON (4mm×4mm)パッケージ

2 アプリケーション

- 通信機器向けの非絶縁型降圧レギュレータ
- 二次高圧ポスト・レギュレータ
- 42V車載システム

3 概要

LM5009AはLM5009 COT降圧レギュレータの機能を変更したものです。LM5009Aでは次のように機能が変更されています。最小入力電圧は6Vになり、オン時間の式はわずかに異なり、最小負荷電流の要件はなくなりました。

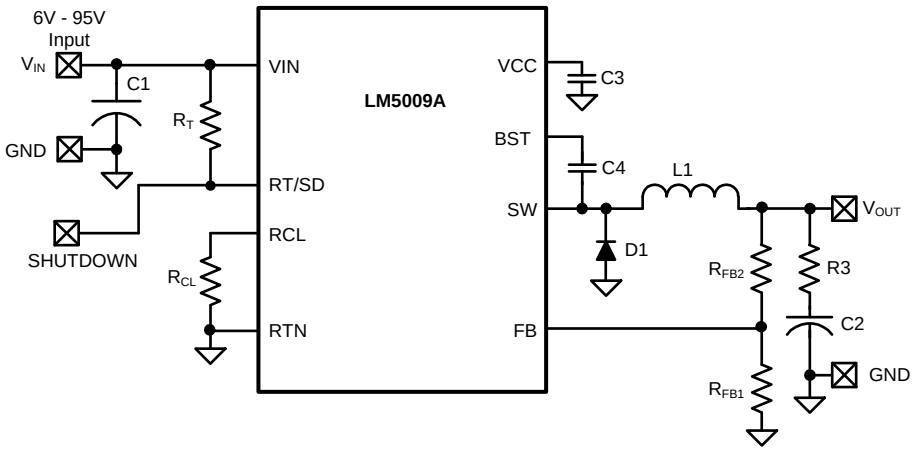
LM5009A降圧スイッチング・レギュレータには、低コストで高効率の降圧レギュレータを実装するため必要なすべての機能が搭載されています。この高電圧レギュレータは100VのNチャネル降圧スイッチを内蔵しています。8ピンVSSOPパッケージおよび放熱特性の優れた8ピンWSONパッケージで供給され、容易に実装できます。レギュレータは、V_{IN}に反比例するオン時間を用いた制御方式に基づきます。この機能により、動作周波数を比較的一定に保つことが可能になります。この制御方式では、ループ補償は不要です。強制オフ時間を持つインテリジェントな電流制限を実装し、オフ時間はV_{OUT}に反比例します。この方式では、最小フォールドバックを提供しつつ、短絡制御を確実に行います。その他に以下の機能があります。サーマル・シャットダウン、低電圧誤動作防止(V_{CC})、ゲート駆動低電圧誤動作防止、最大デューティ・サイクル制限機能、プリチャージ・スイッチ。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM5009A	VSSOP (8)	4.00mm×4.00mm
	WSON (8)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの基本的な降圧レギュレータ



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (February 2013) から **Revision H** に変更 **Page**

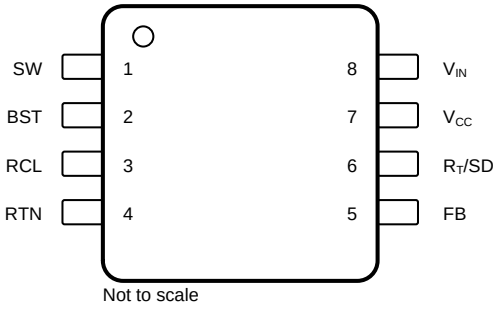
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Changed values in the *Thermal Information* table from 200 to 157.7 (DGK) and from 40 to 42.8 (NGU) ... 4

Revision F (February 2013) から **Revision G** に変更 **Page**

- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



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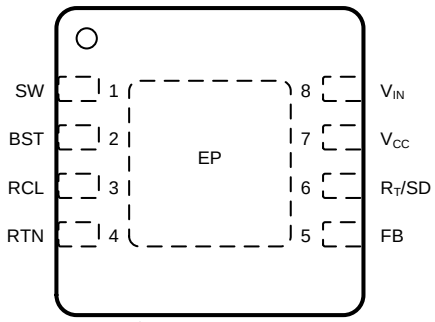
NGU Package
8-Pin WSON
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1	O	Switching node: power switching node. Connect to the output inductor, recirculating diode, and bootstrap capacitor.
BST	2	I	Boost pin (bootstrap capacitor input): an external capacitor is required between the BST and the SW pins. A 0.01-µF ceramic capacitor is recommended. An internal diode charges the capacitor from V_{CC} during each OFF time.
RCL	3	I	Current limit OFF-time set pin: a resistor between this pin and RTN sets the OFF time when current limit is detected. The OFF time is preset to 35 µs if FB = 0 V.
RTN	4	—	Ground pin: ground for the entire circuit.
FB	5	I	Feedback input from regulated output: this pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
R_T/SD	6	I	On time set pin: a resistor between this pin and V_{IN} sets the switch on time as a function of V_{IN}. The minimum recommended on time is 400 ns at the maximum input voltage. This pin is used for remote shutdown.
V_{CC}	7	O	Output from the internal high voltage series pass regulator: this regulated voltage provides gate drive power for the internal Buck switch. An internal diode is provided between this pin and the BST pin. A local 0.47-µF decoupling capacitor is required. The series pass regulator is current limited to 9 mA.
V_{IN}	8	I	Input voltage: input operating range of 6 V to 95 V.
EP	—	—	Exposed pad: the exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	100	V
BST to GND	–0.3	114	V
SW to GND (steady state)		–1	V
BST to V_{CC}		100	V
BST to SW		14	V
V_{CC} to GND		14	V
All other inputs to GND	–0.3	7	V
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	6	95	V
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5009A		UNIT
		DGK (VSSOP)	NGU (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.7	42.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	41.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.9	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.5	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25 ° C. Minimum and maximum limits apply over T_J = –40°C to 125°C for LM5009A. Unless otherwise stated, V_{IN} = 48 V(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} Reg	V_{CC} regulator output(2)	V_{IN} = 48 V	6.6	7	7.4	V
	V_{IN} – V_{CC}	6 V < V_{IN} < 8.5 V		100		mV
	V_{CC} bypass threshold	V_{IN} increasing		8.5		V
	V_{CC} bypass hysteresis			300		mV
	V_{CC} output impedance	V_{IN} = 6 V		100		Ω
		V_{IN} = 10 V		8.8		Ω
		V_{IN} = 48 V		0.8		Ω
	V_{CC} current limit	V_{IN} = 48 V		9.2		mA
	V_{CC} UVLO	V_{CC} increasing		5.3		V
	V_{CC} UVLO hysteresis			190		mV
	V_{CC} UVLO filter delay			3		µs
	Iin operating current	FB = 3 V, V_{IN} = 48 V		550	750	µA
	Iin shutdown current	R_T/SD = 0 V		110	176	µA
CURRENT LIMIT						
	Current limit threshold		0.24	0.3	0.36	A
	Current limit response time	I_{switch} overdrive = 0.1 A, time to switch off		350		ns
T_{OFF-1}	OFF-time generator	FB = 0 V, R_{CL} = 100 K		35		µs
T_{OFF-2}	OFF-time generator	FB = 2.3 V, R_{CL} = 100 K		2.56		µs
ON TIME GENERATOR						
T_{ON-1}	ON-time generator	V_{IN} = 10 V, R_{ON} = 200 K	2.15	2.77	3.5	µs
T_{ON-2}	ON-time generator	V_{IN} = 95 V, R_{ON} = 200 K	200	300	420	ns
RT/SD	Remote shutdown threshold	Rising	0.4	0.7	1.05	V
$RT/SD_{(HYS)}$	Remote shutdown hysteresis			35		mV
MINIMUM OFF TIME						
	Minimum off timer	FB = 0 V		300		ns
REGULATION AND OV COMPARATORS						
	FB reference threshold	Internal reference, trip point for switch ON	2.445	2.5	2.55	V
	FB overvoltage threshold	Trip point for switch OFF		2.875		V
	FB bias current			100		nA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			25		°C

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet R_{\theta JA})$ where $R_{\theta JA}$ (in ° C/W) is the package thermal impedance provided in the Thermal Information section.

(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.

6.6 Switching Characteristics

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = –40°C to 125°C for LM5009A. Unless otherwise stated, V_{IN} = 48 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buck switch $R_{DS(ON)}$ (1)	I_{test} = 200 mA		2.2	4.6	Ω
Gate drive UVLO	$V_{bst} – V_{sw}$ rising	2.8	3.8	4.8	V
Gate drive UVLO hysteresis			490		mV
Precharge switch voltage	At 1 mA		0.8		V
Precharge switch ON time			150		ns

(1) For devices procured in the 8-pin WSON package, the Rds(on) limits are specified by design characterization data only.

6.7 Typical Characteristics

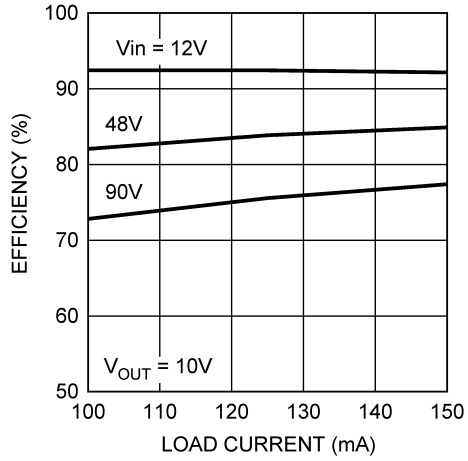


Figure 1. Efficiency vs Load Current and V_{IN} (Circuit of Figure 10)

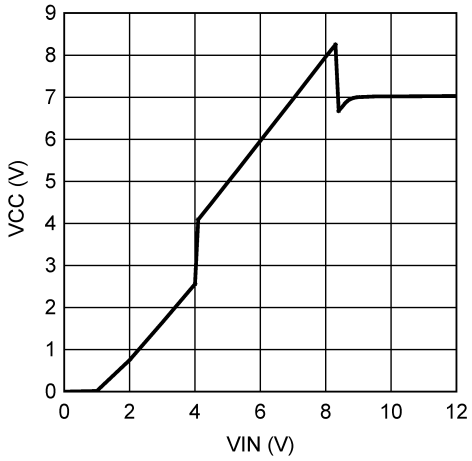


Figure 2. V_{CC} vs V_{IN}

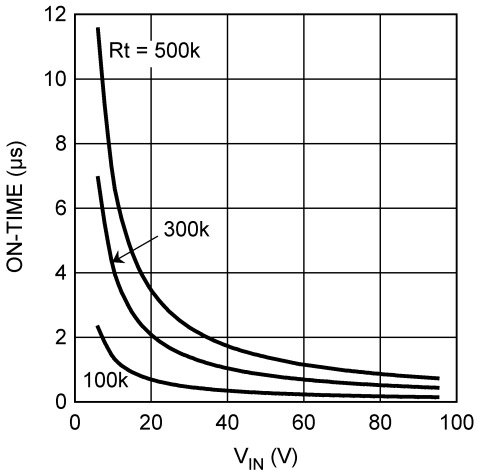


Figure 3. ON Time vs Input Voltage and R_T

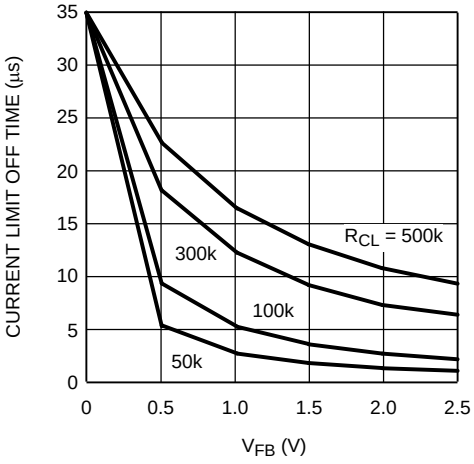


Figure 4. Current Limit OFF Time vs V_{FB} and R_{CL}

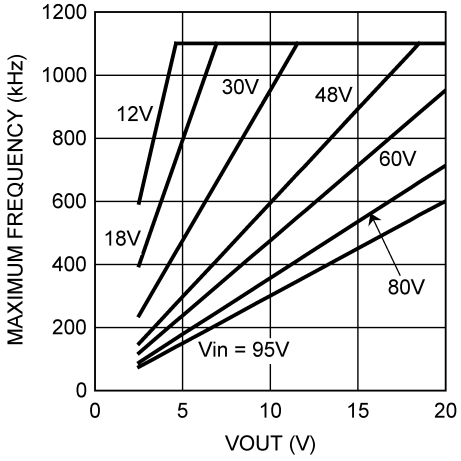


Figure 5. Maximum Frequency vs V_{OUT} and V_{IN}

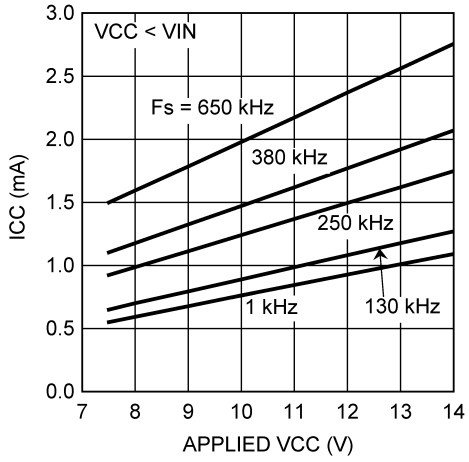


Figure 6. I_{CC} Current vs Applied V_{CC} Voltage

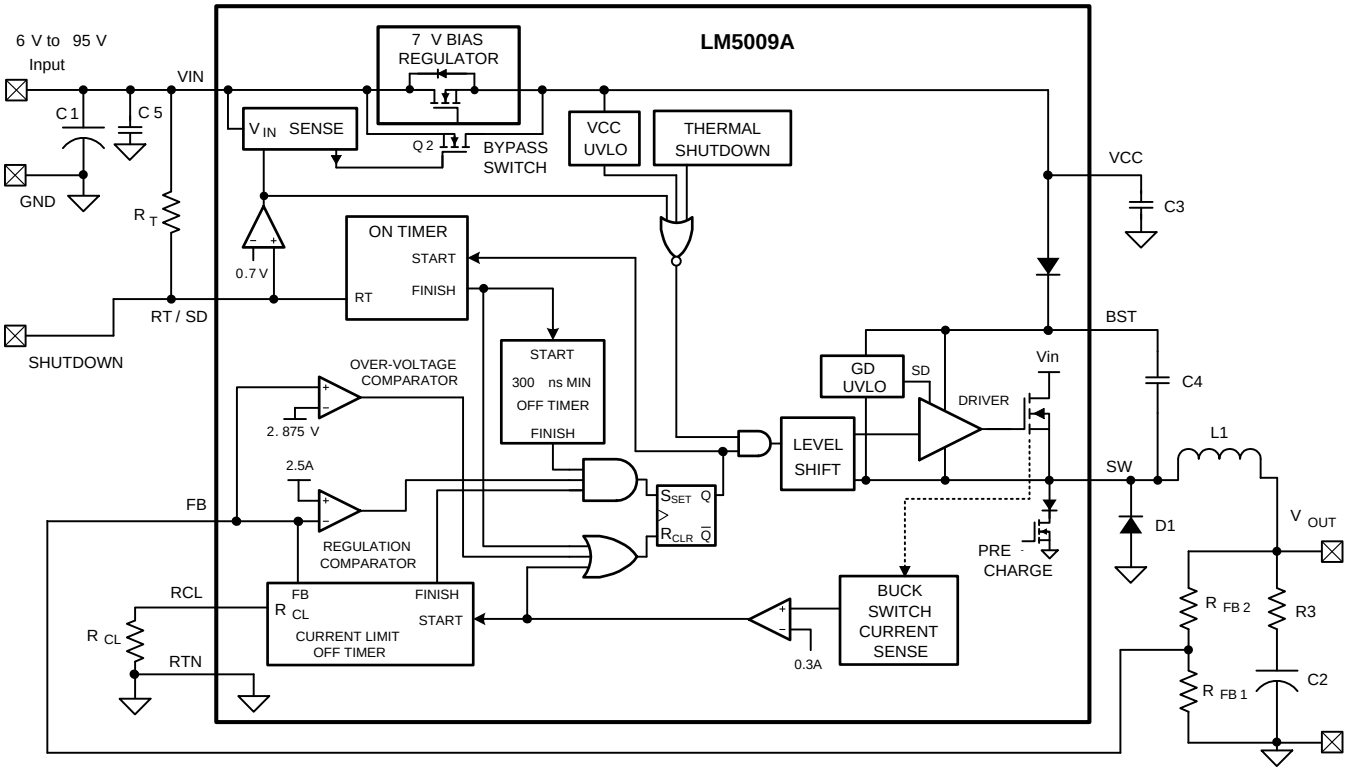
7 Detailed Description

7.1 Overview

The LM5009A device is a step-down switching regulator featuring all of the functions required to implement a low-cost, efficient, buck bias power converter. This high-voltage regulator contains a 100-V, N-channel buck switch, is easy to implement, and is provided in the 8-pin VSSOP and the thermally-enhanced, 8-pin WSON packages. The regulator is based on a control scheme using an ON time inversely proportional to V_{IN}. The control scheme requires no loop compensation. Current limit is implemented with forced OFF time, which is inversely proportional to V_{OUT}. This scheme ensures short circuit control while providing minimum foldback.

The LM5009A is applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48-V Telecom and the new 42-V Automotive power bus ranges.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Circuit Overview

The LM5009A is a buck DC-DC regulator that uses a control scheme in which the ON time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the ON-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_T). Following the ON period the switch remains off for at least the minimum off-timer period of 300 ns. If FB is still below the reference at that time, the switch turns on again for another ON-time period. This continues until regulation is achieved.

Feature Description (continued)

The LM5009A operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the ON time, then ramps back to zero before the end of the OFF time. The next ON-time period starts when the voltage at FB falls below the internal reference; until then, the inductor current remains zero. In this mode, the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore, at light loads the conversion efficiency is maintained, because the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency is calculated with Equation 1.

$$F = \frac{V_{OUT}^2 \times L \times 1.04 \times 10^{20}}{R_L \times (R_T)^2} \quad (1)$$

where

- R_L = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency is calculated with Equation 2.

$$F = \frac{V_{OUT}}{1.385 \times 10^{-10} \times R_T} \quad (2)$$

The output voltage (V_{OUT}) is programmed by two external resistors as shown in *Functional Block Diagram*. The regulation point is calculated with Equation 3.

$$V_{OUT} = 2.5 \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (3)$$

The LM5009A regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25 mV to 50 mV of ripple voltage at the feedback pin (FB) is required for the LM5009A. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in *Functional Block Diagram*).

For applications where lower output voltage ripple is required, the output is taken directly from a low-ESR output capacitor, as shown in Figure 7. However, R3 slightly degrades the load regulation.

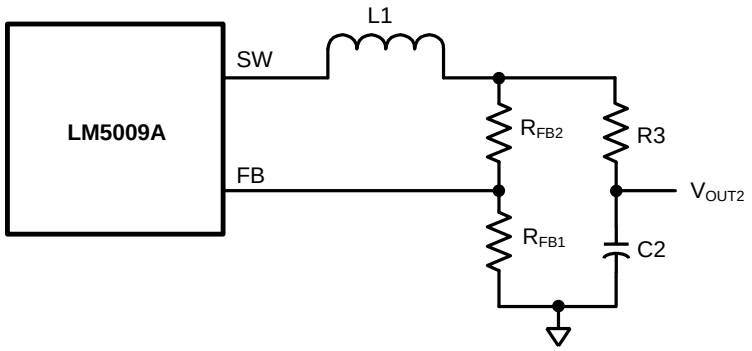


Figure 7. Low Ripple Output Configuration

Feature Description (continued)

7.3.2 Start-Up Regulator (V_{CC})

The high-voltage bias regulator is integrated within the LM5009A. The input pin (V_{IN}) is connected directly to line voltages between 6 V and 95 V, with transient capability to 100 V. Referring to *Functional Block Diagram* and Figure 2, when V_{IN} is between 6 V and the bypass threshold (nominally 8.5 V), the bypass switch (Q2) is on, and V_{CC} tracks V_{IN} within 100 mV to 150 mV. The bypass switch on-resistance is approximately 100 Ω, with inherent current limiting at approximately 100 mA. When V_{IN} is above the bypass threshold Q2 is turned off, and V_{CC} is regulated at 7 V. The V_{CC} regulator output current is limited at approximately 9.2 mA. When the LM5009A is shutdown using the R_T/SD pin, the V_{CC} bypass switch is shut off regardless of the voltage at V_{IN}.

When V_{IN} exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 µs to 3 µs. The capacitor at V_{CC} (C3) must be a minimum of 0.47 µF to prevent the voltage at V_{CC} from rising above the absolute maximum rating in response to a step input applied at V_{IN}. C3 must be placed as close as possible to the V_{CC} and RTN pins. In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5 V and 14 V is diode connected to the V_{CC} pin to shut off the V_{CC} regulator, thereby reducing internal power dissipation. The current required into the V_{CC} pin is shown in Figure 6. Internally a diode connects V_{CC} to V_{IN} requiring that the auxiliary voltage be less than V_{IN}.

The turnon sequence is shown in Figure 8. During the initial delay (t1) V_{CC} ramps up at a rate determined by the current limit and C3 while internal circuitry stabilizes. When V_{CC} reaches UVLO (typically 5.3 V) the buck switch is enabled. The inductor current increases to the current limit threshold (I_{LIM}) and during t2 V_{OUT} increases as the output capacitor charges up. When V_{OUT} reaches the intended voltage, the average inductor current decreases (t3) to the nominal load current (I_O).

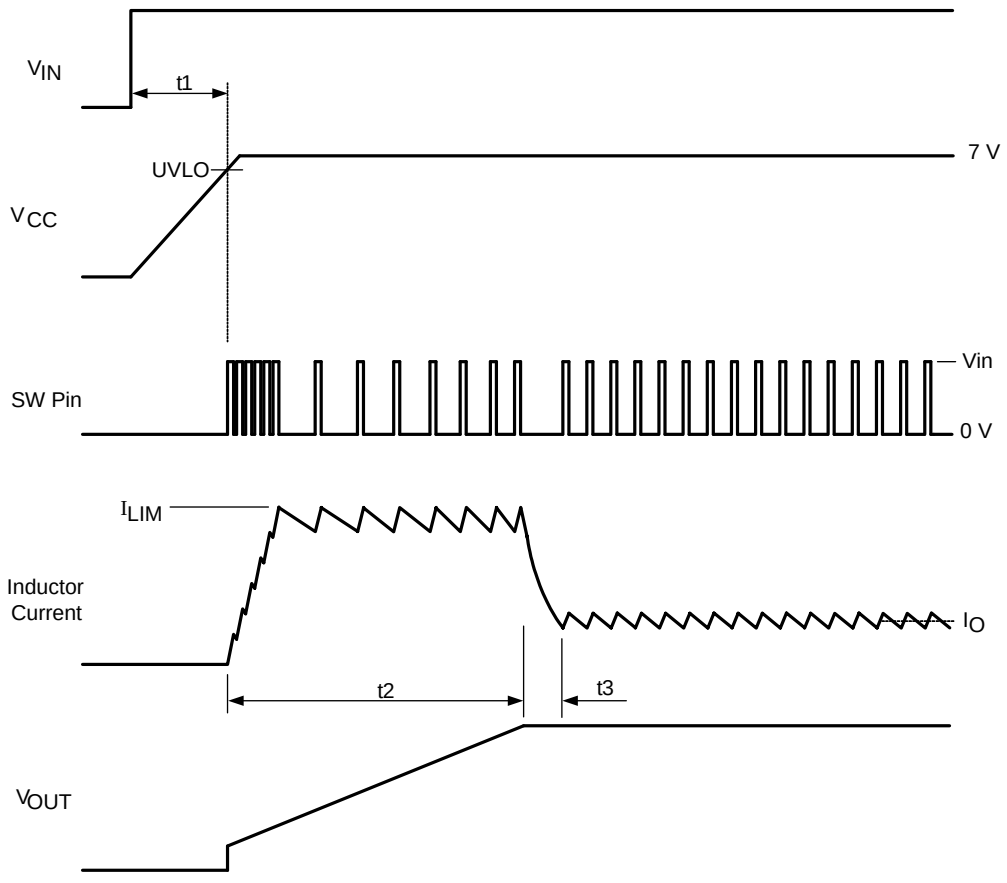


Figure 8. Start-Up Sequence

Feature Description (continued)

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5-V reference. In normal operation (the output voltage is regulated), an ON-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch stays on for the ON time, causing the FB voltage to rise above 2.5 V. After the ON-time period, the buck switch stays off until the FB voltage again falls below 2.5 V. During start-up, the FB voltage is below 2.5 V at the end of each ON time, resulting in the minimum OFF-time of 300 ns. Bias current at the FB pin is nominally 100 nA.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.875-V reference. If the voltage at FB rises above 2.875 V, the ON-time pulse is immediately terminated. This condition can occur if the input voltage or the output load change suddenly. The buck switch does not turn on again until the voltage at FB falls below 2.5 V.

7.3.5 ON-Time Generator and Shutdown

The ON time for the LM5009A is determined by the R_T resistor, and is inversely proportional to the input voltage (V_{IN}). This results in a nearly constant frequency as V_{IN} is varied over the V_{IN} range. The ON-time equation for the LM5009A is calculated with Equation 4.

$$T_{ON} = 1.385 \times 10^{-10} \times R_T / V_{IN} \quad (4)$$

R_T must be selected for a minimum ON time (at maximum V_{IN}) greater than 400 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}.

7.3.6 Current Limit

The LM5009A contains an intelligent current limit OFF timer. If the current in the Buck switch exceeds 0.3 A, the present cycle is immediately terminated, and a non-resetable OFF timer is initiated. The length of OFF time is controlled by an external resistor (R_{CL}) and the FB voltage (see Figure 4). When FB = 0 V, a maximum OFF time is required, and the time is preset to 35 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of
95 V. In cases of overload where the FB voltage is above 0 V (not a short circuit), the current limit OFF time is less than 35 µs. Reducing the OFF time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The OFF time is calculated with Equation 5.

$$T_{OFF} = \frac{10^{-5}}{0.285 + \frac{V_{FB}}{(6.35 \times 10^{-6} \times R_{CL})}} \quad (5)$$

The current limit sensing circuit is blanked for the first 50 ns to 70 ns of each ON time, so it is not falsely tripped by the current surge which occurs at turnon. The current surge is required by the recirculating diode (D1) for the turnoff recovery.

7.3.7 N-Channel Buck Switch and Driver

The LM5009A integrates an N-channel Buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the ON time.

During each OFF time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum OFF timer, set to 300 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

Feature Description (continued)

The internal precharge switch at the SW pin is turned on for approximately 150 ns during the minimum OFF-time period, ensuring sufficient voltage exists across the bootstrap capacitor for the ON time. This feature helps prevent operating problems which can occur during very light-load conditions, involving a long OFF time, during which the voltage across the bootstrap capacitor could otherwise reduce below the gate drive UVLO threshold. The precharge switch also helps prevent start-up problems which can occur if the output voltage is precharged prior to turnon. After current limit detection, the precharge switch is turned on for the entire duration of the forced OFF time.

7.3.8 Thermal Protection

The LM5009A must be operated so the junction temperature does not exceed 125°C during normal operation. An internal thermal shutdown circuit is provided to shutdown the LM5009A in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state by disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C, normal operation is resumed (typical hysteresis = 25°C).

7.4 Device Functional Modes

The LM5009A is remotely disabled by taking the R_T/SD pin to ground, as shown in Figure 9. The voltage at the R_T/SD pin is between 1.5 V and 3 V, depending on V_{IN} and the value of the R_T resistor.

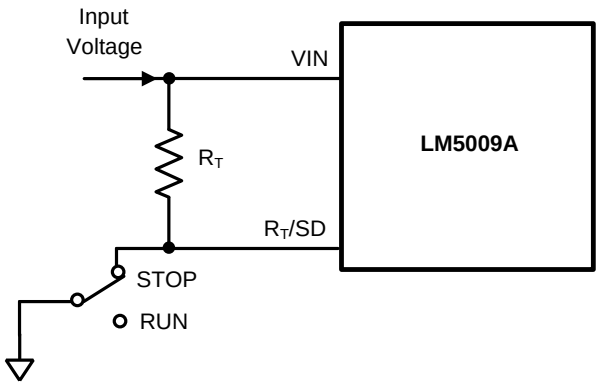


Figure 9. Shutdown Implementation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5009A is a nonsynchronous buck regulator designed to operate over a wide input voltage range and output current. Spreadsheet-based quick-start calculation tools and the on-line WEBENCH® software can be used to create a buck design along with the bill of materials, estimated efficiency, and the complete solution cost.

8.2 Typical Application

The final circuit is shown in Figure 10. The circuit was tested, and the resulting performance is shown in Figure 11 and Figure 12.

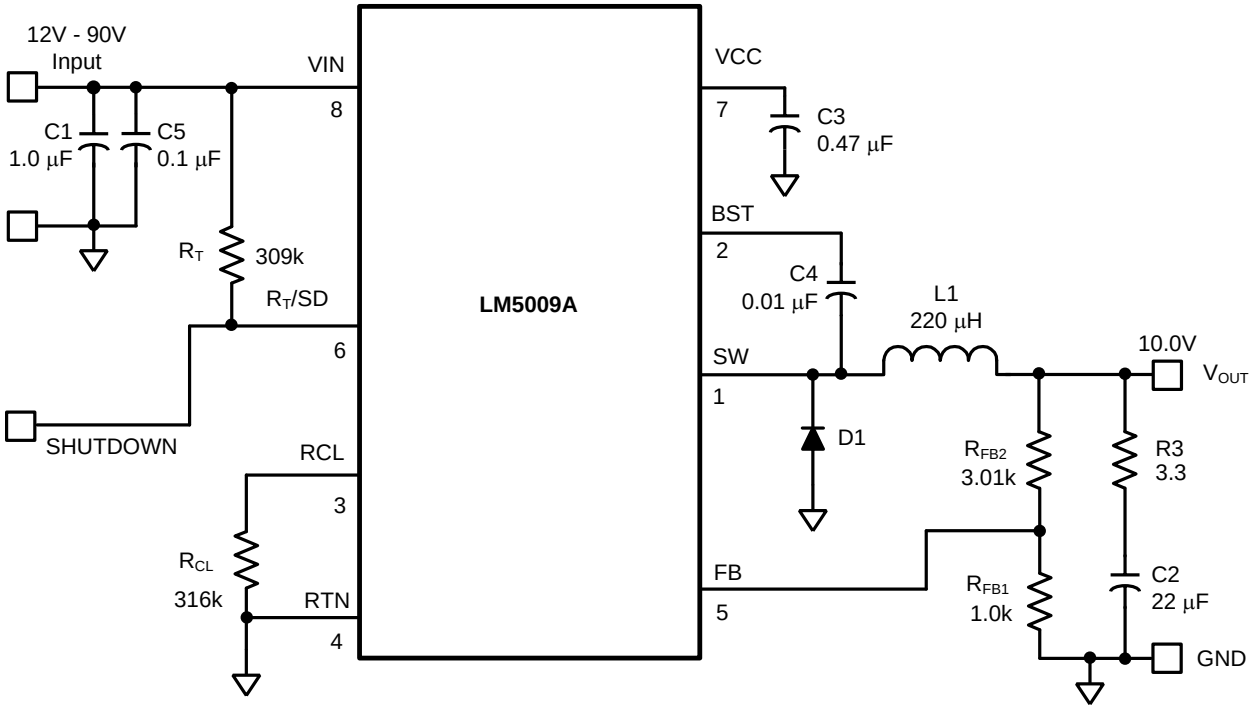


Figure 10. LM5009A Example Circuit

8.2.1 Design Requirements

A guide for determining the component values is illustrated with a design example. See *Functional Block Diagram* and the Bill of Materials listed in Table 2.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	12 V to 90 V
Output voltage	10 V
Load current range	100 mA to 150 mA

8.2.2 Detailed Design Procedure

Table 2. Bill of Materials

ITEM	DESCRIPTION	PART NUMBER	VALUE
C1	Ceramic capacitor	TDK C4532X7R2A105M	1 µF, 100 V
C2	Ceramic capacitor	TDK C4532X7R1E226M	22 µF, 25 V
C3	Ceramic capacitor	Kemet C1206C474K5RAC	0.47 µF, 50 V
C4	Ceramic capacitor	Kemet C1206C103K5RAC	0.01 µF, 50 V
C5	Ceramic capacitor	TDK C3216X7R2A104M	0.1 µF, 100 V
D1	Schottky power diode	Diodes Inc. DFLS1100	100 V, 1 A
L1	Power inductor	COILTRONICS DR125-221-R or TDK SLF10145T-221MR65	220 µH
R_{FB2}	Resistor	Vishay CRCW12063011F	3.01 kΩ
R_{FB1}	Resistor	Vishay CRCW12061001F	1 kΩ
R3	Resistor	Vishay CRCW12063R30F	3.3 Ω
R_T	Resistor	Vishay CRCW12063093F	309 kΩ
R_{CL}	Resistor	Vishay CRCW12063163F	316 kΩ
U1	Switching regulator	Texas Instruments LM5009A	—

8.2.2.1 R_{FB1} and R_{FB2}

$$V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (6)$$

Because V_{FB} = 2.5 V, the ratio of R_{FB2} to R_{FB1} calculates as 3:1. Standard values of 3.01 kΩ and 1 kΩ are chosen. Other values could be used as long as the 3:1 ratio is maintained.

8.2.2.2 F_s and R_T

The recommended operating frequency range for the LM5009A is 50 kHz to 1.1 MHz. Unless the application requires a specific frequency, the choice of frequency is generally a compromise, because it affects the size of L1 and C2, and the switching losses. The maximum allowed frequency, based on a minimum ON time of 400 ns, is calculated with Equation 7.

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 400\ ns) \quad (7)$$

For this exercise, F_{MAX} = 277 kHz. From Equation 2, R_T calculates to 260 kΩ. A standard value, 309-kΩ resistor is used to allow for tolerances in Equation 2, resulting in a frequency of 234 kHz.

8.2.2.3 L1

The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum V_{IN}.

8.2.2.3.1 Minimum Load Current

To maintain continuous conduction at minimum I_O (100 mA), the ripple amplitude (I_{OR}) must be less than 200 mA peak-to-peak so the lower peak of the waveform does not reach zero. L1 is calculated using Equation 8.

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_s \times V_{IN}} \quad (8)$$

At V_{IN} = 90 V, L1(min) calculates to 190 µH. The next larger standard value (220 µH) is chosen and with this value I_{OR} calculates to 173 mA peak-to-peak at V_{IN} = 90 V, and 32 mA peak-to-peak at V_{IN} = 12 V.

8.2.2.3.2 Maximum Load Current

At a load current of 150 mA, the peak of the ripple waveform must not reach the minimum value of the LM5009A's current limit threshold (240 mA). Therefore, the ripple amplitude must be less than 180 mA peak-to-peak, which is already satisfied in the above calculation. With L1 = 220 µH, at maximum V_{IN} and I_O, the peak of the ripple is 236 mA. While L1 must carry this peak current without saturating or exceeding the temperature rating, it also must be capable of carrying the maximum value of the LM5009A's current limit threshold (360 mA) without saturating, because the current limit is reached during startup.

The DC resistance of the inductor must be as low as possible to minimize the power loss.

8.2.2.4 C3

The capacitor on the V_{CC} output provides not only noise filtering and stability, but the primary purpose is to prevent false triggering of the V_{CC} UVLO at the buck switch on and off transitions. C3 must be no smaller than 0.47 µF.

8.2.2.5 C2 and R3

When selecting the output filter capacitor C2, the items to consider are ripple voltage due to the ESR, ripple voltage due to the capacitance, and the nature of the load.

8.2.2.6 ESR and R3

A low ESR for C2 is generally desirable so as to minimize power losses and heating within the capacitor. However, the regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5009A, the minimum ripple required at pin 5 is 25 mV peak-to-peak, requiring a minimum ripple at V_{OUT} of 100 mV. Because the minimum ripple current (at minimum V_{IN}) is 32 mA peak-to-peak, the minimum ESR required at V_{OUT} is 100 mV / 32 mA = 3.12 Ω. Because quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in *Functional Block Diagram*. R3's value, along with C2's ESR, must result in at least 25 mV peak-to-peak ripple at pin 5. Generally, R3 is 0.5 Ω to 4 Ω.

8.2.2.7 C2

C2 must generally be no smaller than 3.3 µF. Typically, the value is 10 µF to 20 µF with the optimum value determined by the load. If the load current is fairly constant, a small value suffices for C2. If the load current includes significant transients, a larger value is necessary. For each application, experimentation is required to determine the optimum values for R3 and C2.

8.2.2.8 R_{CL}

When current limit is detected, the minimum OFF-time set by this resistor must be greater than the maximum normal OFF time, which occurs at maximum input voltage. Using Equation 4, the minimum ON time is 476 ns, yielding an OFF time of 3.8 µs (at 234 kHz). Due to the 25% tolerance on the ON time, the OFF-time tolerance is also 25%, yielding a maximum OFF time of 4.75 µs. Allowing for the response time of the current limit detection circuit (350 ns) increases the maximum OFF time to 5.1 µs. This is increased an additional 25% to 6.4 µs to allow for the tolerances of Equation 5. Using Equation 5, R_{CL} calculates to 310 kΩ at V_{FB} = 2.5 V. A standard value 316-kΩ resistor is used.

8.2.2.9 D1

The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is only this diode's voltage which forces the inductor current to reduce during the forced OFF time. For this reason, a higher voltage is better, although that affects efficiency. A good choice is a Schottky power diode, such as the DFLS1100. The reverse voltage rating of D1 must be at least as great as the maximum V_{IN}, and the current rating must be greater than the maximum current limit threshold (360 mA).

8.2.2.10 C1

C1 supplies most of the switch current during the ON time, and limit the voltage ripple at V_{IN}, on the assumption that the voltage source feeding V_{IN} has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into pin 8 suddenly increases to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turnoff. The average input current during this ON time is the load current (150 mA). For a worst-case calculation, C1 must supply this average load current during the maximum ON time. To keep the input voltage ripple to less than 2 V (for this exercise), C1 is calculated with Equation 9.

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.15A \times 3.57\ \mu s}{2.0V} = 0.268\ \mu F \tag{9}$$

Quality ceramic capacitors in this value have a low ESR, which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1-µF, 100-V X7R capacitor is used.

8.2.2.11 C4

The recommended value for C4 is 0.01 µF, as this is appropriate in the majority of applications. A high-quality ceramic capacitor, with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turnon. A low ESR also ensures a quick recharge during each OFF time. At minimum V_{IN}, when the ON time is at maximum, it is possible during start-up that C4 does not fully re-charge during each 300 ns OFF time. The circuit is not able to complete the start-up, and achieve output regulation. This can occur when the frequency is intended to be low (for example, R_T = 500 K). In this case, C4 must be increased so it can maintain sufficient voltage across the buck switch driver during each ON time.

8.2.2.12 C5

This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at V_{IN}. TI recommends placing a low-ESR, 0.1-µF ceramic chip capacitor close to the LM5009A.

8.2.2.13 Ripple Configuration

The LM5009A uses a constant-ON-time (COT) control scheme where the ON time is terminated by a one-shot and the OFF time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the OFF time. Furthermore, this change in feedback voltage (V_{FB}) during OFF time must be large enough to dominate any noise present at the feedback node.

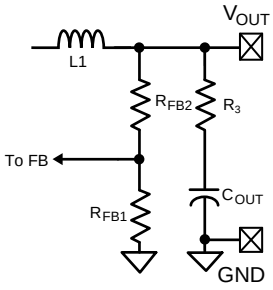
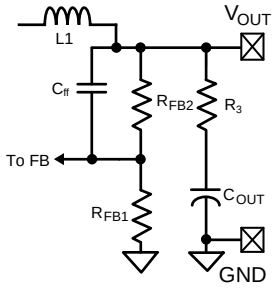
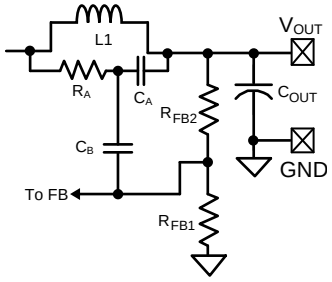
Table 3 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R3.

The capacitive ripple is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the OFF time. The resistive ripple is in phase with the inductor current and decreases monotonically during the OFF time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied, then unstable switching behavior is observed in COT converters with multiple ON-time bursts in close succession followed by a long OFF time.

The type 3 ripple method uses a ripple injection circuit with R_A, C_A, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then ac-coupled into the feedback node (FB) using the capacitor C_B. This circuit is suited for applications where low output voltage ripple is imperative because this circuit does not use the output voltage ripple.

Table 3. Ripple Configuration

TYPE 1	TYPE 2	TYPE 3
Lowest cost	Reduced ripple	Minimum ripple
		
$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$ (10)	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \text{ IIR}_{FB1})}$ $R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$ (11)	$R_A C_A \leq \frac{(V_{IN,min} - V_O) \times T_{ON(@\ V_{IN,min})}}{25mV}$ (12)

See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details on each ripple generation method.

8.2.3 Application Curves

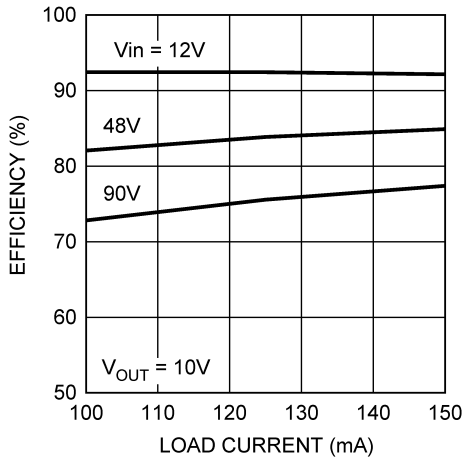


Figure 11. Efficiency vs Load Current and V_{IN}

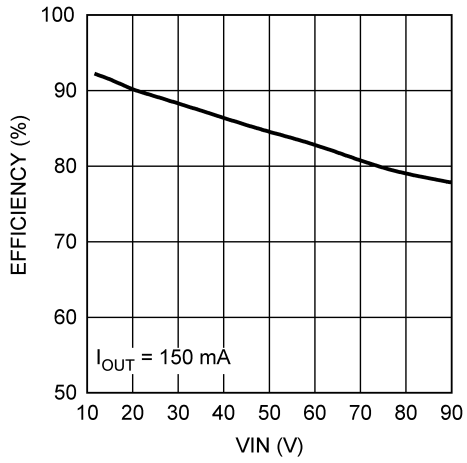


Figure 12. Efficiency vs V_{IN}

9 Power Supply Recommendations

The LM5009A is designed to operate with an input power supply capable of supplying a voltage range from 6 V to 95 V. The input power supply must be well regulated and capable of supplying sufficient current to the regulator during peak load operation. Also, like in all applications, the power-supply source impedance must be small compared to the module input impedance to maintain the stability of the converter.

10 Layout

10.1 Layout Guidelines

The LM5009A regulation and overvoltage comparators are very fast, and as such respond to short duration noise pulses. Therefore, layout considerations are critical for optimum performance. The components at pins 1, 2, 3, 5, and 6 must be as physically close as possible to the IC, thereby minimizing noise pickup in the PC tracks. The current loop formed by D1, L1, and C2 must be as small as possible. The ground connection from D1 to C1 must be as short and direct as possible.

If the internal dissipation of the LM5009A produces excessive junction temperatures during normal operation, good use of the PCB ground plane can help to dissipate heat. The exposed pad on the bottom of the 8-pin WSON package is soldered to a ground plane on the PCB, and that plane must extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PCB traces, where possible, can also help conduct heat away from the IC. Judicious positioning of the PCB within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

10.2 Layout Example

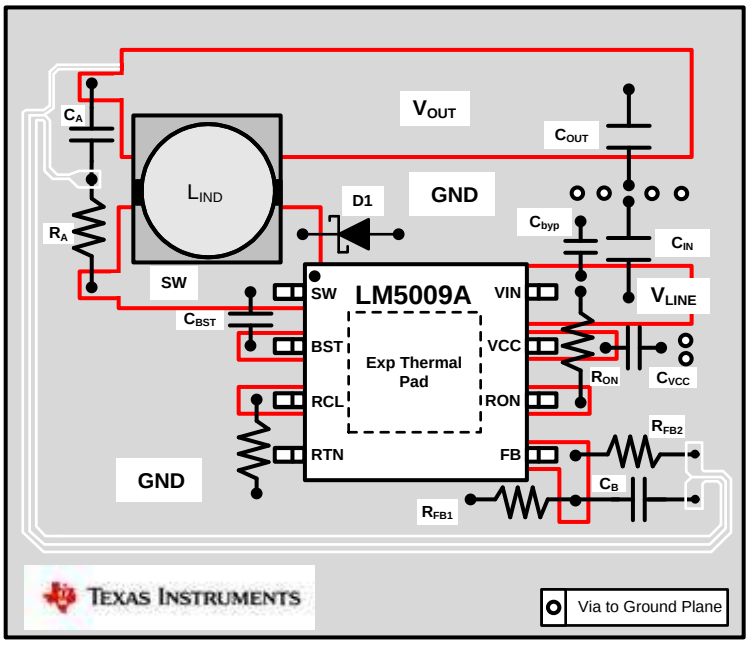


Figure 13. LM5009A Buck Layout Example With the WSON Package

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

AN-1481コンスタント・オンタイム(COT)方式のレギュレータにおける出力リップルの制御とESRインピーダンスの確保 (SNVA166)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5009AMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009AMM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009AMM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009AMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009AMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009AMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SLLA
LM5009ASD/NOPB	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD
LM5009ASD/NOPB.A	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD
LM5009ASD/NOPB.B	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD
LM5009ASDX/NOPB	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD
LM5009ASDX/NOPB.A	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD
LM5009ASDX/NOPB.B	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5009ASD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

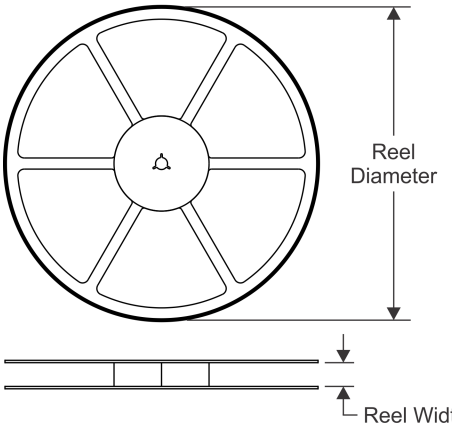
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

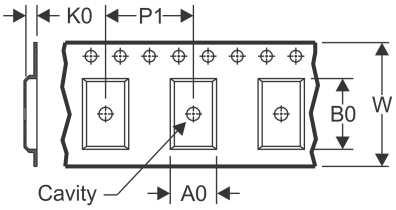
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

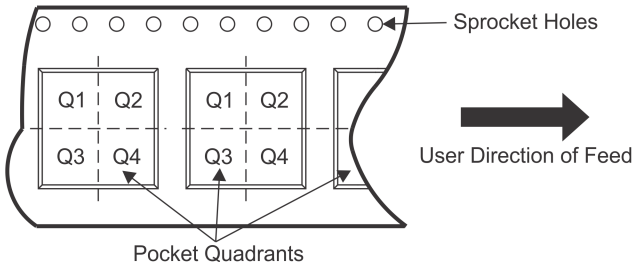


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

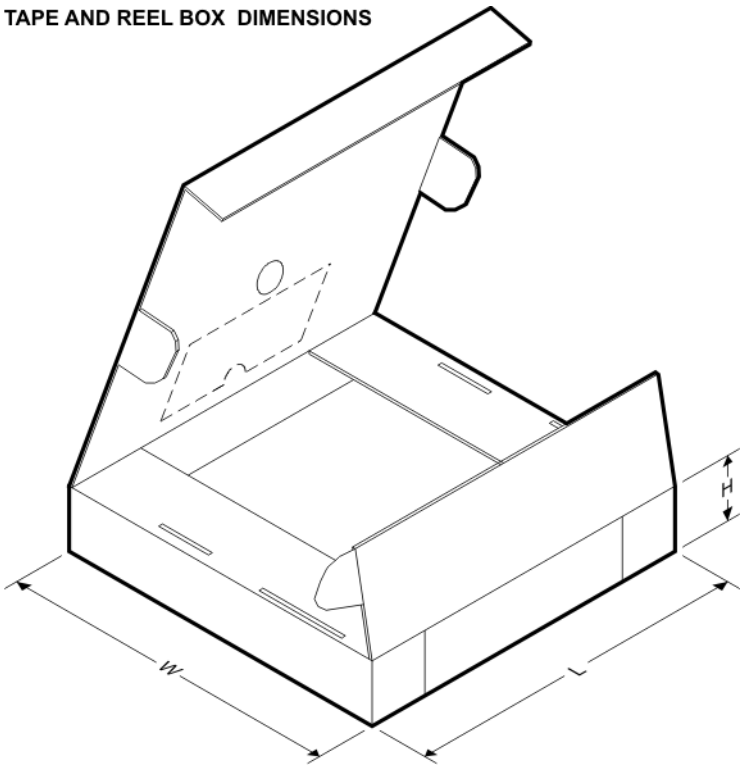
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5009AMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009AMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009ASD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5009ASDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

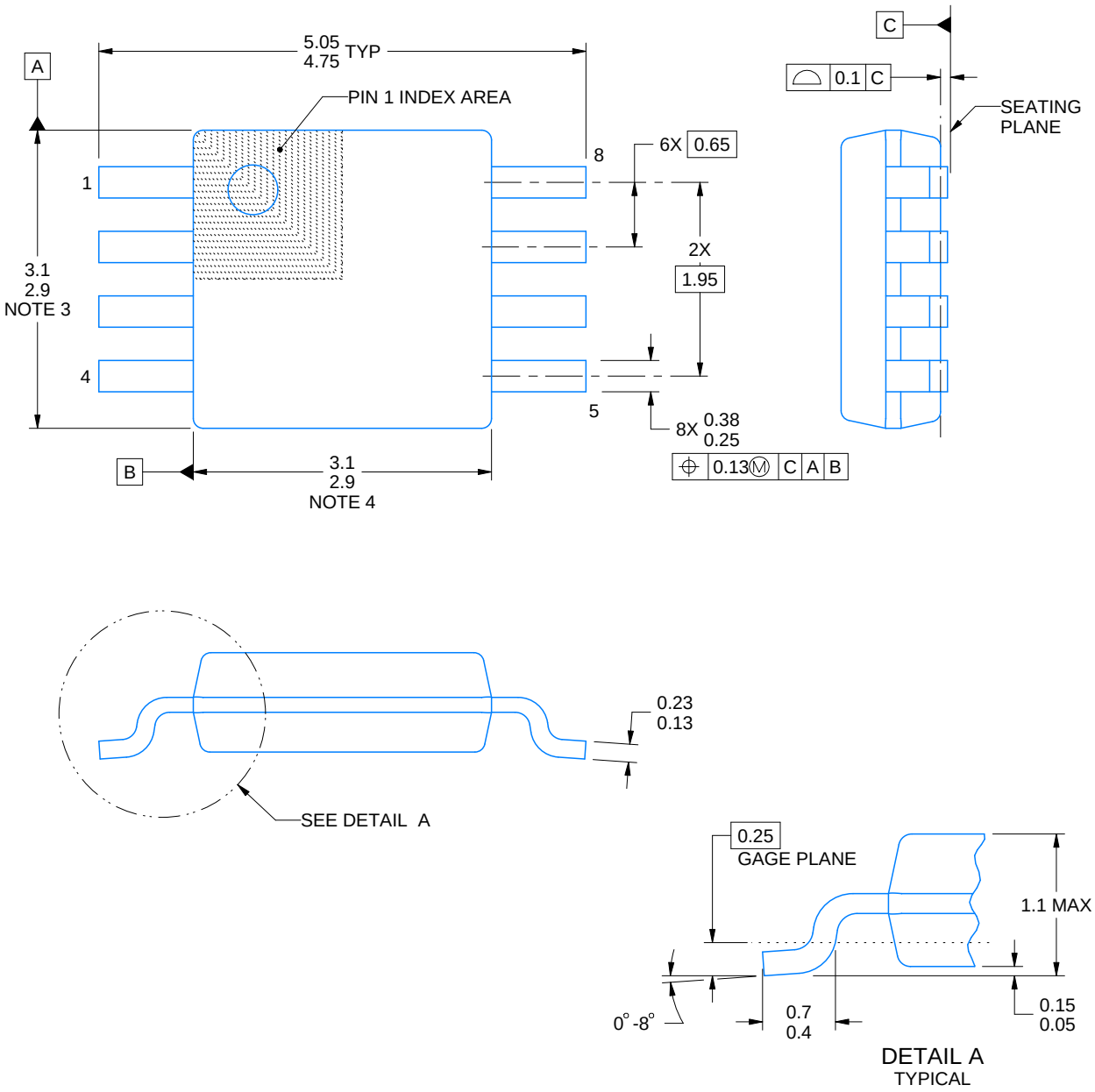
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5009AMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5009AMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5009ASD/NOPB	WSON	NGU	8	1000	208.0	191.0	35.0
LM5009ASDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

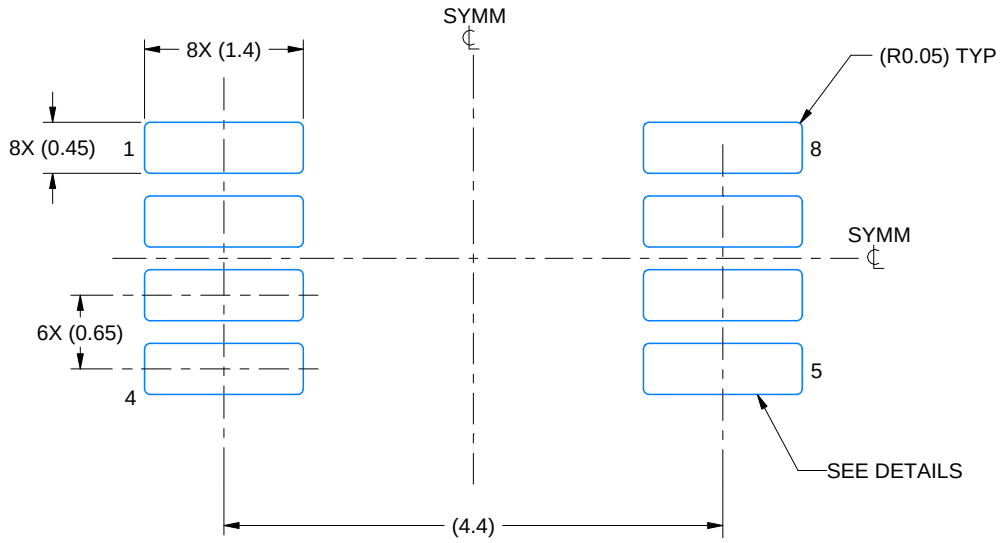
SMALL OUTLINE PACKAGE



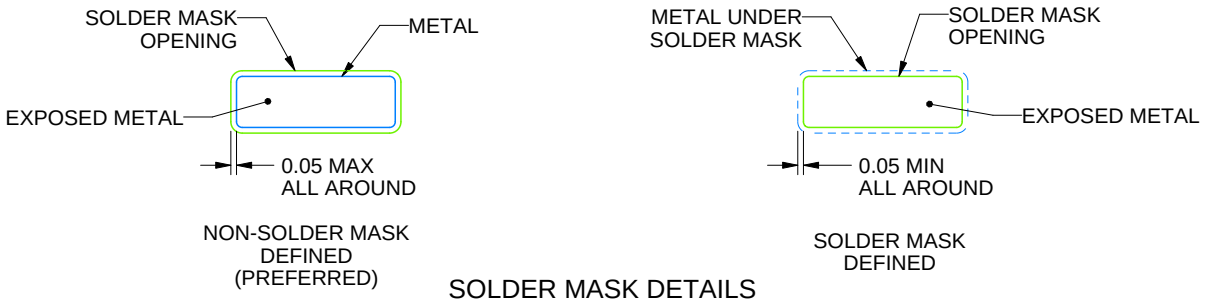
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

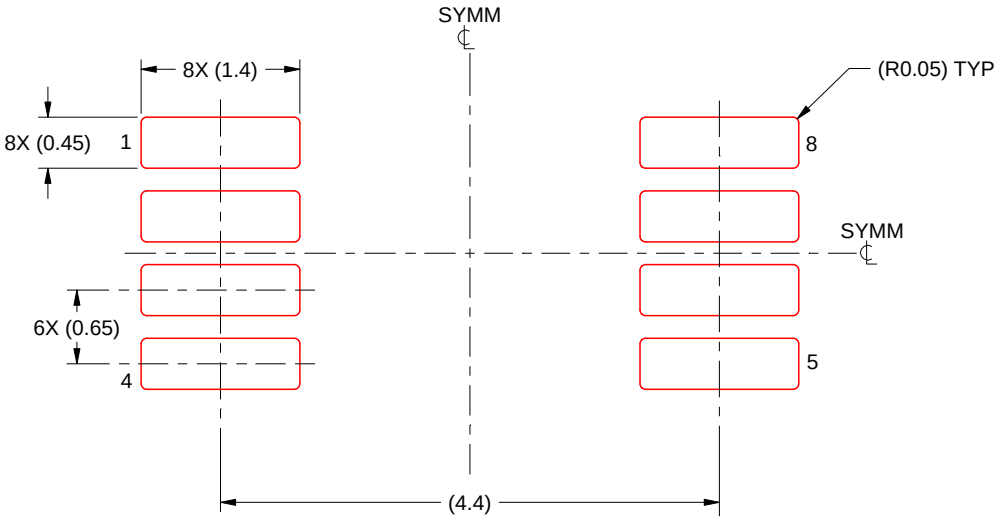


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



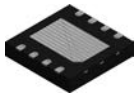
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

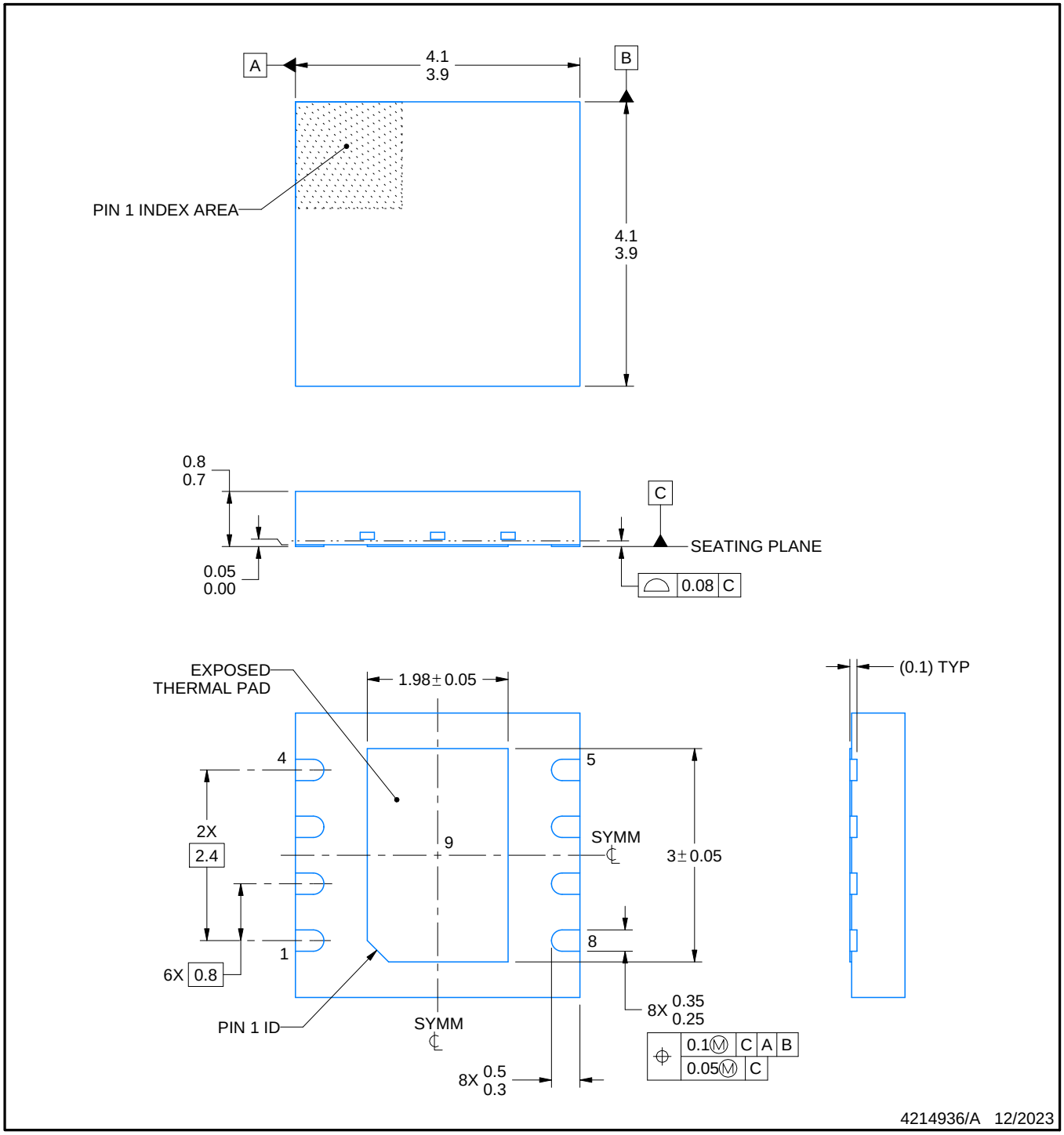
NGU0008B



PACKAGE OUTLINE

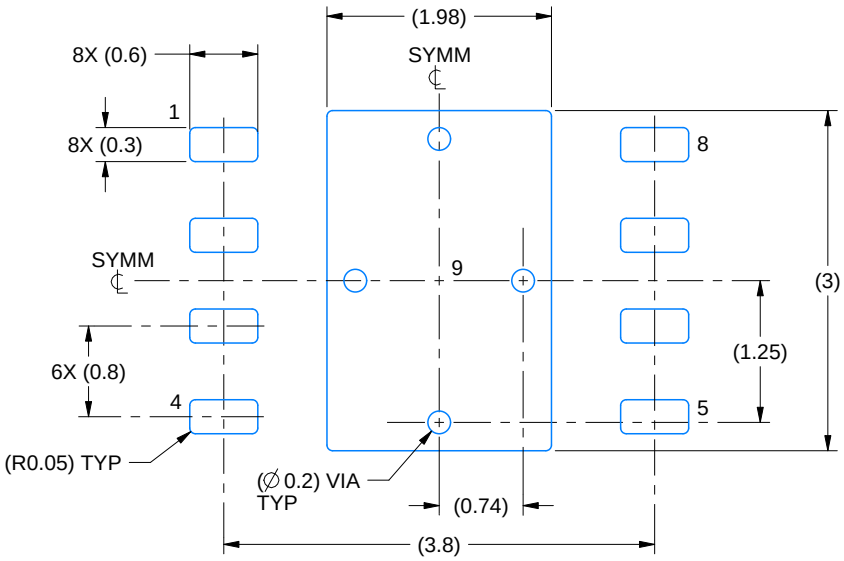
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

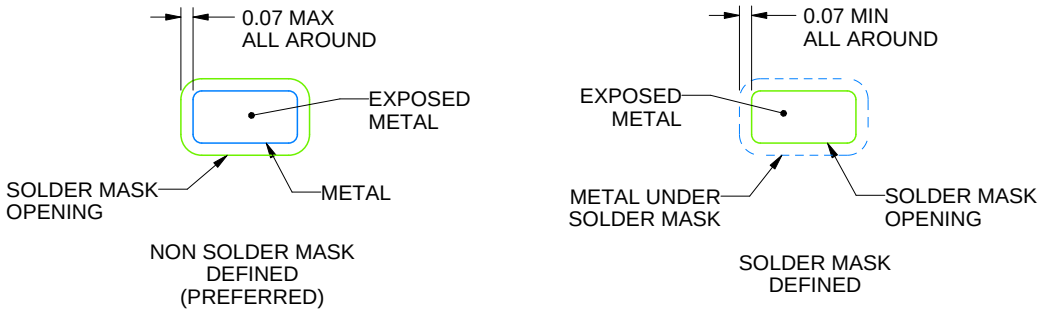


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

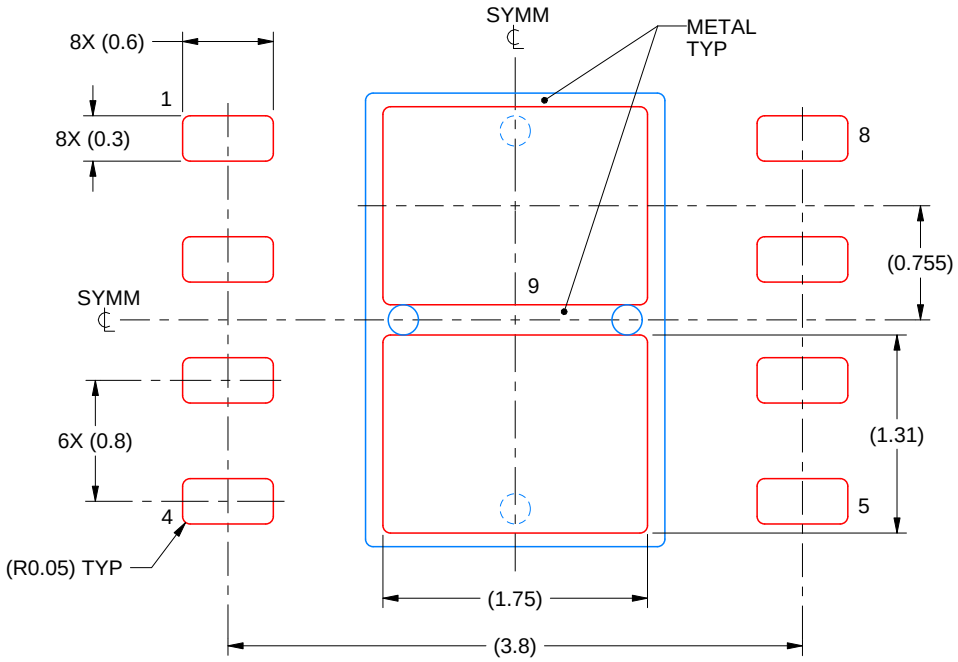


SOLDER MASK DETAILS

4214936/A 12/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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