

LMP8278Q High Common Mode, 14 x Gain, Precision Current Sensing Amplifier

Check for Samples: [LMP8278](#)

FEATURES

- $TCV_{os} \pm 15 \mu V/^{\circ}C$ Max
- CMRR 80 dB Min
- Input Offset Voltage ± 2 mV max
- CMVR -2V to 40V
- Operating Ambient Temperature Range $-40^{\circ}C$ to $125^{\circ}C$
- Single Supply Operation
- Min / Max Limits 100% Tested unless Otherwise Noted
- LMP8278Q Available in Automotive AEC-Q100 Grade 1 Qualified Version

APPLICATIONS

- High Side and Low Side Driver Configuration Current Sensing
- Automotive Fuel Injection Control
- Transmission Control
- Power Steering
- Battery Management Systems

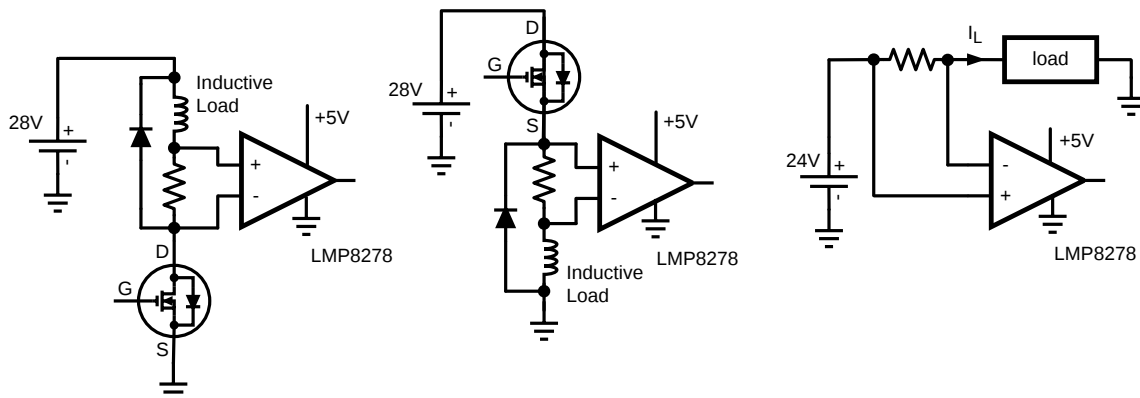
DESCRIPTION

The LMP8278 is a fixed 14x gain precision current sense amplifier. The part amplifies and filters small differential signals in the presence of high common mode voltages. The part operates from a single 5V supply voltage. With an input common mode voltage range from -2V to +28V the gain is very precise ($\pm 0.5\%$). The part can handle common mode voltages in the range -2V to +40V with relaxed specifications. The LMP8278 is a member of the Linear Monolithic Precision (LMP™) family and is ideal for unidirectional current sensing applications. The parameter values that are shown in the Electrical Characteristics table are 100% tested and all bold values are also 100% tested over temperature, unless otherwise noted.

The part has a precise gain of 14x which is adequate in most targeted applications to drive an ADC to its full scale value. The fixed gain is achieved in two separate stages, a preamplifier with a gain of 7x and an output stage buffer amplifier with a gain of 2x. The connection between the two stages of the signal path is brought out on two pins to enable the possibility to create an additional filter network around the output buffer amplifier. These pins can also be used for alternative configurations with different gain as described in [Application Information](#).

The LMP8278Q incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard.

Typical Applications

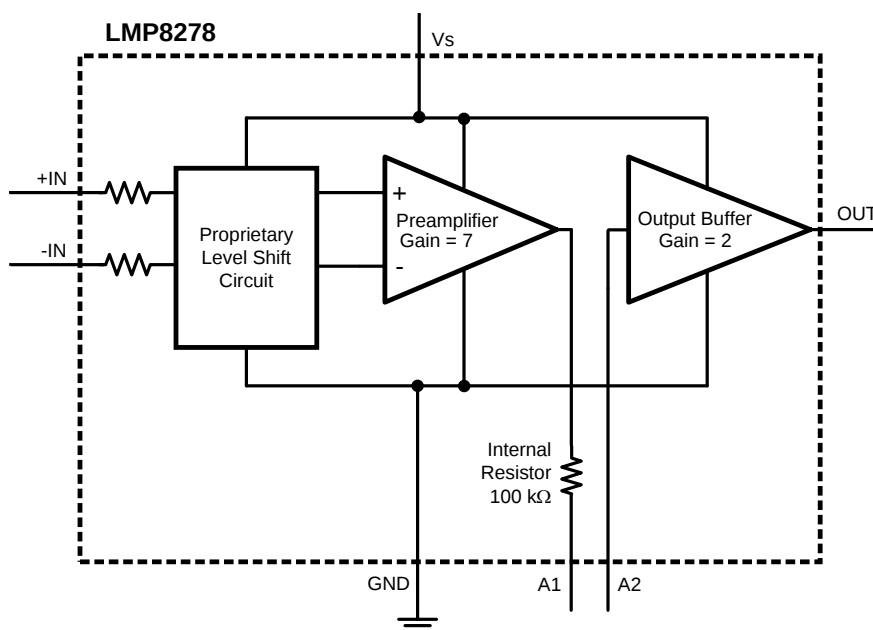


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LMP is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

Block Diagram



Connection Diagram

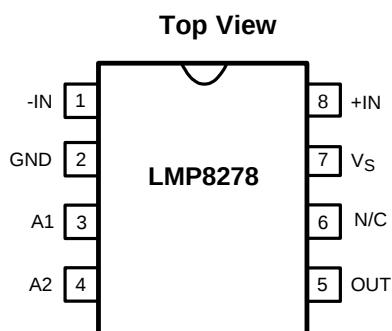


Figure 1. 8-Pin VSSOP Package
See Package Number DGK0008A

PIN DESCRIPTIONS

	Pin	Name	Description
Power Supply	2	GND	Power Ground
	7	V_S	Positive Supply Voltage
Inputs	1	-IN	Negative Input
	8	+IN	Positive Input
Filter Network	3	A1	Preamplifier output
	4	A2	Input from the external filter network and / or A1
Output	5	OUT	Single ended output
NC	6	N/C	No Connect (floating)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

ESD Tolerance ⁽²⁾	
Human Body	
For input pins only	±8000V
For all other pins	±2000V
Machine Model	200V
Charge Device Model	1000V
Supply Voltage (V _S - GND)	6V
Continuous Input Voltage (-IN and +IN) ⁽³⁾	-12V to 50V
Max Voltage at A1, A2 and OUT	V _S +0.3V
Min Voltage at A1, A2 and OUT	GND -0.3V
Storage Temperature Range	-65°C to 150°C
Junction Temperature ⁽⁴⁾	150°C
For soldering specs see: SNOA549C	

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Human Body Model per MIL-STD-883, Method 3015.7. Machine Model, per JESD22-A115-A. Field-Induced Charge-Device Model, per JESD22-C101-C.
- (3) For the VSSOP package, the pitch of the solder pads is too narrow for reliable use at higher voltages (V_{CM} >25V). Therefore, it is strongly advised to add a conformal coating on the PCB assembled with the LMP8278 / LMP8278Q.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation P_{DMAX} = (T_{J(MAX)} - T_A) / θ_{JA} or the number given in Absolute Maximum Ratings, whichever is lower.

Operating Ratings ⁽¹⁾

Supply Voltage (V _S - GND)	4.5V to 5.5V
Temperature Range ⁽²⁾	-40°C to +125°C
Package Thermal Resistance ⁽²⁾	
8-Pin VSSOP (θ _{JA})	230°C/W

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation P_{DMAX} = (T_{J(MAX)} - T_A) / θ_{JA} or the number given in Absolute Maximum Ratings, whichever is lower.

5.0V Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits ensured at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 28\text{V}$, and $R_L = \infty$, 10nF between V_S and GND . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
Overall Performance (From –IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I _S	Supply Current			0.3	0.4	0.55	mA
A _V	Total Gain	–2V < V _{CM} < 28V		13.93	14	14.07	V/V
		–2V < V _{CM} < 40V		13.86	14	14.14	
	Gain Drift	–40°C ≤ T _A ≤ 125°C			±2	±25	ppm/°C
SR	Slew Rate	V _{IN} = ±0.2V			0.7		V/μs
BW	Bandwidth				90		kHz
V _{OS}	Input Offset Voltage	V _{CM} = V _S / 2			±0.25	±2	mV
TCV _{OS}	Input Offset Voltage Drift ⁽⁴⁾	–40°C ≤ T _A ≤ 125°C			±2.5	±15	μV/°C
e _n	Input Referred Voltage Noise	0.1 Hz – 10 Hz, 6–Sigma			11		μV _{PP}
		Spectral Density, 1 kHz			285		nV/√Hz
PSRR	Power Supply Rejection Ratio	DC, 4.5V ≤ V _S ≤ 5.5V, V _{CM} = V _S /2		70	80		dB
Preamplifier (From input pins –IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R _{CM}	Input Impedance Common Mode	–2V ≤ V _{CM} ≤ 40		100	125		kΩ
R _{DM}	Input Impedance Differential Mode ⁽⁵⁾	–2V ≤ V _{CM} ≤ 40		60	85		kΩ
V _{OS}	Input Offset Voltage	V _{CM} = V _S / 2			±0.25	±2	mV
TCV _{OS}	Input Offset Voltage Drift ⁽⁴⁾	–40°C ≤ T _A ≤ 125°C			±2.5	±15	μV/°C
DC CMRR	DC Common Mode Rejection Ratio	–2V ≤ V _{CM} ≤ 40V		80	90		dB
AC CMRR	AC Common Mode Rejection Ratio	f = 1 kHz			90		dB
		f = 10 kHz			85		
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR		–2		40	V
A1 _V	Gain			6.93	7.0	7.07	V/V
R _{F-INT}	Output Impedance Filter Resistor			97	100	103	kΩ
TCR _{F-INT}	Output Impedance Filter Resistor Drift				20	±100	ppm/°C
A1 V _{OUT}	Preamplifier Output Voltage Swing	V _{OL}	R _L = ∞		4	10	mV
		V _{OH}		4.80	4.95	V	
Output Buffer (From A2 (pin 4) to OUT (pin 5))							
V _{OS}	Input Offset Voltage	0V ≤ V _{CM} ≤ V _S –1			±0.25	±2	mV
A2 _V	Gain			1.98	2	2.02	V/V
I _B	Input Bias Current of Output Buffer ⁽⁶⁾⁽⁵⁾				±20		pA
						±20	nA
A2 V _{OUT}	Output Buffer Output Voltage Swing ⁽⁷⁾⁽⁸⁾	V _{OL}	R _L = 100 kΩ		7	20	mV
		V _{OH}		4.80	4.99	V	
A2 V _{OUT}	Output Buffer Output Voltage Swing ⁽⁷⁾⁽⁸⁾	V _{OL}	R _L = 10 kΩ		15	30	mV
		V _{OH}		4.75	4.95	V	

- (1) The Electrical Characteristics table lists ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Datasheet min/max specification limits are ensured by test, unless otherwise noted.
- (3) Typical values represent the most likely parameter norms at $T_A = +25^\circ\text{C}$ and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
- (5) Specification is ensured by design and is not tested in production.
- (6) Positive current corresponds to current flowing into the device.
- (7) For this test input is driven from A1 stage.
- (8) For V_{OL} , R_L is connected to V_S and for V_{OH} , R_L is connected to GND .

5.0V Electrical Characteristics ⁽¹⁾ (continued)

Unless otherwise specified, all limits ensured at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 28\text{V}$, and $R_L = \infty$, 10nF between V_S and GND . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
I_{SC}	Output Short-Circuit Current ⁽⁶⁾ ⁽⁹⁾	Sourcing, $V_{\text{IN}} = V_S$, $V_{\text{OUT}} = \text{GND}$	-10			mA
		Sinking, $V_{\text{IN}} = \text{GND}$, $V_{\text{OUT}} = V_S$	10			

- (9) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

Typical Performance Characteristics

Unless otherwise specified, measurements taken at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 28\text{V}$, and $R_L = \infty$, 10nF between V_S and GND .

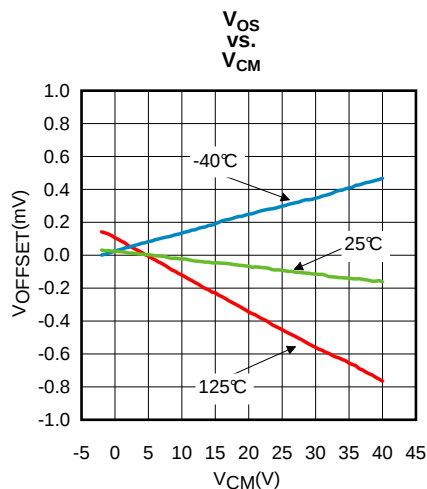


Figure 2.

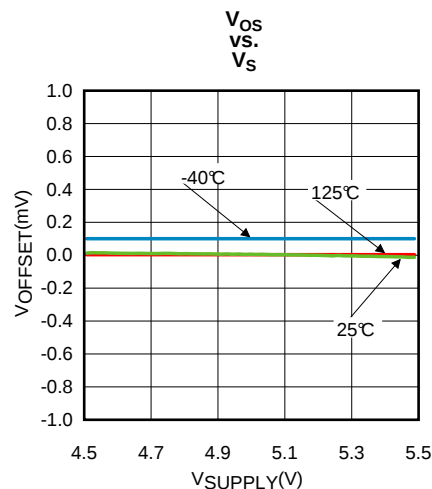


Figure 3.

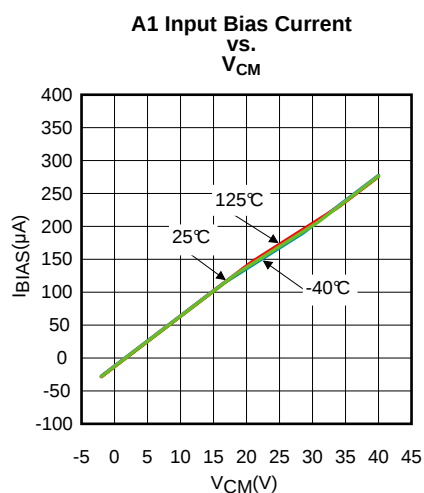


Figure 4.

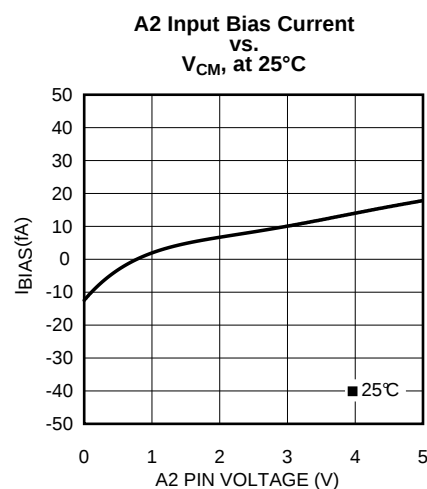


Figure 5.

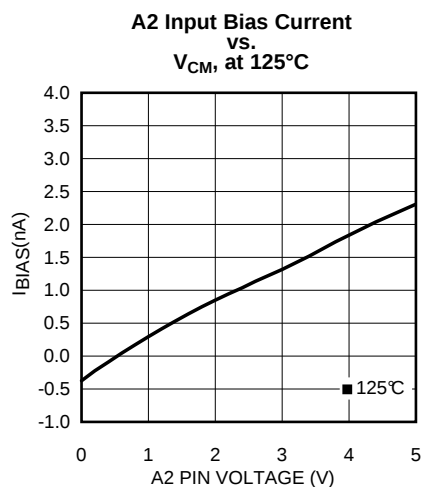


Figure 6.

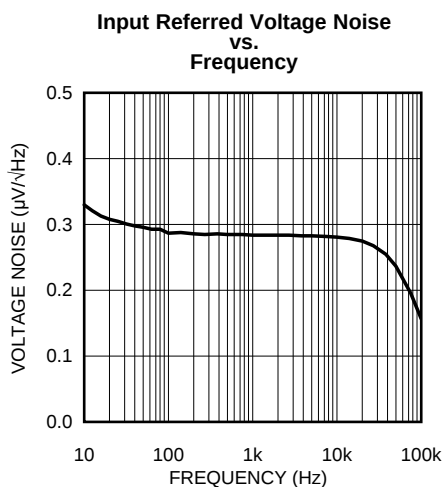


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified, measurements taken at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 28\text{V}$, and $R_L = \infty$, 10nF between V_S and GND .

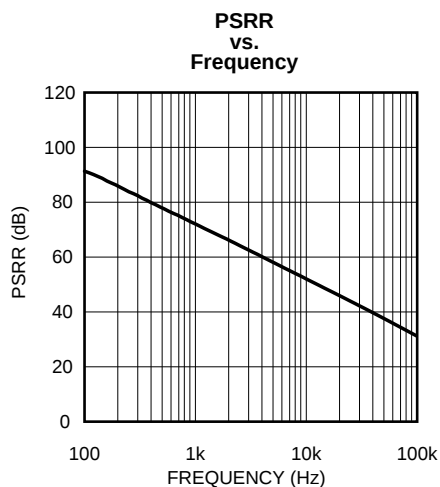


Figure 8.

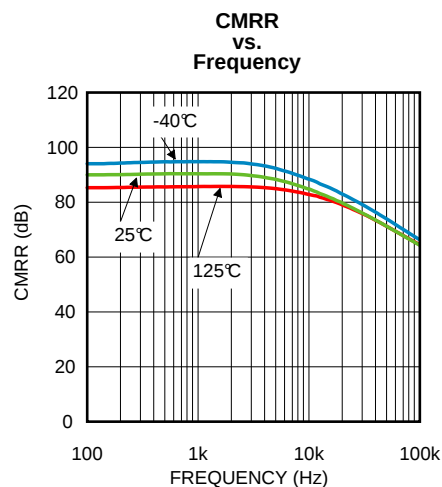


Figure 9.

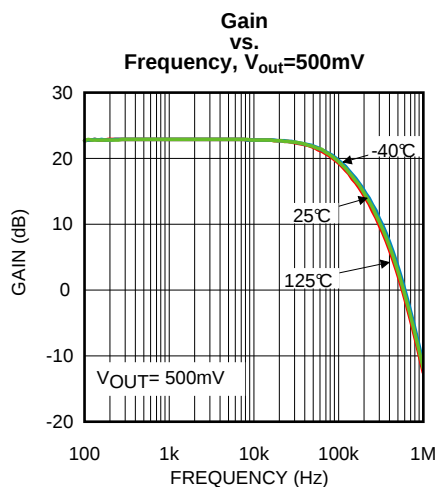


Figure 10.

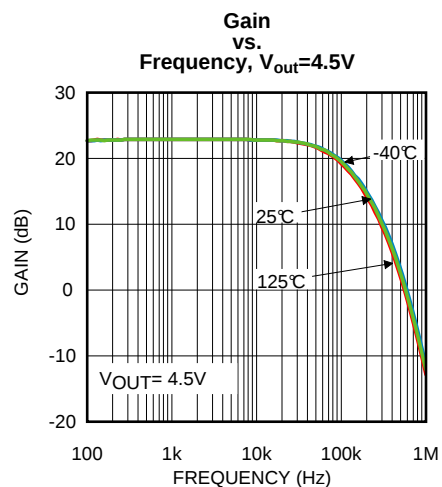


Figure 11.

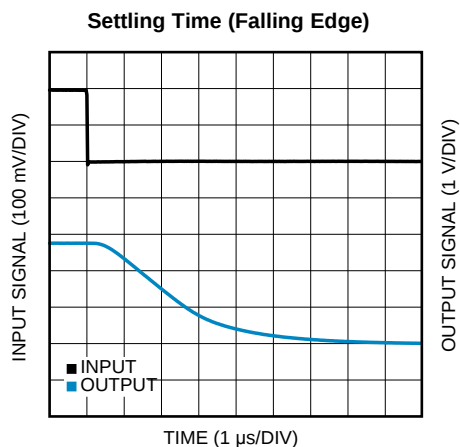


Figure 12.

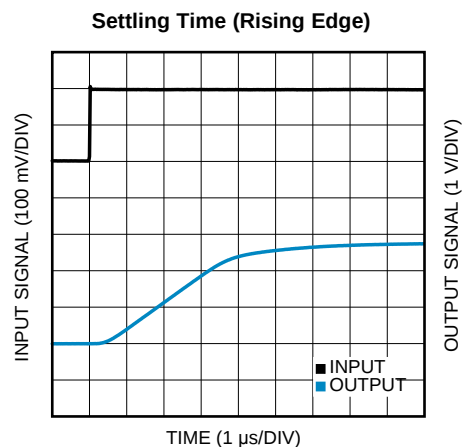


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified, measurements taken at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 28\text{V}$, and $R_L = \infty$, 10nF between V_S and GND .

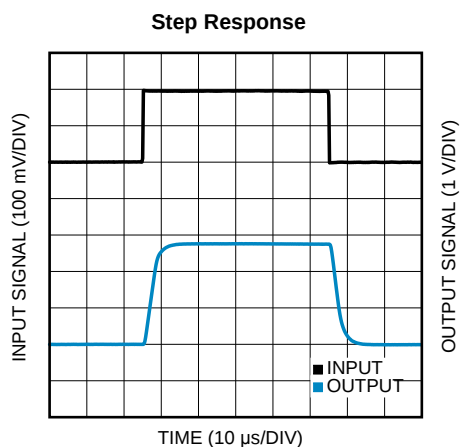


Figure 14.

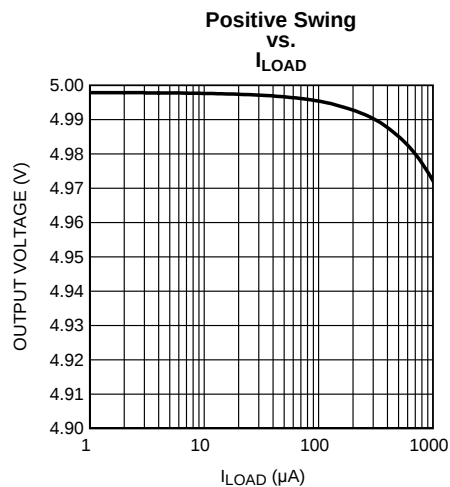


Figure 15.

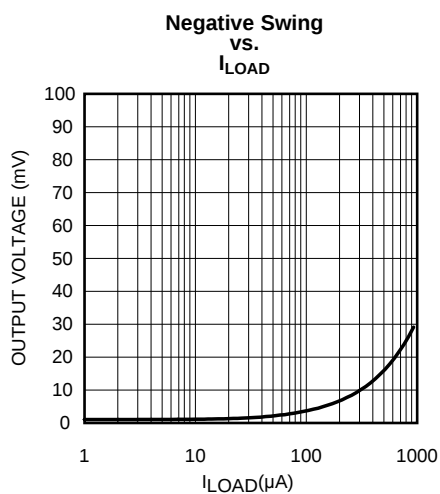


Figure 16.

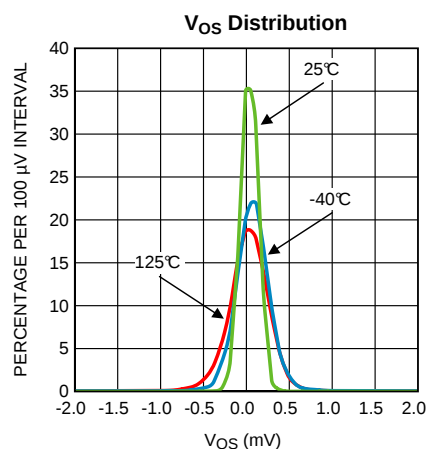


Figure 17.

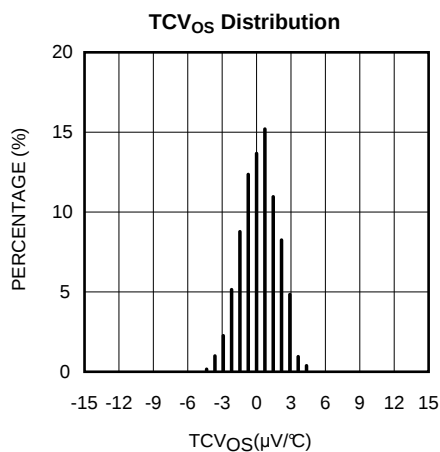


Figure 18.

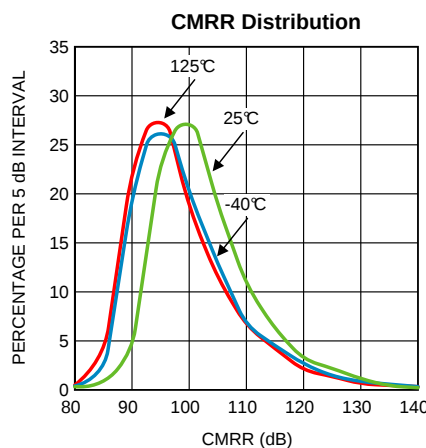


Figure 19.

APPLICATION INFORMATION

GENERAL

The LMP8278 is a fixed gain differential voltage precision amplifier with a gain of 14x and a -2V to +40V input common mode voltage range when operating from a single 5V supply. The LMP8278 is a member of the LMP™ family and is ideal for unidirectional current sensing applications. Because of its proprietary level-shift input stage the LMP8278 achieves very low offset, very low thermal offset drift, and very high CMRR. The LMP8278 amplifies and filters small differential signals in the presence of high common mode voltages.

The LMP8278 uses level shift resistors at the inputs. Because of these resistors, the LMP8278 can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected current sense amplifiers might sustain permanent damage.

The LMP8278 is available in an 8-Pin VSSOP package. For the VSSOP package, the pitch of the solder pads is too narrow for reliable use at higher voltages ($V_{CM} > 25V$). Therefore, it is strongly advised to add a conformal coating on the PCB assembled with the LMP8278 in VSSOP package.

PERFORMANCE GUARANTIES

To guaranty the high performance of the LMP8278, minimum and maximum values shown in the [Electrical Characteristics](#) of this datasheet are 100% tested and all bold limits are also 100% tested over temperature, unless otherwise noted.

THEORY OF OPERATION

The schematic shown in [Figure 20](#) gives a schematic representation of the internal operation of the LMP8278.

The signal on the input pins is typically a small differential voltage across a current sensing shunt resistor. The input signal may appear at a high common mode voltage. The input signals are accessed through two input resistors. The proprietary level shift circuit brings the common mode voltage behind the input resistors within the supply rails. Subsequently, the signal is gained up by a factor of 7 and brought out on the A1 pin through a trimmed 100 kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as will be explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 and brought out on the OUT pin.

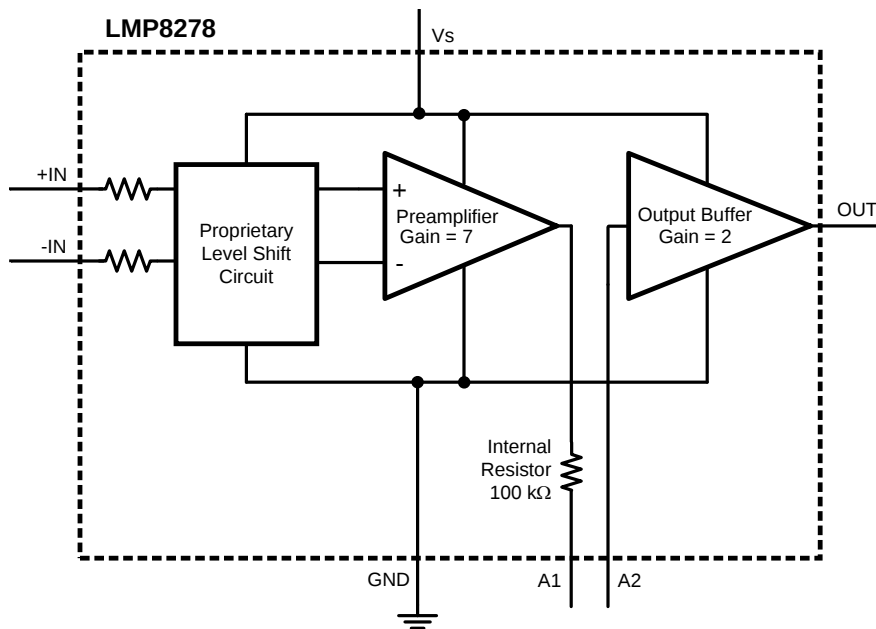


Figure 20. Theory of Operation

ADDITIONAL SECOND ORDER LOW PASS FILTER

The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first order low pass filter with a time constant determined by the 100 kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second order Sallen-Key low pass filter, as illustrated in [Figure 21](#), by adding external components R_2 , C_1 and C_2 . Together with the internal 100 kΩ resistor R_1 , this circuit creates a second order low-pass filter characteristic.

When the corner frequency of the additional filter is much lower than 90 kHz, the transfer function of the described amplifier can be written as:

$$H(s) = \frac{K_1 * K_2 \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s * \left[\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2} + \frac{(1 - K_2)}{R_2 C_1} \right] + \frac{1}{R_1 R_2 C_1 C_2}}$$

where

- K_1 equals the gain of the preamplifier
- K_2 that of the buffer amplifier

(1)

The above equation can be written in the normalized frequency response for a 2nd order low pass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\frac{(j\omega)^2}{\omega_0^2} + \frac{j\omega}{Q\omega_0} + 1}$$

(2)

The cut-off frequency ω_0 in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

(3)

And the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1 - K_2) * R_1 C_2}$$

(4)

With $K_2 > 1x$, the above equation results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{(K-1)}}}{R_1 C_1 + R_2 C_1 - \frac{(K-1) R_1 C_2}{(K-1)}}$$

(5)

For any filter gain $K > 1x$, the design procedure can be very simple if the two capacitors are chosen in a certain ratio.

$$C_2 = \frac{C_1}{K - 1}$$

(6)

In this case, given the predetermined value of $R_1 = 100 \text{ k}\Omega$ (the internal resistor), the quality factor is set solely by the value of the resistor R_2 .

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with the following equation:

$$R_2 = \frac{R_1}{(K-1)Q^2} \quad (7)$$

For the gain of 2 for the LMP8278 this results in:

$$R_2 = \frac{R_1}{Q^2} \quad (8)$$

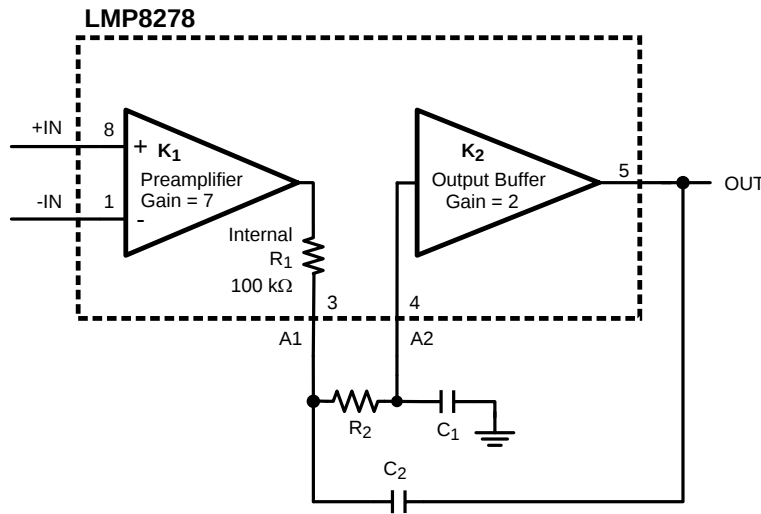


Figure 21. Second Order Low Pass Filter

For instance, the value of Q can be set to $0.5\sqrt{2}$ to create a Butterworth response, to $1/\sqrt{3}$ to create a Bessel response, or to 0.5 to create a critically damped response. Once the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C_1 = \frac{(K-1)Q}{R_1\omega_0} \quad (9)$$

Which for the gain=2 will give:

$$C_1 = \frac{Q}{R_1\omega_0} \quad (10)$$

For C_2 the value is calculated with:

$$C_2 = \frac{C_1}{K-1} \quad (11)$$

Or, for a gain=2, $C_2=C_1$

Note that the frequency response achieved using this procedure will only be accurate if the cut-off frequency of the second order filter is much smaller than the intrinsic 90 kHz low-pass response. In other words, choose the frequency response of the circuit such that the internal poles of the LMP8278 do not affect the external second order filter.

For a desired $Q = 0.707$ and a cut off frequency = 3 kHz, this will result in rounded values for $R_2 = 200 \text{ k}\Omega$, $C_1:C_2 = 390 \text{ pF}$.

GAIN ADJUSTMENT

The gain of the LMP8278 is 14; however, this gain can be adjusted as the signal path in between the two internal amplifiers is available on the external pins.

Reduce Gain

Figure 22 shows the configuration that can be used to reduce the gain of the LMP8278.

R_r creates a resistive divider together with the internal $100 \text{ k}\Omega$ resistor such that the reduced gain G_r becomes:

$$G_r = \frac{14 R_r}{R_r + 100 \text{ k}\Omega} \quad (12)$$

Given a desired value of the reduced gain G_r , using this equation the required value for R_r can be calculated with:

$$R_r = 100 \text{ k}\Omega \times \frac{G_r}{14 - G_r} \quad (13)$$

Increase Gain

Figure 23 shows the configuration that can be used to increase the gain of the LMP8278.

R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i becomes:

$$G_i = \frac{14 R_i}{R_i - 100 \text{ k}\Omega} \quad (14)$$

From this equation, for a desired value of the gain, the required value of R_i can be calculated with:

$$R_i = 100 \text{ k}\Omega \times \frac{G_i}{G_i - 14} \quad (15)$$

It should be noted from the equation for the gain G_i that for large gains R_i approaches $100 \text{ k}\Omega$. In this case, the denominator in the equation becomes close to zero. In practice, for large gains the denominator will be determined by tolerances in the values of the external resistor R_i and the internal $100 \text{ k}\Omega$ resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system will even become unstable. It is recommended to limit the application of this technique to gain values of 35 or smaller.

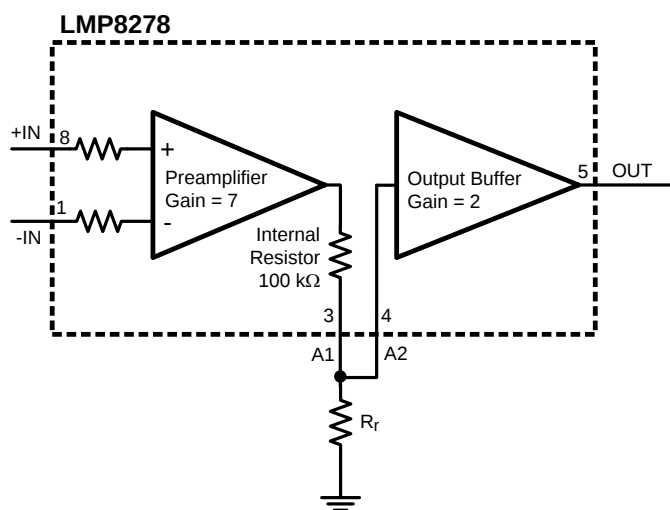


Figure 22. Reduce Gain

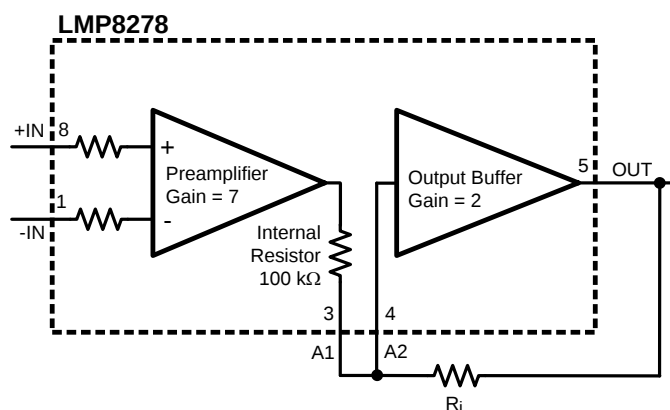


Figure 23. Increase Gain

POWER SUPPLY DECOUPLING

In order to decouple the LMP8278 from AC noise on the power supply, it is recommended to use a 0.1 μF bypass capacitor between the V_S and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 μF bypass capacitor may further reduce the supply noise.

DRIVING SWITCHED CAPACITIVE LOADS

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP8278 is driving such ADCs the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in [Figure 24](#) where the output is connected to a capacitor that is driven by a rail to rail square wave.

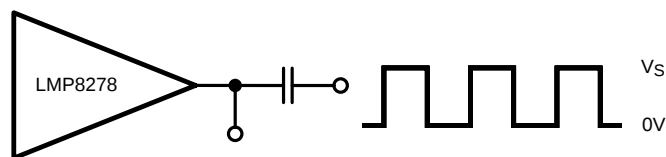


Figure 24. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP8278 output. The resulting V_{OUT} disturbance signal is shown in Figure 25.

The figure can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, an additional RC filter can be placed in between the LMP8278 and the ADC as illustrated in Figure 26.

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample and hold capacitor at the input of the ADC and the RC time constant of the external filter should be such that the speed of the system is not affected.

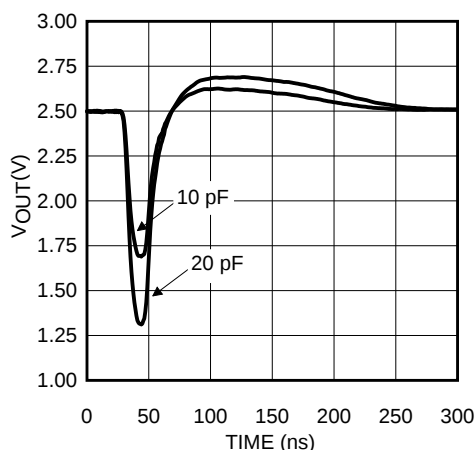


Figure 25. Capacitive Load Response

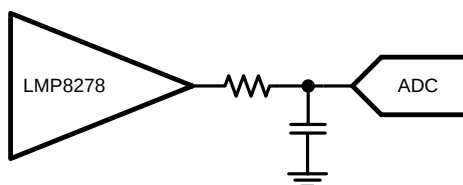


Figure 26. Reduce Error When Driving ADCs

LOW SIDE CURRENT SENSING APPLICATION

Figure 27 illustrates a low side current sensing application with a low side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common mode voltage range of the LMP8278 and because of the high AC common mode rejection ratio, the LMP8278 is very well suited for this application.

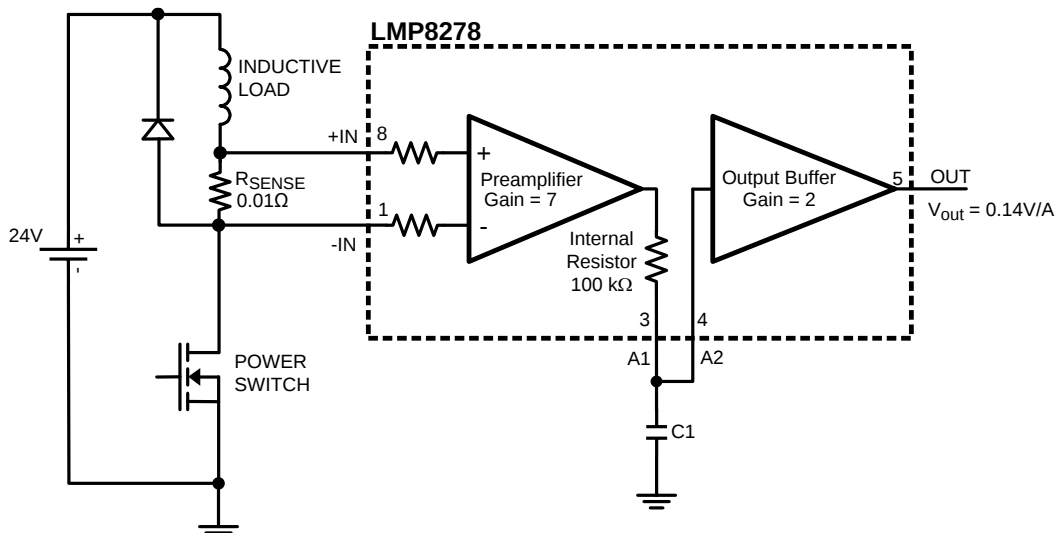


Figure 27. Low Side Current Sensing Application

HIGH SIDE CURRENT SENSING APPLICATION

Figure 28 illustrates the application of the LMP8278 in a high side sensing application. This application is similar to the low side sensing discussed above, except in this application the common mode voltage on the shunt drops below ground when the driver is switched off. Because the common mode voltage range of the LMP8278 extends below the negative rail, the LMP8278 is also very well suited for this application.

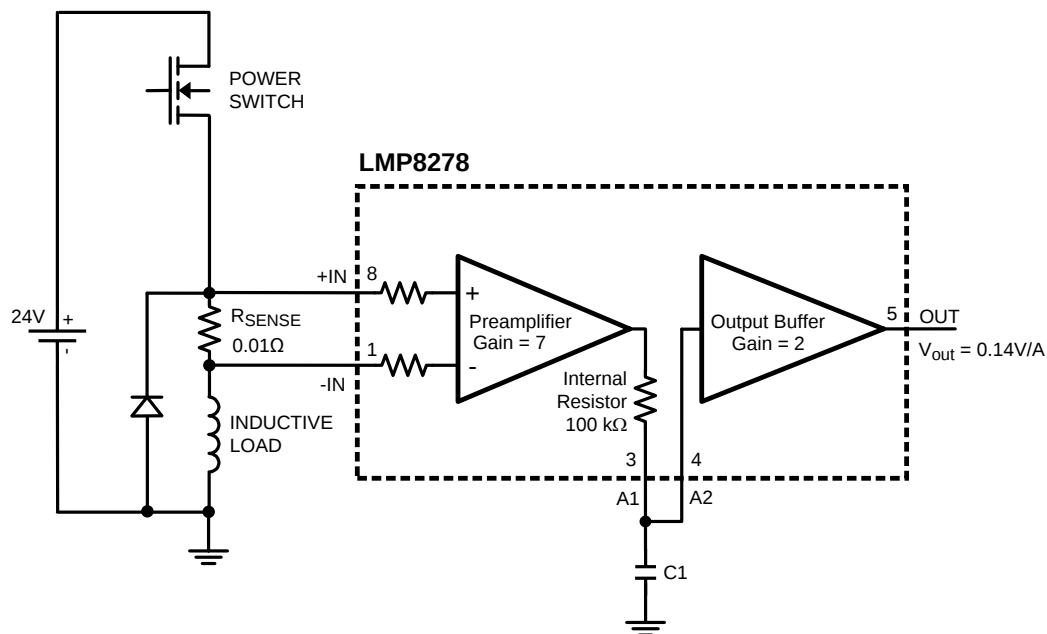


Figure 28. High Side Current Sensing Application

RF-PA CONTROL APPLICATION

Figure 29 illustrates how the LMP8278 can be used to monitor current flow in an RF power amplifier control application. The fact that the LMP8278 can measure small voltages at a high common mode voltage outside its own supply range makes this part a good choice for such an application. The output signal of the LMP8278 is used as an input for the PA controller. The PA controller can be used to regulate the output power of the RF-PA by measuring the output amplifier supply current.

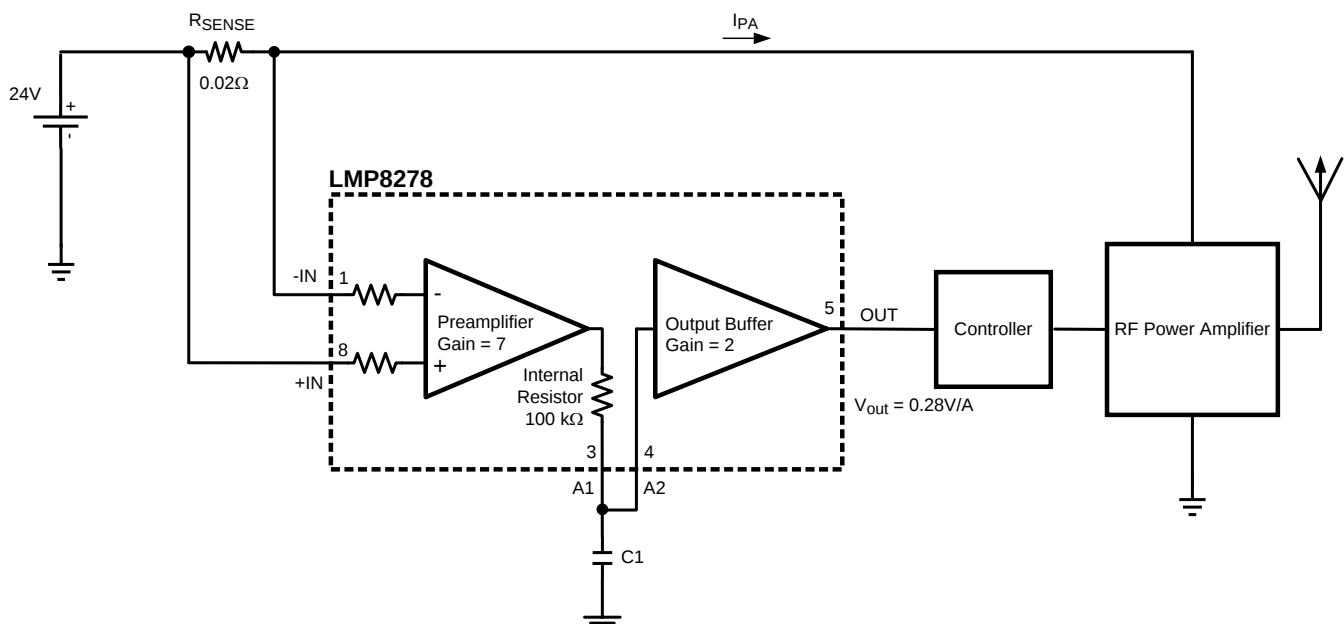


Figure 29. RF Power Amplifier Control Application

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8278QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AB7A	Samples
LMP8278QMME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AB7A	Samples
LMP8278QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AB7A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



www.ti.com

PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8278QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8278QMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8278QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

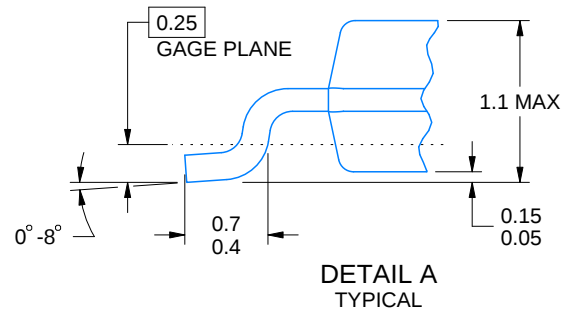
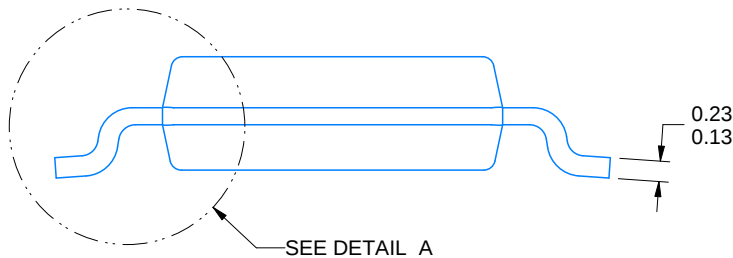
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8278QMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMP8278QMME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LMP8278QMMX/NOPB	VSSOP	DGK	8	3500	356.0	356.0	35.0



VSSOP - 1.1 mm max height

The drawing illustrates the mechanical specifications of a connector housing through three views: front, side, and end.

- Front View:** Shows a central rectangular body with a "PIN 1 INDEX AREA" indicated by a dashed circle. Dimensions include a total width of 5.05 (typical) and 4.75, a height of 8, and a pin pitch of 1.95 (2X). The number of pins is specified as 6X. A vertical dimension of 3.1 (2.9) is noted on the left, associated with "NOTE 3".
- Side View:** Shows the profile of the housing with a "SEATING PLANE" indicated. It includes a feature control frame with a circular symbol, a tolerance of 0.1, and datum C.
- End View:** Shows the internal pin arrangement. It includes a feature control frame with concentricity symbols, a tolerance of 0.13, datum M, and datums C, A, and B. Vertical dimensions of 0.38 and 0.25 are shown for specific pin features.



PowerPAD is a trademark of Texas Instruments.

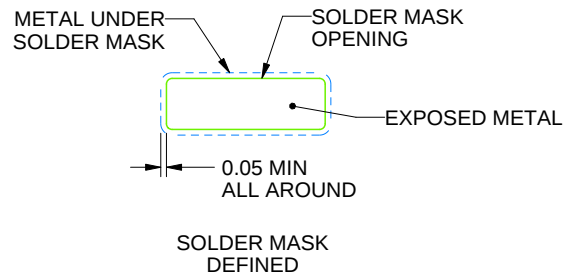
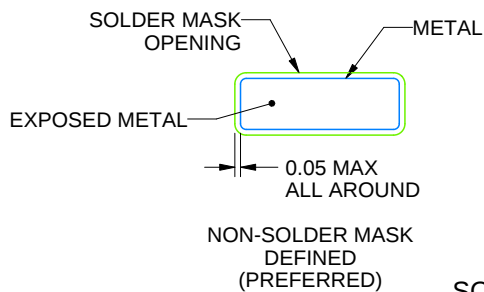
- 
- TEXAS
INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated