TEXAS INSTRUMENTS
LMT85-Q1
JAJSE56 – OCTOBER 2017

LMT85-Q1 1.8V、SC70、アナログ温度センサ

1 特長

- LMT85-Q1は車載用アプリケーション向けにAEC-Q100認定済み:
  - デバイス温度グレード0: -40℃～+150℃
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- 非常に正確: ±0.4℃ (標準値)
- 低電圧1.8Vでの動作
- 平均センサ・ゲイン: -8.2mV/℃
- 低い静止電流: 5.4µA
- 広い温度範囲: -50℃～150℃
- 出力の短絡保護
- 駆動能力±50µAのプッシュプル出力
- 業界標準のLM20/19およびLM35温度センサとフットプリント互換
- コスト効率に優れたサーミスタの代替

2 アプリケーション

- インフォテインメントおよびクラスタ
- パワートレイン・システム
- 煙および熱感知器
- ドローン
- 家電製品

3 概要

LMT85-Q1は高精度のCMOS温度センサで、標準精度は±0.4℃ (最大値±2.7℃)で、リニアなアナログ出力電圧を持ち、この電圧は温度に反比例します。1.8Vの電源電圧で動作し、静止電流が5.4µA、パワーオン時間が0.7msで、効果的なパワーサイクリング・アーキテクチャを実現し、ドローンやセンサ・ノードなどバッテリ駆動のアプリケーションで消費電力を最小化できます。LMT85-Q1デバイスはAEC-Q100グレード0認定済みで、較正なしで動作温度範囲の全体にわたり、最大±2.7℃の精度を維持します。このため、LMT85-Q1はインフォテイメント、クラスタ、パワートレイン・システムなどの車載用アプリケーションに適しています。広い動作範囲にわたる精度や、その他の特長から、LMT85-Q1はサーミスタの優れた代替となります。

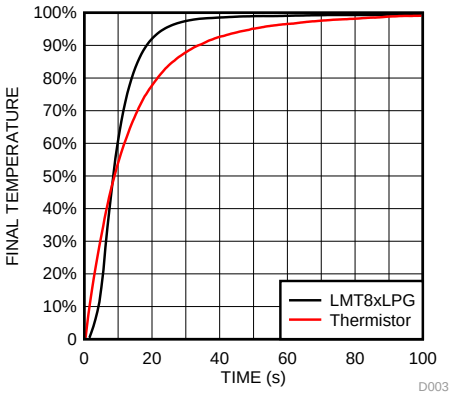
異なる平均センサ・ゲインおよび類似の精度を持つデバイスについては、「*類似の代替デバイス*」で、LMT8xファミリの他のデバイスを参照してください。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMT85-Q1	SOT (5)	2.00mm×1.25mm

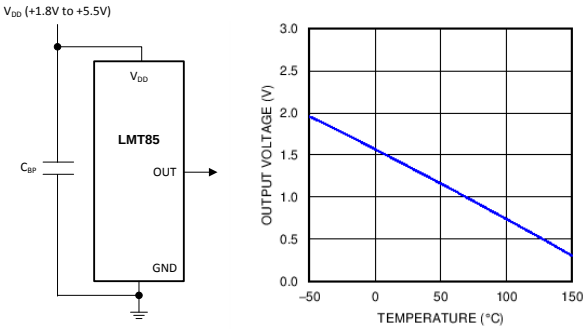
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

熱時定数



* 高速な熱応答NTC

出力電圧と温度との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年10月	*	初版。車載用デバイスをSNIS200から、単独のデータシートへ移動.

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5 Device Comparison Tables

Table 1. Available Device Packages

ORDER NUMBER(1)	PACKAGE	PIN	BODY SIZE (NOM)	MOUNTING TYPE
LMT85DCK	SOT (AKA(2): SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount
LMT85LP	TO-92 (AKA(2): LP)	3	4.30 mm × 3.50 mm	Through-hole; straight leads
LMT85LPG	TO-92S (AKA(2): LPG)	3	4.00 mm × 3.15 mm	Through-hole; straight leads
LMT85LPM	TO-92 (AKA(2): LPM)	3	4.30 mm × 3.50 mm	Through-hole; formed leads
LMT85DCK-Q1	SOT (AKA(2): SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount

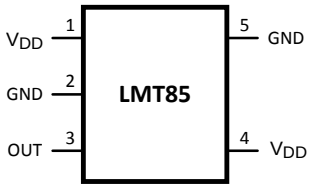
(1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.
(2) AKA = Also Known As

Table 2. Comparable Alternative Devices

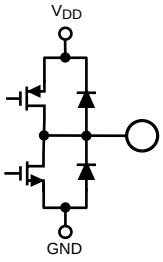
DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
LMT84-Q1	–5.5 mV/°C	1.5 V to 5.5 V
LMT85-Q1	–8.2 mV/°C	1.8 V to 5.5 V
LMT86-Q1	–10.9 mV/°C	2.2 V to 5.5 V
LMT87-Q1	–13.6 mV/°C	2.7 V to 5.5 V

6 Pin Configuration and Functions

DCK Package
5-Pin SOT/SC70
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	SOT (SC70)		EQUIVALENT CIRCUIT	FUNCTION
GND	2(1) , 5	Ground	N/A	Power Supply Ground
OUT	3	Analog Output		Outputs a voltage that is inversely proportional to temperature
V_{DD}	1, 4	Power	N/A	Positive Supply Voltage

(1) Direct connection to the back side of the die

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7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
Supply voltage	−0.3	6	V
Voltage at output pin	−0.3	(V_{DD} + 0.5)	V
Output current	–7	7	mA
Input current at any pin (3)	–5	5	mA
Maximum junction temperature (T_{JMAX})		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) Soldering process must comply with Reflow Temperature Profile specifications. Refer towww.ti.com/packaging .
(3) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V), the current at that pin should be limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
LMT85DCK-Q1 in SC70 package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified temperature	$T_{MIN} \le T_A \le T_{MAX}$		°C
	−50 ≤ T_A ≤ 150		°C
Supply voltage (V_{DD})	1.8	5.5	V

7.4 Thermal Information(1)

THERMAL METRIC(2)		LMT85-Q1 DCK (SOT/SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3)(4)	275	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	°C/W

(1) For information on self-heating and thermal response time, see section *Mounting and Thermal Conductivity*.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(3) The junction to ambient thermal resistance ($R_{\theta JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(4) Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

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7.5 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in Table 3.

PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
Temperature accuracy (3)	$T_A = T_J$= 20°C to 150°C; V_{DD} = 1.8 V to 5.5 V	–2.7	±0.4	2.7	°C
	$T_A = T_J$= 0°C to 150°C; V_{DD} = 1.9 V to 5.5 V	–2.7	±0.7	2.7	°C
	$T_A = T_J$= 0°C to 150°C; V_{DD} = 2.6 V to 5.5 V		±0.3		°C
	$T_A = T_J$= –50°C to 0°C; V_{DD} = 2.3 V to 5.5 V	–2.7	±0.7	2.7	°C
	$T_A = T_J$= –50°C to 0°C; V_{DD} = 2.9 V to 5.5 V		±0.25		°C

(1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

7.6 Electrical Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = +1.8V to +5.5V. MIN and MAX limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted; typical values apply for $T_A = T_J$ = 25°C.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
	Average sensor gain (output transfer function slope)	–30°C and 90°C used to calculate average sensor gain		–8.2		mV/°C
	Load regulation (3)	Source ≤ 50 µA, (V_{DD} - V_{OUT}) ≥ 200 mV	–1	–0.22		mV
		Sink ≤ 50 µA, V_{OUT} ≥ 200 mV		0.26	1	mV
	Line regulation (4)			200		µV/V
I_S	Supply current	$T_A = T_J$ = 30°C to 150°C, (V_{DD} - V_{OUT}) ≥ 100 mV		5.4	8.1	µA
		$T_A = T_J$ = -50°C to 150°C, (V_{DD} - V_{OUT}) ≥ 100 mV		5.4	9	µA
C_L	Output load capacitance			1100		pF
	Power-on time (5)	C_L= 0 pF to 1100 pF		0.7	1.9	ms
	Output drive	$T_A = T_J$ = 25°C	–50		+50	µA

(1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Source currents are flowing out of the LMT85-Q1. Sink currents are flowing into the LMT85-Q1.
(4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in Output Voltage Shift.
(5) Specified by design and characterization.

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7.7 Typical Characteristics

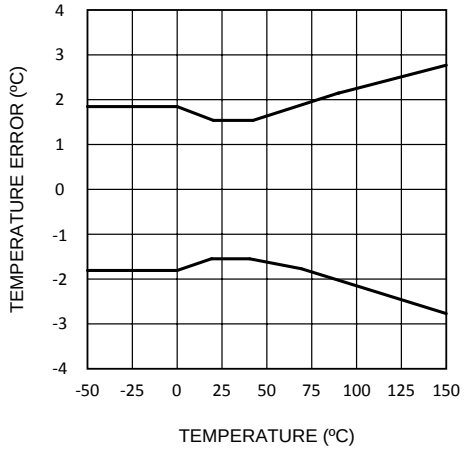

Figure 1. Temperature Error vs Temperature

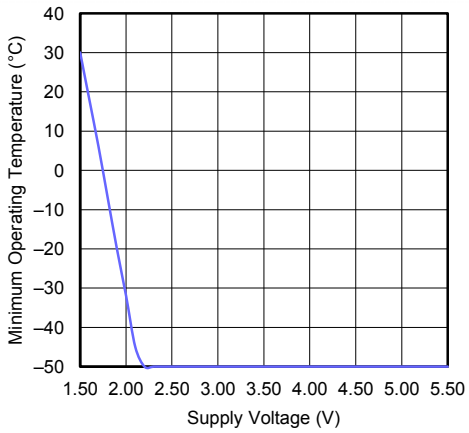

Figure 2. Minimum Operating Temperature vs Supply Voltage

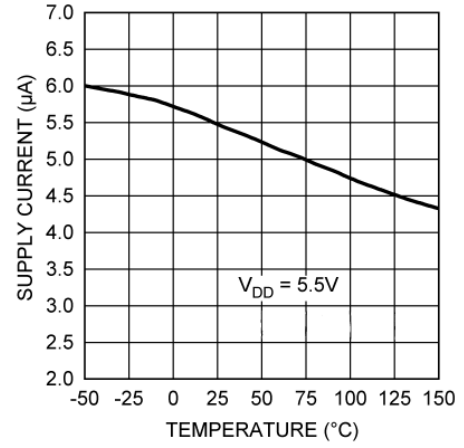

Figure 3. Supply Current vs Temperature

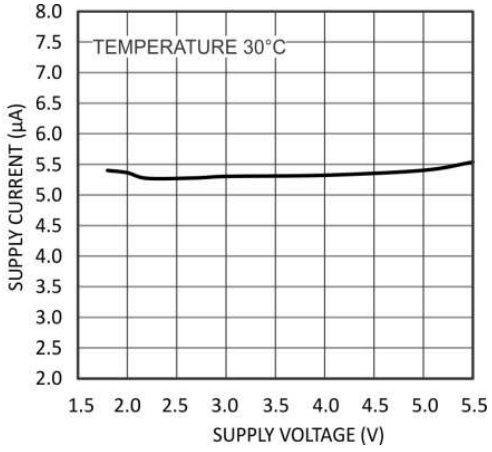

Figure 4. Supply Current vs Supply Voltage

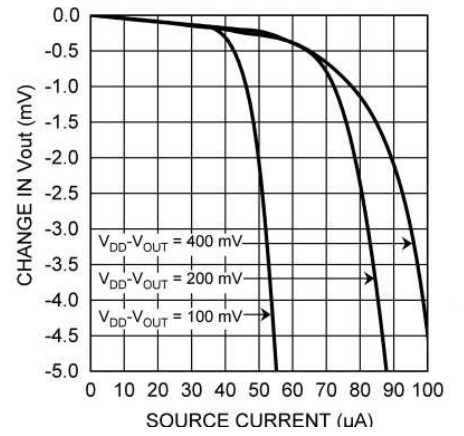

Figure 5. Load Regulation, Sourcing Current

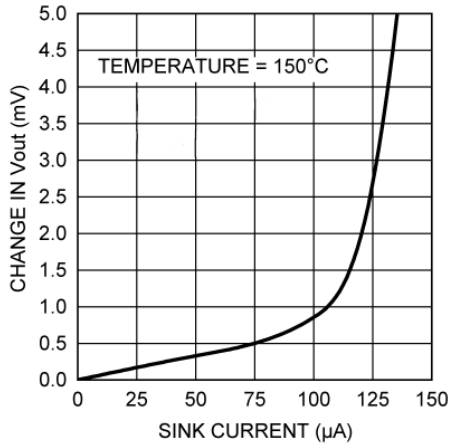

Figure 6. Load Regulation, Sinking Current

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Typical Characteristics (continued)

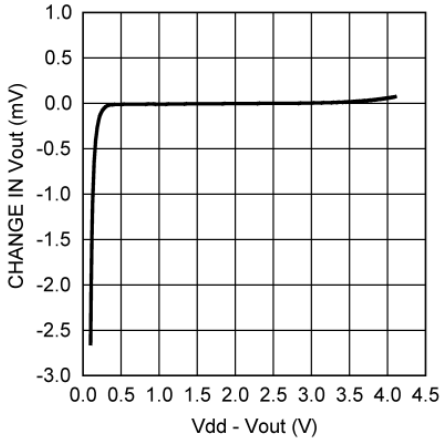

Figure 7. Change in Vout vs Overhead Voltage

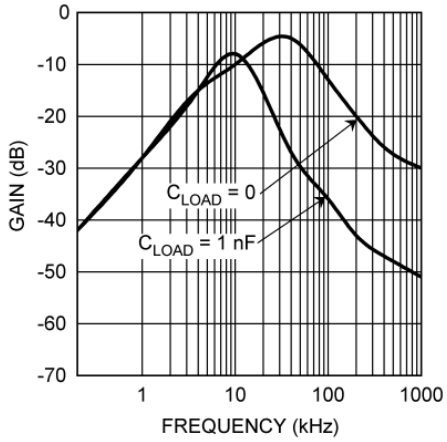

Figure 8. Supply-Noise Gain vs Frequency

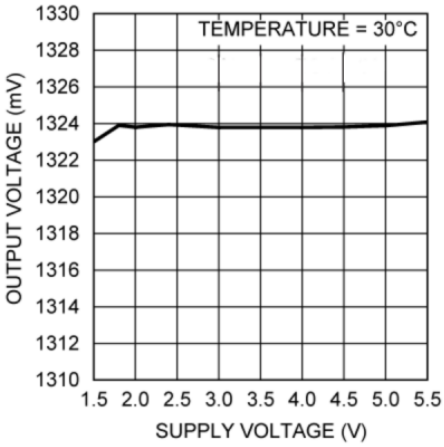

Figure 9. Output Voltage vs Supply Voltage

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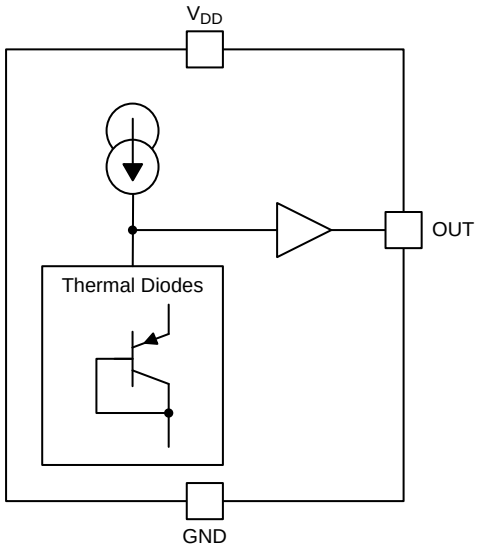
8 Detailed Description

8.1 Overview

The LMT85-Q1 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

8.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (−50°C to 150°C).



8.3 Feature Description

8.3.1 LMT85-Q1 Transfer Function

The output voltage of the LMT85-Q1, across the complete operating temperature range, is shown in Table 3. This table is the reference from which the LMT85 accuracy specifications (listed in the *Accuracy Characteristics* section) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the LMT85-Q1 product folder under *Tools and Software Models*.

Table 3. LMT85-Q1 Transfer Table

TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)
-50	1955		-10	1648		30	1324		70	991		110	651
-49	1949		-9	1639		31	1316		71	983		111	642
-48	1942		-8	1631		32	1308		72	974		112	634
-47	1935		-7	1623		33	1299		73	966		113	625
-46	1928		-6	1615		34	1291		74	957		114	617
-45	1921		-5	1607		35	1283		75	949		115	608
-44	1915		-4	1599		36	1275		76	941		116	599
-43	1908		-3	1591		37	1267		77	932		117	591
-42	1900		-2	1583		38	1258		78	924		118	582
-41	1892		-1	1575		39	1250		79	915		119	573
-40	1885		0	1567		40	1242		80	907		120	565
-39	1877		1	1559		41	1234		81	898		121	556
-38	1869		2	1551		42	1225		82	890		122	547

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Feature Description (continued)

Table 3. LMT85-Q1 Transfer Table (continued)

TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)		TEMP (°C)	V_{OUT} (mV)
-37	1861		3	1543		43	1217		83	881		123	539
-36	1853		4	1535		44	1209		84	873		124	530
-35	1845		5	1527		45	1201		85	865		125	521
-34	1838		6	1519		46	1192		86	856		126	513
-33	1830		7	1511		47	1184		87	848		127	504
-32	1822		8	1502		48	1176		88	839		128	495
-31	1814		9	1494		49	1167		89	831		129	487
-30	1806		10	1486		50	1159		90	822		130	478
-29	1798		11	1478		51	1151		91	814		131	469
-28	1790		12	1470		52	1143		92	805		132	460
-27	1783		13	1462		53	1134		93	797		133	452
-26	1775		14	1454		54	1126		94	788		134	443
-25	1767		15	1446		55	1118		95	779		135	434
-24	1759		16	1438		56	1109		96	771		136	425
-23	1751		17	1430		57	1101		97	762		137	416
-22	1743		18	1421		58	1093		98	754		138	408
-21	1735		19	1413		59	1084		99	745		139	399
-20	1727		20	1405		60	1076		100	737		140	390
-19	1719		21	1397		61	1067		101	728		141	381
-18	1711		22	1389		62	1059		102	720		142	372
-17	1703		23	1381		63	1051		103	711		143	363
-16	1695		24	1373		64	1042		104	702		144	354
-15	1687		25	1365		65	1034		105	694		145	346
-14	1679		26	1356		66	1025		106	685		146	337
-13	1671		27	1348		67	1017		107	677		147	328
-12	1663		28	1340		68	1008		108	668		148	319
-11	1656		29	1332		69	1000		109	660		149	310
												150	301

Although the LMT85-Q1 is very linear, its response does have a slight umbrella parabolic shape. This shape is very accurately reflected in Table 3. The Transfer Table can be calculated by using the parabolic equation (Equation 1).

$$V_{TEMP}(mV) = 1324.0mV - \left[8.194\frac{mV}{°C}(T - 30°C)\right] - \left[0.00262\frac{mV}{°C^2}(T - 30°C)^2\right] \quad (1)$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. Equation 1 can be solved for T resulting in:

$$T = \frac{8.194 - \sqrt{(-8.194)^2 + 4 \times 0.00262 \times (1324 - V_{TEMP}(mV))}}{2 \times -0.00262} + 30 \quad (2)$$

For an even less accurate linear transfer function approximation, a line can easily be calculated over the desired temperature range using values from the Table and a two-point equation (Equation 3):

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1}\right) \times (T - T_1)$$

where

- V is in mV,
- T is in °C,
- T_1 and V_1 are the coordinates of the lowest temperature,
- and T_2 and V_2 are the coordinates of the highest temperature. (3)

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For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

$$V - 1405\ mV = \left(\frac{1159\ mV - 1405\ mV}{50^oC - 20^oC}\right) \times (T - 20^oC) \quad (4)$$

$$V - 1405\ mV = (-8.20\ mV / {}^oC) \times (T - 20^oC) \quad (5)$$

$$V = (-8.20\ mV / {}^oC) \times T + 1569\ mV \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

8.4 Device Functional Modes

8.4.1 Mounting and Thermal Conductivity

The LMT85-Q1 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT85 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT85-Q1 will also affect the temperature reading.

Alternatively, the LMT85-Q1 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT85-Q1 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or V_{DD}, the output from the LMT85 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ($R_{\theta JA}$ or θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use Equation 7 to calculate the rise in the LMT85-Q1 die temperature:

$$T_J = T_A + \theta_{JA}\left[(V_{DD}I_S) + (V_{DD} - V_{OUT})\, I_L\right] \quad (7)$$

where

- T_A is the ambient temperature,
- I_S is the supply current,
- $I_L$is the load current on the output,
- and V_O is the output voltage.

For example, in an application where T_A = 30°C, V_{DD} = 5 V, I_S = 5.4 µA, V_{OUT} = 1324 mV, and I_L = 2 µA, the junction temperature would be 30.014°C, showing a self-heating error of only 0.014°C. Because the junction temperature of the LMT85-Q1 is the actual temperature being measured, take care to minimize the load current that the LMT85-Q1 is required to drive. *Thermal Information* shows the thermal resistance of the LMT85-Q1.

8.4.2 Output and Noise Considerations

A push-pull output gives the LMT85-Q1 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT85-Q1 device is ideal for this and other applications which require strong source or sink current.

The LMT85-Q1 supply-noise gain (the ratio of the AC signal on V_{OUT} to the AC signal on V_{DD}) was measured during bench tests. The typical attenuation is shown in Figure 8 found in the *Typical Characteristics* . A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT85-Q1.

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Device Functional Modes (continued)

8.4.3 Capacitive Loads

The LMT85-Q1 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the LMT85-Q1 can drive a capacitive load less than or equal to 1100 pF as shown in Figure 10. For capacitive loads greater than 1100 pF, a series resistor may be required on the output, as shown in Figure 11.

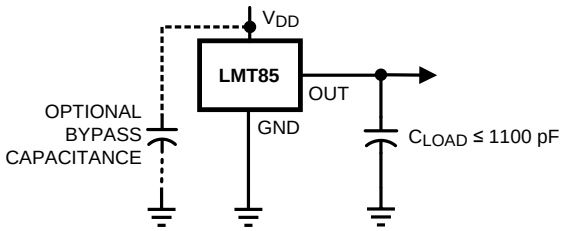

Figure 10. LMT85-Q1 No Decoupling Required for Capacitive Loads Less Than 1100 pF

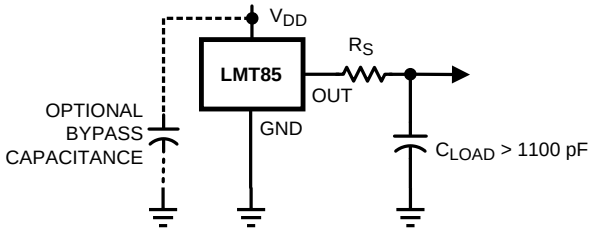

Figure 11. LMT85-Q1 with Series Resistor for Capacitive Loading Greater Than 1100 pF

Table 4. Recommended Series Resistor Values

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 μF	800 Ω

8.4.4 Output Voltage Shift

The LMT85-Q1 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT}. The shift typically occurs when V_{DD}- V_{OUT} = 1 V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT}. Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic. The accuracy specifications in the *Accuracy Characteristics* table already include this possible shift.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMT85-Q1 features make it suitable for many general temperature-sensing applications. It can operate down to 1.8-V supply with 5.4-µA power consumption, making it ideal for battery powered devices.

9.2 Typical Applications

9.2.1 Connection to an ADC

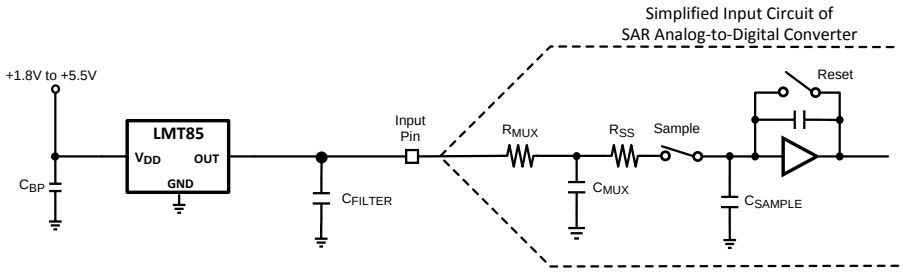

Figure 12. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

9.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT85 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}).

9.2.1.2 Detailed Design Procedure

The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

9.2.1.3 Application Curve

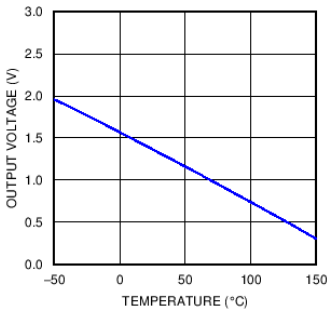

Figure 13. Analog Output Transfer Function

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Typical Applications (continued)

9.2.2 Conserving Power Dissipation With Shutdown

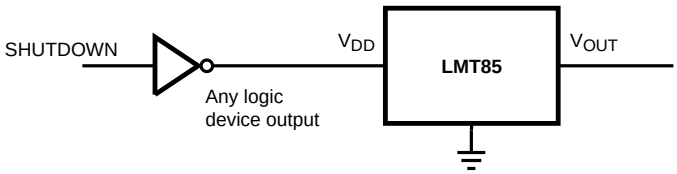


Figure 14. Simple Shutdown Connection of the LMT85-Q1

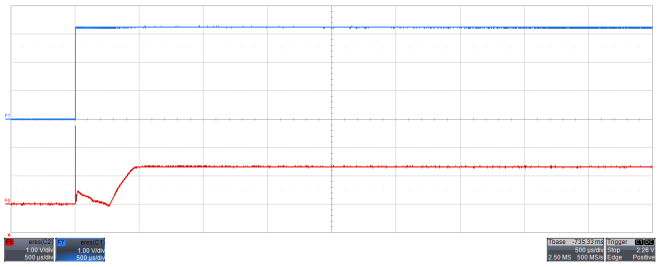
9.2.2.1 Design Requirements

Because the power consumption of the LMT85-Q1 is less than 9 µA, it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a micro controller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

9.2.2.2 Detailed Design Procedure

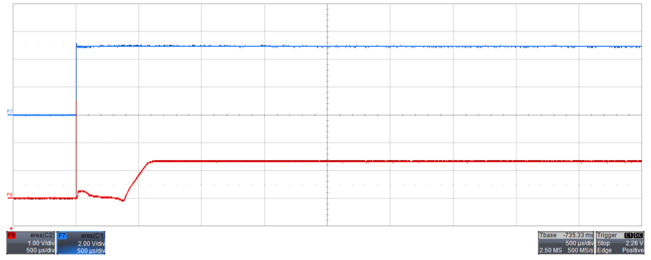
Simply connect the V_{DD} pin of the LMT85-Q1 directly to the logic shutdown signal from a microcontroller.

9.2.2.3 Application Curves



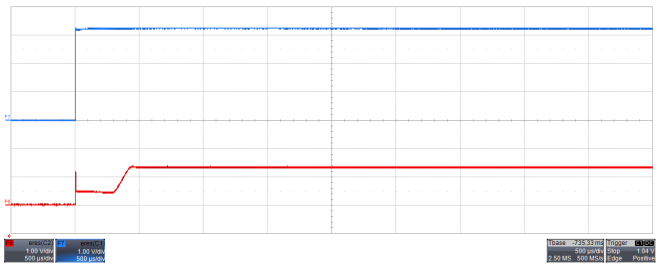
Time: 500 µs/div; Top Trace: V_{DD} 1 V/div;
Bottom Trace: OUT 1 V/div

Figure 15. Output Turnon Response Time Without a Capacitive Load and V_{DD} = 3.3 V



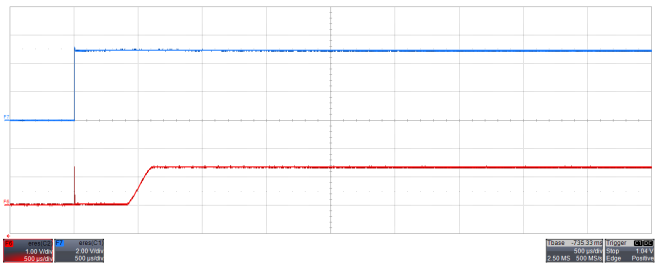
Time: 500 µs/div; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 16. Output Turnon Response Time Without a Capacitive Load and V_{DD} = 5 V



Time: 500 µs/div; Top trace: V_{DD} 1V/div;
Bottom trace: OUT 1 V/div

Figure 17. Output Turnon Response Time With 1.1-nF Capacitive Load and V_{DD} = 3.3 V



Time: 500 µs/div; Top trace: V_{DD} 2 V/div;
Bottom trace: OUT 1 V/div

Figure 18. Output Turnon Response Time With 1.1-nF Capacitive Load and V_{DD} = 5 V

10 Power Supply Recommendations

The low supply current and supply range (1.8 V to 5.5 V) of the LMT85-Q1 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT85-Q1.

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11 Layout

11.1 Layout Guidelines

The LMT85-Q1 is extremely simple to layout. If a power-supply bypass capacitor is used, it should be connected as shown in the *Layout Example*

11.2 Layout Example

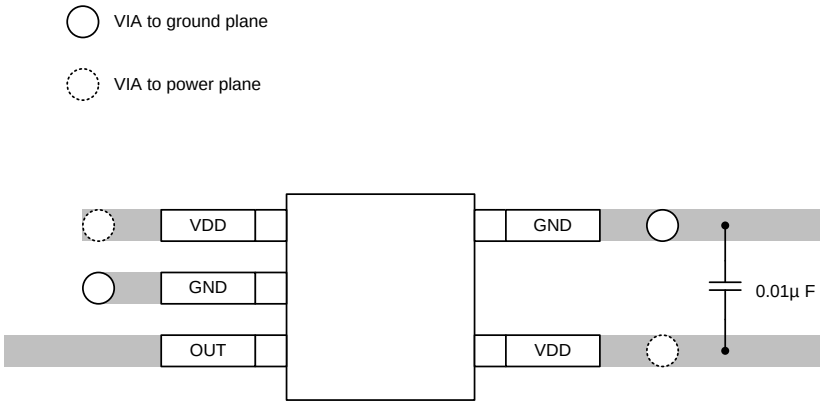

Figure 19. SC70 Package Recommended Layout

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12 デバイスおよびドキュメントのサポート

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMT85QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-50 to 150	BRA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMT85-Q1 :

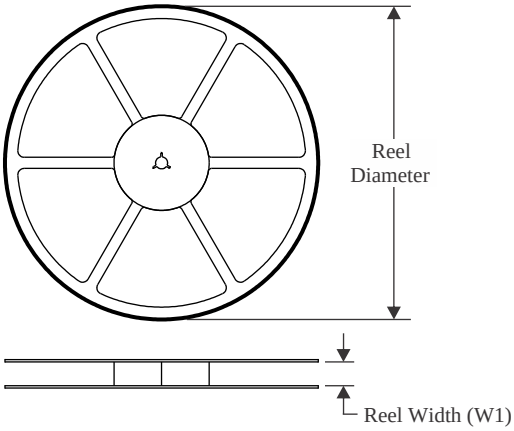
- Catalog : LMT85

NOTE: Qualified Version Definitions:

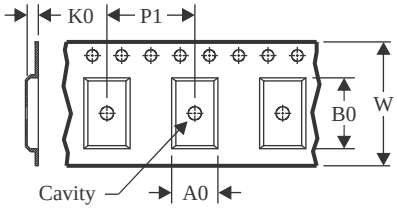
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

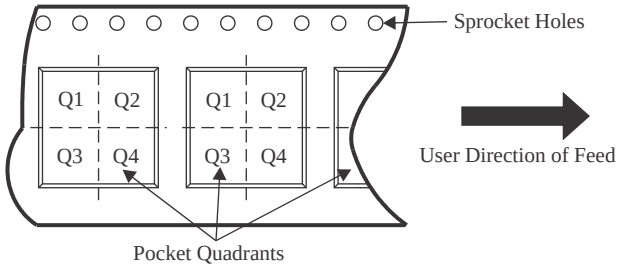


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

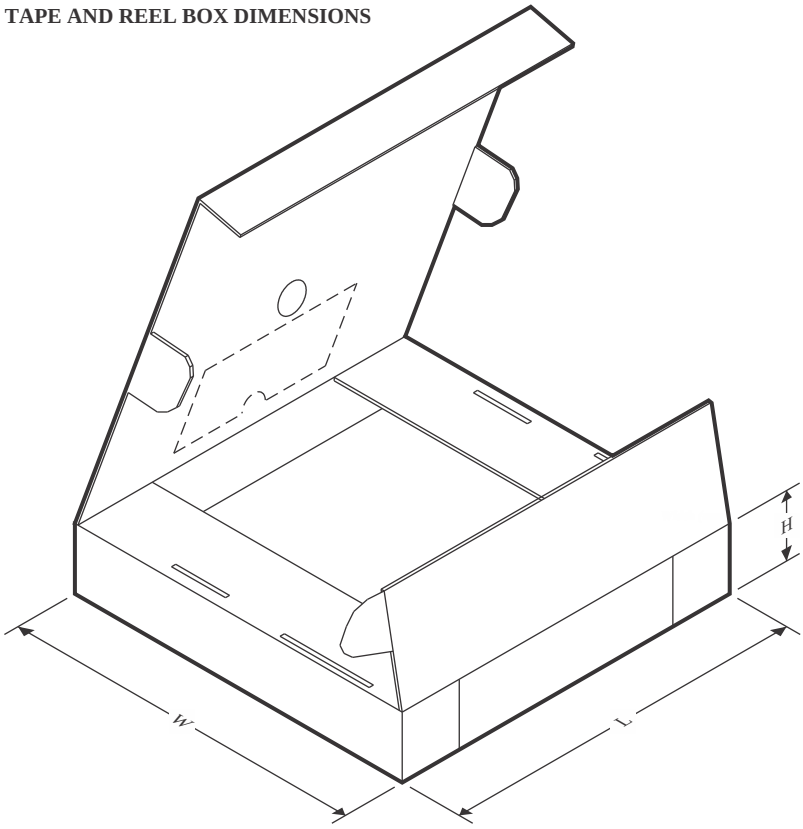
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT85QDCKRQ1	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

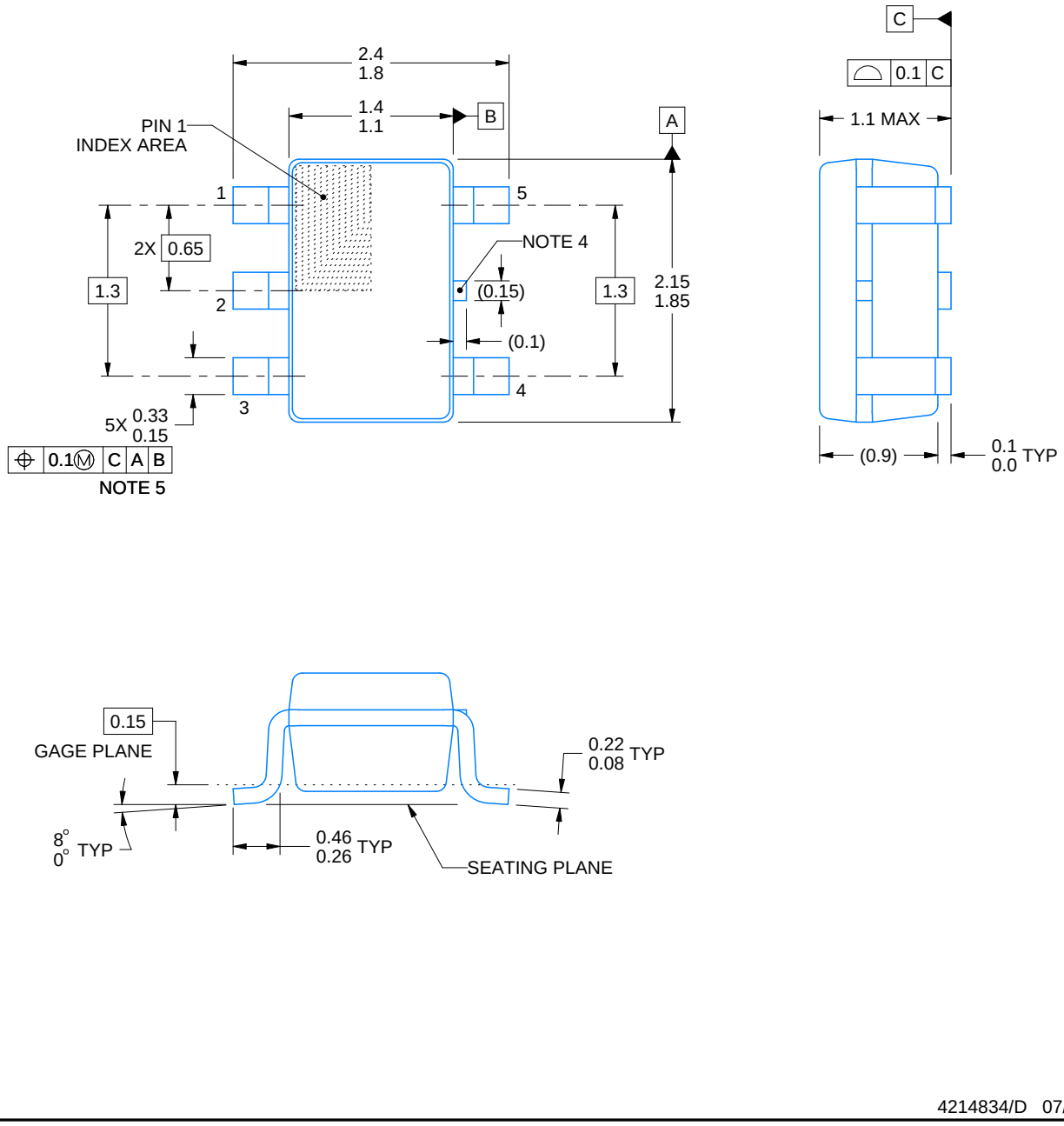
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT85QDCKRQ1	SC70	DCK	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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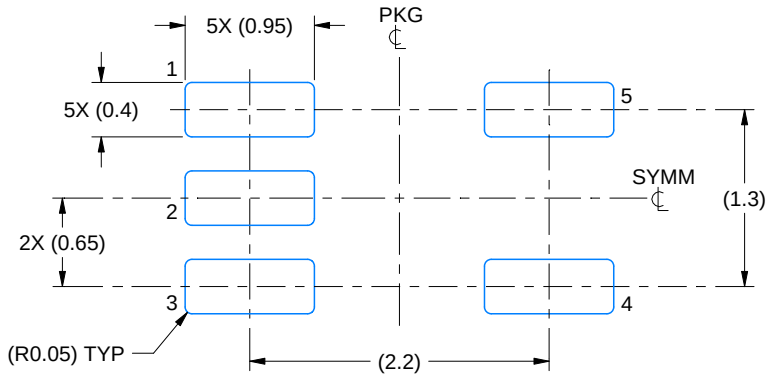
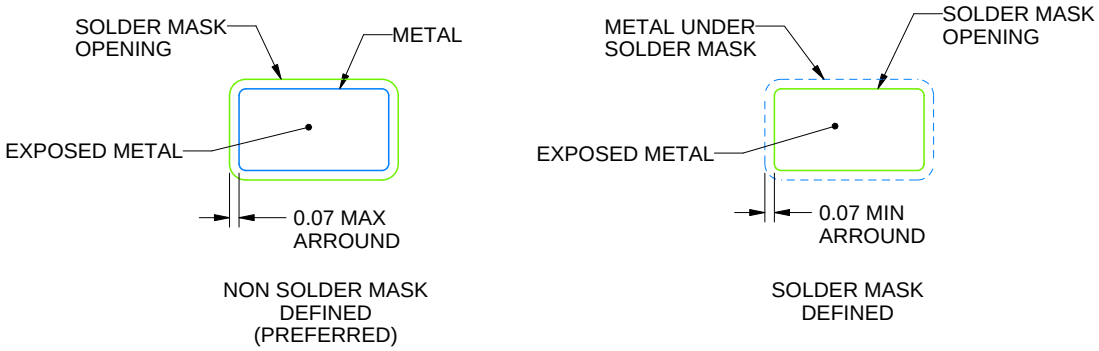
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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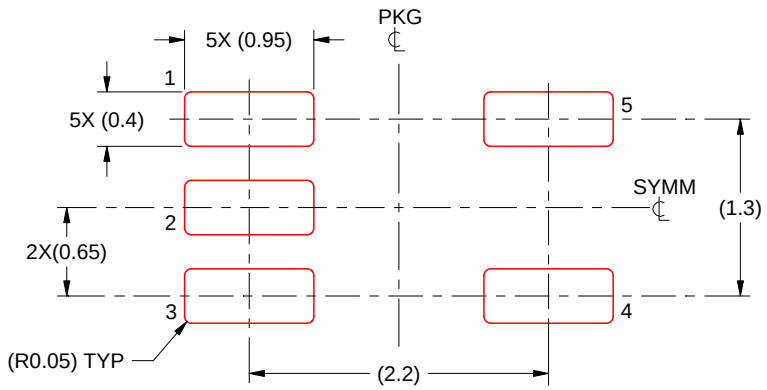
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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