# LMV34x-N シングル、レール・ツー・レール出力、CMOS動作アンプ、シャットダウン機能付き

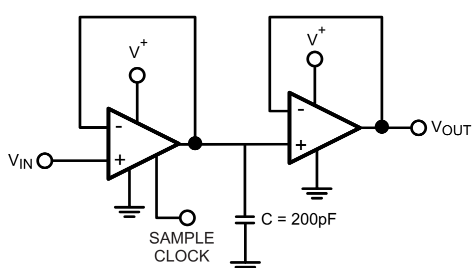
## 1 特長

- (特記のない限り電源電圧2.7V時の標準値)
- 2.7Vおよび5Vの定格
- 10kHzにおける入力換算電圧ノイズ: 29nV/$\sqrt{\text{Hz}}$
- 消費電流(アンプごとに): 100µA
- ゲイン帯域幅積: 1MHz
- スルーレート: 1V/µs
- シャットダウン電流(LMV341-N): 45pA
- シャットダウンからのターンオン時間(LMV341-N): 5µs
- 入力バイアス電流: 20fA

## 2 アプリケーション

- コードレスまたは携帯電話
- ノート PC
- 携帯情報端末
- PCMCIAまたはオーディオ
- 携帯用またはバッテリ駆動の電子機器
- 消費電流の監視
- バッテリ監視
- バッファ
- フィルタ
- ドライバ

**サンプル/ホールド回路**






## 3 概要

LMV34x-Nデバイスは、シングル/デュアル/クワッドの低電圧、低消費電力のオペアンプです。低電圧のポータブル・アプリケーションに特化して設計されています。この製品には、低い入力バイアス電流、レール・ツー・レール出力、広い温度範囲など重要な特長があります。

特許を取得したクラスABターンアラウンド段により、消費電力とオフセット電圧、および高い周波数でのノイズが大幅に低減されています。PMOS入力段により、20fA (標準値)という非常に低い入力バイアス電流と、高い入力インピーダンスを実現しています。

LMV34x-Nは拡張工業用温度範囲である-40℃～125℃で動作するため、広範な拡張環境アプリケーションに対応できます。LMV341-Nは、サイズ、動作速度、省電力の点で、テキサス・インスツルメンツのSilicon Dustアンプのポートフォリオを拡張する製品です。LMV34x-Nデバイスは、2.7V～5.5Vの電圧範囲で動作する定格で、すべての製品がレール・ツー・レール出力を備えています。

LMV341-Nにはシャットダウン・ピンがあり、デバイスをディセーブルするために使用できます。シャットダウン・モードでは、消費電流が45pA (標準値)に低下します。LMV34x-Nデバイスは10kHzで電圧ノイズが29nV、GBWが1MHz、スルーレートが1V/µs、0.25 mVos、シャットダウン電流が0.1µAです(LMV341-N)。

LMV341-Nは小型6ピンSC70パッケージで、LMV342-Nは省スペースの8ピンVSSOPおよびSOICパッケージで、LMV344-Nは14ピンTSSOPおよびSOICパッケージで供給されます。これらの小型パッケージのアンプは、PCB占有面積をできるだけ抑えたいアプリケーションに理想的なソリューションです。PCBの面積が限られているアプリケーションの例として、携帯電話やPDAなどの携帯用電子機器が挙げられます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| LMV341-N | SC70 (6) | 2.00mm×1.25mm |
| LMV342-N | VSSOP (8) | 3.00mm×3.00mm |
| | SOIC (8) | 4.90mm×3.91mm |
| LMV344-N | TSSOP (14) | 5.00mm×4.40mm |
| | SOIC (14) | 8.64mm×3.91mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

# 目次



## 4 改訂履歴

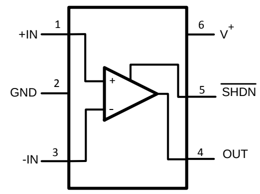
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| **Revision G (March 2013) から Revision H に変更** | **Page** |
|---|---|
| • 「*ESD定格*」の表、「*機能概要*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 | 1 |
| • Changed *Thermal Information* table | 5 |

| **Revision F (March 2012) から Revision G に変更** | **Page** |
|---|---|
| • ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 | 1 |

# 5 Pin Configuration and Functions

**DCK Package**
**6-Pin SC70**
**Top View**

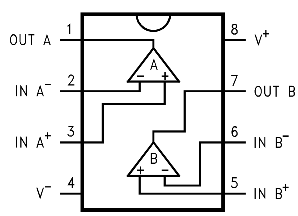



**Pin Functions – LMV341-N**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN | 1 | I | Noninverting input |
| –IN | 3 | I | Inverting input |
| GND | 2 | P | Negative supply input |
| OUT | 4 | O | Output |
| $V^+$ | 6 | P | Positive supply input |
| $\overline{\text{SHDN}}$ | 5 | I | Active low enable input |

(1) I = Input, O = Output, and P = Power

**DGK or D Package**
**8-Pin VSSOP or SOIC**
**Top View**

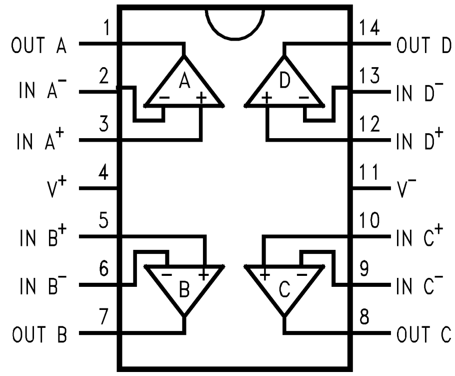



**Pin Functions – LMV342-N**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN $A^+$ | 3 | I | Noninverting input, channel A |
| IN $A^–$ | 2 | I | Inverting input, channel A |
| IN $B^+$ | 5 | I | Noninverting input, channel B |
| IN $B^–$ | 6 | I | Inverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| $V^+$ | 8 | P | Positive (highest) power supply |
| $V^–$ | 4 | P | Negative (lowest) power supply |

(1) I = Input, O = Output, and P = Power

**PW or D Package**
**14-Pin TSSOP or SOIC**
**Top View**




## Pin Functions – LMV344-N

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN A+ | 3 | I | Noninverting input, channel A |
| IN A– | 2 | I | Inverting input, channel A |
| IN B+ | 5 | I | Noninverting input, channel B |
| IN B– | 6 | I | Inverting input, channel B |
| IN C+ | 10 | I | Noninverting input, channel C |
| IN C– | 9 | I | Inverting input, channel C |
| IN D+ | 12 | I | Noninverting input, channel D |
| IN D– | 13 | I | Inverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V+ | 4 | P | Positive (highest) power supply |
| V– | 11 | P | Negative (lowest) power supply |

(1) I = Input, O = Output, and P = Power

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Differential input voltage | | ±Supply voltage | | |
| Supply voltage ($V^+ – V^−$) | | | 6 | V |
| Output short circuit to $V^+$ | | See(3) | | |
| Output short circuit to $V^−$ | | See(4) | | |
| Lead temperature | Infrared or convection reflow (20 s) | | 235 | °C |
| | Wave soldering (10 s) | | 260 | |
| Junction temperature, $T_J$(5) | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Shorting output to $V^+$ will adversely affect reliability.
(4) Shorting output to $V^-$ will adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM)(1) | ±2000 | V |
| | | Machine model (MM)(2) | ±200 | |

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage | 2.7 | 5.5 | V |
| Temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LMV341-N | LMV342-N | | LMV344-N | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DCK (SC70) | D (SOIC) | DGK (VSSOP) | D (SOIC) | PW (TSSOP) | |
| | | 6 PINS | 8 PINS | 8 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 414 | 190 | 235 | 145 | 155 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 116.1 | 65.2 | 68.4 | 45.9 | 50.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.3 | 61.4 | 98.8 | 44.1 | 66.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.8 | 16.1 | 9.8 | 10.2 | 6.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.7 | 60.8 | 97.3 | 43.7 | 65.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics – 2.7 V (DC)

$T_J$ = 25°C, $V^+$ = 2.7 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$/ 2, $V_O$ = $V^+$/ 2, and $R_L$ > 1 MΩ (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | LMV341-N | $T_J$ = 25°C | | 0.25 | 4 | mV |
| | | | −40°C ≤ $T_J$ ≤ 125°C | | | 4.5 | |
| | | LMV342-N and LMV344-N | $T_J$ = 25°C | | 0.55 | 5 | |
| | | | −40°C ≤ $T_J$ ≤ 125°C | | | 5.5 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 1.7 | | µV/°C |
| $I_B$ | Input bias current | $T_J$ = 25°C | | | 0.02 | 120 | pA |
| | | -40°C ≤ $T_J$ ≤ 150°C | | | | 250 | |
| $I_{OS}$ | Input offset current | | | | 6.6 | | fA |
| $I_S$ | Supply current | Per amplifier | $T_J$ = 25°C | | 100 | 170 | µA |
| | | | −40°C ≤ $T_J$ ≤ 125°C | | | 230 | |
| | | Shutdown mode, $V_{SD}$ = 0 V, LMV341-N | $T_J$ = 25°C | | $4.5 \times 10^{-5}$ | 1 | |
| | | | −40°C ≤ $T_J$ ≤ 125°C | | | 1.5 | |
| CMRR | Common-mode rejection ratio | 0 V ≤ $V_{CM}$ ≤ 1.7 V, 0 V ≤ $V_{CM}$ ≤ 1.6 V | $T_J$ = 25°C | 56 | 80 | | dB |
| | | | −40°C ≤ $T_J$ ≤ 125°C | 50 | | | |
| PSRR | Power supply rejection ratio | 2.7 V ≤ $V^+$ ≤ 5 V | $T_J$ = 25°C | 65 | 82 | | dB |
| | | | −40°C ≤ $T_J$ ≤ 125°C | 60 | | | |
| $V_{CM}$ | Input common-mode voltage | For CMRR ≥ 50 dB | V+ | | 1.9 | 1.7 | V |
| | | | V– | 0 | −0.2 | | |
| $A_V$ | Large signal voltage gain | $R_L$ = 10 kΩ to 1.35 V | $T_J$ = 25°C | 78 | 113 | | dB |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 70 | | | |
| | | $R_L$ = 2 kΩ to 1.35 V | $T_J$ = 25°C | 72 | 103 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 64 | | | |
| $V_O$ | Output swing | $R_L$ = 2 kΩ to 1.35 V | $T_J$ = 25°C | | 24 | 60 | mV |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 95 | |
| | | | $T_J$ = 25°C | 60 | 26 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 95 | | | |
| | | $R_L$ = 10 kΩ to 1.35 V | $T_J$ = 25°C | | 5 | 30 | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 40 | |
| | | | $T_J$ = 25°C | 30 | 5.3 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 40 | | | |
| $I_O$ | Output short-circuit current | Sourcing, LMV341-N and LMV342-N | | 20 | 32 | | mA |
| | | Sourcing, LMV344-N | | 18 | 24 | | |
| | | Sinking | | 15 | 24 | | |
| $t_{on}$ | Turnon time from shutdown | LMV341-N | | | 5 | | µs |
| $V_{SD}$ | Shutdown pin voltage | ON mode, LMV341-N | | 2.4 | 1.7 | 2.7 | V |
| | | Shutdown mode, LMV341-N | | 0 | 1 | 0.8 | |

(1) Electrical characteristic values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

## 6.6 Electrical Characteristics – 2.7 V (AC)

$T_J$ = 25°C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = $V^+$/ 2, $V_O$ = $V^+$/ 2, and $R_L$ > 1 MΩ (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|
| SR | Slew rate | $R_L$ = 10 kΩ[4] | | 1 | | V/µs |
| GBW | Gain bandwidth product | $R_L$ = 100 kΩ, $C_L$ = 200 pF | | 1 | | MHz |
| $\Phi_m$ | Phase margin | $R_L$ = 100 kΩ | | 72 | | ° |
| $G_m$ | Gain margin | $R_L$ = 100 kΩ | | 20 | | dB |
| $e_n$ | Input-referred voltage noise | f = 1 kHz | | 40 | | nV/√Hz |
| $i_n$ | Input-referred current noise | f = 1 kHz | | 0.001 | | pA/√Hz |
| THD | Total harmonic distortion | f = 1 kHz, $A_V$ = +1, $R_L$ = 600 Ω, $V_{IN}$ = $1V_{PP}$ | | 0.017% | | |

(1) Electrical characteristic values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with 2-$V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

## 6.7 Electrical Characteristics – 5 V (DC)

$T_J$ = 25°C, $V^+$ = 5 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$/ 2, $V_O$ = $V^+$/ 2, and $R_L$ > 1 MΩ (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | LMV341-N | $T_J$ = 25°C | | 0.025 | 4 | mV |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 4.5 | |
| | | LMV342-N and LMV344-N | $T_J$ = 25°C | | 0.7 | 5 | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 5.5 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 1.9 | | µV/°C |
| $I_B$ | Input bias current | $T_J$ = 25°C | | | 0.02 | 200 | pA |
| | | –40°C ≤ $T_J$ ≤ 125°C | | | | 375 | |
| $I_{OS}$ | Input offset current | | | | 6.6 | | fA |
| $I_S$ | Supply current | Per amplifier | $T_J$ = 25°C | | 107 | 200 | µA |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 260 | |
| | | Shutdown mode, $V_{SD}$ = 0 V, LMV341-N | $T_J$ = 25°C | | 0.033 | 1 | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 1.5 | |
| CMRR | Common-mode rejection ratio | 0 V ≤ $V_{CM}$ ≤ 4 V, 0 V ≤ $V_{CM}$ ≤ 3.9 V | $T_J$ = 25°C | 56 | 86 | | dB |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 50 | | | |
| PSRR | Power supply rejection ratio | 2.7 V ≤ $V^+$ ≤ 5 V | $T_J$ = 25°C | 65 | 82 | | dB |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 60 | | | |
| $V_{CM}$ | Input common-mode voltage | For CMRR ≥ 50 dB | V+ | | 4.2 | 4 | V |
| | | | V– | 0 | −0.2 | | |
| $A_V$ | Large signal voltage gain[4] | $R_L$ = 10 kΩ to 2.5 V | $T_J$ = 25°C | 78 | 116 | | dB |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 70 | | | |
| | | $R_L$ = 2 kΩ to 2.5 V | $T_J$ = 25°C | 72 | 107 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 64 | | | |

(1) Electrical characteristic values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) $R_L$ is connected to mid-supply. The output voltage is GND + 0.2 V ≤ $V_O$ ≤ $V^+$– 0.2 V

## Electrical Characteristics – 5 V (DC) (continued)

$T_J$ = 25°C, $V^+$ = 5 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$/ 2, $V_O$ = $V^+$/ 2, and $R_L$ > 1 MΩ (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output swing | $R_L$ = 2 kΩ to 2.5 V | $T_J$ = 25°C | | 32 | 60 | mV |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 95 | |
| | | | $T_J$ = 25°C | 60 | 34 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 95 | | | |
| | | $R_L$ = 10 kΩ to 2.5 V | $T_J$ = 25°C | | 7 | 30 | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 40 | |
| | | | $T_J$ = 25°C | 30 | 7 | | |
| | | | –40°C ≤ $T_J$ ≤ 125°C | 40 | | | |
| $I_O$ | Output short-circuit current | Sourcing | | 85 | 113 | | mA |
| | | Sinking | | 50 | 75 | | |
| $t_{on}$ | Turnon time from shutdown | LMV341-N | | | 5 | | µs |
| $V_{SD}$ | Shutdown pin voltage | ON mode, LMV341-N | | 4.5 | 3.1 | 5 | V |
| | | Shutdown mode, LMV341-N | | 0 | 1 | 0.8 | |

## 6.8 Electrical Characteristics – 5 V (AC)

$T_J$ = 25°C, $V^+$ = 5 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$/ 2, $V_O$ = $V^+$/ 2 and $R_L$ > 1 MΩ (unless otherwise noted)(1)

| PARAMETER | | CONDITIONS | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|
| SR | Slew rate | $R_L$ = 10 kΩ(4) | | 1 | | V/µs |
| GBW | Gain-bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 200 pF | | 1 | | MHz |
| $\Phi_m$ | Phase margin | $R_L$ = 100 kΩ | | 70 | | deg |
| $G_m$ | Gain margin | $R_L$ = 100 kΩ | | 20 | | dB |
| $e_n$ | Input-referred voltage noise | f = 1 kHz | | 39 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input-referred current noise | f = 1 kHz | | 0.001 | | $pA/\sqrt{Hz}$ |
| THD | Total harmonic distortion | f = 1 kHz, $A_V$ = +1, $R_L$ = 600 Ω, $V_{IN}$ = 1$V_{PP}$ | | 0.012% | | |

(1) Electrical characteristic values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with 2-$V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

## 6.9 Typical Characteristics

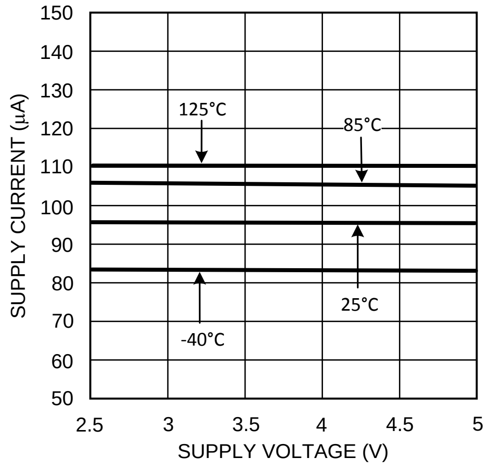



**Figure 1. Supply Current vs Supply Voltage (LMV341-N)**

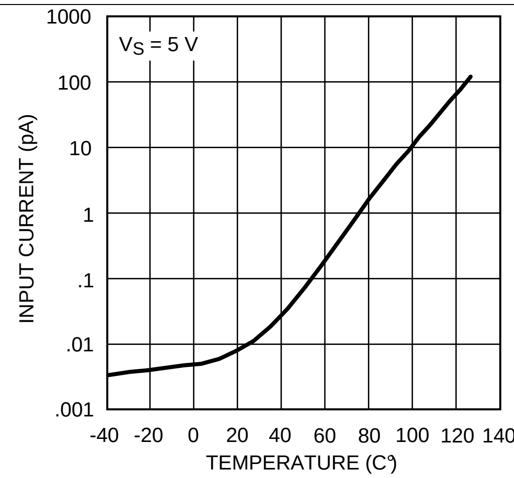



**Figure 2. Input Current vs Temperature**

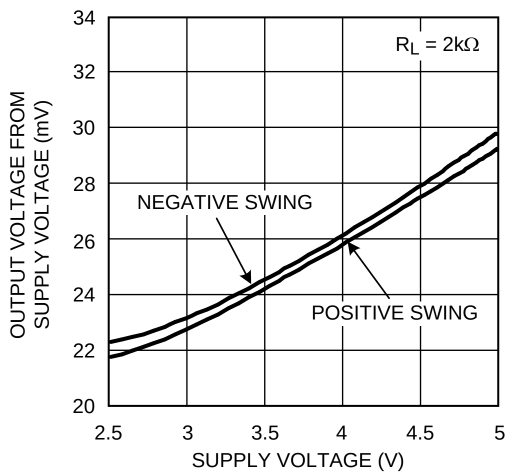



**Figure 3. Output Voltage Swing vs Supply Voltage**

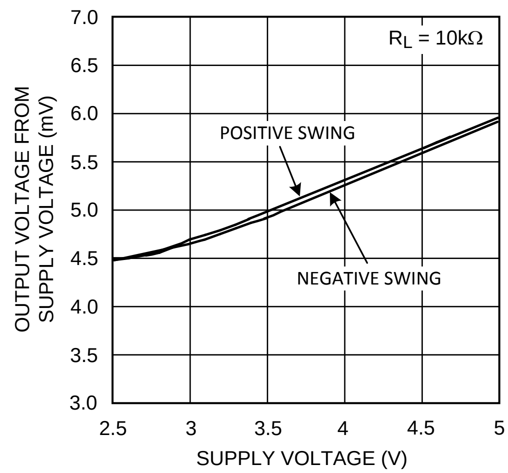



**Figure 4. Output Voltage Swing vs Supply Voltage**

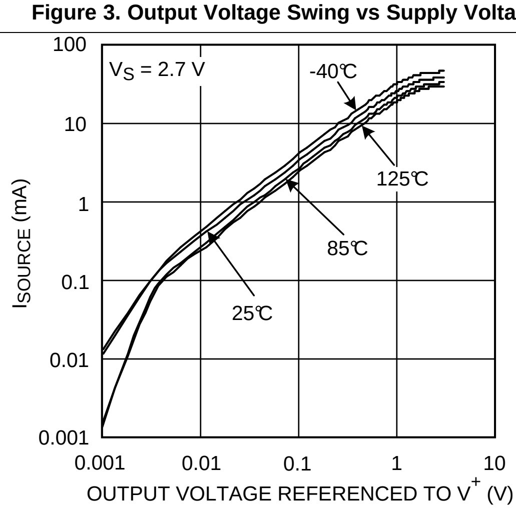



**Figure 5. $I_{SOURCE}$ vs $V_{OUT}$**

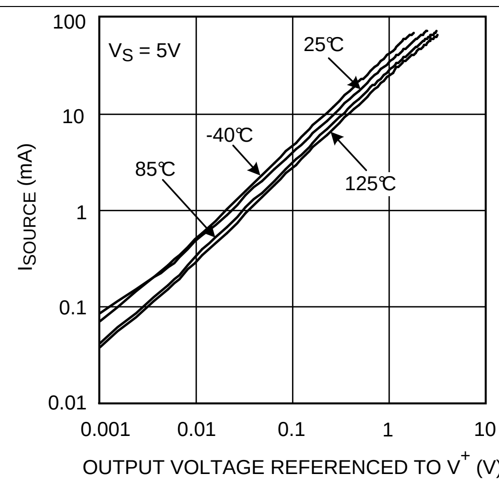



**Figure 6. $I_{SOURCE}$ vs $V_{OUT}$**

## Typical Characteristics (continued)

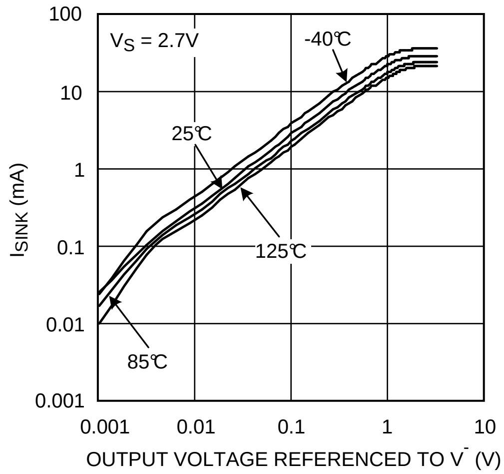



**Figure 7. $I_{SINK}$ vs $V_{OUT}$**

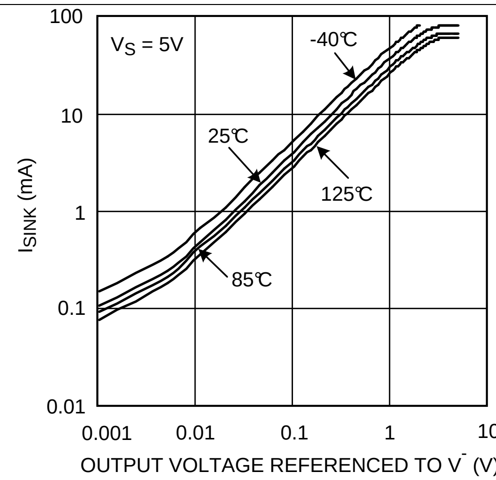



**Figure 8. $I_{SINK}$ vs $V_{OUT}$**

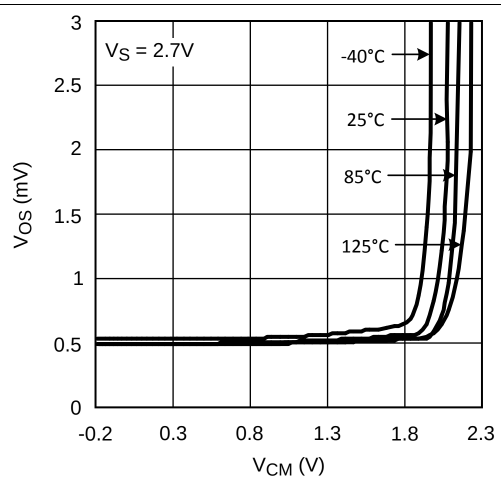



**Figure 9. $V_{OS}$ vs $V_{CM}$**

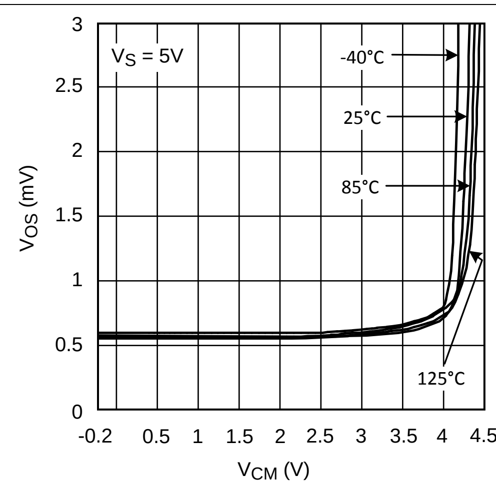



**Figure 10. $V_{OS}$ vs $V_{CM}$**

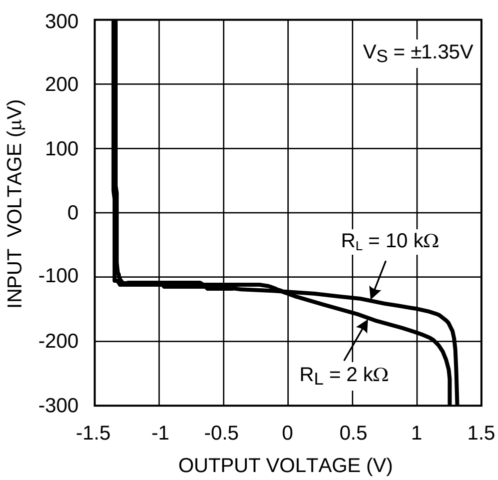



**Figure 11. $V_{IN}$ vs $V_{OUT}$**

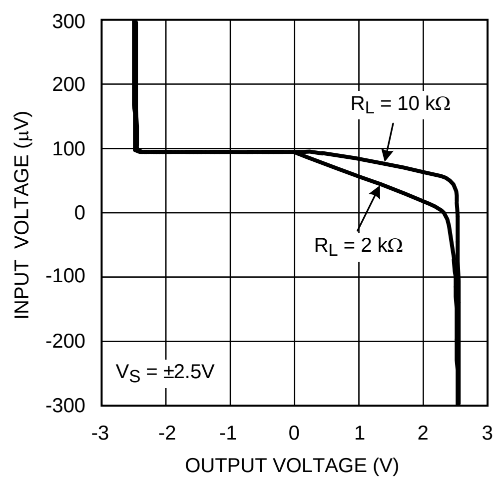



**Figure 12. $V_{IN}$ vs $V_{OUT}$**

## Typical Characteristics (continued)

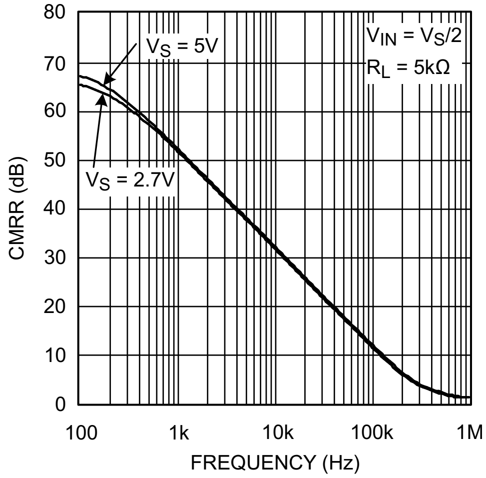



**Figure 13. CMRR vs Frequency**

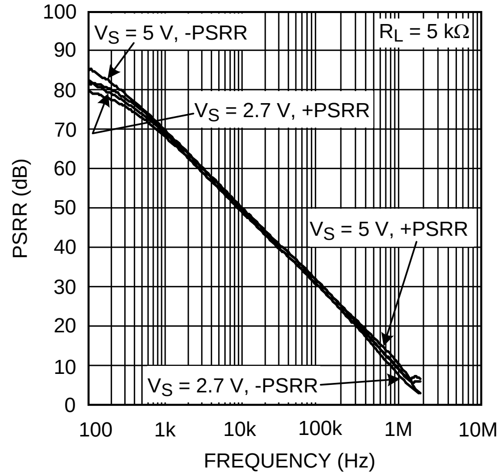



**Figure 14. PSRR vs Frequency**

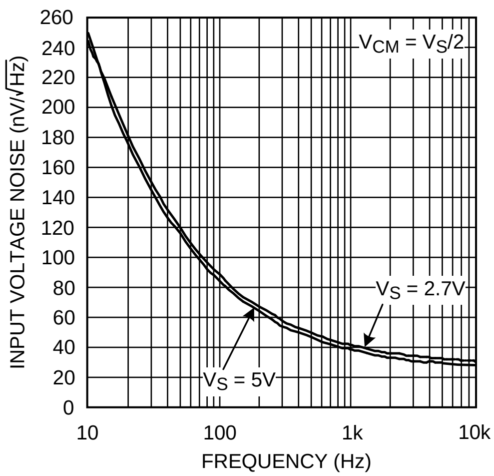



**Figure 15. Input Voltage Noise vs Frequency**

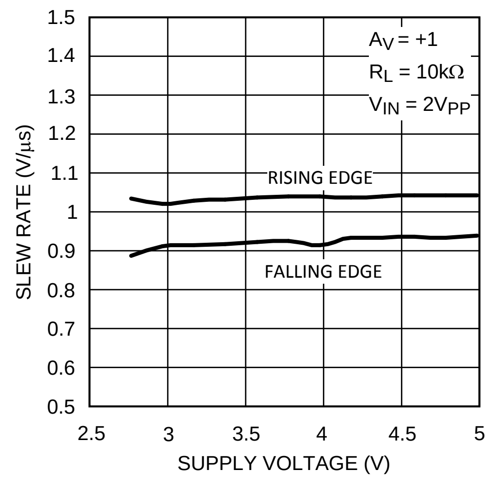



**Figure 16. Slew Rate vs $V_{SUPPLY}$**

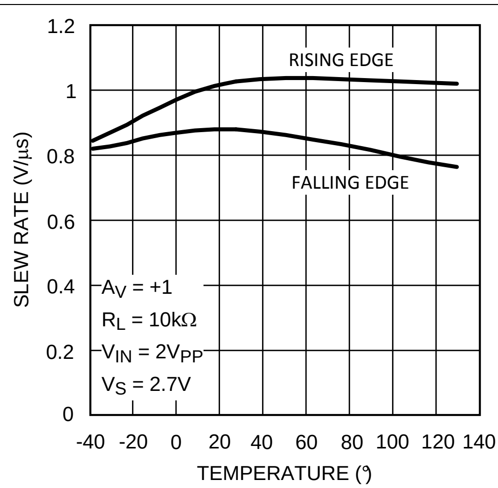



**Figure 17. Slew Rate vs Temperature**

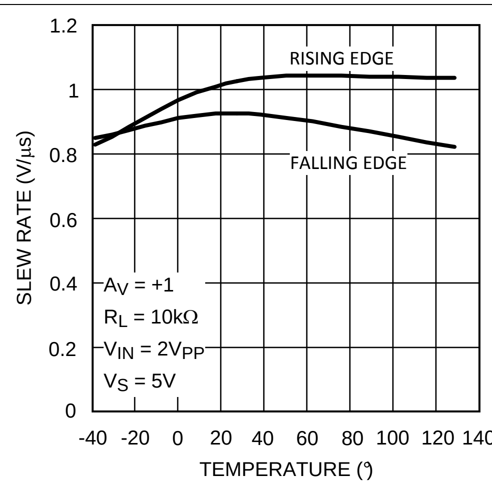



**Figure 18. Slew Rate vs Temperature**

## Typical Characteristics (continued)

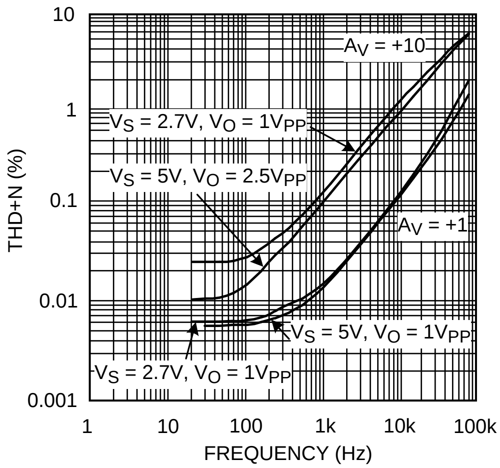



**Figure 19. THD+N vs Frequency**

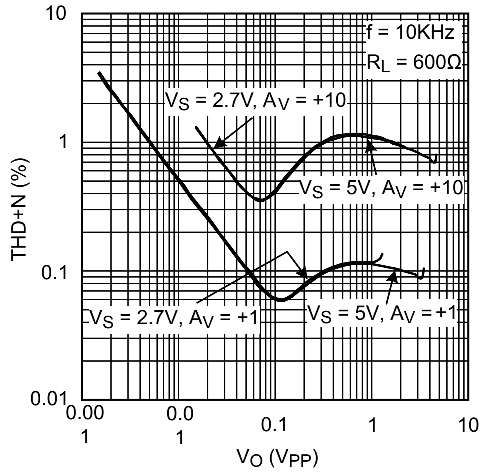



**Figure 20. THD+N vs $V_{OUT}$**

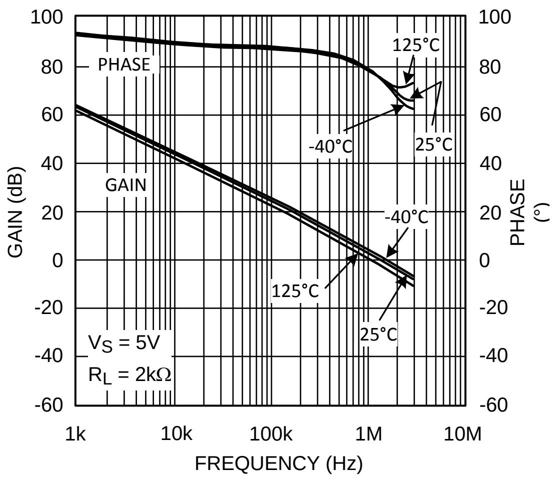



**Figure 21. Open-Loop Frequency Over Temperature**

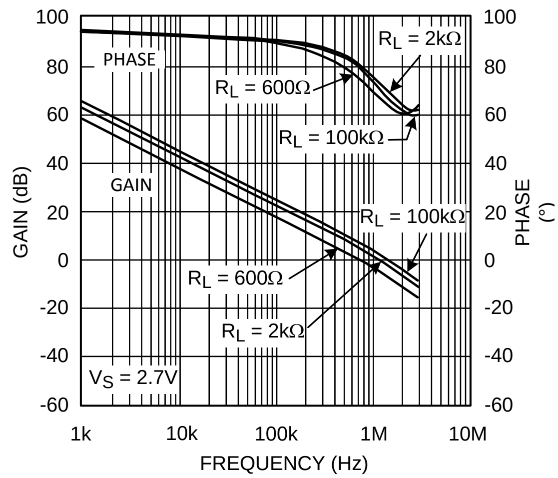



**Figure 22. Open-Loop Frequency Response**

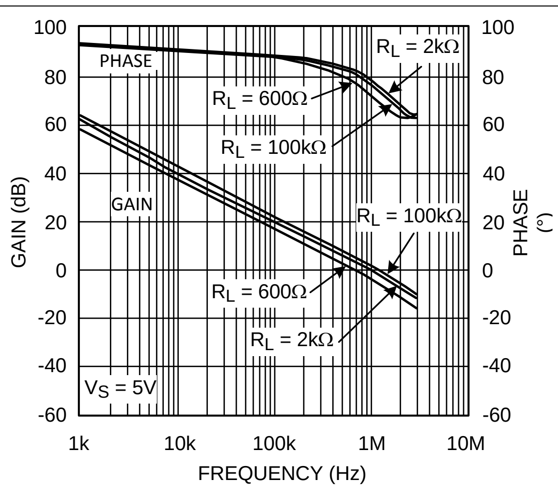



**Figure 23. Open-Loop Frequency Response**

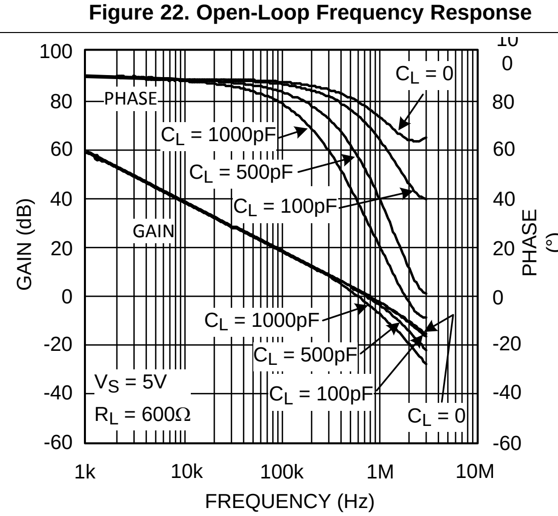



**Figure 24. Gain and Phase vs $C_L$**

## Typical Characteristics (continued)

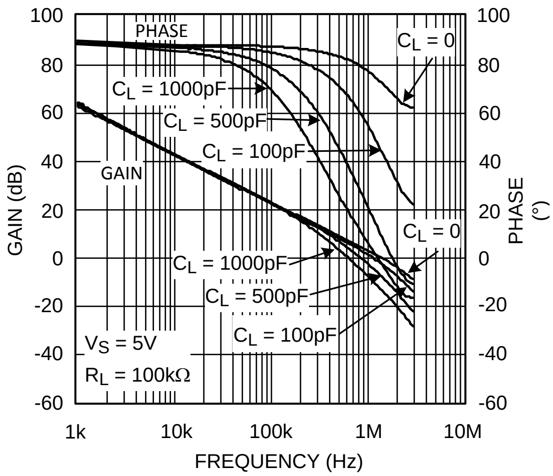



**Figure 25. Gain and Phase vs $C_L$**

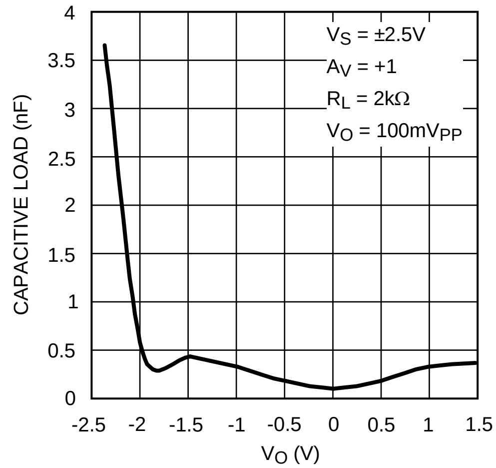



**Figure 26. Stability vs Capacitive Load**

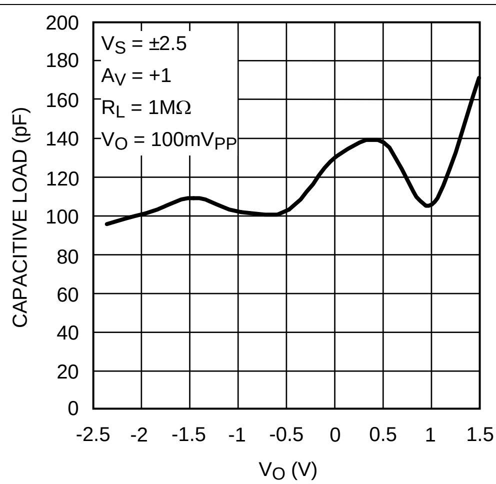



**Figure 27. Stability vs Capacitive Load**

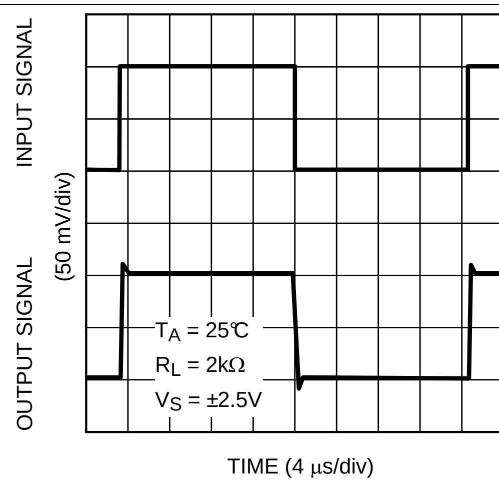



**Figure 28. Noninverting Small Signal Pulse Response**

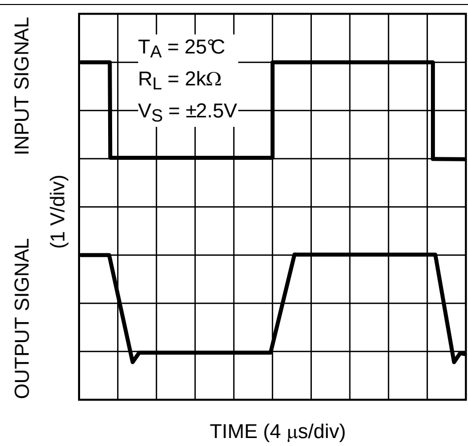



**Figure 29. Noninverting Large Signal Pulse Response**

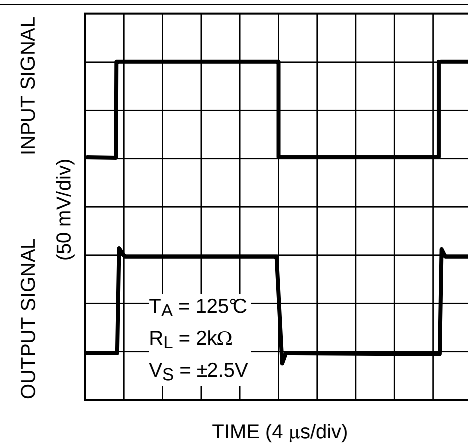



**Figure 30. Noninverting Small Signal Pulse Response**

## Typical Characteristics (continued)

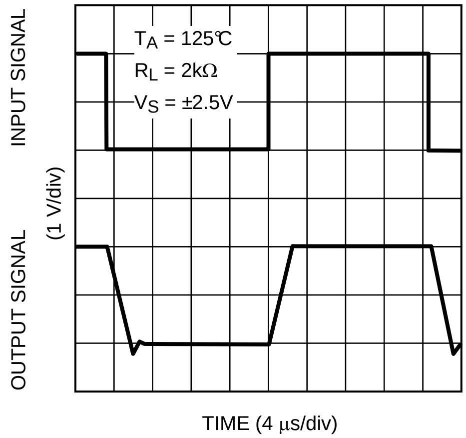



**Figure 31. Noninverting Large Signal Pulse Response**

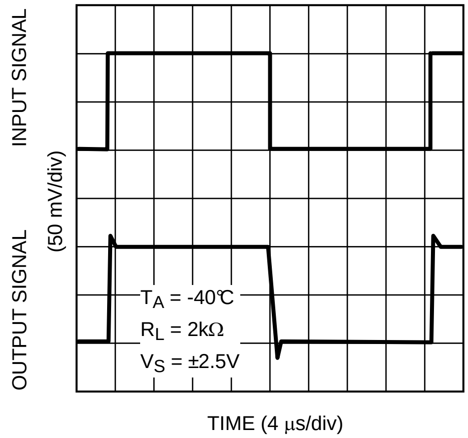



**Figure 32. Noninverting Small Signal Pulse Response**

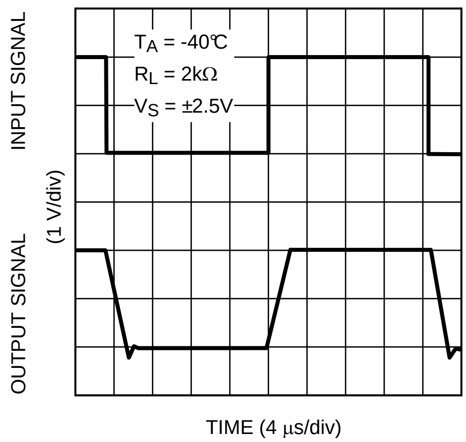



**Figure 33. Noninverting Large Signal Pulse Response**

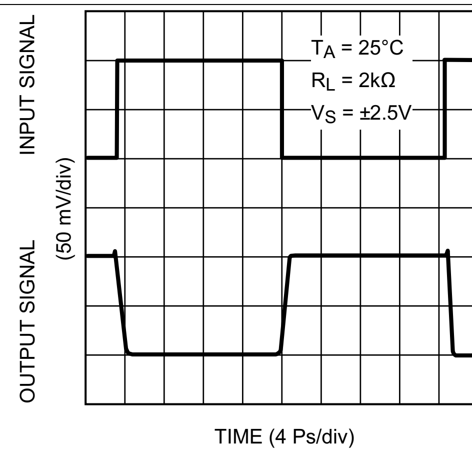



**Figure 34. Inverting Small Signal Pulse Response**

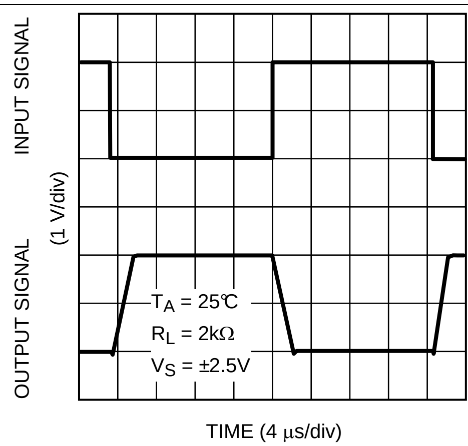



**Figure 35. Inverting Large Signal Pulse Response**

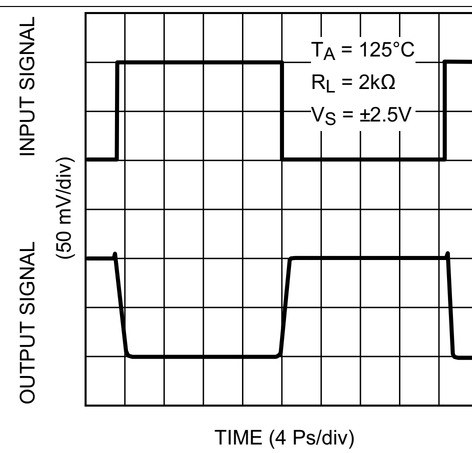



**Figure 36. Inverting Small Signal Pulse Response**

## Typical Characteristics (continued)

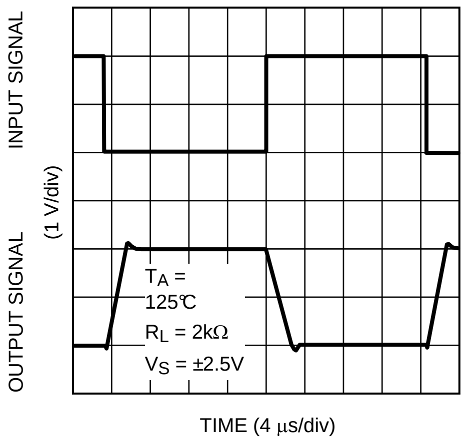



**Figure 37. Inverting Large Signal Pulse Response**

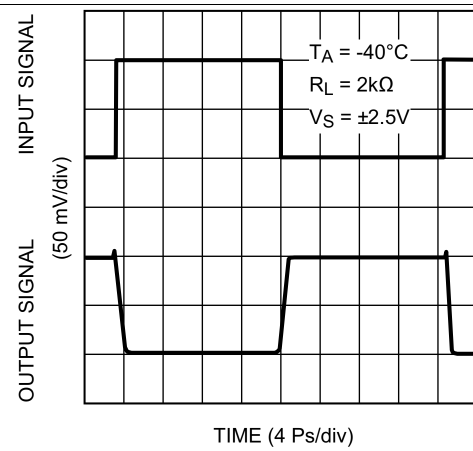



**Figure 38. Inverting Small Signal Pulse Response**

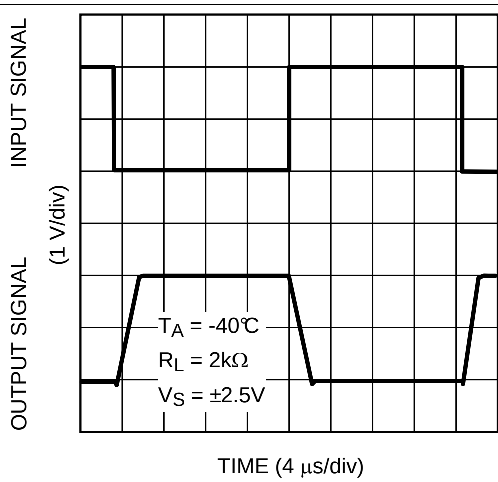



**Figure 39. Inverting Large Signal Pulse Response**

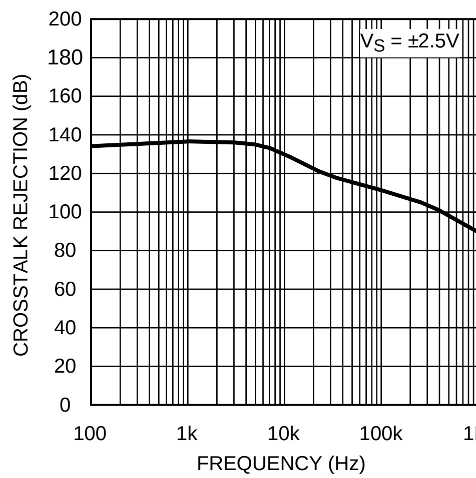


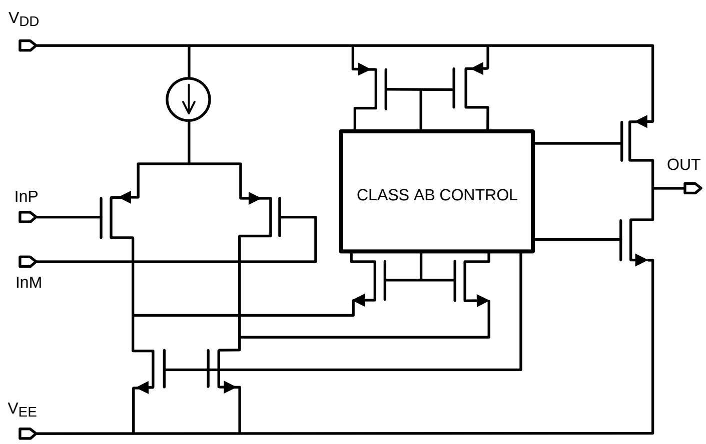

**Figure 40. Crosstalk Rejection vs Frequency**

# 7 Detailed Description

## 7.1 Overview

TI's LMV34x-N family of amplifiers have 1-MHz bandwidth, 1-V/µs slew rate, a rail-to-rail output stage, and consume only 100 µA of current per amplifier while active. When in shutdown mode it only consumes 45-pA supply consumption with only 20 fA of input bias current. Lastly, these operational amplifiers provide an input-referred voltage noise 29 nV√Hz (at 10 kHz).

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Class AB Turnaround Stage Amplifier

This patented folded cascode stage has a combined class AB amplifier stage, which replaces the conventional folded cascode stage. Therefore, the class AB folded cascode stage runs at a much lower quiescent current compared to conventional-folded cascode stages. This results in significantly smaller offset and noise contributions. The reduced offset and noise contributions in turn reduce the offset voltage level and the voltage noise level at the input of LMV34x-N. Also the lower quiescent current results in a high open-loop gain for the amplifier. The lower quiescent current does not affect the slew rate of the amplifier nor its ability to handle the total current swing coming from the input stage.

The input voltage noise of the device at low frequencies, below 1 kHz, is slightly higher than devices with a BJT input stage; however, the PMOS input stage results in a much lower input bias current and the input voltage noise drops at frequencies above 1 kHz.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Feature

The LMV341-N is capable of being turned off to conserve power and increase battery life in portable devices. Once in shutdown mode the supply current is drastically reduced, 1-µA maximum, and the output is *tri-stated*.

The device is disabled when the shutdown pin voltage is pulled low. The shutdown pin must never be left unconnected. Leaving the pin floating results in an undefined operation mode and the device may oscillate between shutdown and active modes.

The LMV341-N typically turns on 2.8 µs after the shutdown voltage is pulled high. The device turns off in less than 400 ns after shutdown voltage is pulled low. Figure 41 and Figure 42 show the turnon and turnoff time of the LMV341-N, respectively. To reduce the effect of the capacitance added to the circuit by the scope probe, in the turnoff time circuit a resistive load of 600 Ω is added. Figure 43 and Figure 44 show the test circuits used to obtain the two plots.

## Device Functional Modes (continued)

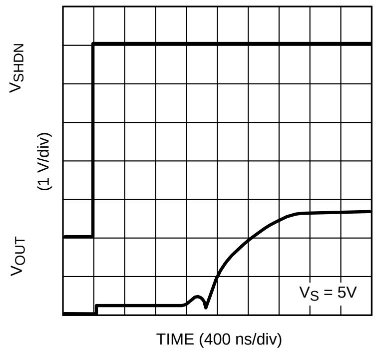


**Figure 41. Turnon Time Plot**

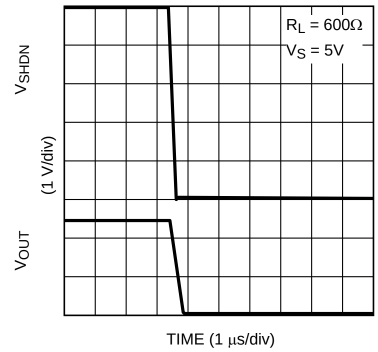


**Figure 42. Turnoff Time Plot**

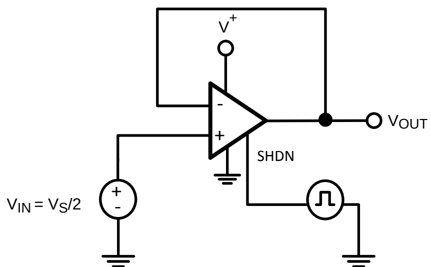


**Figure 43. Turnon Time Circuit**

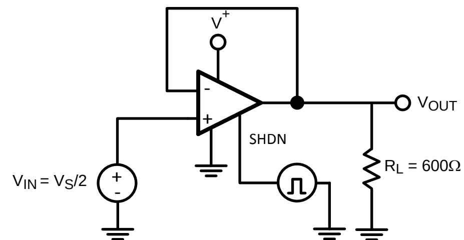


**Figure 44. Turnoff Time Circuit**

### 7.4.2 Low Input Bias Current

LMV34x-N amplifiers have a PMOS input stage. As a result, they have a much lower input bias current than devices with BJT input stages. This feature makes these devices ideal for sensor circuits. A typical curve of the input bias current of the LMV341-N is shown in Figure 45.

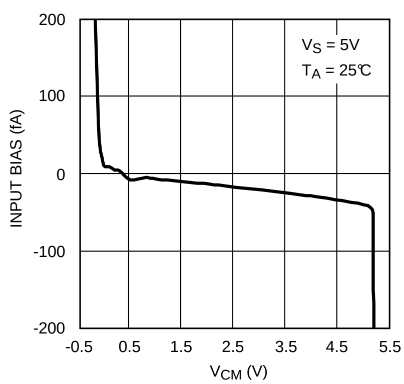


**Figure 45. Input Bias Current vs $V_{CM}$**

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LMV34x-N amplifier family features low voltage, low power, rail-to-rail output as well as a shutdown capability, making it well suited for low voltage portable applications.

## 8.2 Typical Application

### 8.2.1 Sample and Hold Circuit

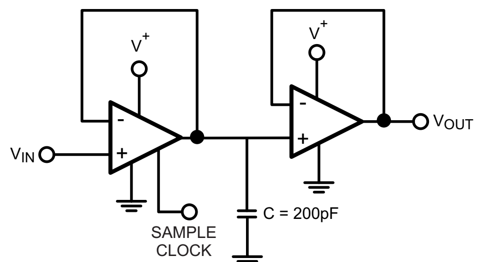


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**Figure 46. Sample and Hold Circuit**

#### *8.2.1.1 Design Requirements*

The lower input bias current of the LMV341-N results in a very high input impedance. The output impedance when the device is in shutdown mode is quite high. These high impedances, along with the ability of the shutdown pin to be derived from a separate power source, make LMV341-N a good choice for sample and hold circuits. The sample clock must be connected to the shutdown pin of the amplifier to rapidly turn the device on or off.

#### *8.2.1.2 Detailed Design Procedure*

Figure 46 shows the schematic of a simple sample and hold circuit. When the sample clock is high the first amplifier is in normal operation mode and the second amplifier acts as a buffer. The capacitor, which appears as a load on the first amplifier, is charging at this time. The voltage across the capacitor is that of the noninverting input of the first amplifier because it is connected as a voltage-follower. When the sample clock is low the first amplifier is shut off, bringing the output impedance to a high value. The high impedance of this output, along with the very high impedance on the input of the second amplifier, prevents the capacitor from discharging. There is very little voltage droop while the first amplifier is in shutdown mode. The second amplifier, which is still in normal operation mode and is connected as a voltage follower, also provides the voltage sampled on the capacitor at its output.

## Typical Application (continued)

### *8.2.1.3 Application Curve*

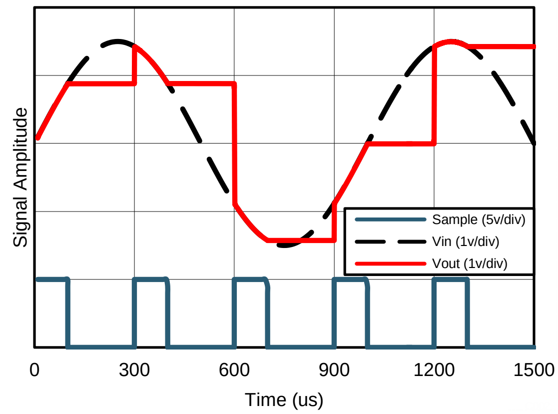


**Figure 47. Sample and Hold Circuit Results**

## 9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between $V^+$ and $V^-$ supply leads. For dual supplies, place one capacitor between $V^+$ and ground, and one capacitor between $V^-$ and ground.

# 10 Layout

## 10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed-circuit board need to be considered. A 6.8-µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the $V^+$ pin needs to be bypassed with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both $V^+$ and $V^-$ pins need to be bypassed.

It is good practice to use a ground plane on a printed-circuit board to provide all components with a low inductive ground connection.

Surface-mount components in 0805 size or smaller are recommended in the LMV341-N application circuits. Designers can take advantage of the VSSOP miniature sizes to condense board layout to save space and reduce stray capacitance.

## 10.2 Layout Example

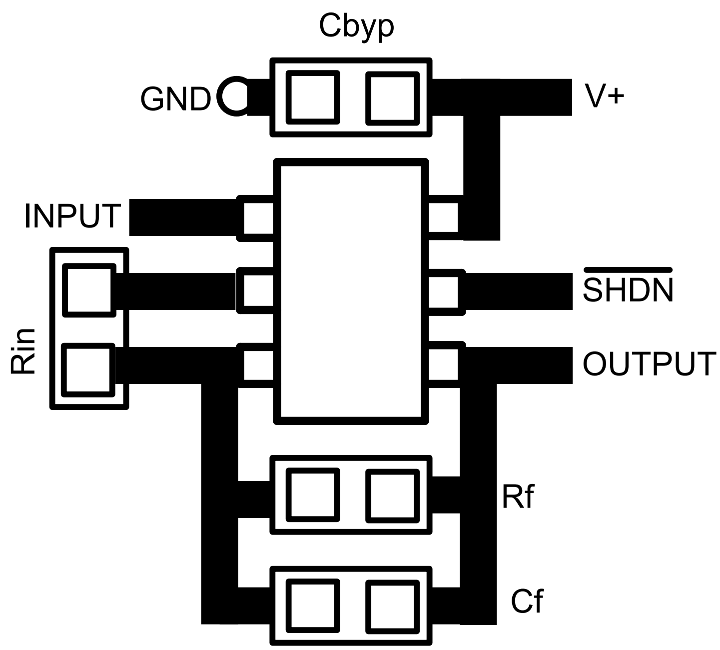


**Figure 48. PCB Layout Example**

# 11 デバイスおよびドキュメントのサポート

## 11.1 デバイス・サポート

### 11.1.1 開発サポート

開発サポートについては、以下を参照してください。

- LMV341-N PSPICEモデル(LMV342およびLMV344にも適用可能です)
- TINA-TI SPICEベースのアナログ・シミュレーション・プログラム
- DIP アダプタ評価モジュール
- TIユニバーサル・オペアンプ評価モジュール
- TI Filterproソフトウェア

## 11.2 ドキュメントのサポート

### 11.2.1 関連資料

関連資料については、以下を参照してください。

*『AN-31オペアンプ回路コレクション』*(SNLA140)

## 11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

**表 1. 関連リンク**

| 製品 | プロダクト・フォルダ | サンプルとご購入 | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|---|---|---|---|---|---|
| LMV341-N | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| LMV342-N | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| LMV344-N | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

## 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.6 商標

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## 11.7 静電気放電に関する注意事項

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### 11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV341MG/NOPB | ACTIVE | SC70 | DCK | 6 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | A78 | Samples |
| LMV341MGX/NOPB | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | A78 | Samples |
| LMV342MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMV34 2MA | Samples |
| LMV342MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMV34 2MA | Samples |
| LMV342MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | A82A | Samples |
| LMV342MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | A82A | Samples |
| LMV344MA/NOPB | ACTIVE | SOIC | D | 14 | 55 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMV344MA | Samples |
| LMV344MAX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMV344MA | Samples |
| LMV344MT/NOPB | ACTIVE | TSSOP | PW | 14 | 94 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LMV34 4MT | Samples |
| LMV344MTX/NOPB | ACTIVE | TSSOP | PW | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LMV34 4MT | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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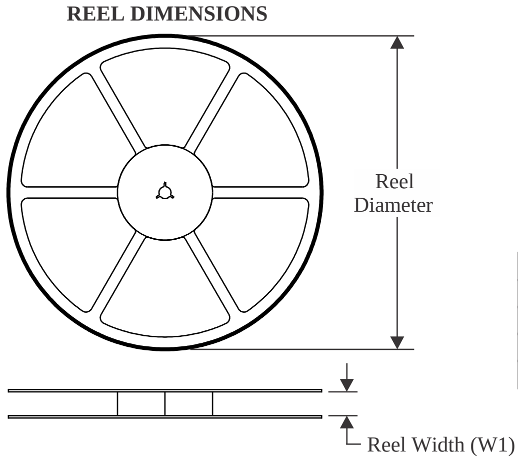
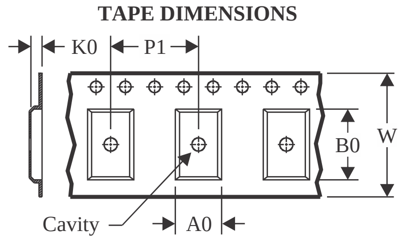
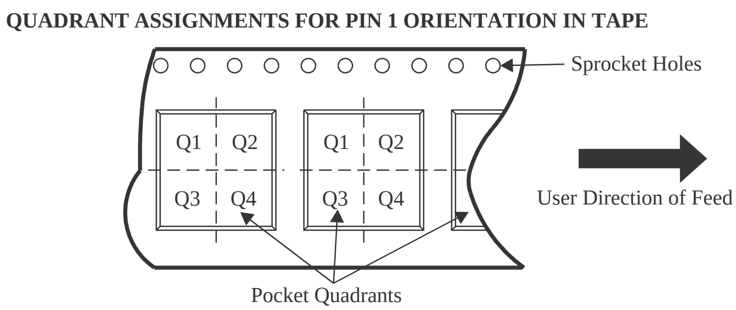
## TAPE AND REEL INFORMATION



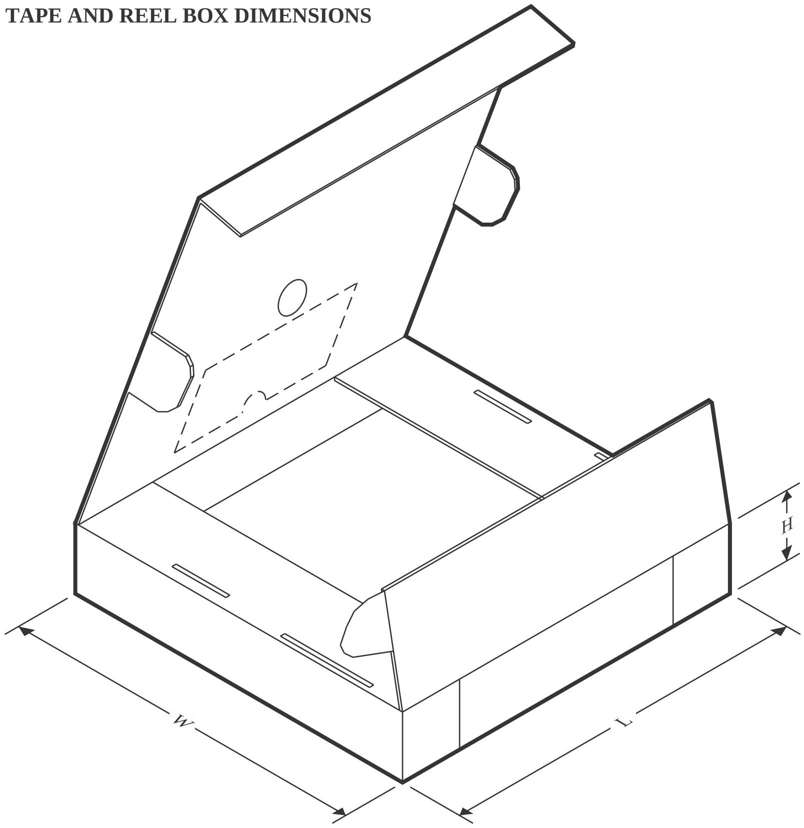

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV341MG/NOPB | SC70 | DCK | 6 | 1000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV341MGX/NOPB | SC70 | DCK | 6 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV342MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMV342MM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV342MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV344MAX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LMV344MTX/NOPB | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.95 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

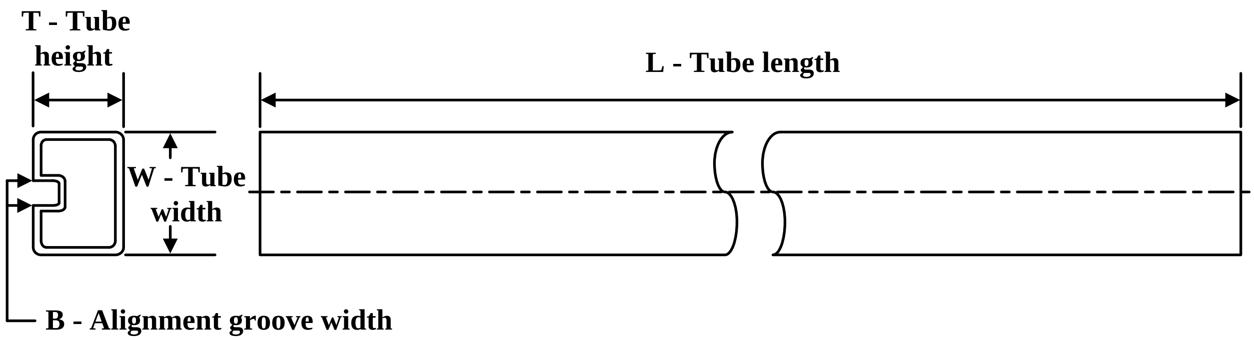
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMV341MG/NOPB | SC70 | DCK | 6 | 1000 | 208.0 | 191.0 | 35.0 |
| LMV341MGX/NOPB | SC70 | DCK | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| LMV342MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMV342MM/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMV342MMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LMV344MAX/NOPB | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| LMV344MTX/NOPB | TSSOP | PW | 14 | 2500 | 367.0 | 367.0 | 35.0 |

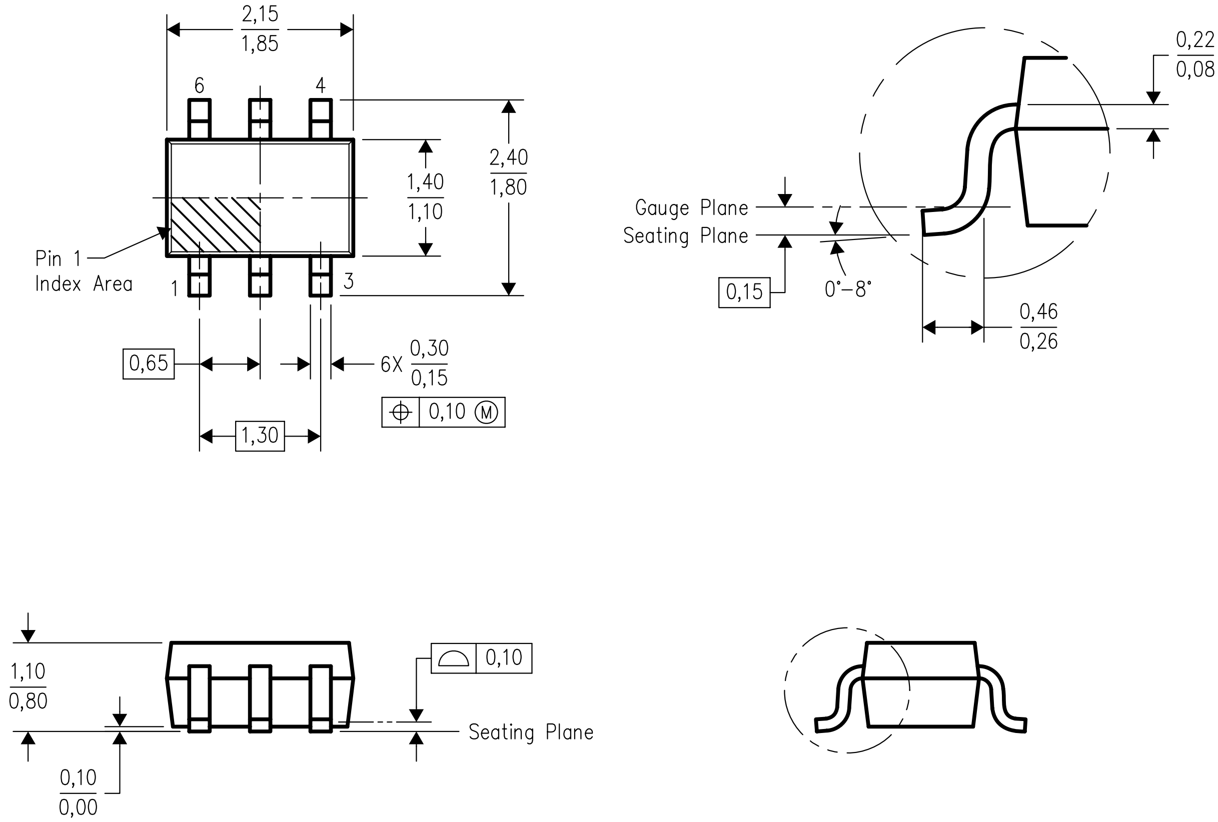
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LMV342MA/NOPB | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |
| LMV344MA/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LMV344MT/NOPB | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |
| LMV344MT/NOPB | PW | TSSOP | 14 | 94 | 530 | 10.2 | 3600 | 3.5 |

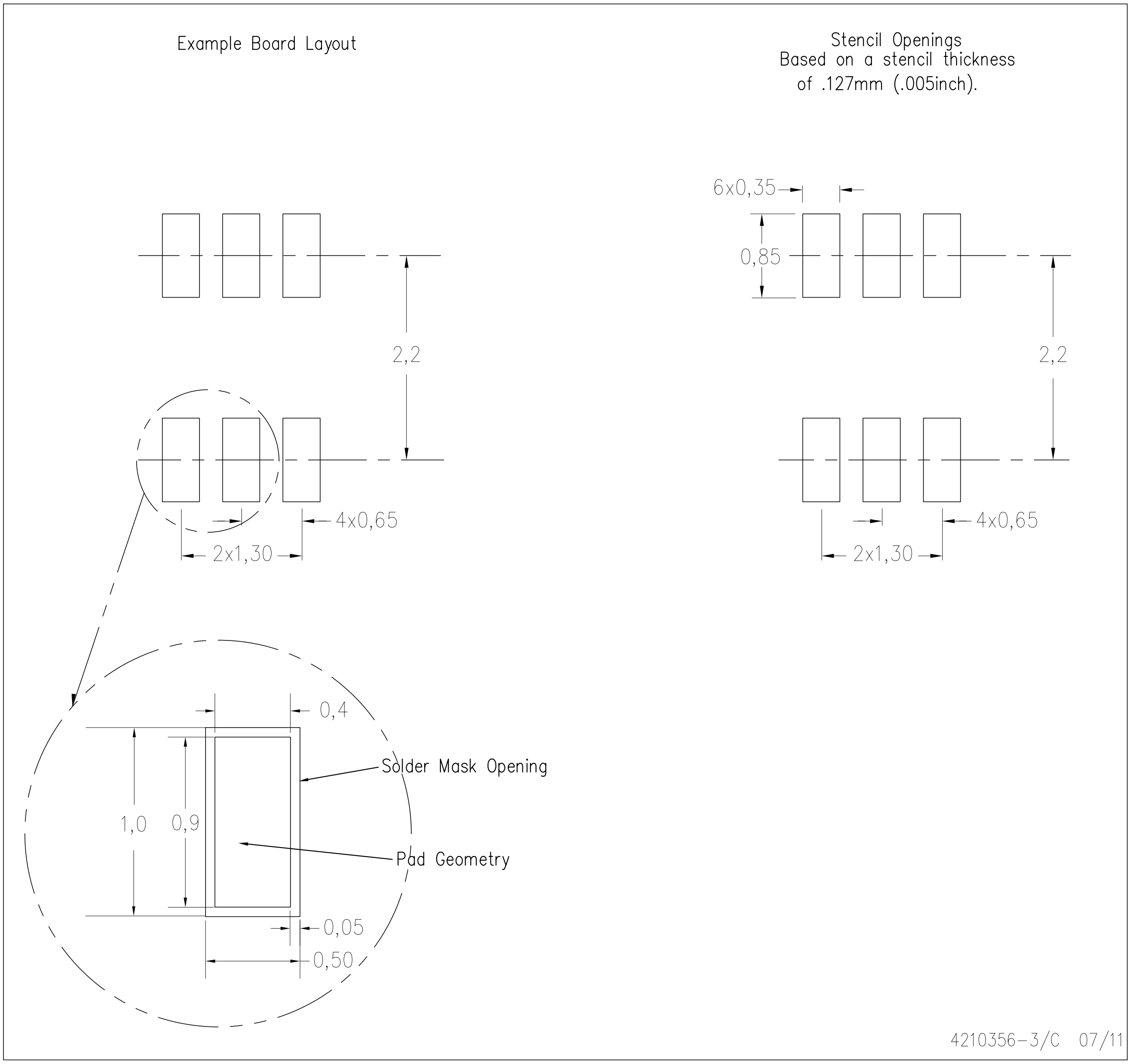
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/G 01/2007

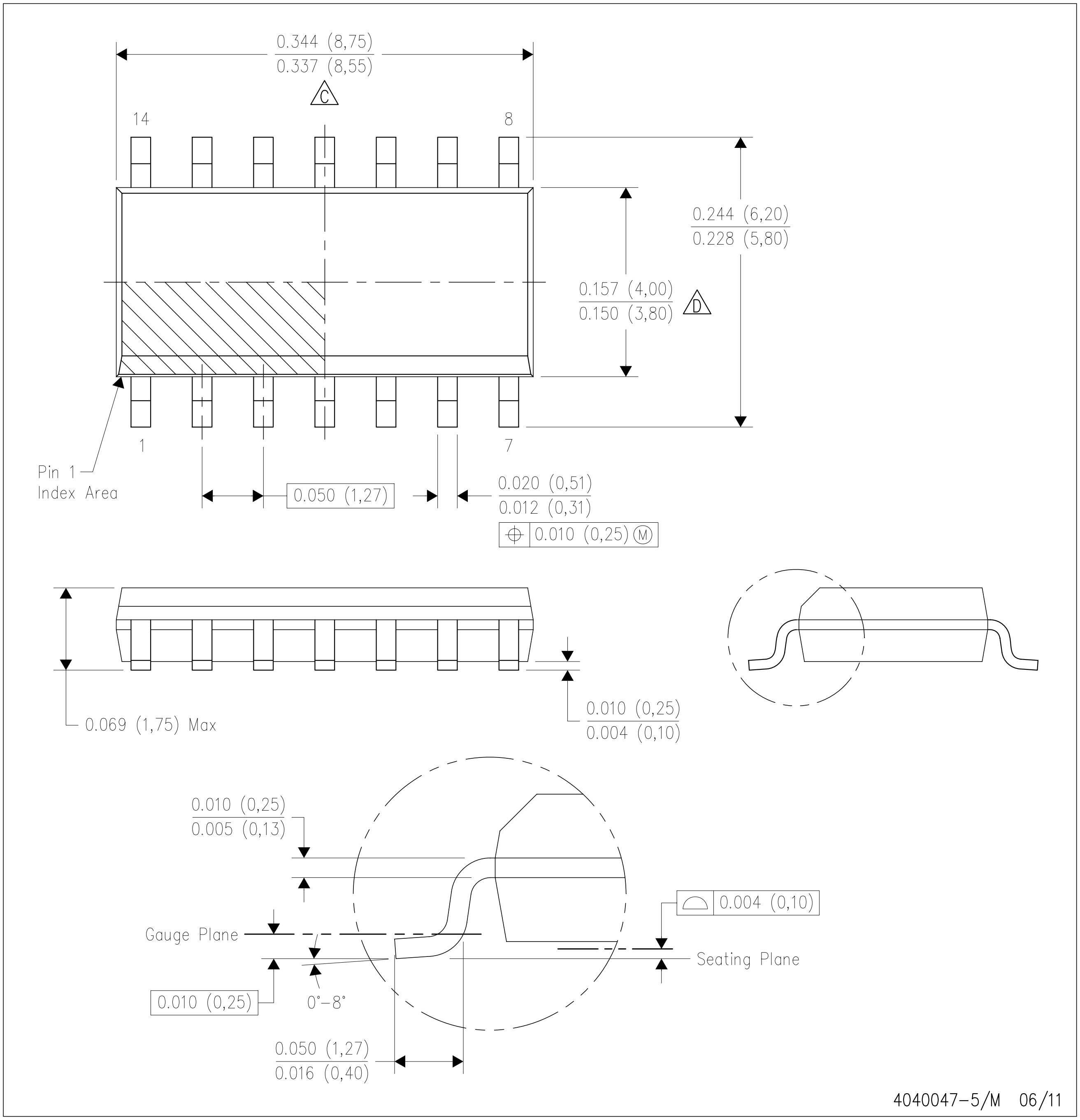
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



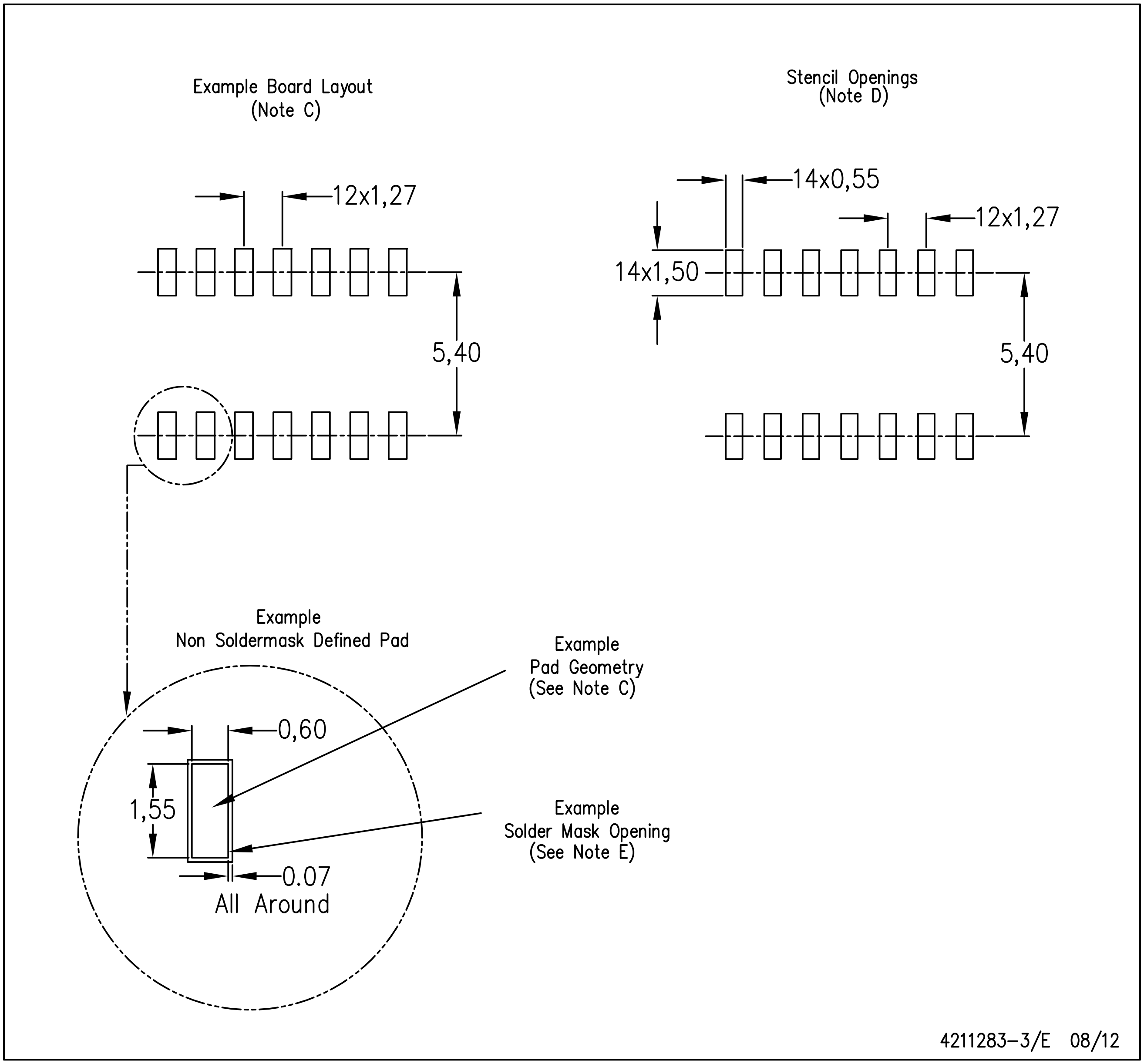

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



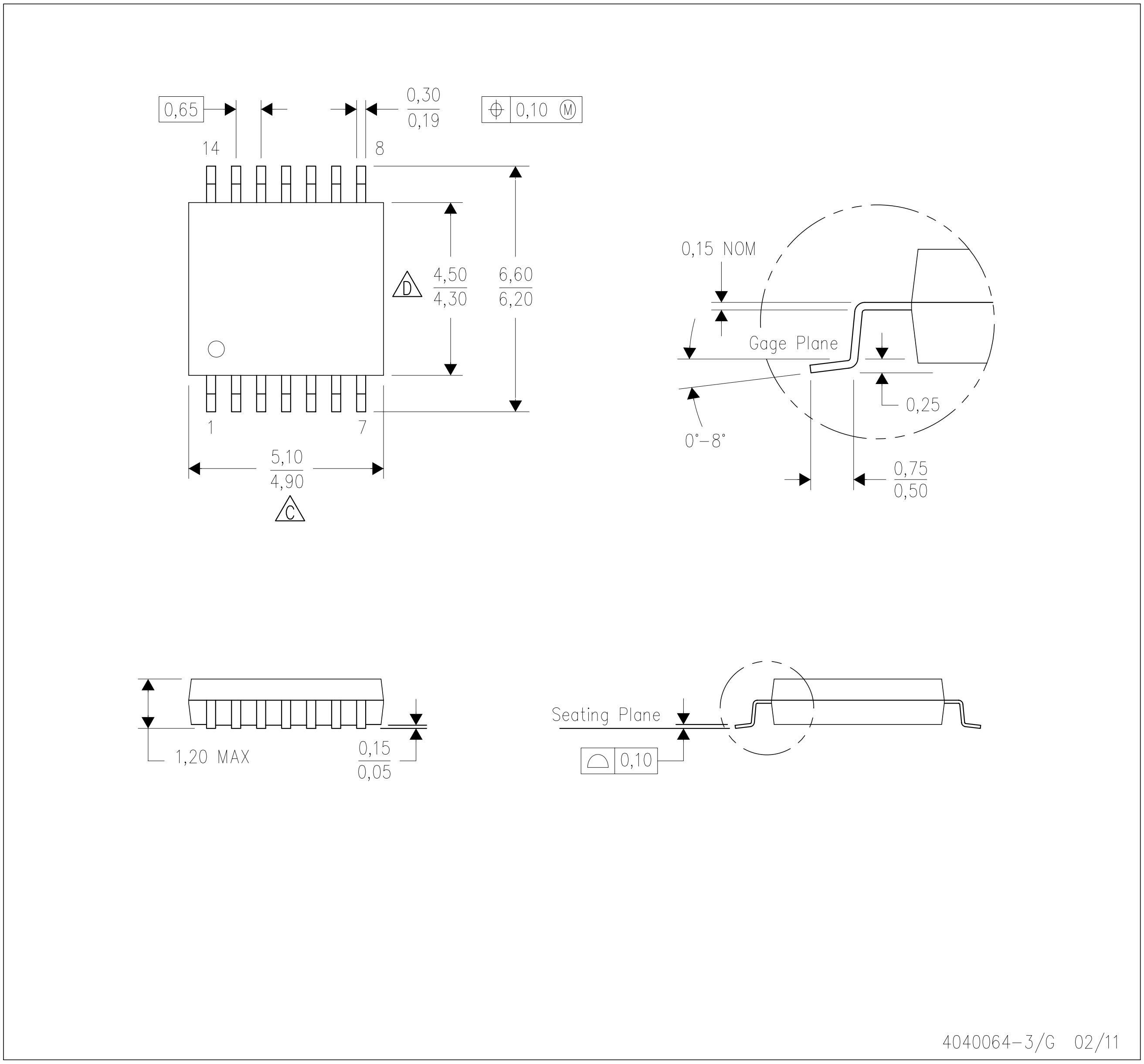

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



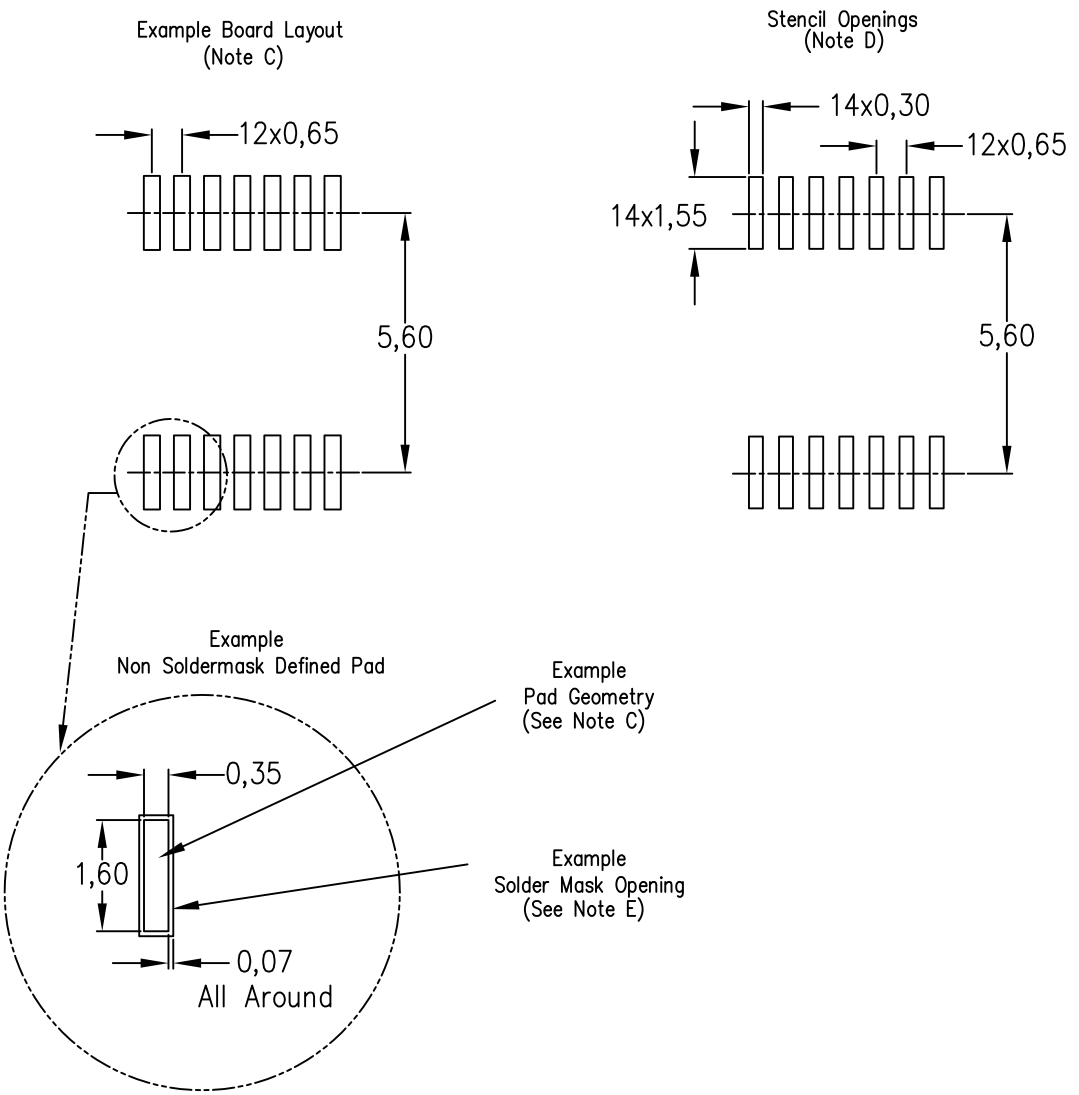

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



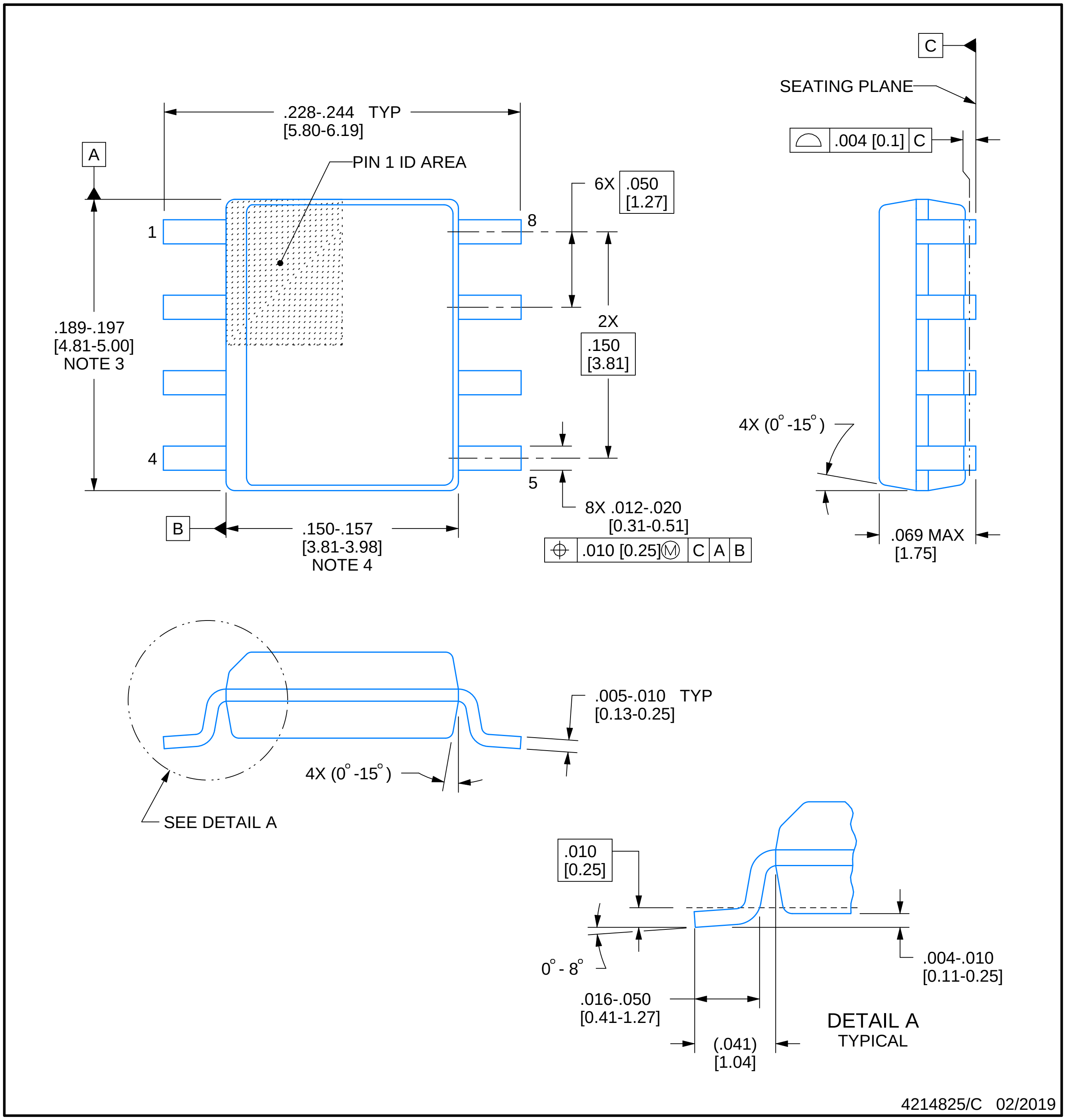

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



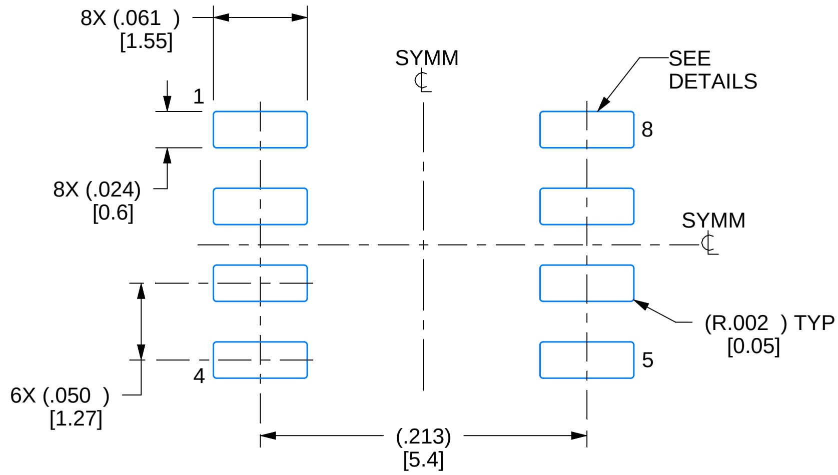

4211284–2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

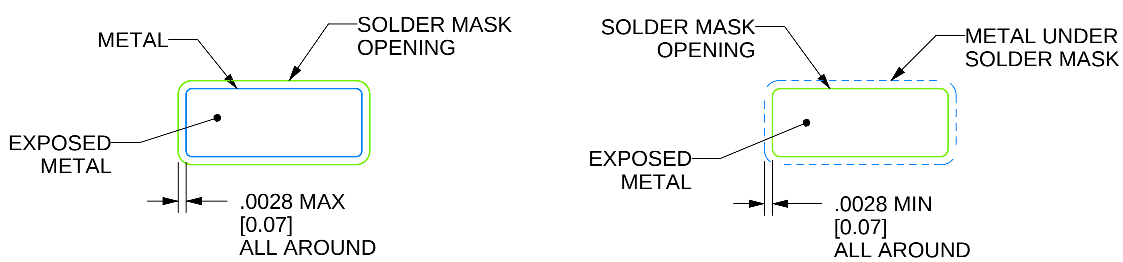



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




NON SOLDER MASK
DEFINED

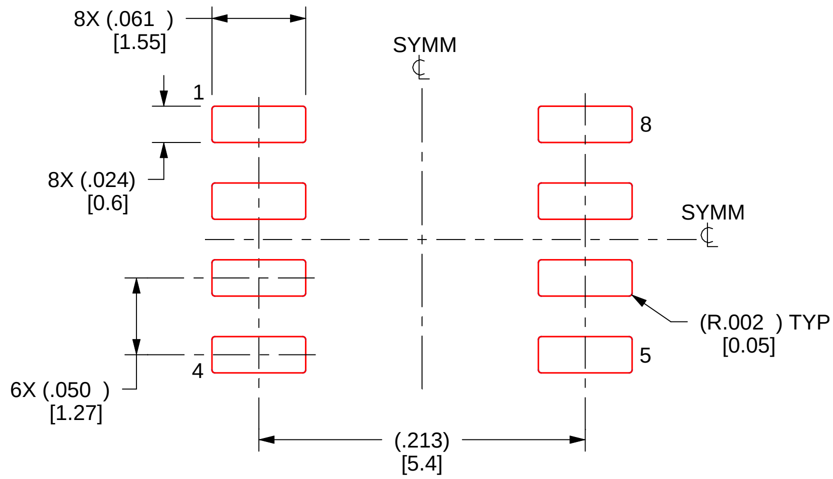
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

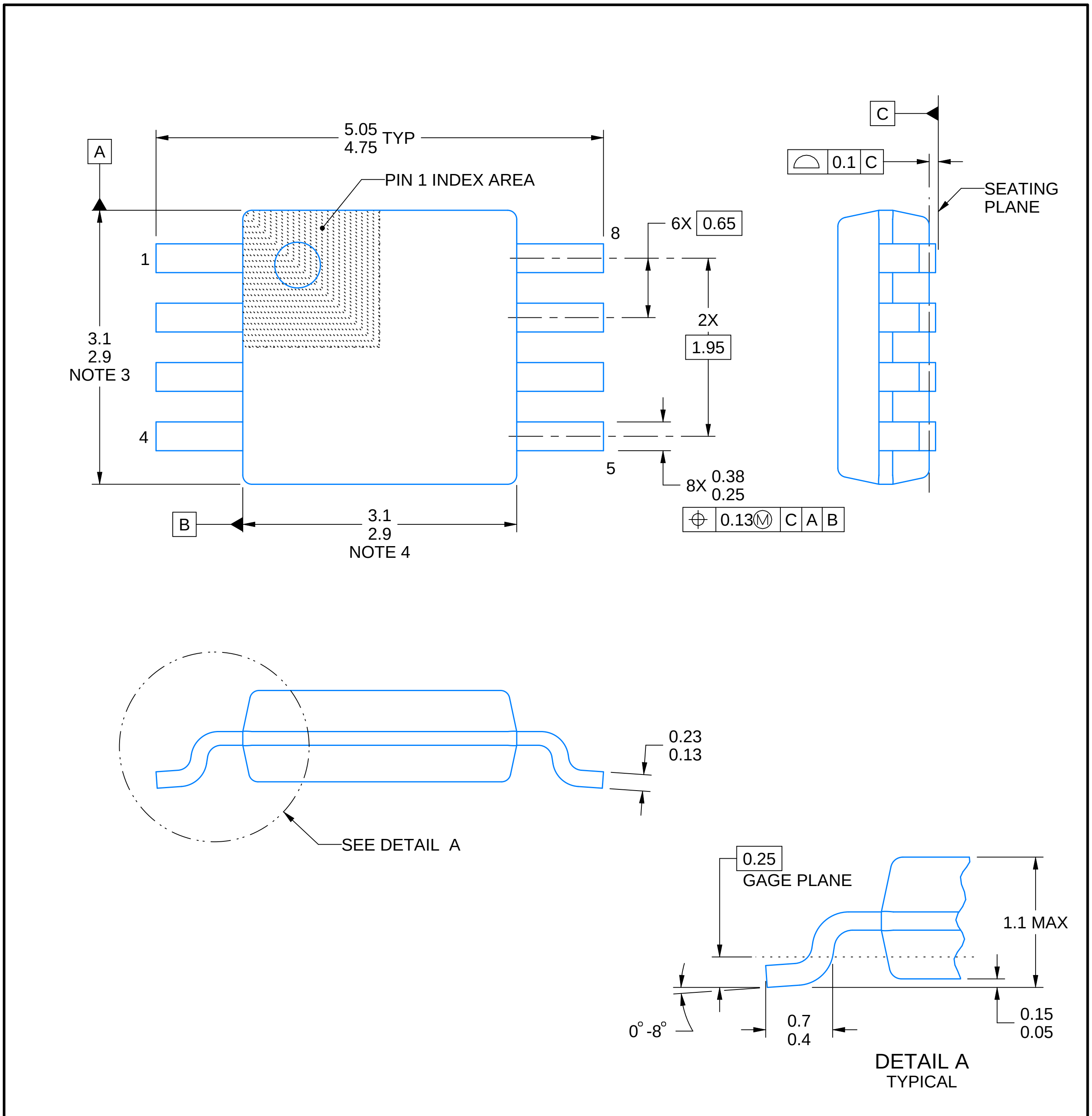



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

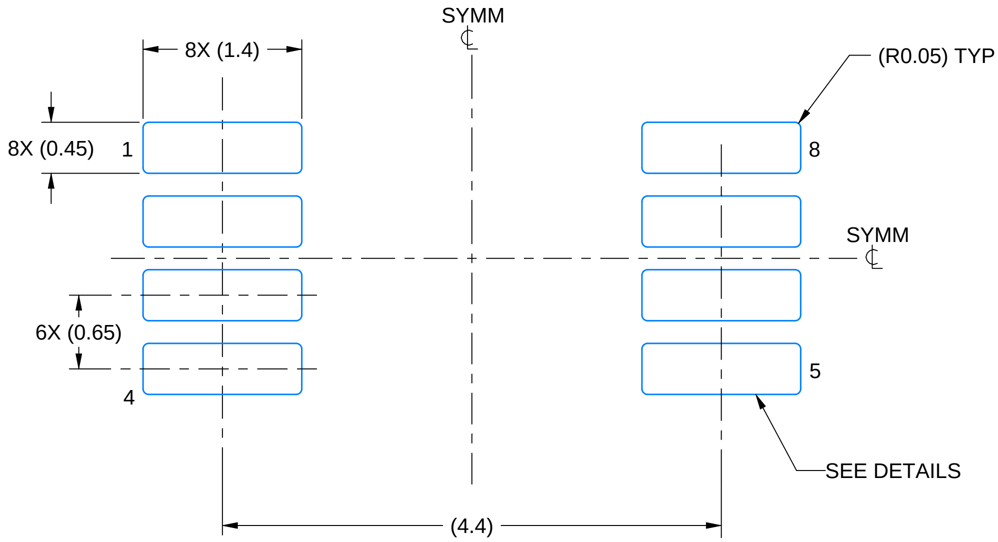



4214862/A 04/2023

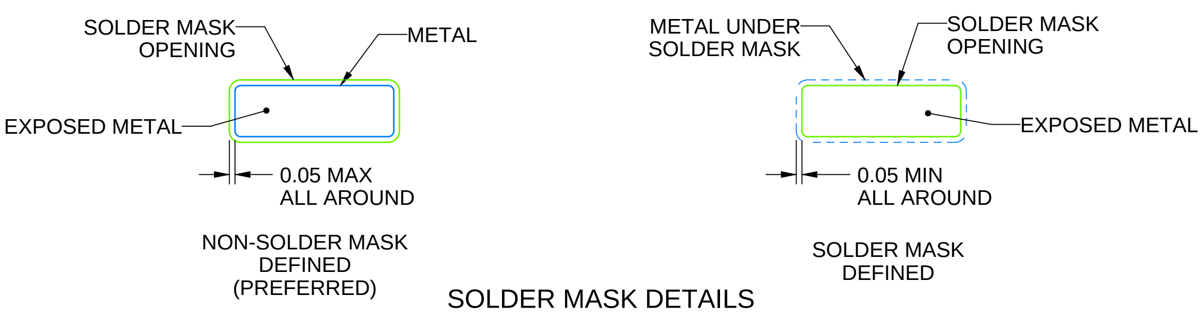
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

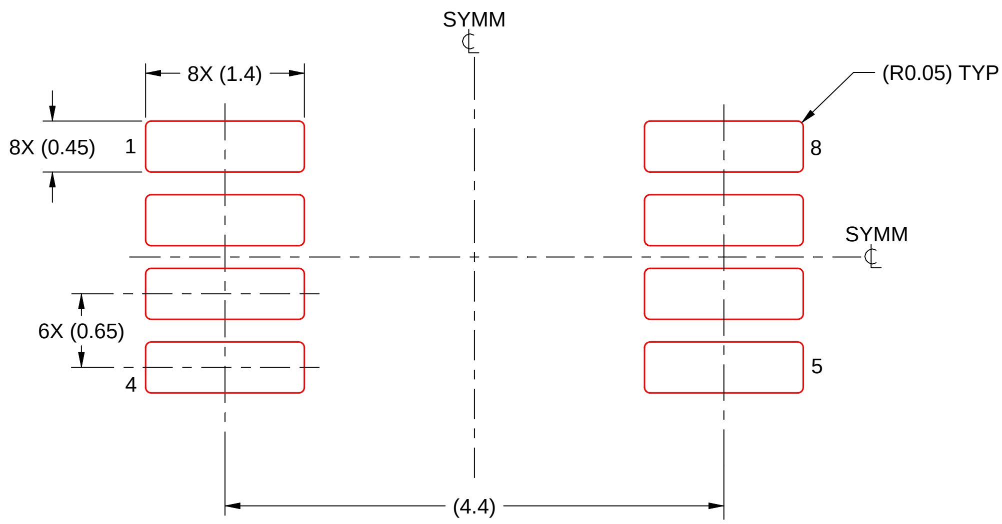



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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