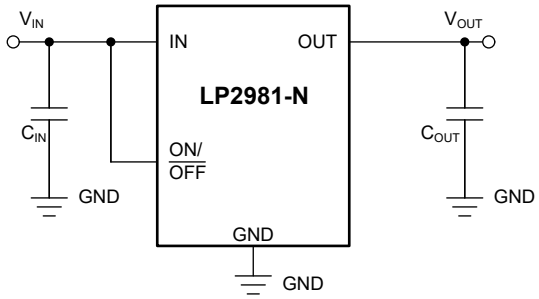
LP2981-N 100mA、低ドロップアウト レギュレータ、SOT-23 パッケージ

1 特長

- 入力電圧 (V_{IN}) 範囲:
  - 従来のチップ:2.1 V ～ 16 V
  - 新しいチップ:2.5V～16V
- 出力電圧 (V_{OUT}) 範囲:1.2 V ～ 5.0 V
- 出力電圧 (V_{OUT}) 精度:
  - ±0.75% (A グレードの従来チップ)
  - ±1.25% (標準グレードの従来チップ)
  - ±0.5% (A グレードおよび標準グレードの新チップ)
- 負荷および温度に対する出力電圧 (V_{OUT}) 精度:±1% (新チップ)
- 出力電流:最大 100mA
- 低い I_Q (新チップ):69µA (I_{LOAD} = 0 mA の場合)
- 低い I_Q (新チップ):620µA (I_{LOAD} = 100 mA の場合)
- シャットダウン電流と温度との関係:
  - < 1µA (従来チップ)
  - ≤ 1.75µA (新チップ)
- 出力電流制限および過熱保護
- 2.2µF のセラミック・コンデンサで安定動作 (新チップ)
- 高 PSRR (新チップ):
  - 1kHz で 75dB、1MHz で 45dB
- 動作時接合部温度:-40℃～+125℃
- パッケージ:5 ピン SOT-23 (DBV)

2 アプリケーション

- 電気メーター
- マイクロ インバータ
- サーバー PSU (12V 出力)
- 住宅用ブレーカ



代表的なアプリケーション回路

3 概要

LP2981-N は、固定出力、低ドロップアウト (LDO) の電圧レギュレータで、2.5V～16V の入力電圧範囲 (新チップの場合のみ) と最大 100mA の負荷電流に対応します。LP2981-N は、1.2V～5.0V の出力範囲をサポートしています (新チップ)。

さらに、LP2981-N (新チップ) は、負荷および温度の全範囲にわたって 1% の出力精度を備えており、低電圧マイクロコントローラ (MCU) およびプロセッサのニーズを満たすことができます。

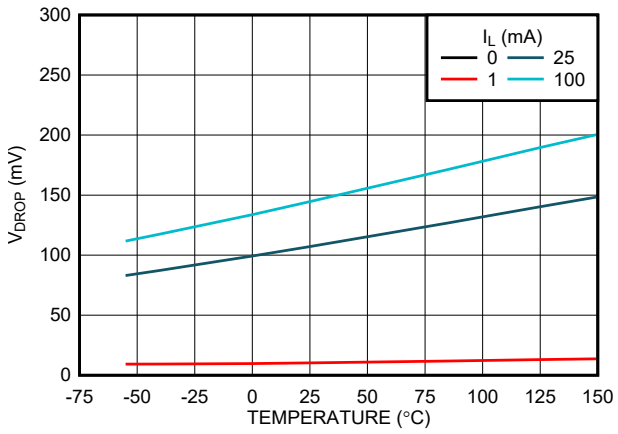
新チップの広帯域の PSRR 特性は、1kHz で 75dB、1MHz で 45dB であり、上流の DC/DC コンバータのスイッチング周波数を減衰して、レギュレータ後のフィルタ処理を最小化できます。

内部ソフトスタート時間および電流制限保護により、スタートアップ時の突入電流が減少し、入力静電容量を最小化しました。過電流および過熱保護などの一般的な保護機能を備えています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)(2)
LP2981-N	SOT-23 (5)	2.90mm × 2.80mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



ドロップアウト電圧と温度との関係 (新チップ)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

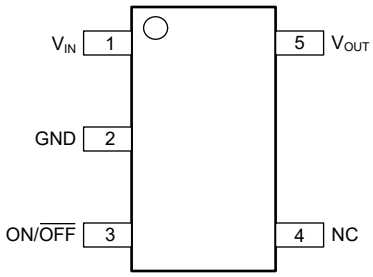


図 4-1. DBV Package, 5-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See the *セクション 7.1.2* section for more information.
2	GND	—	Common ground (device substrate).
3	ON/$\overline{\text{OFF}}$	I	Enable pin for the LDO. Driving the ON/$\overline{\text{OFF}}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *セクション 5.5* table. Tie this pin to V_{IN} if unused.
4	NC	—	For new chip: Not internally connected. This pin can be left open or tied to ground for improved thermal performance. For legacy chip: DO NOT CONNECT. Device pin 4 is reserved for post packaging test and calibration of the LP2981-N V_{OUT} accuracy. Device pin 4 must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 4 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 4 can activate the trim circuitry forcing V_{OUT} to move out of tolerance.
5	OUT	O	Output of the regulator. Use a capacitor with a value of 2.2 µF or larger from this pin to ground. See the *セクション 7.1.2* section for more information.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range(for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	9	
	Output voltage range(for new chip)	–0.3	V_{IN} + 0.3 or 9 (whichever is smaller)	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{OFF}$ pin voltage range (for new chip)	–0.3	18	
$V_{IN} – V_{OUT}$	Input-output voltage (for legacy chip)	–0.3	16	
	Input-output voltage (for new chip)	–0.3	18	
Current	Maximum output current	Internally limited		mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 1,2 and 5) (1)	±2000	±3000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 3 and 4) (1)	±1000		
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	N/A	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.1		16	V
	Supply input voltage (for new chip)	2.5		16	
$V_{IN} – V_{OUT}$	Input-output differential (for legacy chip)	0.7		11	
	Input-output differential (for new chip)	0		16	
V_{OUT}	Output voltage (for new chip)	1.2		5	
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		100	mA
C_{IN} (1)	Input capacitor		1		µF
C_{OUT}	Output capacitor (for legacy chip)	2.2	4.7		
	Output capacitance (for new chip) (1)	1	2.2	200	
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.

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5.4 Thermal Information

THERMAL METRIC (1)		Legacy Chip (2) DBV (SOT23-5) 5 PINS	New Chip (2) DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.7	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.0	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.8	47.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	46.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the *Impact of board layout on LDO thermal performance* application report.

5.5 Electrical Characteristics

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	Legacy chip (Standard grade)	–1.25		1.25	%
			Legacy chip (A grade)	–0.75		0.75	%
			New chip	–0.5		0.5	%
		1 mA < I_L < 100 mA	Legacy chip (Standard grade)	–2.0		2.0	%
			Legacy chip (A grade)	–1.0		1.0	%
			New chip	–0.5		0.5	%
		1 mA < I_L < 100 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (Standard grade)	–3.5		3.5	%
			Legacy chip (A grade)	–2.5		2.5	%
			New chip	–1		1	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	
$\Delta V_{OUT(\Delta ILOAD)}$	Load regulation	1 mA < I_L < 100 mA, –40°C ≤ T_J ≤ 125°C, V_{IN} = $V_{O(NOM)}$+0.5 V	New chip		0.1	0.5	%/A

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specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} - V_{OUT}	Dropout voltage[1]	I_{OUT} = 0 mA	Legacy chip		1	3	mV
			New chip		1	2.75	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			5	
			New chip			3	
		I_{OUT} = 1 mA	Legacy chip		7	10	
			New chip		11.5	14	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			17	
		I_{OUT} = 25 mA	Legacy chip		70	100	
			New chip		110	132	
		I_{OUT} = 25 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			150	
			New chip			167	
		I_{OUT} = 100 mA	Legacy chip		200	250	
			New chip		160	175	
		I_{OUT} = 100 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			375	
			New chip			218	
I_{GND}	GND pin current	I_{OUT} = 0 mA	Legacy chip		65	95	µA
			New chip		69	95	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I_{OUT} = 1 mA	Legacy chip		80	110	
			New chip		78	110	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			170	
			New chip			140	
		I_{OUT} = 25 mA	Legacy chip		200	300	
			New chip		225	295	
		I_{OUT} = 25 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			550	
			New chip			345	
		I_{OUT} = 100 mA	Legacy chip		600	800	
			New chip		620	790	
		I_{OUT} = 100 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			1500	
			New chip			950	
		$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	Legacy chip		0.01	0.8	
			New chip		1.25	1.75	
		$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.05	2	
			New chip		1.12	2.75	
V_{UVLO+}	Rising bias supply UVLO	V_{IN} rising, –40°C ≤ T_J ≤ 125°C	New chip		2.2	2.4	V
V_{UVLO-}	Falling bias supply UVLO	V_{IN} falling, –40°C ≤ T_J ≤ 125°C		1.9			
$V_{UVLO(HYST)}$	UVLO hysteresis	–40°C ≤ T_J ≤ 125°C			0.130		
$I_{O(SC)}$	Short Output Current	R_L = 0 Ω (steady state)	Legacy chip		150		mA
			New chip		150		

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specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

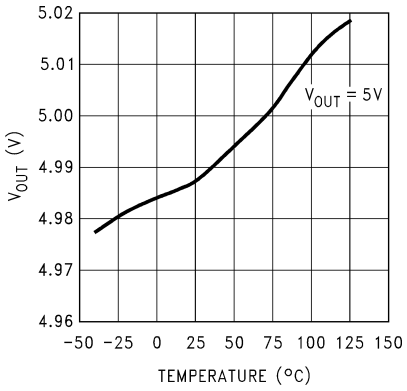
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	Low = Output OFF	Legacy chip		0.5		V
			New chip		0.72		
		Low = Output OFF, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip	1.6			
			New chip	1.6			
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V	Legacy chip		0.01		µA
			New chip		0.42		
		$V_{ON/OFF}$ = 0 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			–1	
			New chip			–0.9	
		$V_{ON/OFF}$ = 5 V	Legacy chip		5		
			New chip		0.011		
		$V_{ON/OFF}$ = 5 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			2.20	
IO(PK)	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ –5% (steady state)	Legacy chip (A version)	150	400		mA
			Legacy chip (Standard version)		150		
			New chip		350		
$\Delta V_O/\Delta V_{IN}$	Ripple Rejection	f = 1 kHz, C_{OUT} = 10 µF	Legacy chip		63		dB
			New chip		75		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, C_{OUT} = 2.2 µF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	Legacy chip		160		μ_{VRMS}
		Bandwidth = 300 Hz to 50 kHz, C_{OUT} = 2.2 µF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	New chip		140		
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170		°C
T_{sd-}		Reset, temperature decreasing			150		

(1) Dropout voltage (V_{DO}) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential. V_{DO} is measured with V_{IN} = $V_{OUT(nom)}$ – 100 mV for fixed output devices.

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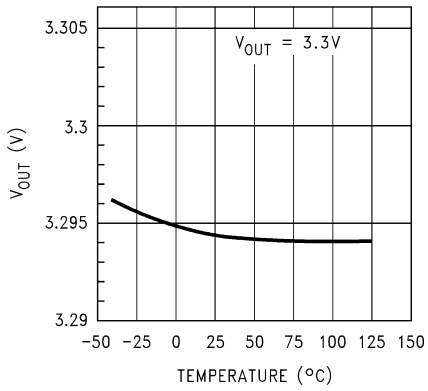
5.6 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.



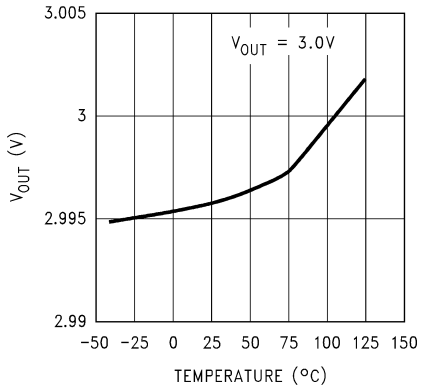
V_{IN} = 6 V, V_{OUT} = 5 V

図 5-1. Output Voltage versus Temperature (Legacy Chip)



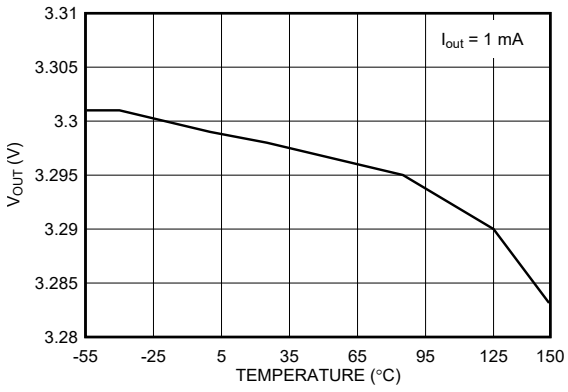
V_{IN} = 4.3 V, V_{OUT} = 3.3 V

図 5-2. Output Voltage versus Temperature (Legacy Chip)



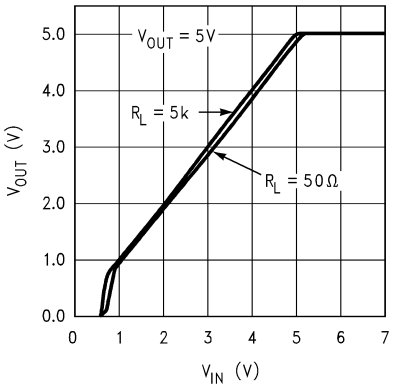
V_{IN} = 4.0 V, V_{OUT} = 3.0 V

図 5-3. Output Voltage versus Temperature (Legacy Chip)



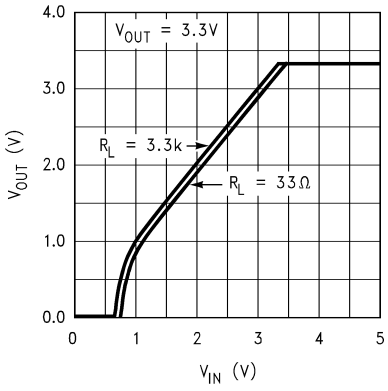
V_{IN} = 4.3 V, V_{OUT} = 3.3 V

図 5-4. Output Voltage versus Temperature (New Chip)



V_{OUT} = 5.0 V

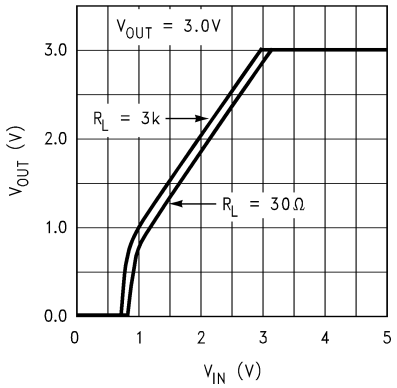
図 5-5. Output Voltage versus V_{IN} (Legacy Chip)



V_{OUT} = 3.3 V

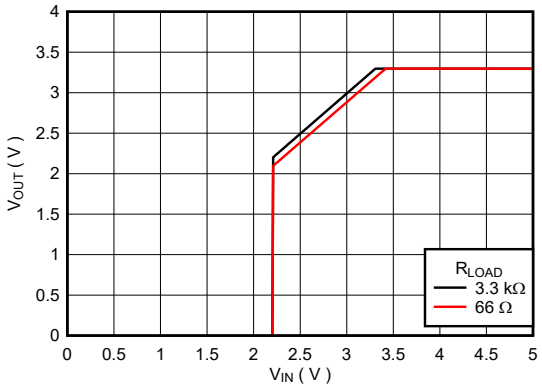
図 5-6. Output Voltage versus V_{IN} (Legacy Chip)

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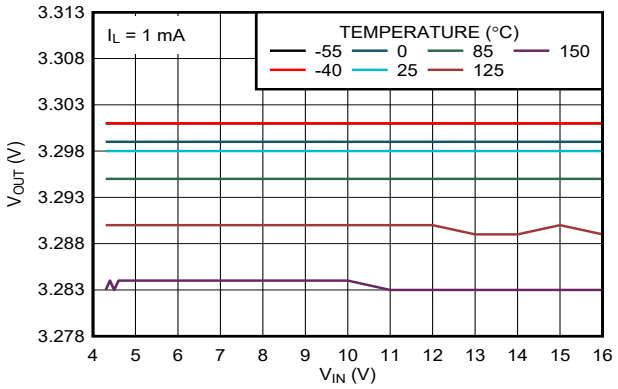
V_{OUT} = 3.0 V

図 5-7. Output Voltage versus V_{IN} (Legacy Chip)



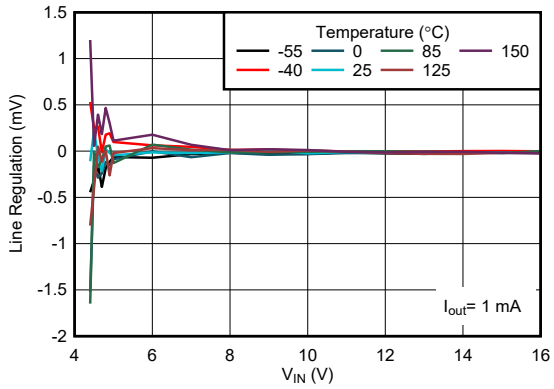
V_{OUT} = 3.3 V

図 5-8. Output Voltage versus V_{IN} (New Chip)



V_{OUT} = 3.3 V, I_L = 1 mA

図 5-9. Output Voltage versus V_{IN} and Temperature (New Chip)



V_{OUT} = 3.3 , I_L = 1 mA

図 5-10. Line Regulation versus V_{IN} & Temperature (New Chip)

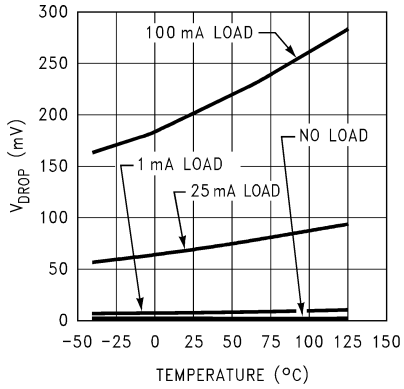


図 5-11. Dropout Voltage (V_{DO}) versus Temperature (Legacy Chip)

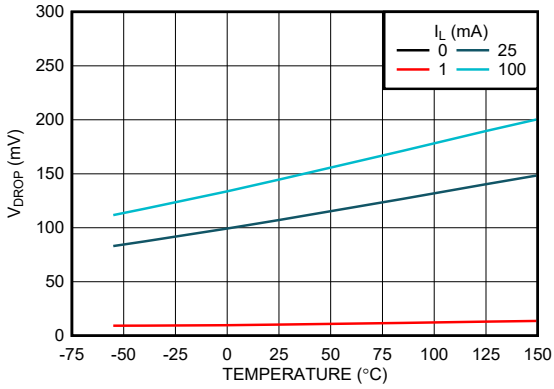


図 5-12. Dropout Voltage (V_{DO}) versus Temperature (New Chip)

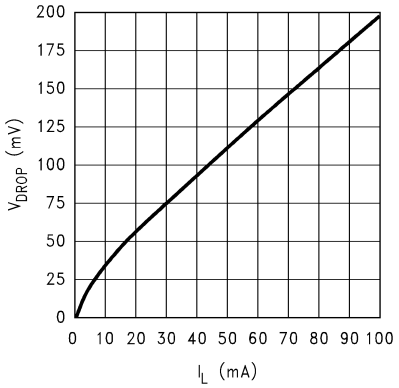


図 5-13. Dropout Voltage (V_{DO}) versus Load Current (Legacy Chip)

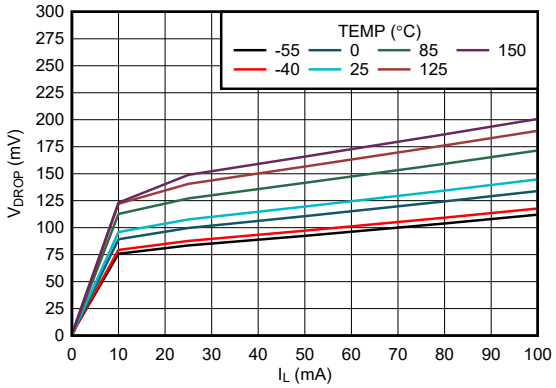


図 5-14. Dropout Voltage (V_{DO}) versus Load Current (New Chip)

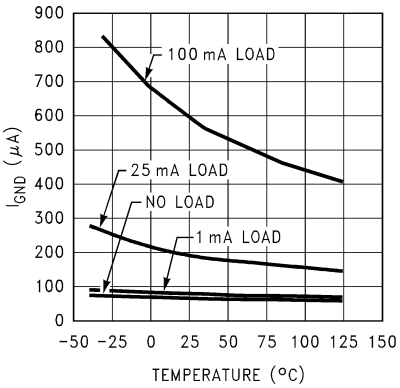


図 5-15. Ground Pin Current (I_{GND}) versus Temperature (Legacy Chip)

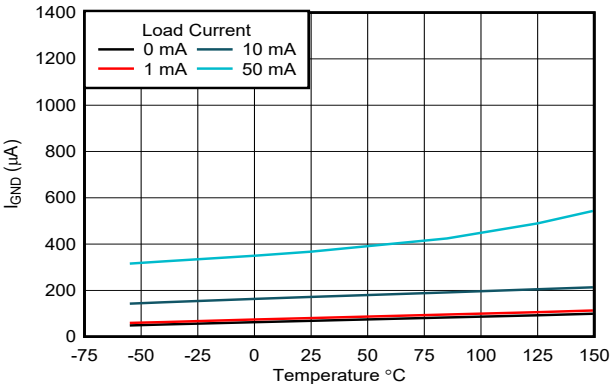


図 5-16. Ground Pin Current (I_{GND}) versus Temperature (New Chip)

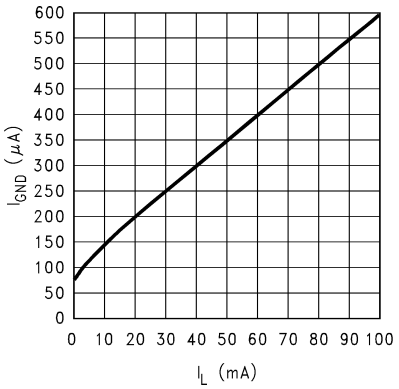


図 5-17. Ground Pin Current (I_{GND}) versus Load Current (Legacy Chip)

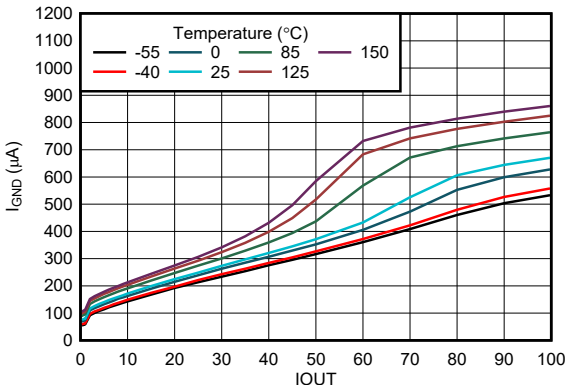
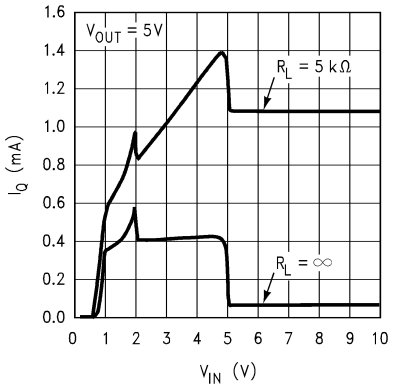


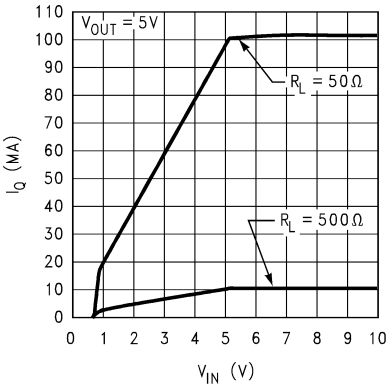
図 5-18. Ground Pin Current (I_{GND}) versus Load Current (New Chip)

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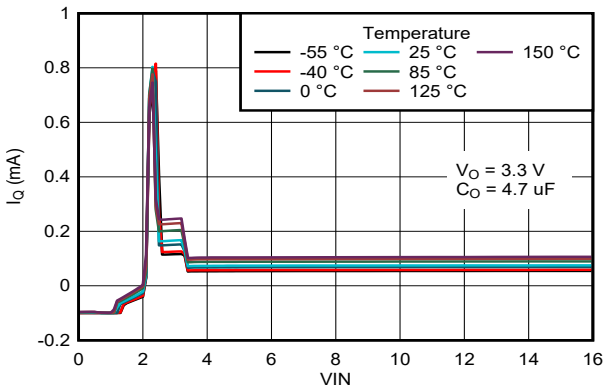
V_{OUT} = 5 V, R_L = ∞ and R_L = 5 kΩ

図 5-19. Input Current versus Input Voltage (V_{IN}) (Legacy Chip)



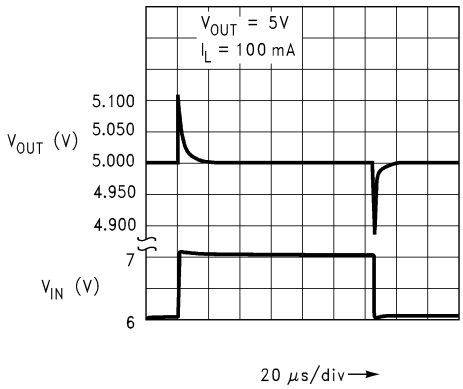
V_{OUT} = 5 V, R_L = 500 Ω and R_L = 50 Ω

図 5-20. Input Current versus Input Voltage (V_{IN}) (Legacy Chip)



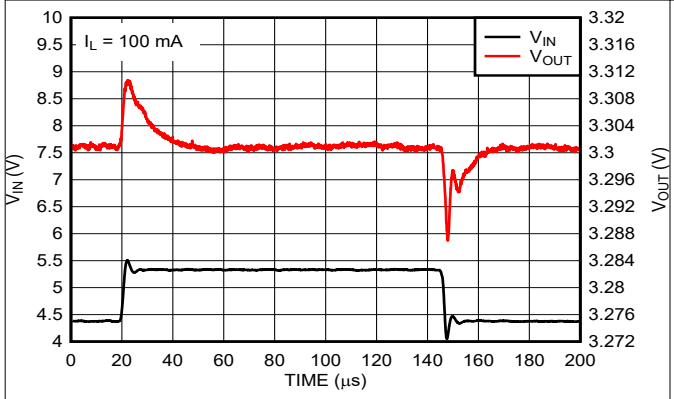
V_{OUT} = 3.3 V, R_L = 3.3 kΩ

図 5-21. Input Current versus Input Voltage (V_{IN}) (New Chip)



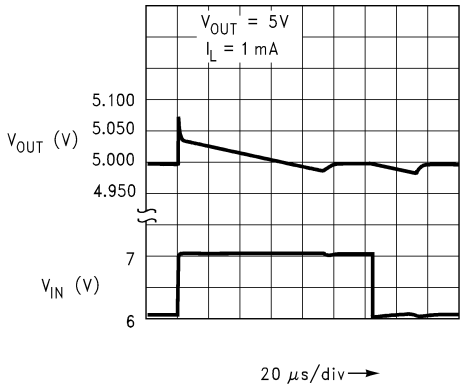
V_{OUT} = 5 V, I_L = 100 mA

図 5-22. Line Transient Response (Legacy Chip)



V_{OUT} = 3.3 V, I_L = 100 mA

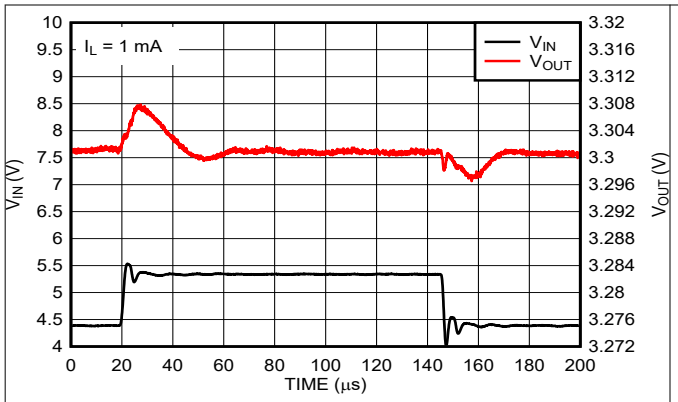
図 5-23. Line Transient Response (New Chip)



V_{OUT} = 5 V, I_L = 1 mA

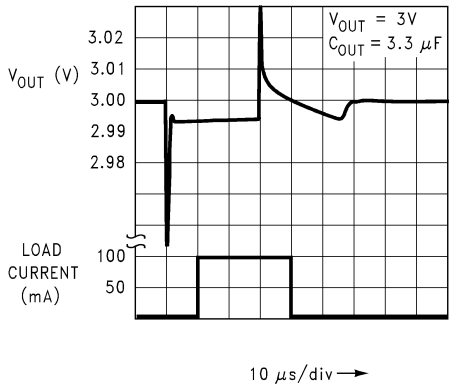
図 5-24. Line Transient Response (Legacy Chip)

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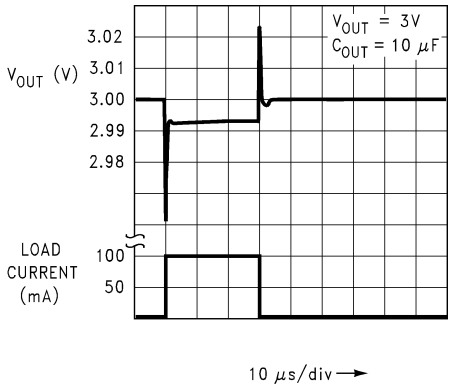
V_{OUT} = 3.3 V, I_L = 1 mA

図 5-25. Line Transient Response (New Chip)



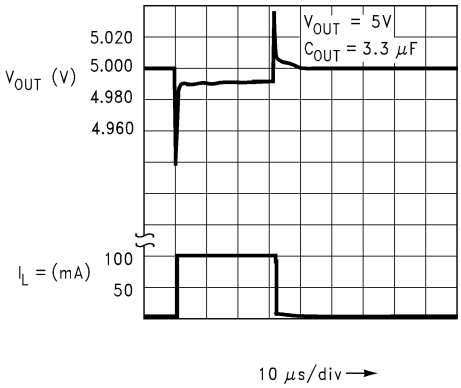
V_{OUT} = 3.0 V, C_{OUT} = 3.3 µF

図 5-26. Load Transient Response (Legacy Chip)



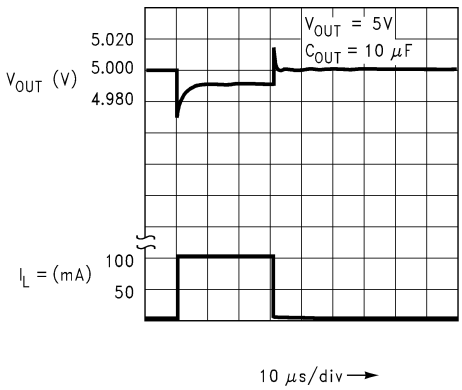
V_{OUT} = 3.0 V, C_{OUT} = 10 µF

図 5-27. Load Transient Response (Legacy Chip)



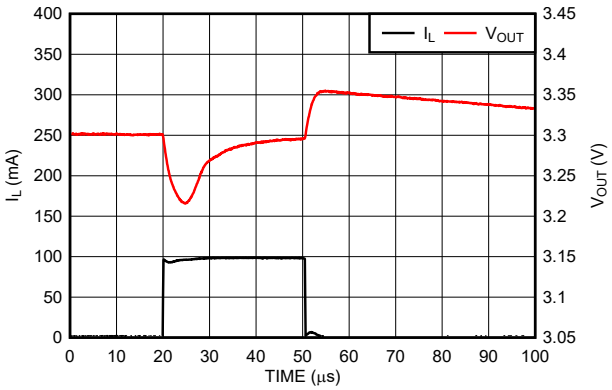
V_{OUT} = 5.0 V, C_{OUT} = 3.3 µF

図 5-28. Load Transient Response (Legacy Chip)



V_{OUT} = 5.0 V, C_{OUT} = 10 µF

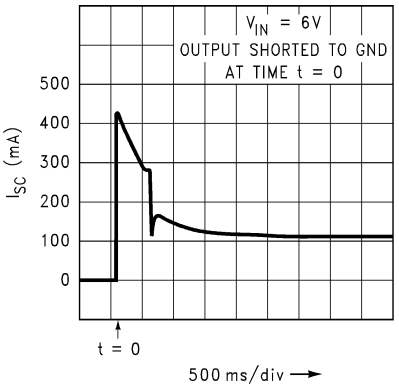
図 5-29. Load Transient Response (Legacy Chip)



V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

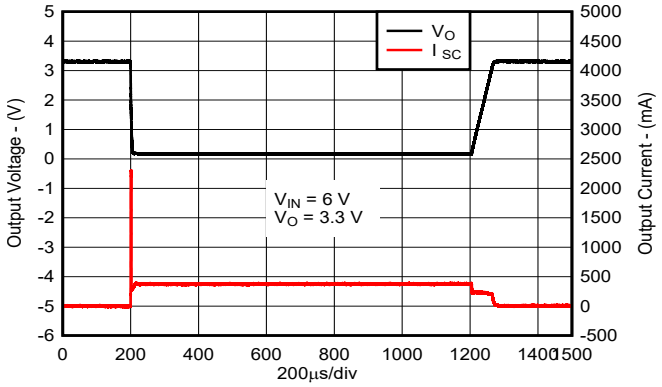
図 5-30. Load Transient Response (New Chip)

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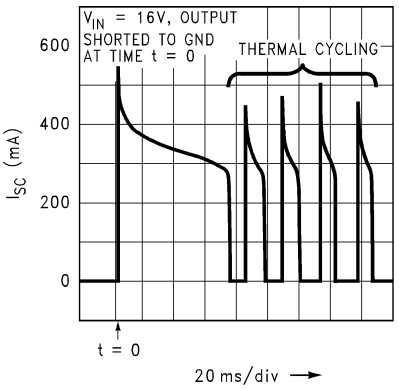
V_{IN} = 6.0 V

図 5-31. Short Circuit Current versus Time (Legacy Chip)



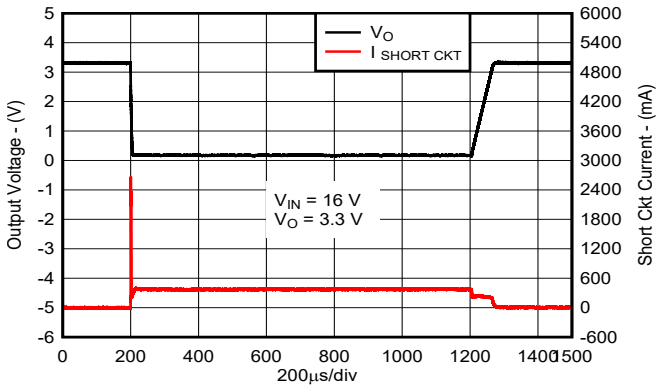
V_{IN} = 6.0 V

図 5-32. Short Circuit Current versus Time (New Chip)



V_{IN} = 16.0 V

図 5-33. Short Circuit Current versus Time (Legacy Chip)



V_{IN} = 16.0 V

図 5-34. Short Circuit Current versus Time (New Chip)

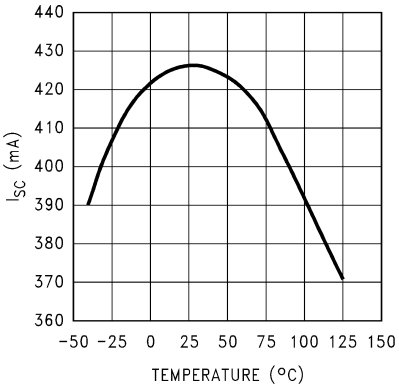


図 5-35. Instantaneous Short Circuit Current versus Temperature (Legacy Chip)

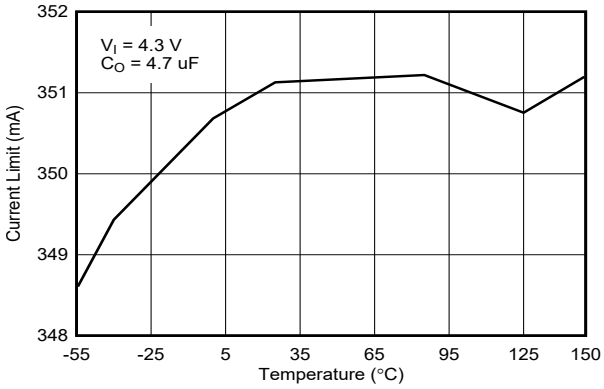
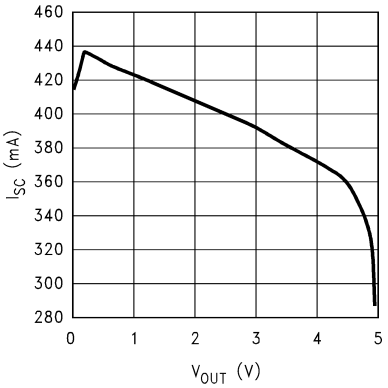


図 5-36. Instantaneous Short Circuit Current versus Temperature (New Chip)

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V_{IN} = 6.0 V

図 5-37. Short Circuit Current versus Output Voltage (V_{OUT}) (Legacy Chip)

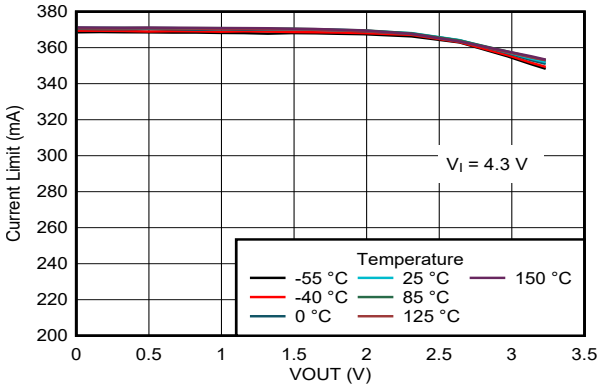
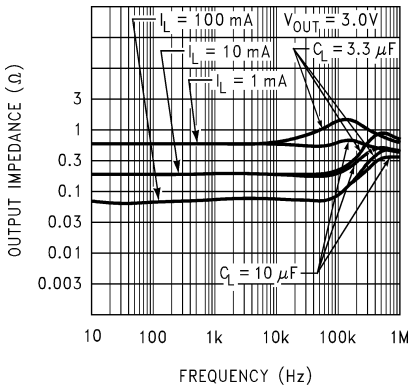
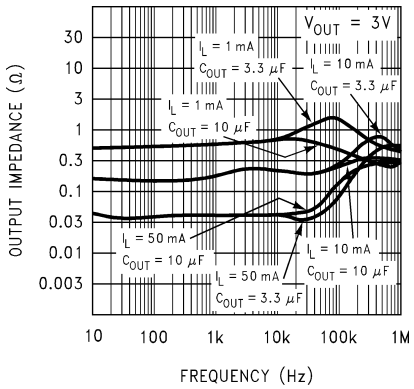


図 5-38. Short Circuit Current versus Output Voltage (V_{OUT}) (New Chip)



V_{OUT} = 3.0 V

図 5-39. Output Impedance versus Frequency (Legacy Chip)



V_{OUT} = 3.0 V

図 5-40. Output Impedance versus Frequency (Legacy Chip)

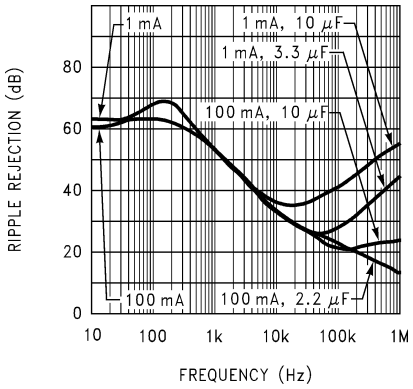


図 5-41. Ripple Rejection versus Frequency (Legacy Chip)

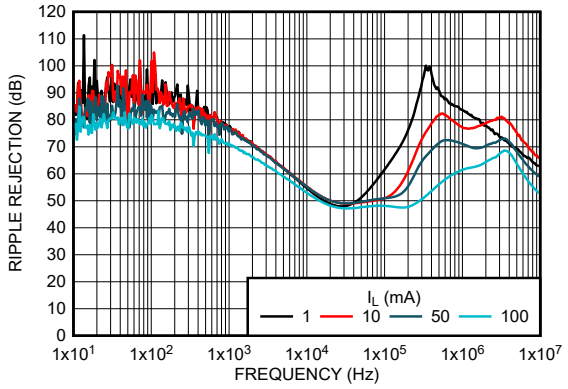


図 5-42. Ripple Rejection versus Load Current (I_L) & Frequency (New Chip)

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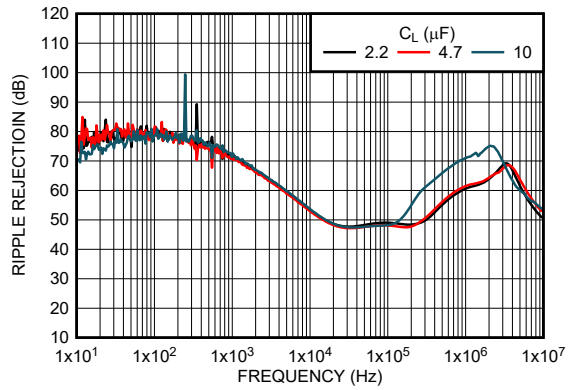


図 5-43. Ripple Rejection versus Output Capacitor (C_L) & Frequency (New Chip)

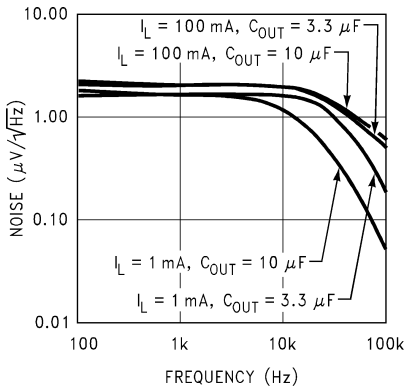


図 5-44. Output Noise Density versus Frequency (Legacy Chip)

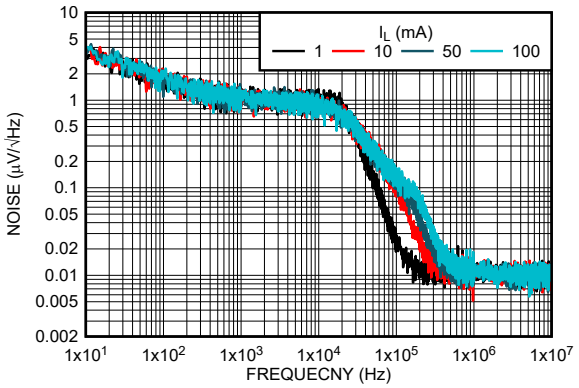


図 5-45. Output Noise Density versus Load Current (I_L) Frequency (New Chip)

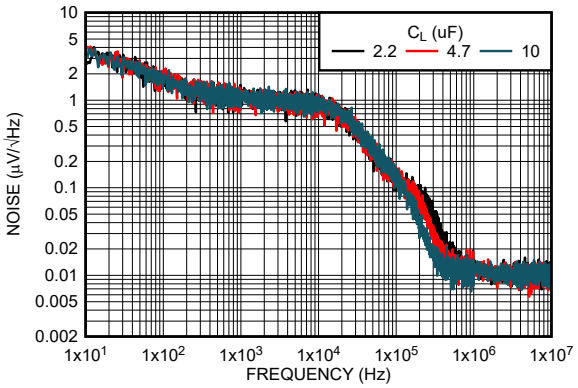


図 5-46. Output Noise Density versus Output Capacitor (C_L) Frequency (New Chip)

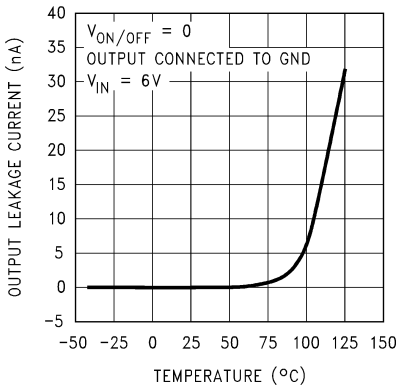


図 5-47. Input-to-Output Leakage versus Temperature (Legacy Chip)

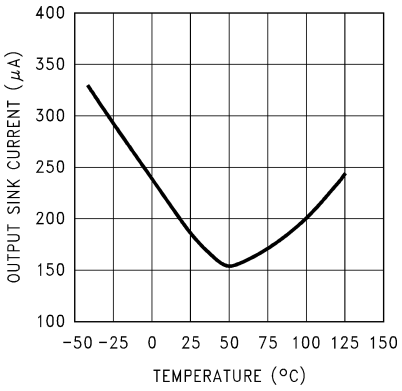


図 5-48. Output Reverse Leakage versus Temperature (Legacy Chip)

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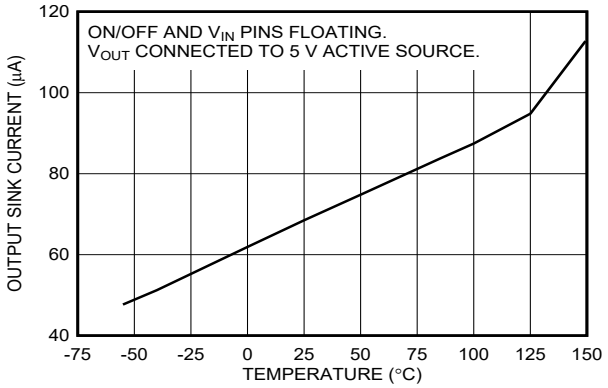
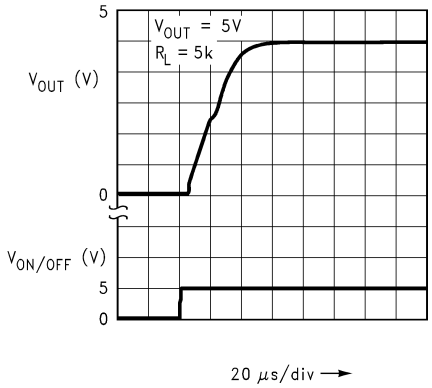
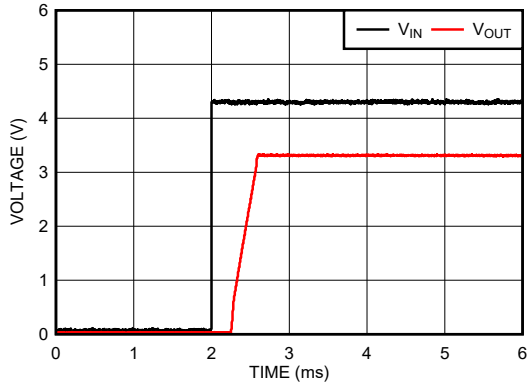


図 5-49. Output Reverse Leakage versus Temperature (New Chip)



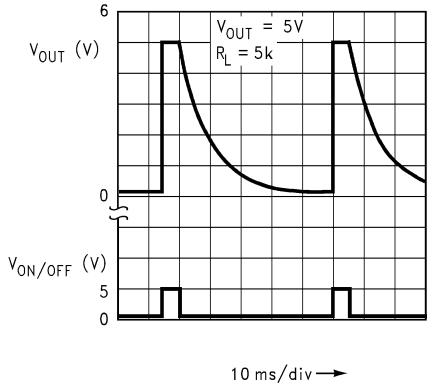
V_{OUT} = 5 V, R_L = 5 kΩ

図 5-50. Turn-on Waveform (Legacy Chip)



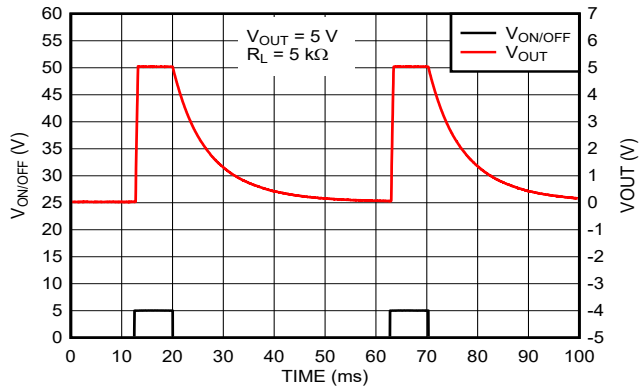
V_{OUT} = 3.3 V, R_L = 3.3 kΩ

図 5-51. Turn-on Waveform (New Chip)



V_{OUT} = 5 V, R_L = 5 kΩ

図 5-52. Turn-off Waveform (Legacy Chip)



V_{OUT} = 5 V, R_L = 5 kΩ

図 5-53. Turn-off Waveform (New Chip)

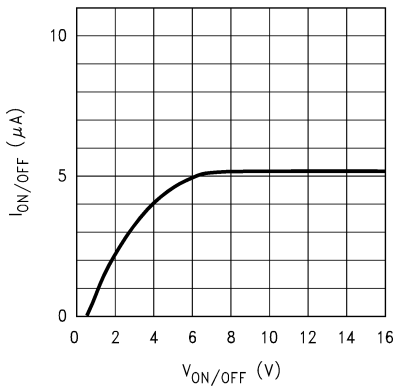
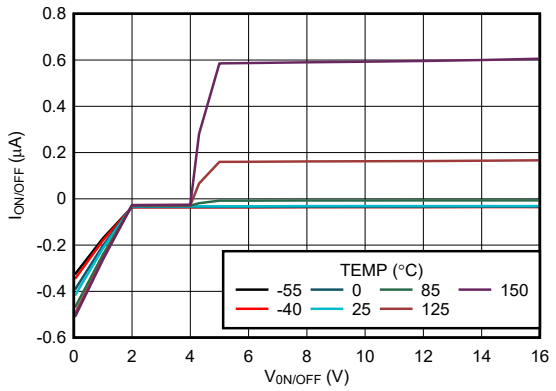


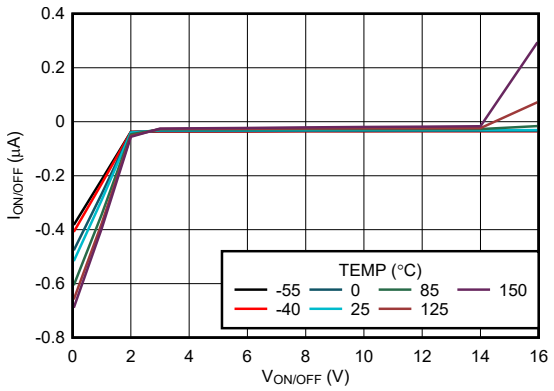
図 5-54. ON/ $\overline{\text{OFF}}$ Pin Current versus $V_{ON/\overline{OFF}}$ (Legacy Chip)

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V_{IN} = 4.3 V

図 5-55. ON/ $\overline{OFF}$ Pin Current versus $V_{ON/\overline{OFF}}$ (New Chip)



V_{IN} = 16.0 V

図 5-56. ON/ $\overline{OFF}$ Pin Current versus $V_{ON/\overline{OFF}}$ (New Chip)

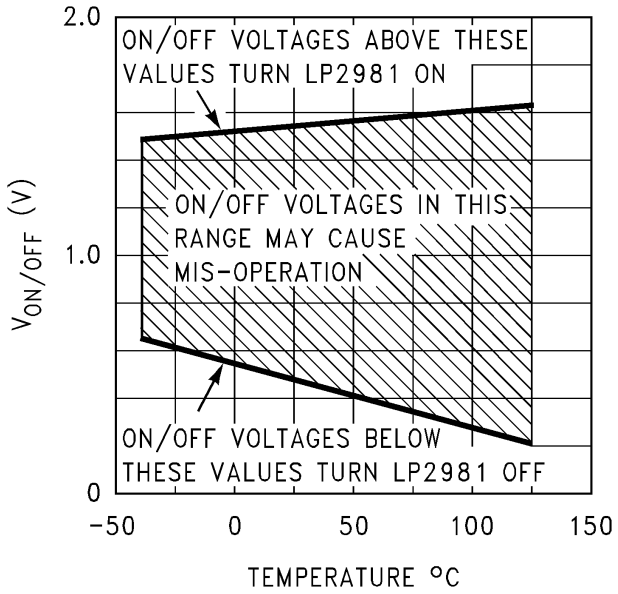


図 5-57. ON/ $\overline{OFF}$ Threshold versus Temperature (Legacy Chip)

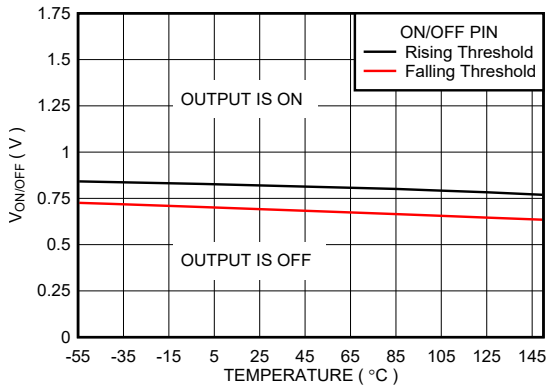


図 5-58. ON/ $\overline{OFF}$ Threshold versus Temperature (New Chip)

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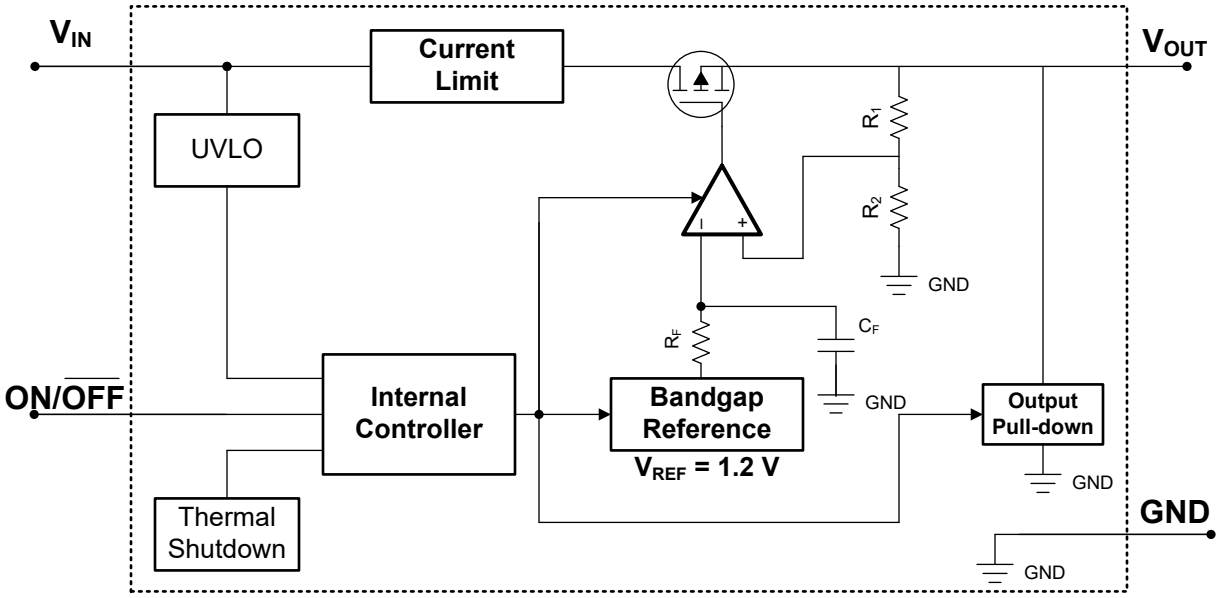
6 Detailed Description

6.1 Overview

The LP2981-N is a fixed-output, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and non-portable applications. The LP2981-N has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 100 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled when the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

For the new chip, the device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *セクション 5.3* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

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$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the current limit.

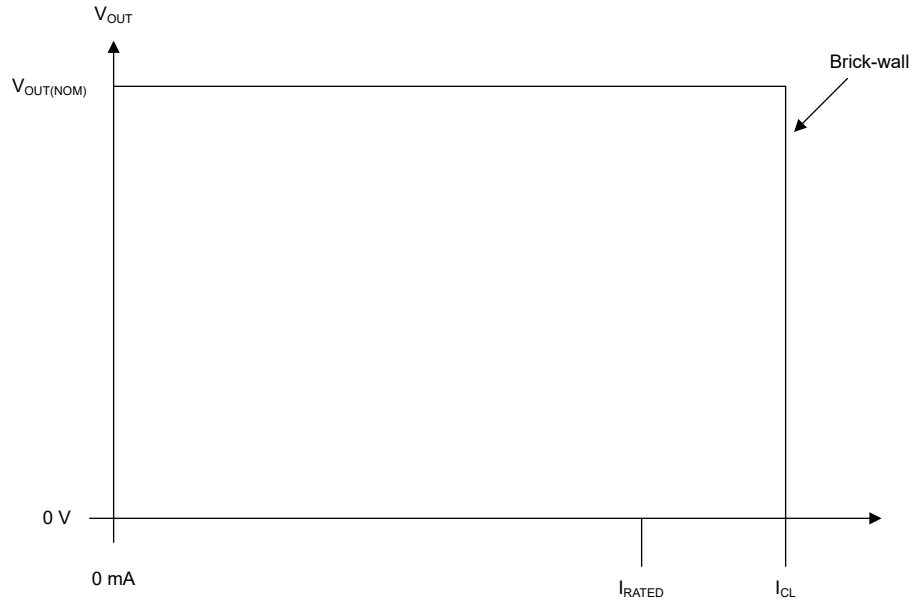


図 6-1. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

For the new chip, the device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *セクション 5.5* table.

6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). Limits for Thermal shutdown circuit are defined in *セクション 5.5*.

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

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For reliable operation, limit the junction temperature to the maximum listed in the *セクション 5.3* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.6 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < V_{IN} < V_{UVLO}

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *セクション 7.1.5* section for more details.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See the *セクション 5.5* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{OFF}$ voltage has previously exceeded the ON/$\overline{OFF}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

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6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *セクション 5.5* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The LP2981-N is a linear voltage regulator operating from 2.5 V to 16 V (for new chip) on the input and regulates voltages between 1.2 V to 5 V with ±1% accuracy (across line, load and temperature) and 100-mA maximum output current.

Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified for a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

7.1.1 Recommended Capacitor Types

7.1.1.1 Recommended Capacitors for the Legacy Chip

Tantalum Capacitors: For the legacy chip LP2981-N, tantalum capacitors are the best choice for use at the output of the LDO. Most good quality tantalums can be used with the LP2981-N, but check the manufacturer's data sheet to be sure the ESR is in range. At lower temperatures, as ESR increases, a capacitor with ESR, near the upper limit for stability at room temperature can cause instability. For very low temperature applications, output tantalum capacitors can be used in parallel configuration to prevent the ESR from going up too high.

Ceramic Capacitors: For the legacy chip LP2981-N, ceramic capacitors are not recommended for use at the output of the LDO. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2981-N. A 2.2-µF ceramic was measured and found to have an ESR of about 15 mΩ, which is low enough to cause oscillations.If a ceramic capacitor is used on the output, a 1-Ω resistor is required be placed in series with the capacitor.

Aluminum Capacitors: For the legacy chip LP2981-N, aluminum electrolytics are not typically used with the LDO, because of the large physical size. These aluminimum capacitors must meet the same ESR requirements over the operating temperature range, more difficult because of their steep increase at cold temperature. An aluminum electrolytic can exhibit an ESR increase of as much as 50x when going from 20°C to −40°C. Also, some aluminum electrolytics are not operational below −25°C because the electrolyte can freeze.

7.1.1.2 Recommended Capacitors for the New Chip

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output

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capacitors listed in the *セクション 5.3* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Input capacitor:

For the legacy chip, an input capacitor (C_{IN}) ≥1 µF is required (the amount of capacitance can be increased without limit). Any good-quality tantalum or ceramic capacitor can be used. The capacitor must be located no more than half an inch from the input pin and returned to a clean analog ground.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Output capacitor:

For the legacy chip, The output capacitor must meet both the requirement for minimum amount of capacitance and equivalent series resistance (ESR) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to 図 7-3, 図 7-4, 図 7-5, and 図 7-6).

For the new chip, Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor, preferably ceramic capacitors, within the range specified in the *セクション 5.3* table for stability.

7.1.3 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (2)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (3)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

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7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (4)$$

注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ can be improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

図 7-1 shows one approach for protecting the device.

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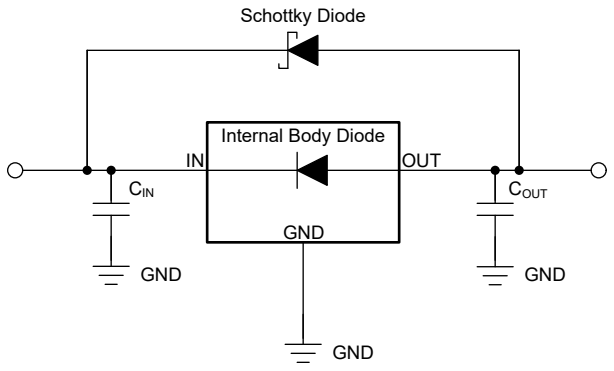
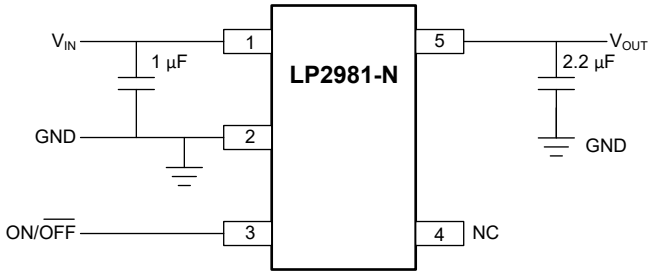


図 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2 Typical Application



*ON/ $\overline{\text{OFF}}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used. Minimum output capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin (see *セクション 7.1.1*).

図 7-2. LP2981-N Typical Application

7.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V ±10%, provided by the DC-DC converter switching at 1 MHz
Output voltage	3.3 V ±1%
Output current	100 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50 kHz	< 1 mV_{RMS}
PSRR at 1 kHz	> 40 dB

7.2.2 Detailed Design Procedure

7.2.2.1 ON and $\overline{\text{OFF}}$ Input Operation

The LP2981-N is shut off by pulling the ON/ $\overline{\text{OFF}}$ input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input is required to be tied to V_{IN} to keep the regulator on at all times (the ON/ $\overline{\text{OFF}}$ input must **not** be left floating).

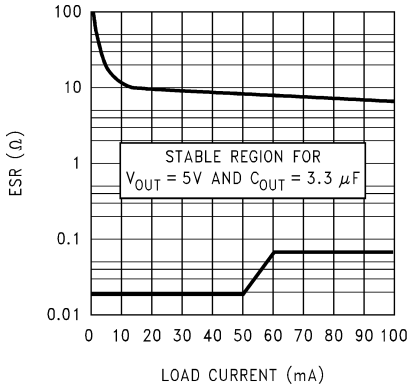
For proper operation of the LDO, the signal source used to drive the ON/ $\overline{\text{OFF}}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds which specify an ON or $\overline{\text{OFF}}$ state (see *セクション 5.5*).

The ON/ $\overline{\text{OFF}}$ signal can come from either a totem-pole output, or an open-collector output with pullup resistor to the LP2981-N input voltage or another logic supply. The high-level voltage can exceed the LP2981-N input voltage, but must remain within the *セクション 5.1* for the ON/ $\overline{\text{OFF}}$ pin.

For the legacy chip only, it is also important that the turnon/turnoff voltage signals applied to the ON/ $\overline{\text{OFF}}$ input have a slew rate which is greater than 40 mV/µs.

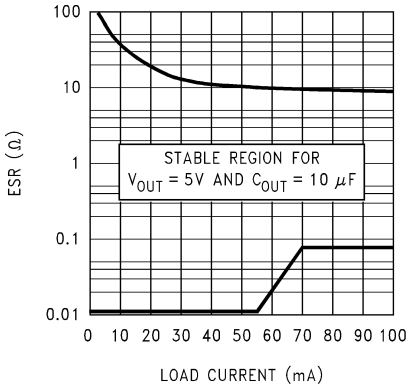
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7.2.3 Application Curves



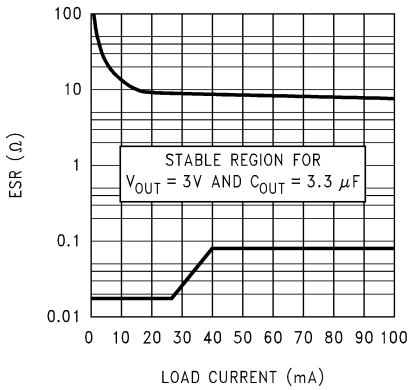
V_{OUT} = 5 V, C_{OUT} = 3.3 µF

図 7-3. 5-V, 3.3-µF ESR Curves (Legacy Chip)



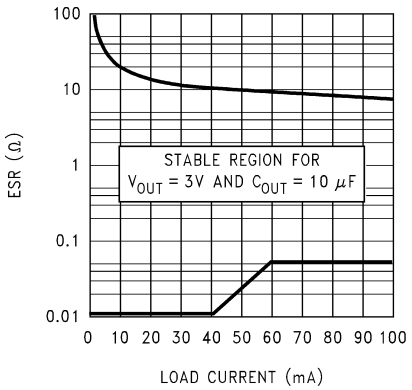
V_{OUT} = 5 V, C_L = 10 µF

図 7-4. 5-V, 10-µF ESR Curves (Legacy Chip)



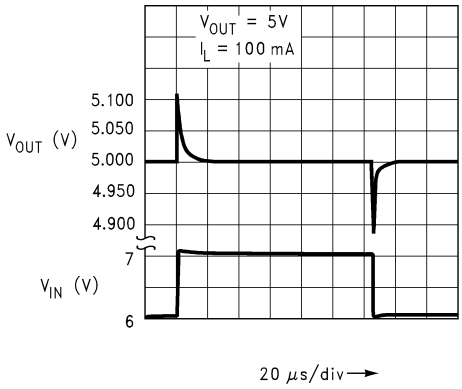
V_{OUT} = 3.0 V, C_{OUT} = 3.3 µF

図 7-5. 3.0-V, 3.3-µF ESR Curves (Legacy Chip)



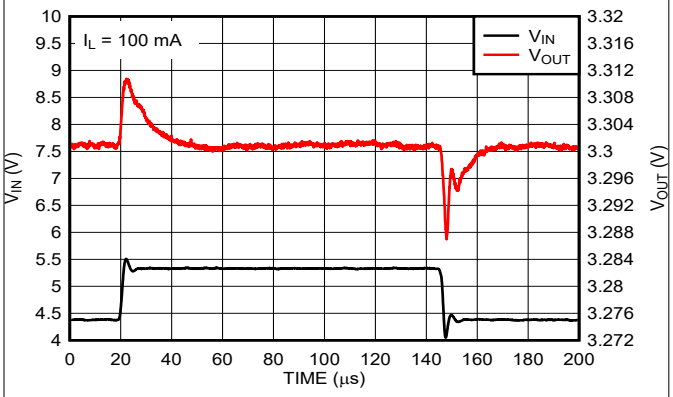
V_{OUT} = 3.0 V, C_L = 10 µF

図 7-6. 3.0-V, 10-µF ESR Curves (Legacy Chip)



V_{OUT} = 5 V, I_L = 100 mA

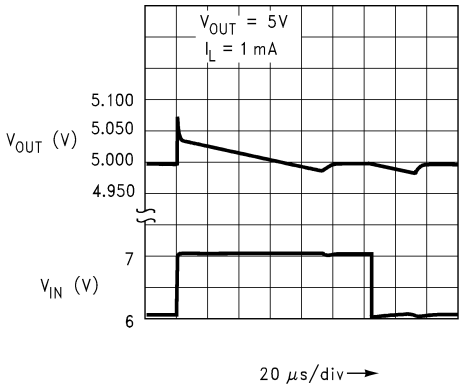
図 7-7. Line Transient Response (Legacy Chip)



V_{OUT} = 3.3 V, I_L = 100 mA

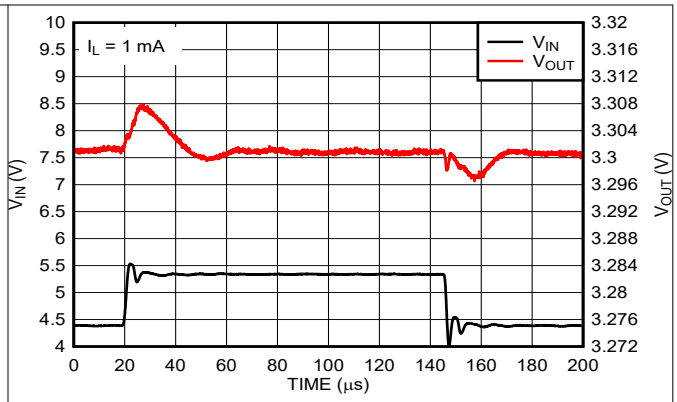
図 7-8. Line Transient Response (New Chip)

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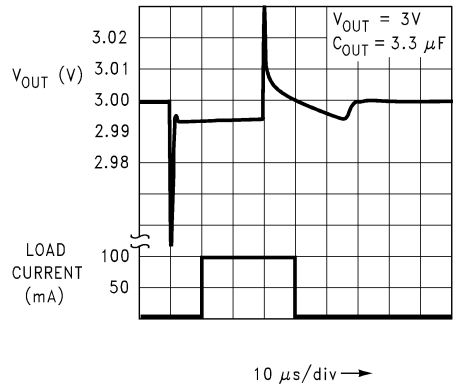
V_{OUT} = 5 V, I_L = 1 mA

図 7-9. Line Transient Response (Legacy Chip)



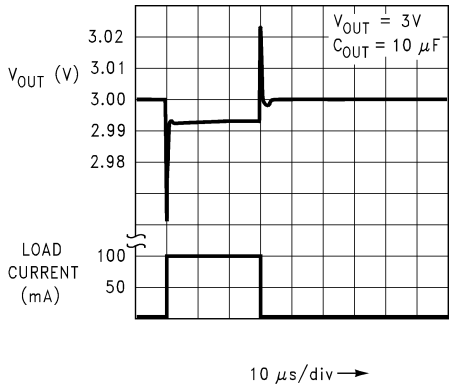
V_{OUT} = 3.3 V, I_L = 1 mA

図 7-10. Line Transient Response (New Chip)



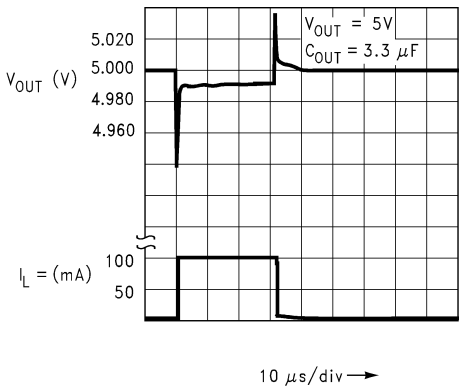
V_{OUT} = 3.0 V, C_{OUT} = 3.3 µF

図 7-11. Load Transient Response (Legacy Chip)



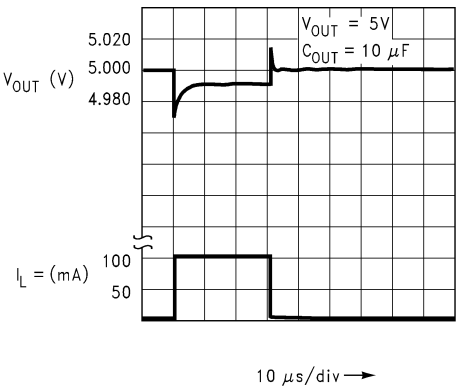
V_{OUT} = 3.0 V, C_{OUT} = 10 µF

図 7-12. Load Transient Response (Legacy Chip)



V_{OUT} = 5.0 V, C_{OUT} = 3.3 µF

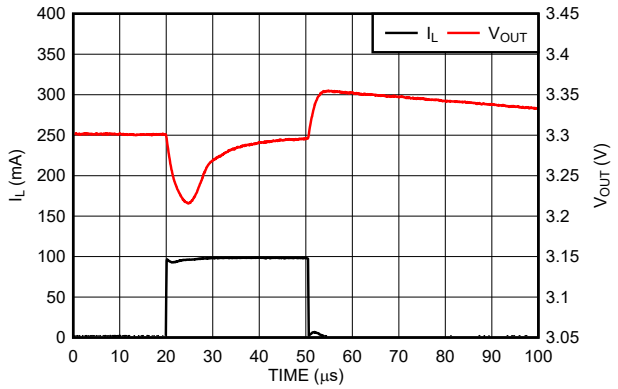
図 7-13. Load Transient Response (Legacy Chip)



V_{OUT} = 5.0 V, C_{OUT} = 10 µF

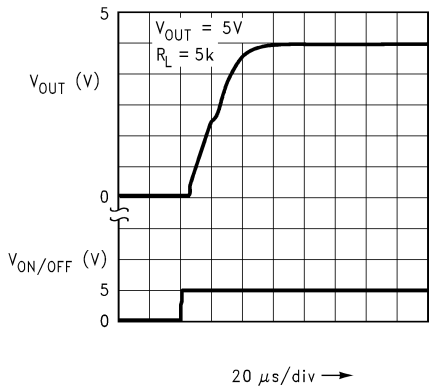
図 7-14. Load Transient Response (Legacy Chip)

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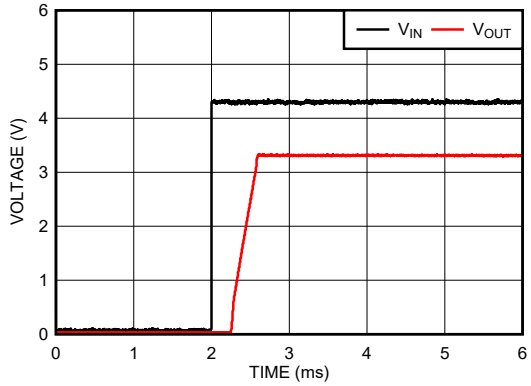
V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

図 7-15. Load Transient Response (New Chip)



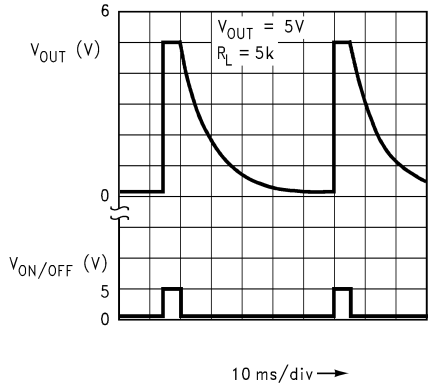
V_{OUT} = 5 V, R_L = 5 kΩ

図 7-16. Turn-on Waveform (Legacy Chip)



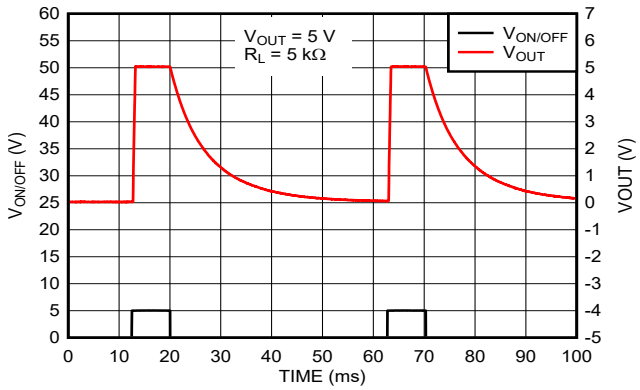
V_{OUT} = 3.3 V, R_L = 3.3 kΩ

図 7-17. Turn-on Waveform (New Chip)



V_{OUT} = 5 V, R_L = 5 kΩ

図 7-18. Turn-off Waveform (Legacy Chip)



V_{OUT} = 5 V, R_L = 5 kΩ

図 7-19. Turn-off Waveform (New Chip)

8 Power Supply Recommendations

The LP2981-N is designed to operate from an input voltage supply range between 2.5 V and 16 V (for the new chip). The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9 Layout

9.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves for the accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

9.2 Layout Example

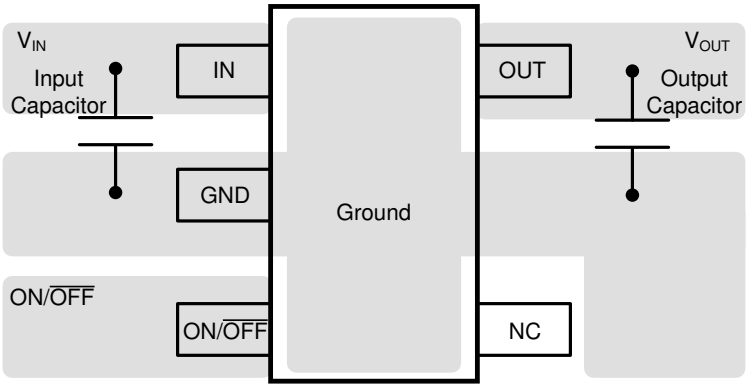


図 9-1. LP2981-N Layout Example

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10 Device and Documentation Support

10.1 Device Nomenclature

表 10-1. Available Options

PRODUCT	V_{OUT}
LP2981**cxxxzX-y.y**/NOPB Legacy chip	**c** is the accuracy specification. **xxx** is the package designator. **z** is the package quantity. **X** is for a large-quantity reel and non-X is for a small-quantity reel. **y.y** is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V).
LP2981**AxxxzX-y.y/M3** New chip	**A** is for higher accuracy and non-A is for standard grade. **xxx** is the package designator. **z** is the package quantity. **X** is for a large-quantity reel and non-X is for a small-quantity reel **y.y** is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). **M3** is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

10.2 サード・パーティ製品に関する免責事項

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10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Related Documentation

For related documentation see the following:

- Texas Instruments, *LDO Noise Demystified*, application note
- Texas Instruments, *LDO PSRR Measurement Simplified*, application note
- Texas Instruments, *A Topical Index of TI LDO Application Notes*, application note

10.5 サポート・リソース

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10.7 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from , to , (from Revision N (April 2016) to Revision O (December 2023))	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 現在のファミリのフォーマットに合わせてドキュメント全体を変更	1
• ドキュメントに M3 デバイスを追加	1
• 「Nine」を「Assorted」に変更	1
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 代表的なアプリケーションの図を更新し、ピン名を Vin、Vout から IN、OUT に変更	1
• Changed layout of National Data Sheet to TI format	24
• Added *Device Nomenclature* section	29
• Added three references to *Related Documentation*	29

Changes from Revision M (September 2015) to Revision N (April 2016)	Page
• 代表的なアプリケーションの図を更新し、ピン名を Vin、Vout から IN、OUT に変更	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2981AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L04A	Samples
LP2981AIM5-3.6/NOPB	LIFEBUY	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0JA	
LP2981AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L03A	Samples
LP2981AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L04A	Samples
LP2981AIM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0JA	Samples
LP2981AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L03A	Samples
LP2981IM5-2.5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L0CB	
LP2981IM5-3.3	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L04B	
LP2981IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L04B	Samples
LP2981IM5-3.6/NOPB	LIFEBUY	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0JB	
LP2981IM5-5.0	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L03B	
LP2981IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L03B	Samples
LP2981IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L05B	Samples
LP2981IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L04B	Samples
LP2981IM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0JB	Samples
LP2981IM5X-5.0	LIFEBUY	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L03B	
LP2981IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L03B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

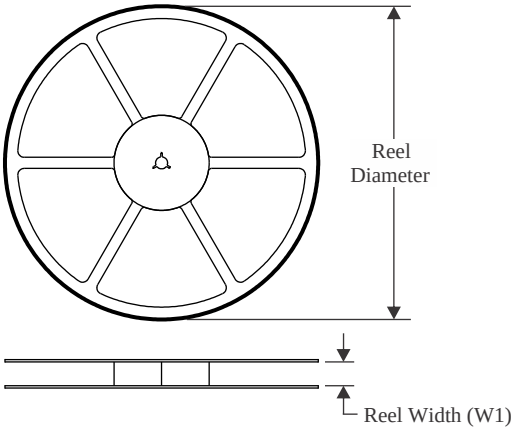
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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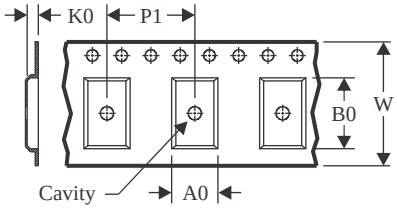
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

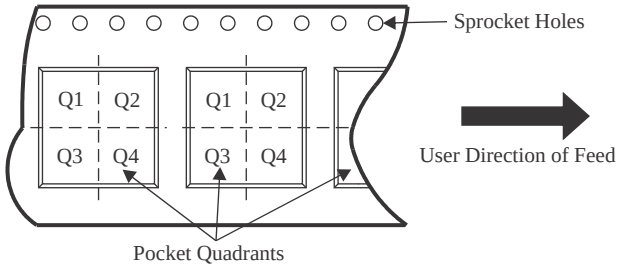


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

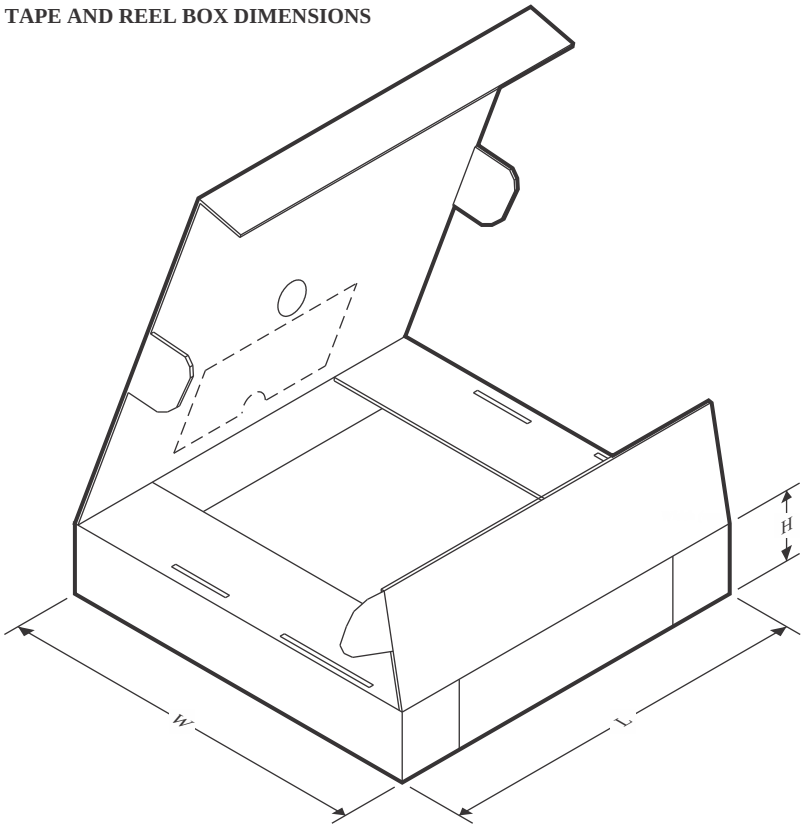


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2981AIM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.6/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2981IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

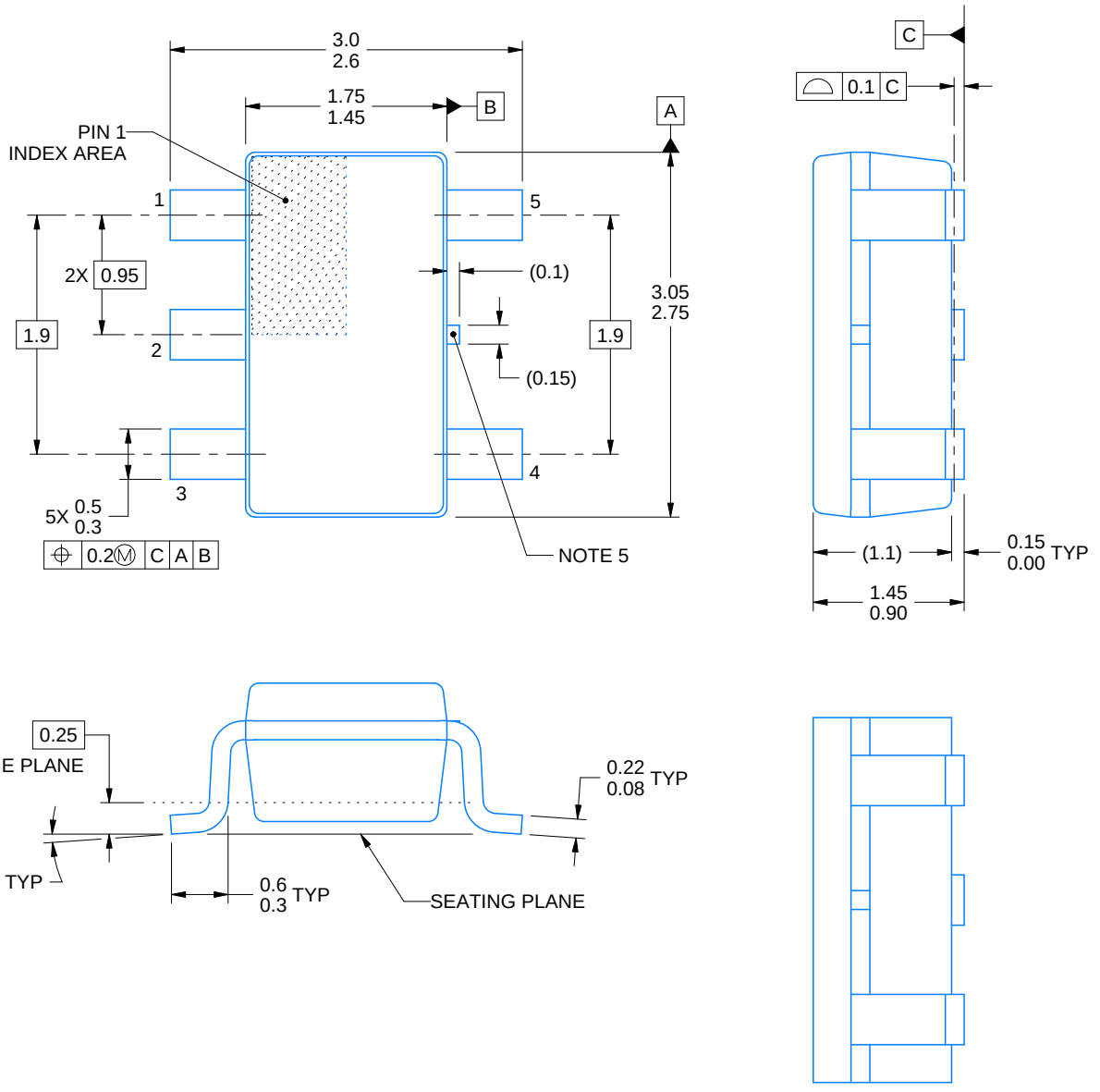
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2981AIM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981AIM5-3.6/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2981AIM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5-2.5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2981IM5-3.3	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2981IM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5-3.6/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2981IM5-5.0	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2981IM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5X-5.0	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2981IM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

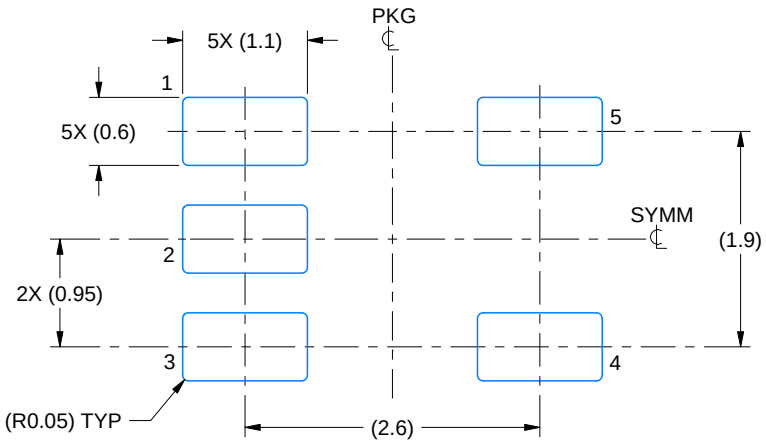


ALTERNATIVE PACKAGE SINGULATION VIEW

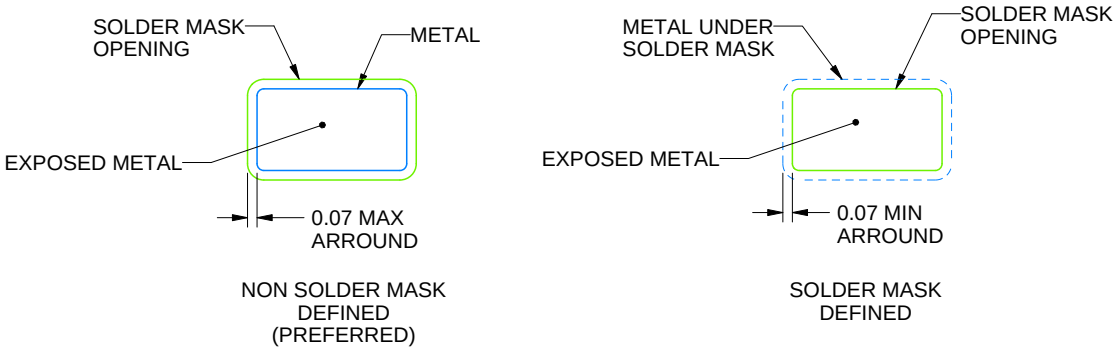
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

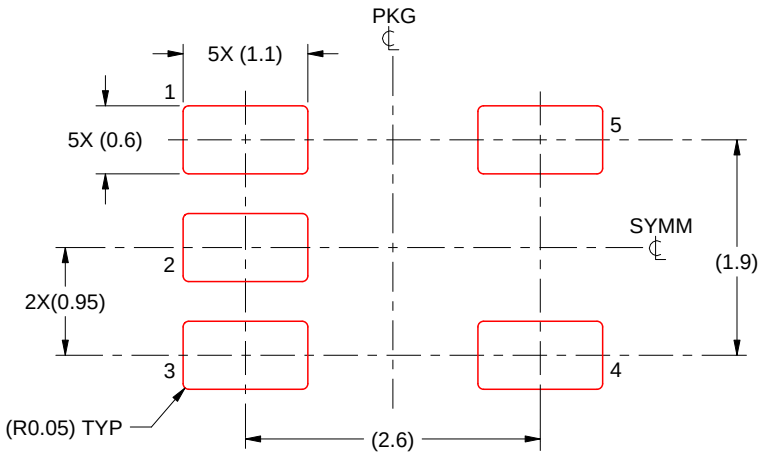


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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