TEXAS INSTRUMENTS
LP5912-EP
JAJSMX5 – JULY 2022

LP5912-EP エンハンスド製品、500mA、低ノイズ、低 I_Q LDO

1 特長

- 入力電圧範囲:1.6 V～6.5 V
- 出力電圧範囲:0.8V～5.5V
- 出力電流:最大 500mA
- 低い出力電圧ノイズ:12μV_{RMS} (標準値)
- PSRR (1kHz 時):75 dB (標準値)
- 出力電圧許容誤差 (V_{OUT} ≥3.3V):±2%
- 低い I_Q (イネーブル、無負荷時):30μA (標準値)
- 低いドロップアウト (V_{OUT} ≥3.3V):
  500mA 負荷で 95mV (標準値)
- 1μF のセラミック入力および出力コンデンサで安定動作
- 過熱および短絡保護
- 逆電流保護
- ノイズ・バイパス・コンデンサが不要
- 自動出力放電による高速なターンオフ
- 140μs (標準値) の遅延を持つパワー・グッド出力
- 内部ソフトスタートにより突入電流を制限
- 動作時接合部温度:–55℃～+125℃
- 防衛、航空宇宙、医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリおよびテスト施設
  - 単一の製造施設
  - 長い製品ライフ・サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ

2 アプリケーション

- 監視システム
- 慣性航法
- 陸上移動無線
- GPS レシーバ
- データ・コンセントレータ・ユニット

3 概要

LP5912-EP は、最大 500mA の出力電流を供給できる低ノイズ LDO です。RF 回路およびアナログ回路の要件を満たすよう設計された LP5912-EP は、低ノイズ、高 PSRR、低静止電流、ラインおよび負荷の優れた過渡応答といった特徴を備えています。LP5912-EP は、ノイズ・バイパス用コンデンサなしでクラス最高レベルの優れたノイズ特性を実現し、出力コンデンサのリモート配置も選択できます。

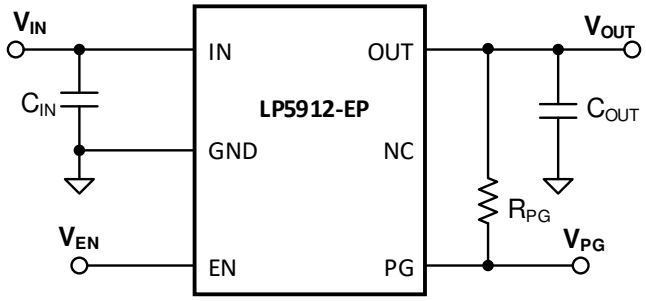
このデバイスは、入力および出力に 1μF のセラミック・コンデンサを使用して動作するよう設計されています(個別にノイズ・バイパス・コンデンサを用意する必要はありません)。

このデバイスでは、0.8V～5.5V (25mV ステップ) の固定出力電圧を使用できます。具体的な電圧オプションについては、テキサス・インスツルメンツの販売部門までお問い合わせください。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
LP5912-EP	WSON (6)	2.00mm × 2.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2022	*	Initial Release

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5 Pin Configuration and Functions

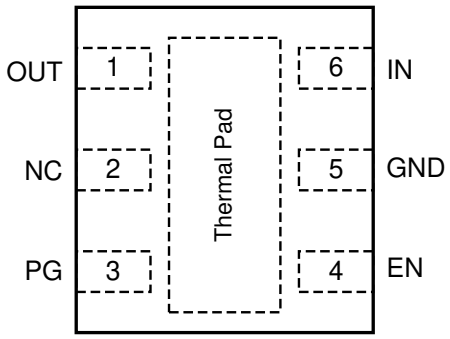

図 5-1. DRV Package, 6-Pin WSON With Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	O	Regulated output voltage.
2	NC	—	No internal connection. Leave open, or connect to ground.
3	PG	O	Power-good indicator. Requires an external pullup resistor.
4	EN	I	Enable input. Logic high = device is on, logic low = device is off, with an internal 3-MΩ pulldown resistor.
5	GND	G	Ground.
6	IN	I	Unregulated input voltage.
Thermal pad		—	Connect this pad to the copper area under the package to improve thermal performance. Use thermal vias to transfer heat to inner layers of the printed circuit board (PCB). Connect the thermal pad to ground, or leave floating. Do not connect the thermal pad to any potential other than ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	IN pin voltage	–0.3	7	V
V_{OUT}	OUT pin voltage	-0.3	7	V
V_{EN}	EN pin voltage	–0.3	7	V
V_{PG}	PG pin voltage	–0.3	7	V
T_J	Junction temperature	–55	150	°C
P_{DISS}	Continuous power dissipation(3)	Internally Limited		W
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.6		6.5	V
V_{OUT}	Output voltage	0.8		5.5	V
V_{EN}	EN input voltage	0		V_{IN}	V
V_{PG}	PG pin off voltage	0		6.5	V
I_{OUT}	Output current	0		500	mA
$T_{J-MAX-OP}$	Operating junction temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP5912-EP DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.6 V, whichever is greater; V_{EN} = 1.35 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA (unless otherwise stated).(1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE AND REGULATION						
ΔV_{OUT}	Output voltage tolerance	For $V_{OUT(NOM)}$ ≥ 3.3 V, $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA	-2		2	%
		For 1.1 V ≤ $V_{OUT(NOM)}$ < 3.3 V, $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA	-3		3	
		For $V_{OUT(NOM)}$ < 1.1 V, 1.6 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 1 mA to 500 mA				
	Line regulation	For $V_{OUT(NOM)}$ ≥ 1.1V, $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V		0.8		%/V
		For $V_{OUT(NOM)}$ < 1.1 V, 1.6 V ≤ V_{IN} ≤ 6.5 V				
	Load regulation	For I_{OUT} = 1mA to 500 mA		0.0022		%/mA
CURRENT LEVELS						
I_{SC}	Short-circuit current limit	T_J = 25°C, (4)	700	900	1100	mA
I_{RO}	Reverse leakage current (5)	V_{IN} < V_{OUT}		10	150	µA
I_Q	Quiescent current (6)	V_{EN} = 1.35 V, I_{OUT} = 0 mA		30	55	µA
		V_{EN} = 1.35 V, I_{OUT} = 500 mA		400	600	
$I_{Q(SD)}$	Quiescent current shutdown mode (6)	V_{EN} = 0 V, –55°C ≤ T_J ≤ 85°C		0.2	1.5	µA
		V_{EN} = 0 V		0.2	5	
I_G	Ground-current (7)	V_{EN} = 1.35 V, I_{OUT} = 0 mA		35		µA
VDO DROPOUT VOLTAGE						
V_{DO}	Dropout voltage (8)	I_{OUT} = 500 mA, 1.6 V ≤ $V_{OUT(NOM)}$ < 3.3 V		170	250	mV
		I_{OUT} = 500 mA, 3.3 V ≤ $V_{OUT(NOM)}$ ≤ 5.5 V		95	180	mV
V_{IN} to V_{OUT} RIPPLE REJECTION						
PSRR	Power-supply rejection ratio (9)	f = 100 Hz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		80		dB
		f = 1 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		75		
		f = 10 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		65		
		f = 100 kHz, V_{OUT} ≥ 1.1 V, I_{OUT} = 20 mA		40		
		f = 100 Hz, 0.8V ≤ V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 1 kHz, 0.8V ≤ V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 10 kHz, 0.8V ≤ V_{OUT} < 1.1 V, I_{OUT} = 20 mA		65		
		f = 100 kHz, 0.8V ≤ V_{OUT} < 1.1 V, I_{OUT} = 20 mA		40		
OUTPUT NOISE VOLTAGE						
e_N	Noise voltage	I_{OUT} = 1 mA, BW = 10 Hz to 100 kHz		12		μV_{RMS}
		I_{OUT} = 500 mA, BW = 10 Hz to 100 kHz		12		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			160		°C
T_{HYS}	Thermal shutdown hysteresis			15		°C
LOGIC INPUT THRESHOLDS						
$V_{EN(OFF)}$	Off threshold				0.25	V
$V_{EN(ON)}$	On threshold		1.35			V
I_{EN}	Input current at EN terminal (10)	V_{IN} = 6 V, V_{EN} = 6 V		3		µA
		V_{IN} = 3.3 V, V_{EN} = 0 V		0.001		µA
PG_{HYS}	PG threshold hysteresis (% of nominal V_{OUT})			4		%

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6.5 Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.6 V, whichever is greater; V_{EN} = 1.35 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA (unless otherwise stated).(1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG_{LTH}	PG low threshold (% of nominal V_{OUT})		86	90	93	%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < PG_{LTH}, sink current = 1 mA			400	mV
$I_{LKG(PG)}$	PG pin leakage current	V_{OUT} < PG_{HTH}, V_{PG} = 6 V			1	µA
TRANSITION CHARACTERISTICS						
ΔV_{OUT}	Line transients (9)	For V_{IN} ↑ and $V_{OUT(NOM)}$ ≥ 1.1 V, V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to ($V_{OUT(NOM)}$ + 1.1 V), V_{IN} trise = 30 µs			1	mV
		For V_{IN} ↑ and $V_{OUT(NOM)}$ < 1.1 V, V_{IN} = 1.6 V to 2.2 V, V_{IN} trise = 30 µs				
		For V_{IN} ↓ and $V_{OUT(NOM)}$ ≥ 1.1 V, V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to ($V_{OUT(NOM)}$ + 1.1 V), V_{IN} trise = 30 µs	-1			
		For V_{IN} ↓ and $V_{OUT(NOM)}$ < 1.1 V, V_{IN} = 1.6 V to 2.2 V, V_{IN} trise = 30 µs				
	Load transients (9)	I_{OUT} = 5 mA to 500 mA, I_{OUT} t_{RISE} = 10 µs	-45			mV
		I_{OUT} = 500 mA to 5 mA, I_{OUT} t_{FALL} = 10 µs			45	
	Overshoot on start-up (9)				5	%
t_{ON}	Turnon time	From V_{EN} > $V_{EN(ON)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$		200		µs
OUTPUT AUTO DISCHARGE RATE						
R_{AD}	Output discharge pulldown resistance	V_{EN} = 0 V, V_{IN} = 3.6 V		100		Ω

(1) All voltages are with respect to the device GND pin, unless otherwise stated.
(2) Minimum and maximum limits are specified through test, design, or statistical correlation over the junction temperature (T_J) range of –55°C to +125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation and poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{θJA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{θJA}$ × P_{D-MAX}).
(4) Short-circuit current (I_{SC}) is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(5) Reverse current (I_{RO}) is measured at the IN pin.
(6) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(7) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device (I_Q + I_{EN}).
(8) Dropout voltage (V_{DO}) is the voltage difference between the input and the output at which the output voltage drops to 150 mV below its nominal value when V_{IN} = V_{OUT} + 0.5 V. Dropout voltage is not a valid condition for output voltages less than 1.6 V as compliance with the minimum operating voltage requirement cannot be assured.
(9) This specification is specified by design.
(10) There is a 3-MΩ pulldown resistor between the EN pin and GND pin on the device.

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

	PARAMETERS	TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Input capacitance (1)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance (1)	Capacitance for stability	0.7	1	10	µF
ESR	Output voltage (1)		5		500	mΩ

(1) This specification is verified by design.

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6.7 Typical Characteristics

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)

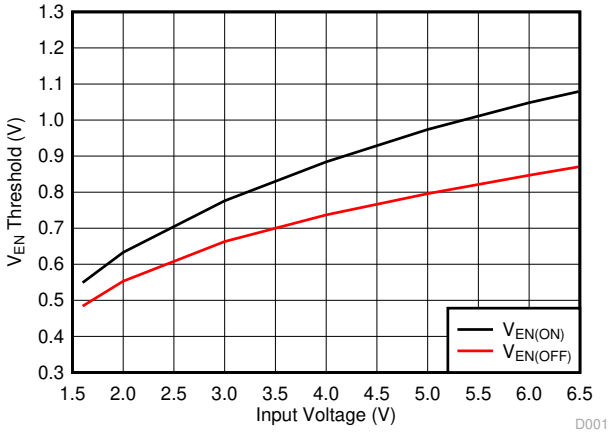


図 6-1. V_{EN} Thresholds vs Input Voltage

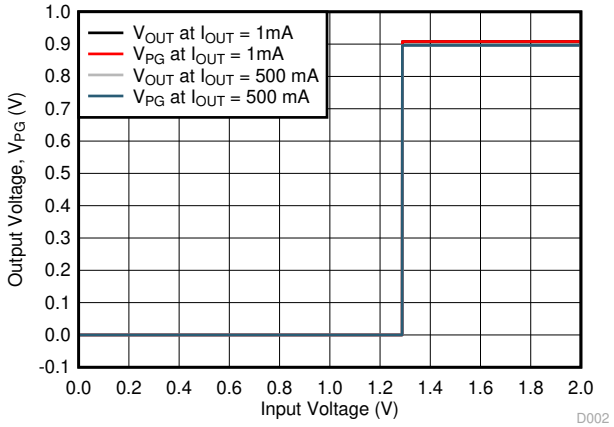


図 6-2. LP5912-0.9 Output Voltage (V_{PG}) vs Input Voltage

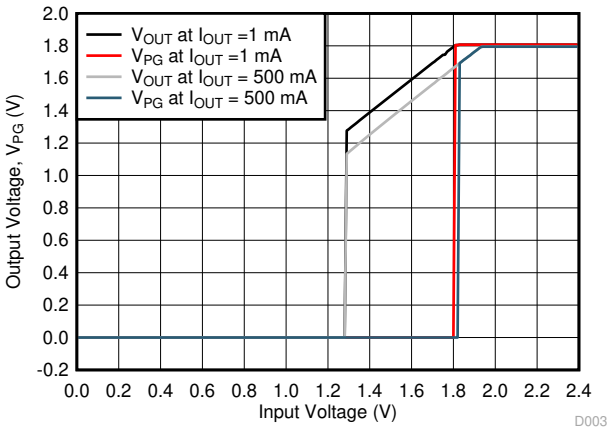


図 6-3. LP5912-1.8 Output Voltage (V_{PG}) vs Input Voltage

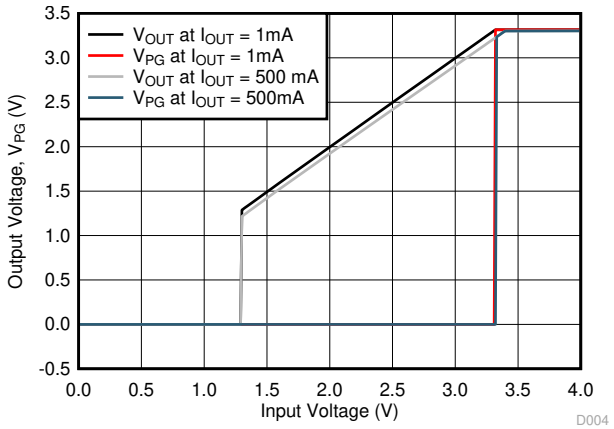
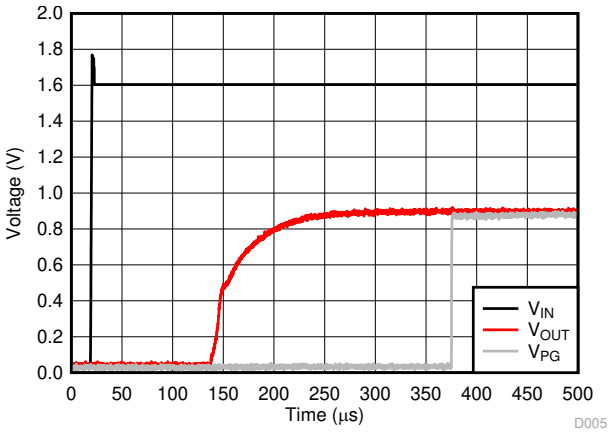
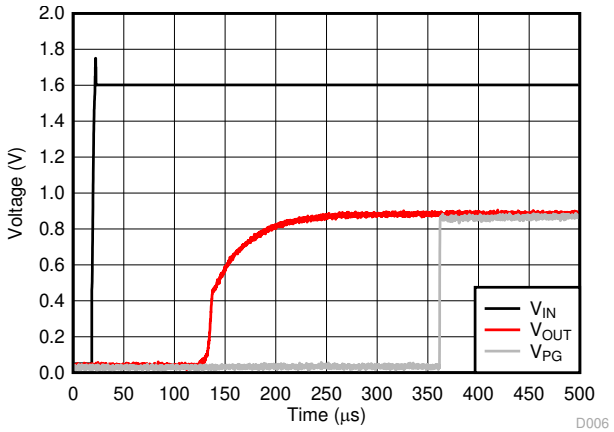


図 6-4. LP5912-3.3 Output Voltage (V_{PG}) vs Input Voltage



V_{IN} = 0 V to 1.6 V, I_{OUT} = 1 mA

図 6-5. LP5912-0.9 Power Up



V_{IN} = 0 V to 1.6 V, I_{OUT} = 500 mA

図 6-6. LP5912-0.9 Power Up

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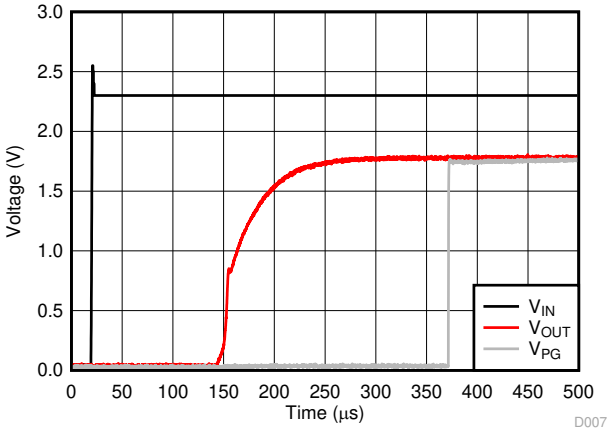
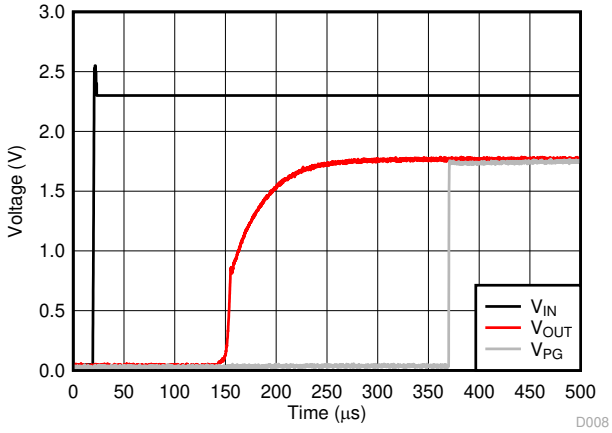
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



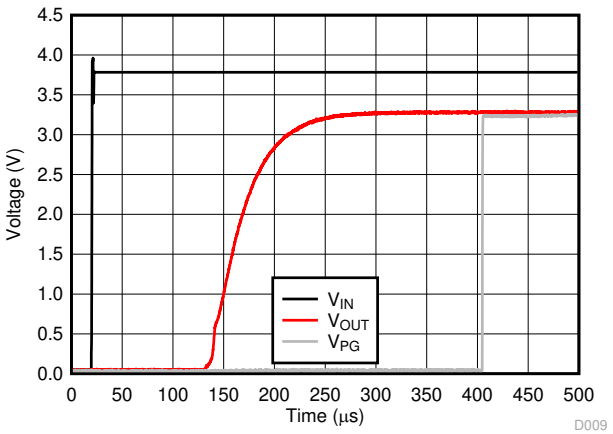
V_{IN} = 0 V to 2.3 V, I_{OUT} = 1 mA

図 6-7. LP5912-1.8 Power Up



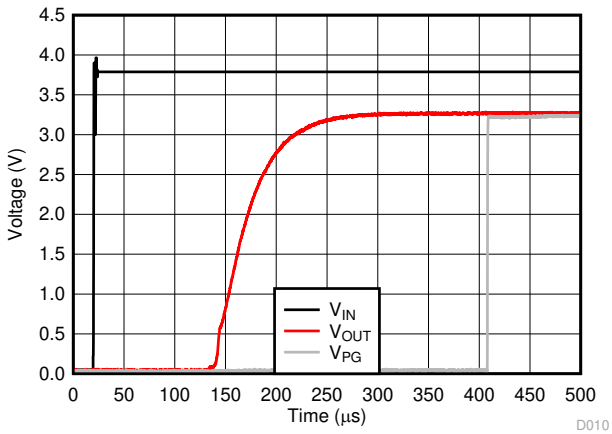
V_{IN} = 0 V to 2.3 V, I_{OUT} = 500 mA

図 6-8. LP5912-1.8 Power Up



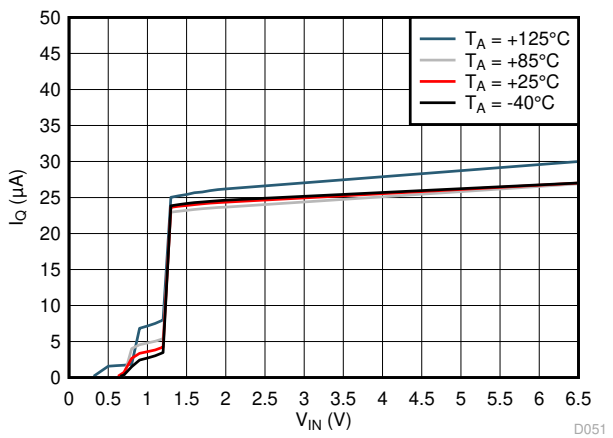
V_{IN} = 0 V to 3.8 V, I_{OUT} = 1 mA

図 6-9. LP5912-3.3 Power Up



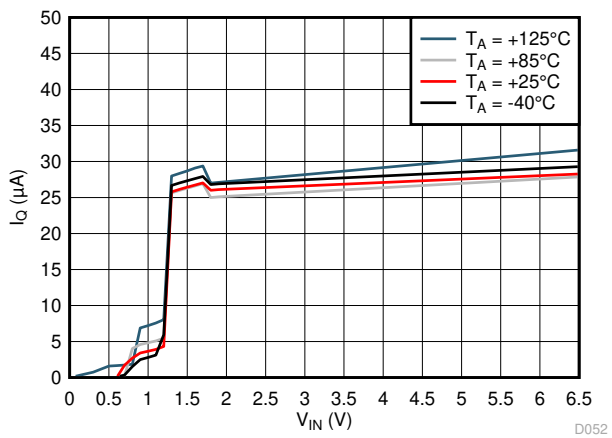
V_{IN} = 0 V to 3.8 V, I_{OUT} = 500 mA

図 6-10. LP5912-3.3 Power Up



I_{OUT} = 0 mA

図 6-11. LP5912-0.9 I_Q (No Load) vs V_{IN}



I_{OUT} = 0 mA

図 6-12. LP5912-1.8 I_Q (No Load) vs V_{IN}

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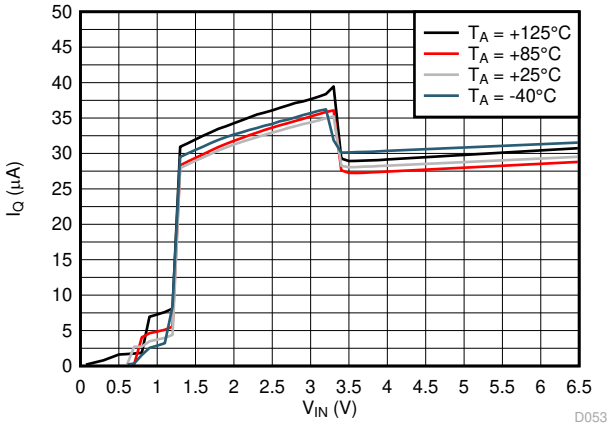
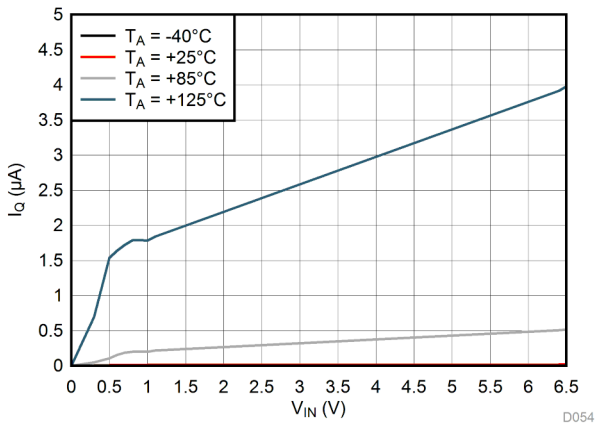
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



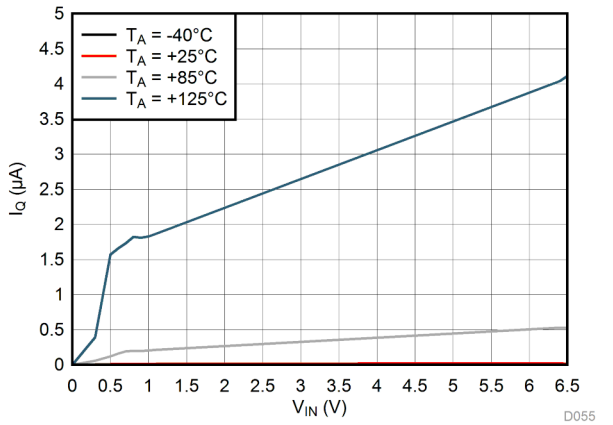
I_{OUT} = 0 mA

図 6-13. LP5912-3.3 I_Q (No Load) vs V_{IN}



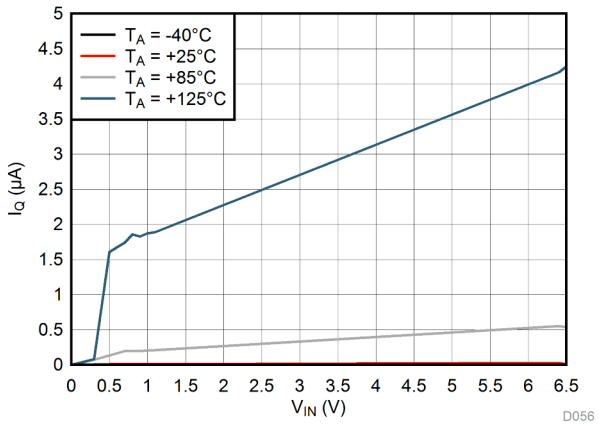
V_{EN} = 0 V

図 6-14. LP5912-0.9 $I_{Q(SD)}$ vs V_{IN}



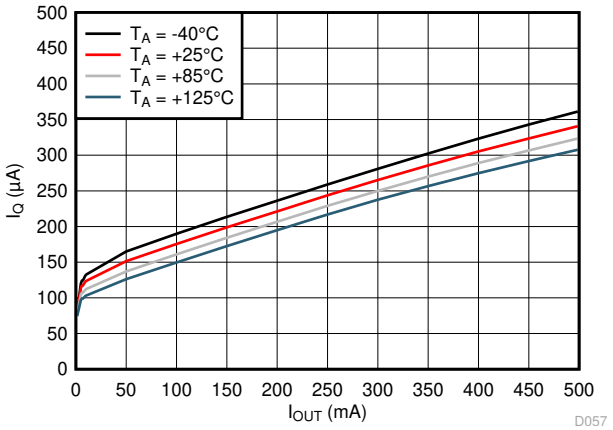
V_{EN} = 0 V

図 6-15. LP5912-1.8 $I_{Q(SD)}$ vs V_{IN}



V_{EN} = 0 V

図 6-16. LP5912-3.3 $I_{Q(SD)}$ vs V_{IN}



V_{IN} = 1.6 V

図 6-17. LP5912-0.9 $I_{Q(SD)}$ vs I_{OUT}

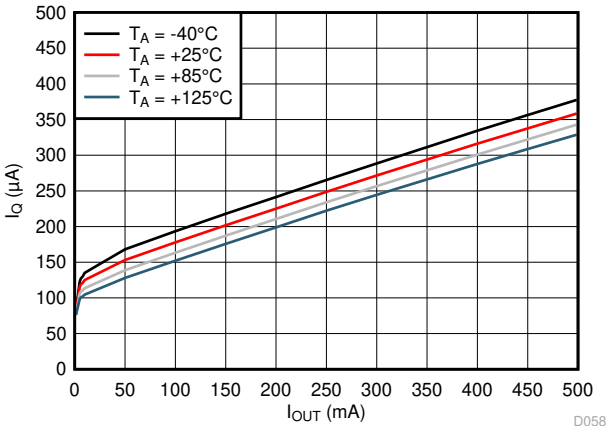


図 6-18. LP5912-1.8 $I_{Q(SD)}$ vs I_{OUT}

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6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)

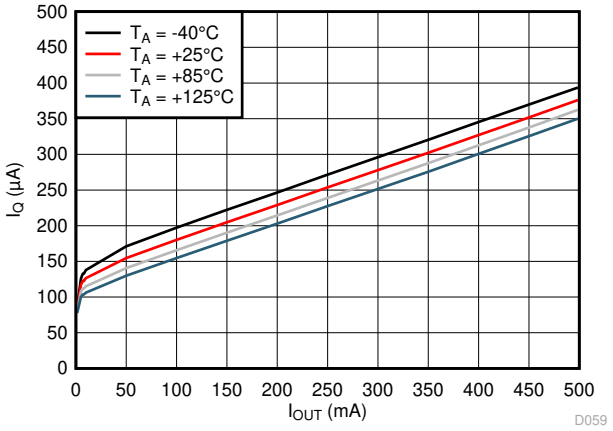
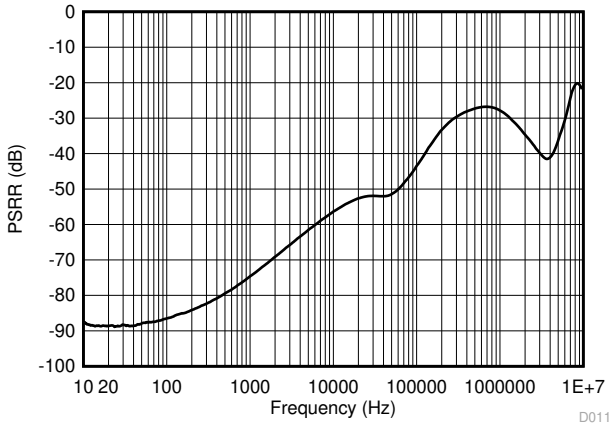
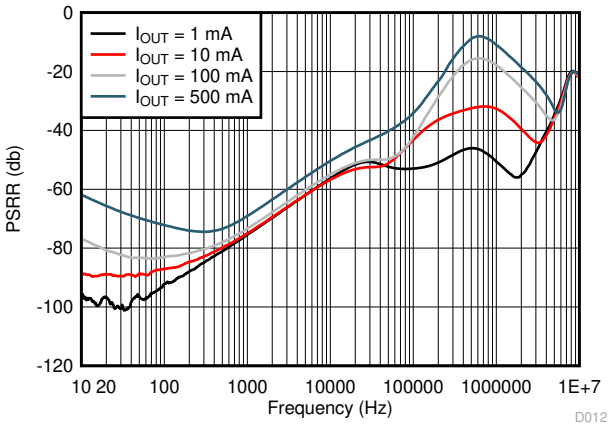


図 6-19. LP5912-3.3 $I_{Q(SD)}$ vs I_{OUT}



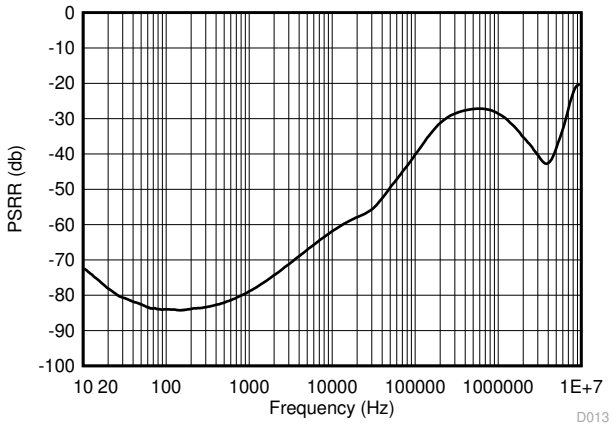
V_{IN} = 1.6 V, I_{OUT} = 20 mA

図 6-20. LP5912-0.9 PSRR vs Frequency



V_{IN} = 1.6 V

図 6-21. LP5912-0.9 PSRR vs Frequency



I_{OUT} = 20 mA

図 6-22. LP5912-1.8 PSRR vs Frequency

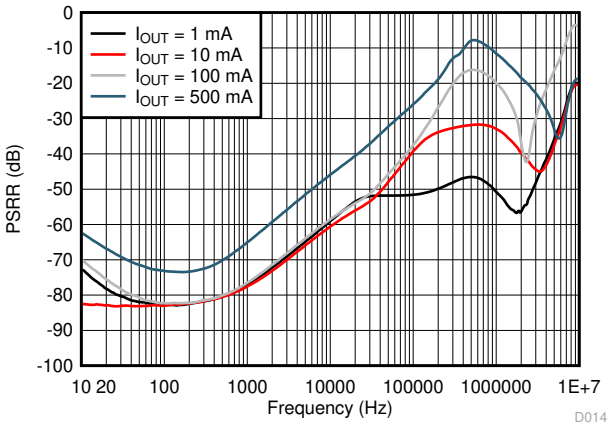
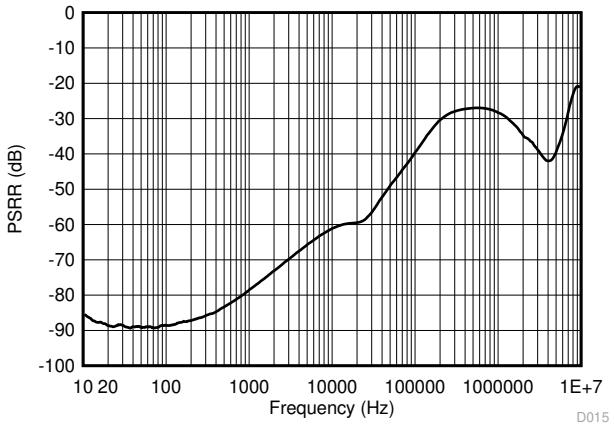


図 6-23. LP5912-1.8 PSRR vs Frequency



I_{OUT} = 20 mA

図 6-24. LP5912-3.3 PSRR vs Frequency

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6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)

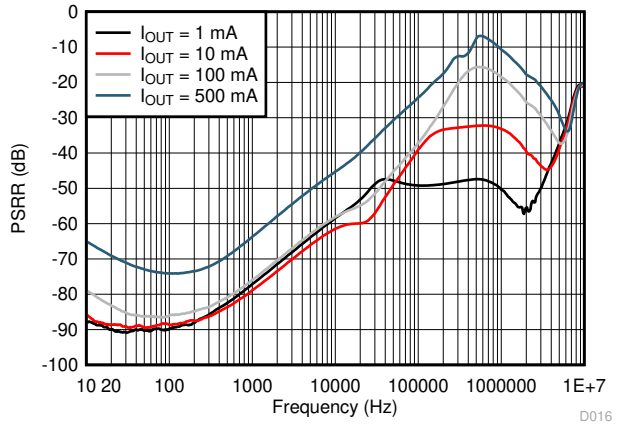
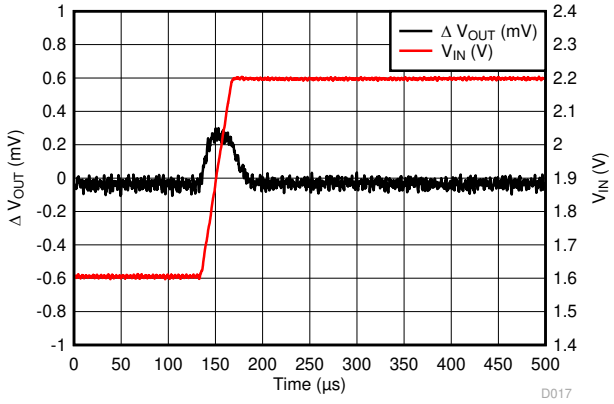
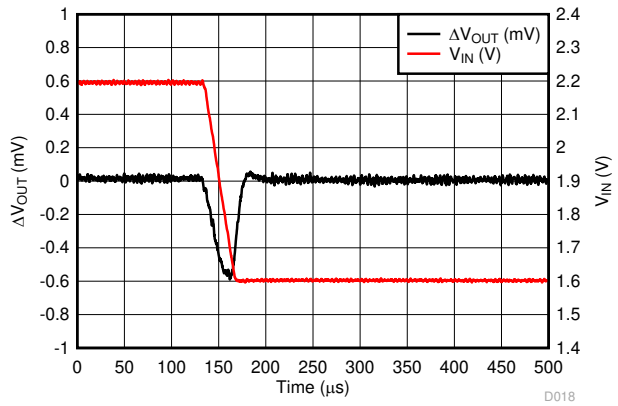


図 6-25. LP5912-3.3 PSRR vs Frequency



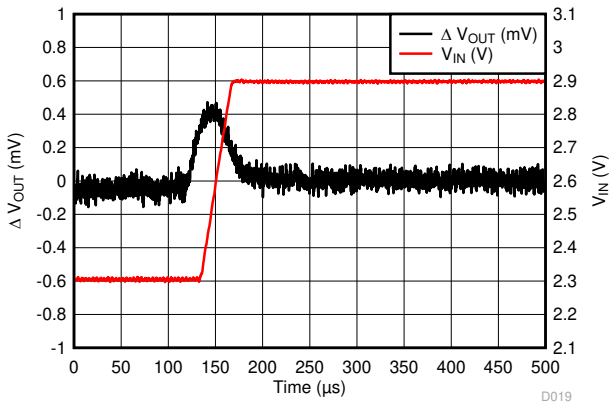
V_{IN} = 1.6 V to 2.2 V, t_r = 30 µs

図 6-26. LP5912-0.9 Line Transient



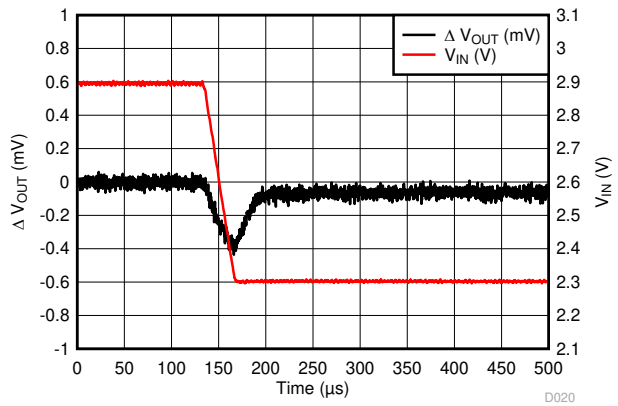
V_{IN} = 2.2 V to 1.6 V, t_f = 30 µs

図 6-27. LP5912-0.9 Line Transient



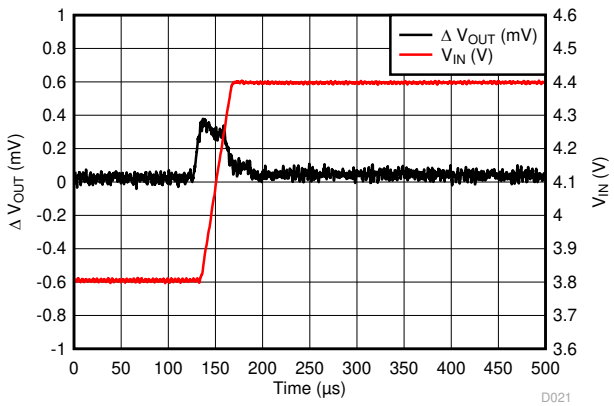
V_{IN} = 2.3 V to 2.9 V, t_r = 30 µs

図 6-28. LP5912-1.8 Line Transient



V_{IN} = 2.9 V to 2.3 V, t_f = 30 µs

図 6-29. LP5912-1.8 Line Transient



V_{IN} = 3.8 V to 4.4 V, t_r = 30 µs

図 6-30. LP5912-3.3 Line Transient

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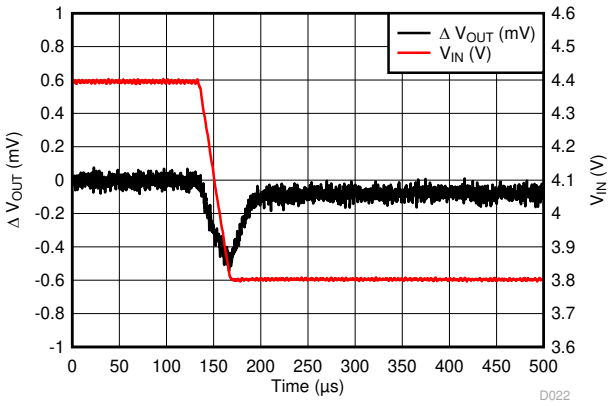
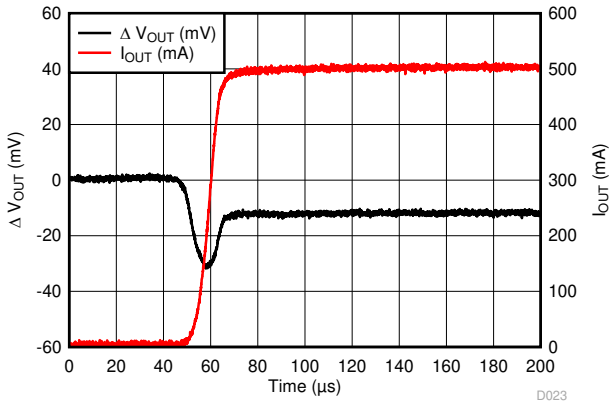
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



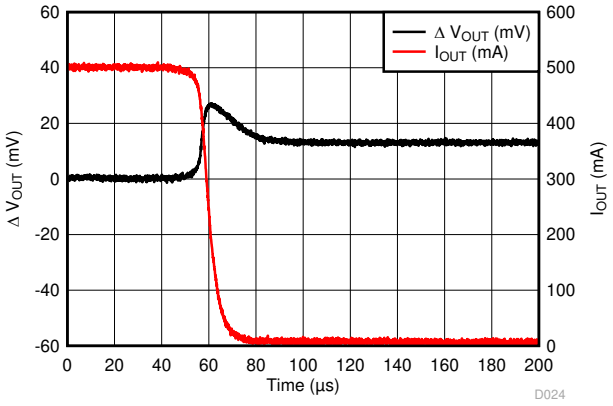
V_{IN} = 4.4 V to 3.8 V, t_f = 30 µs

図 6-31. LP5912-3.3 Line Transient



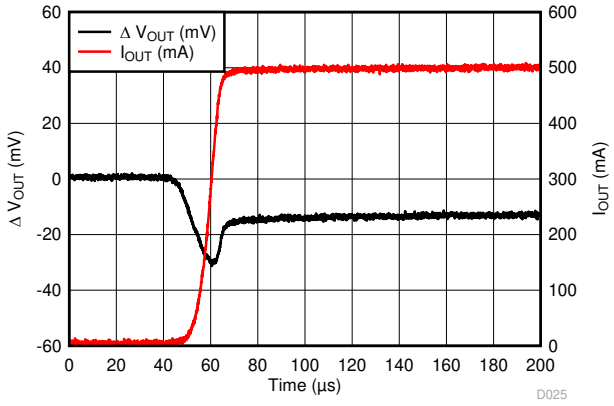
V_{IN} = 1.6 V, I_{OUT} = 5 mA to 500 mA, t_r = 10 µs

図 6-32. LP5912-0.9 Load Transient Response



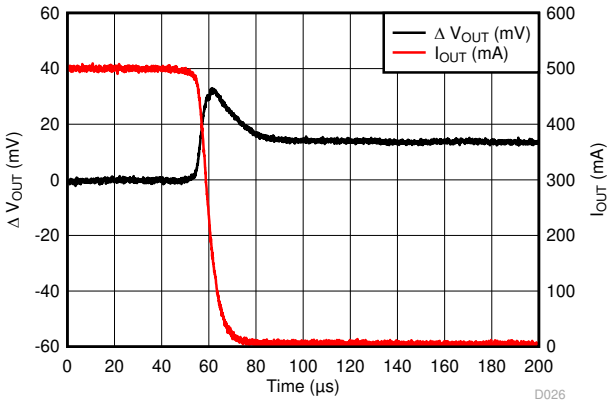
V_{IN} = 1.6 V, I_{OUT} = 500 mA to 5 mA, t_f = 10 µs

図 6-33. LP5912-0.9 Load Transient Response



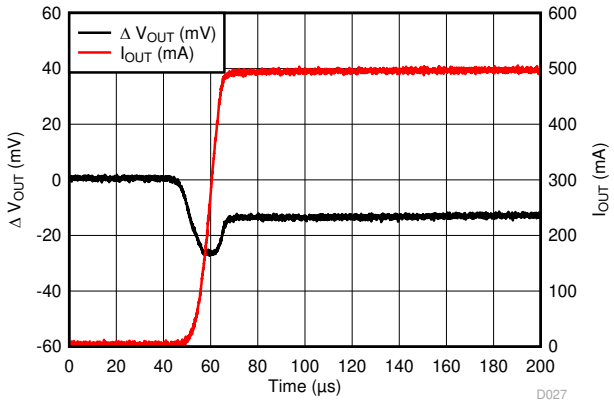
I_{OUT} = 5 mA to 500 mA, t_r = 10 µs

図 6-34. LP5912-1.8 Load Transient Response



I_{OUT} = 500 mA to 5 mA, t_f = 10 µs

図 6-35. LP5912-1.8 Load Transient Response



I_{OUT} = 5 mA to 500 mA, t_r = 10 µs

図 6-36. LP5912-3.3 Load Transient Response

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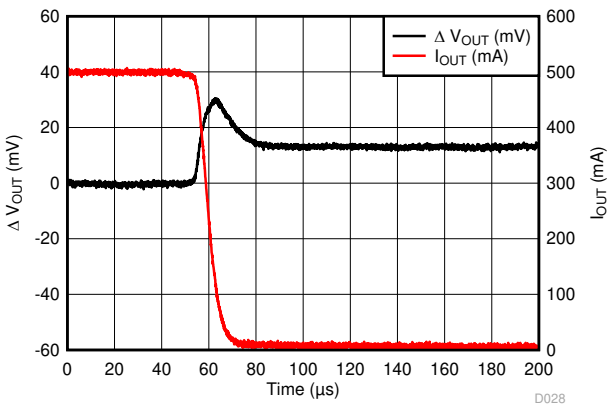
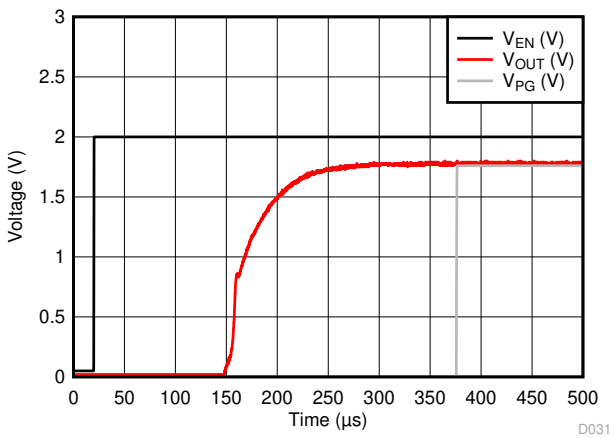
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



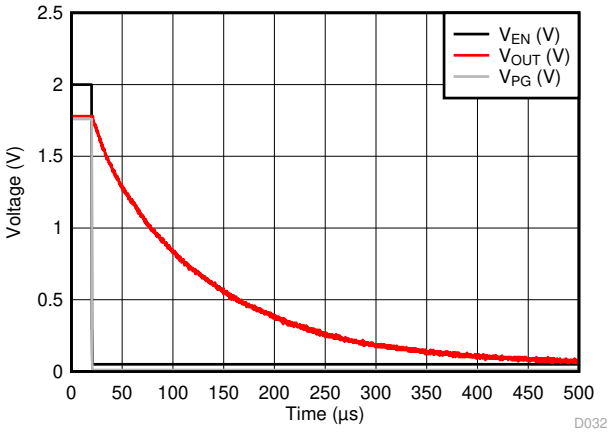
I_{OUT} = 500 mA to 5 mA, t_f = 10 µs

図 6-37. LP5912-3.3 Load Transient Response



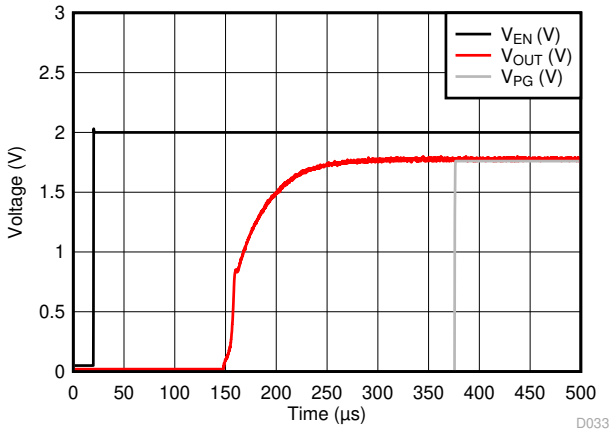
I_{OUT} = 0 mA, C_{OUT} = 1 µF

図 6-38. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$



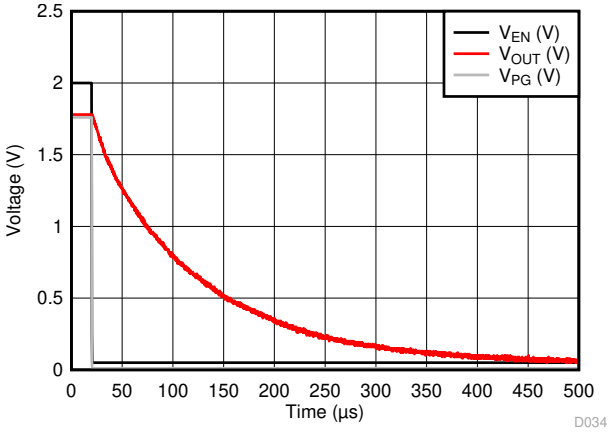
I_{OUT} = 0 mA, C_{OUT} = 1 µF

図 6-39. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$



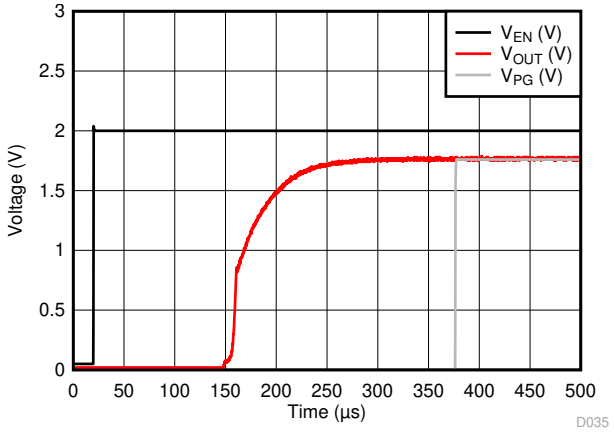
I_{OUT} = 1 mA, C_{OUT} = 1 µF

図 6-40. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$



I_{OUT} = 1 mA, C_{OUT} = 1 µF

図 6-41. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$



I_{OUT} = 500 mA, C_{OUT} = 1 µF

図 6-42. LP5912-1.8 V_{OUT} vs $V_{EN(ON)}$

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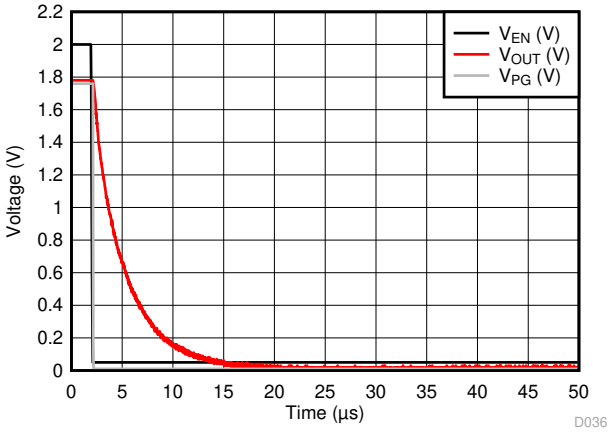
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



I_{OUT} = 500 mA, C_{OUT} = 1 µF

図 6-43. LP5912-1.8 V_{OUT} vs $V_{EN(OFF)}$

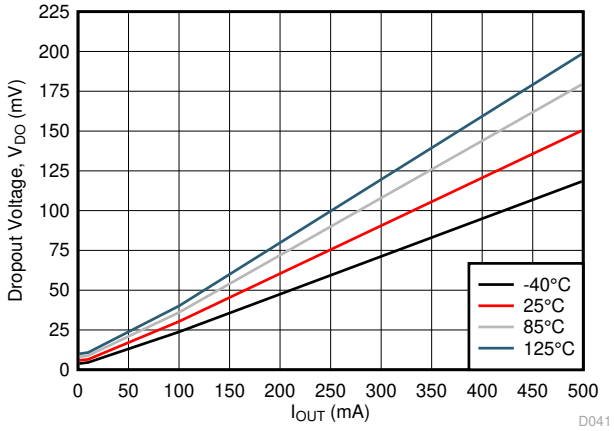


図 6-44. LP5912-1.8 Dropout Voltage (V_{DO}) vs I_{OUT}

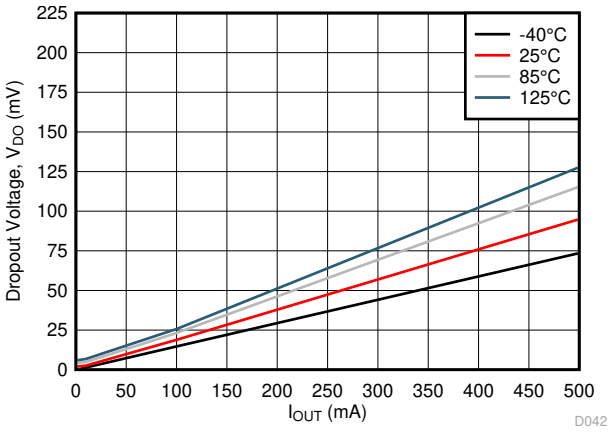
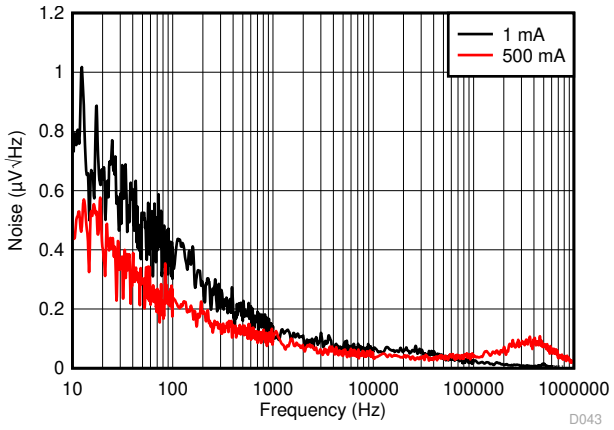


図 6-45. LP5912-3.3 Dropout Voltage (V_{DO}) vs I_{OUT}



V_{IN} = 1.6 V

図 6-46. LP5912-0.9 Noise vs Frequency

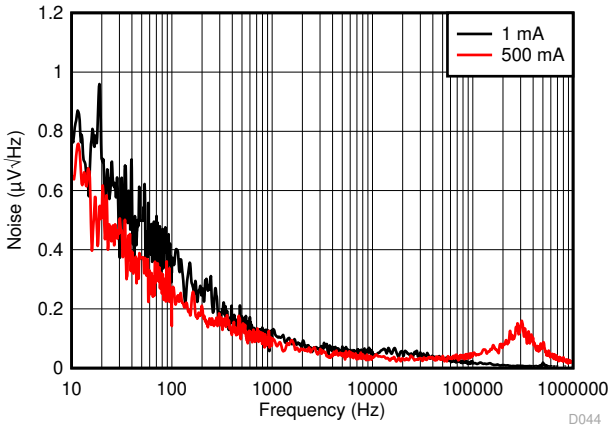


図 6-47. LP5912-1.8 Noise vs Frequency

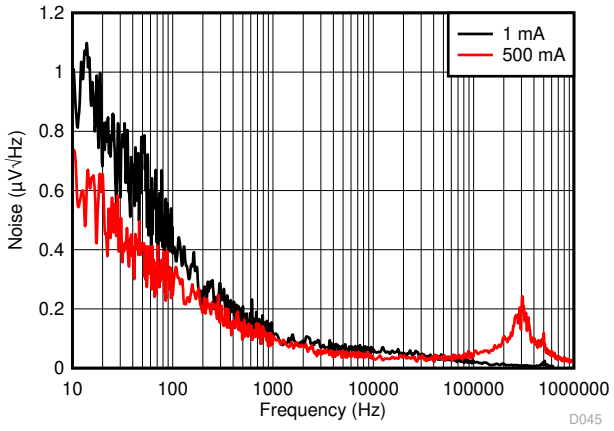


図 6-48. LP5912-3.3 Noise vs Frequency

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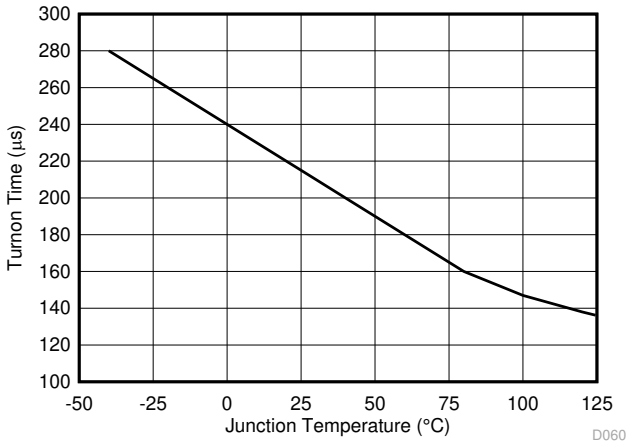
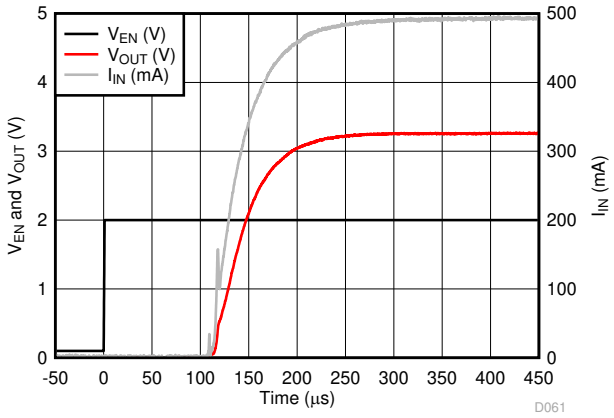
6.7 Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_J = 25°C (unless otherwise noted)



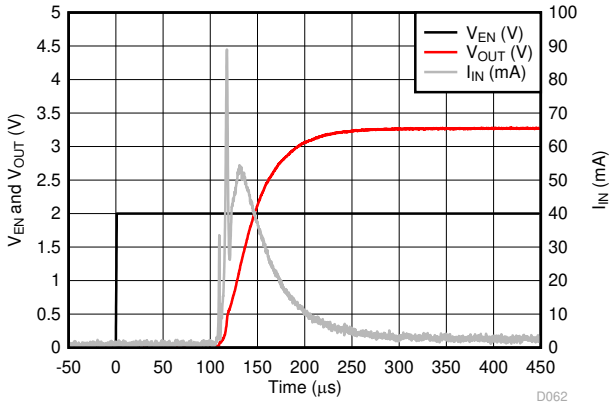
I_{OUT} = 0 mA (no load)

図 6-49. LP5912-3.3 Turn-On Time vs Junction Temperature



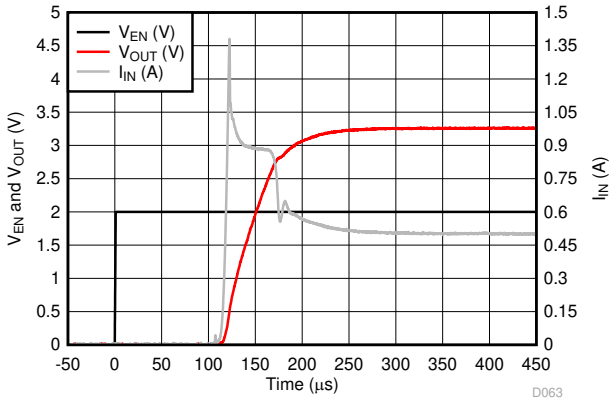
C_{IN} = open, I_{OUT} = 500 mA, C_{OUT} = 1 µF

図 6-50. LP5912-3.3 Inrush Current



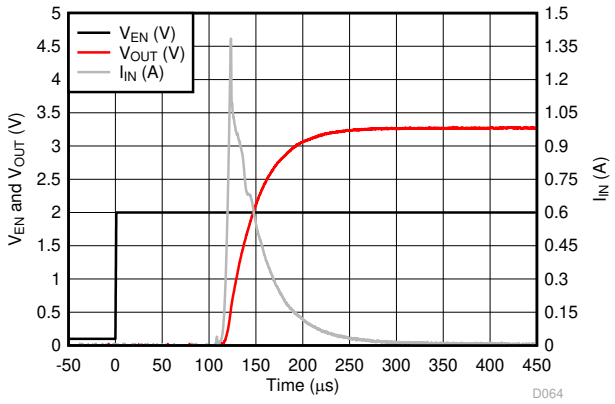
C_{IN} = open, I_{OUT} = 1 mA, C_{OUT} = 1 µF

図 6-51. LP5912-3.3 Inrush Current



C_{IN} = open, I_{OUT} = 500 mA, C_{OUT} = 10 µF

図 6-52. LP5912-3.3 Inrush Current



C_{IN} = open, I_{OUT} = 1 mA, C_{OUT} = 10 µF

図 6-53. LP5912-3.3 Inrush Current

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7 Detailed Description

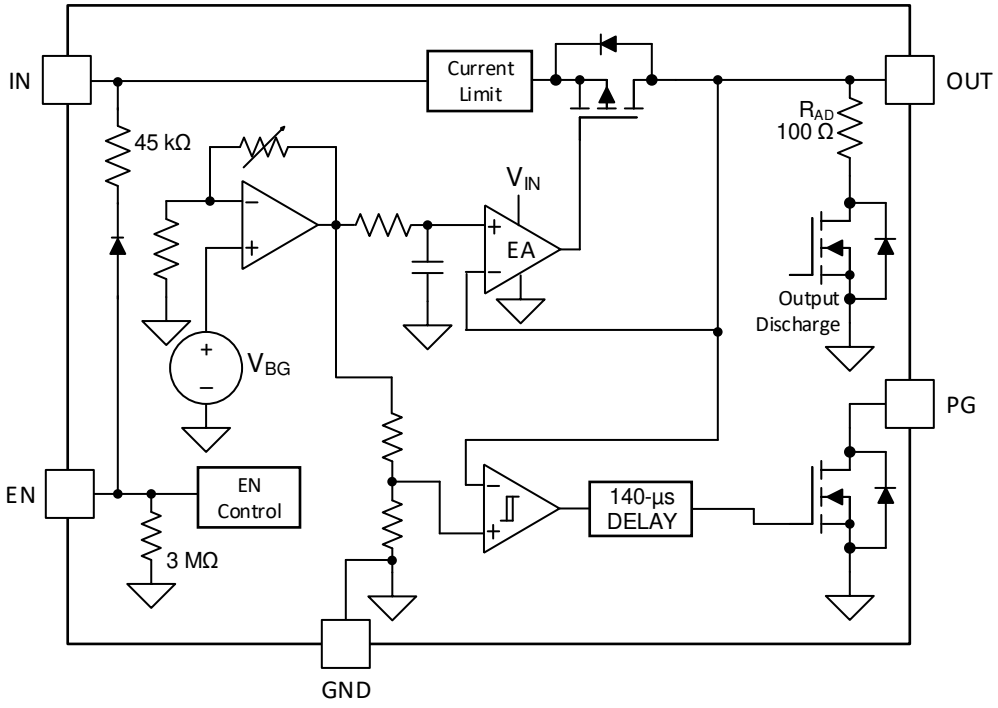
7.1 Overview

The LP5912-EP is a low-noise, high PSRR, low-dropout regulator (LDO) capable of sourcing a 500-mA load. The LP5912-EP can operate down to a 1.6-V input voltage and a 0.8-V output voltage. With this combination of low noise, high PSRR, and low output voltage, the device is designed to power a multitude of loads from noise-sensitive communication components to battery-powered systems.

The LP5912-EP contains several features, as shown in the *Functional Block Diagram*:

- Internal output resistor divider feedback
- Small size and low-noise internal protection circuit current limit
- Reverse current protection
- Current limit and inrush current protection
- Thermal shutdown
- Output auto discharge for fast turnoff
- Power-good output, with a fixed 140-µs typical delay

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP5912-EP enable (EN) pin is internally held low by a 3-MΩ resistor to GND. The EN pin voltage must be higher than the $V_{EN(ON)}$ threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the $V_{EN(OFF)}$ threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

When the device is disabled the output stage is disabled, the PG output pin is low, and the output automatic discharge is on.

7.3.2 Output Automatic Discharge (R_{AD})

The LP5912-EP output employs an internal 100-Ω (typical) pulldown resistance to discharge the output when the EN pin is low. If the LP5912-EP EN pin is low (the device is off) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground.

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7.3.3 Reverse Current Protection (I_{RO})

The LP5912-EP input is protected against reverse current when the output voltage is higher than the input voltage. In the event that extra output capacitance is used at the output, a power-down transient at the input normally causes a large reverse current through a conventional regulator. The LP5912-EP includes a reverse voltage detector that trips when V_{IN} drops below V_{OUT}, shutting off the regulator and opening the p-channel metal-oxide-semiconductor field effect transistor (PMOS) body diode connection, preventing any reverse current from the OUT pin from flowing to the IN pin.

If the LP5912-EP EN pin is low (the LP5912-EP is off) and the OUT pin is held high by a secondary supply, current flows from the secondary supply through the automatic discharge pulldown resistor to ground. This scenario is not reverse current, but is instead automatic discharge pulldown current.

Reverse current (I_{RO}) is measured at the IN pin.

7.3.4 Internal Current Limit (I_{SC})

The internal current limit circuit protects the LDO against high-load current faults or shorting events. The LDO is not designed to operate continuously at the I_{SC} current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

7.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

7.3.6 Power-Good Output (PG)

The LP5912-EP has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages (low impedance to GND). When the output voltage rises above the PG threshold voltage (PGV_{HTH}), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Use a pullup resistor from 10 kΩ to 100 kΩ for best results.

The input supply, V_{IN}, must be no less than the minimum operating voltage of 1.6 V to ensure that the PG pin output status is valid. The PG pin output status is undefined when V_{IN} is less than 1.6 V.

In the power-good function, the PG output pin being pulled high is typically delayed 140 µs after the output voltage rises above the PG_{HTH} threshold voltage. If the output voltage rises above the PG_{HTH} threshold and then falls below the PG_{LTH} threshold voltage, the PG pin falls immediately with no delay time.

If the PG function is not needed, the pullup resistor can be eliminated, and the PG pin can be either connected to ground or left floating.

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7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5912-EP EN pin is internally held low by a 3-MΩ resistor to GND. The EN pin voltage must be higher than the $V_{EN(ON)}$ threshold to ensure that the device is fully enabled under all operating conditions. When the EN pin voltage is lower than the $V_{EN(OFF)}$ threshold, the output stage is disabled, the PG pin goes low, and the output automatic discharge circuit is activated. Any charge on the OUT pin is discharged to ground through the internal 100-Ω (typical) output auto discharge pulldown resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5912-EP does not include a dedicated undervoltage lockout (UVLO) circuit. The device internal circuit is not fully functional until V_{IN} is at least 1.6 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.6 V or (V_{OUT} + V_{DO}).

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8 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP5912-EP is designed to meet the requirements of RF and analog circuits by providing low noise, high PSRR, low quiescent current, and low line or load transient response. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The device delivers this performance in an industry standard WSON package, which for this device is specified with an operating junction temperature (T_J) of –55°C to +125°C.

8.2 Typical Application

図 8-1 shows a typical application circuit for the LP5912-EP. Input and output capacitances may need to be increased above the 1-µF minimum for some applications.

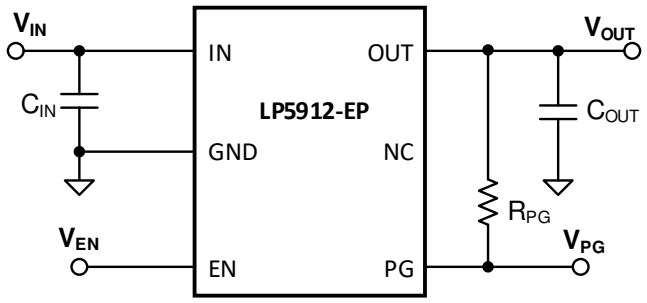

図 8-1. LP5912-EP Typical Application

8.2.1 Design Requirements

Use the parameters listed in 表 8-1 for typical RF linear regulator applications.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.6 V to 6.5 V
Output voltage	0.8 V to 5.5 V
Output current	500 mA
Output capacitor	1 µF to 10 µF
Input and output capacitor ESR range	5 mΩ to 500 mΩ

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8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

As with most low-dropout regulators, the LP5912-EP requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and the smallest possible components. These capacitors must be correctly selected for good performance.

8.2.2.2 Input Capacitor

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load-transient performance. A capacitor of at least 1 µF must be connected between the LP5912-EP IN pin and ground for stable operation over full load-current range. Having more output than input capacitance is acceptable, as long as the input is at least 1 µF.

The input capacitor must be located no more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor can be used at the input.

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To ensure stable operation, good PCB practices must be employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads connect the battery or other power source to the LP5912-EP, increase the value of the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures resulting from surge current when connected to a low-impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, the capacitor must be verified by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains at 1 µF ±30% over the entire operating temperature range.

8.2.2.3 Output Capacitor

The LP5912-EP is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. Use a ceramic capacitor (dielectric types of X5R or X7R) in the 1-µF to 10-µF range, and with an ESR from 5 mΩ to 500 mΩ, in the LP5912-EP application circuit. For this device, the output capacitor must be connected between the OUT pin with a good connection back to the GND pin.

Tantalum or film capacitors can also be used at the device output, V_{OUT}, but these components are not as attractive for reasons of size and cost (see the *Capacitor Characteristics* section).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range of 5 mΩ to 500 mΩ for stability.

8.2.2.4 Capacitor Characteristics

The LP5912-EP is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high-frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR stability requirement for the LP5912-EP.

The preferred choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 10-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. Although a tantalum capacitor can possibly be found with an ESR value within the stable range, low ESR tantalum capacitors are offered with larger capacitance (which means bigger and more costly) than a

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ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases at approximately 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.5 Remote Capacitor Operation

To ensure stability, the LP5912-EP requires at least a 1-µF capacitor at the OUT pin. There is no strict requirement for the location of the output capacitor in regards to the LDO OUT pin; the output capacitor can be located 5 cm to 10 cm away from the LDO. This flexibility means that there is no need to have a special capacitor close to the OUT pin if there are already respective capacitors in the system. This placement flexibility requires that the output capacitor be connected directly between the LP5912-EP OUT pin and GND pin with no vias. This remote capacitor feature can help designers minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum. Thus, use traces that are as wide as possible from the LDO output to the capacitors, keeping the LDO output trace layer as close to ground layer as possible and avoiding vias on the path. If there is a need to use vias, implement as many vias as possible between the connection layers. Keep parasitic wiring inductance less than 35 nH. For applications with fast load transients, use an input capacitor equal to (or larger than) the sum of the capacitance at the output node for the best load-transient performance.

8.2.2.6 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation can be calculated with 式 1, and depends on input voltage, output voltage, and load conditions of the design.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad into the PCB. To ensure the device does not overheat, connect the exposed pad (through thermal vias) to an internal ground plane with an appropriate amount of copper PCB area.

According to 式 2 or 式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A):

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

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8.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface-mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package-specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 4 or 式 5 and are given in the *Thermal Information* table.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where:

- $P_{D(MAX)}$ is explained in 式 3
- T_{TOP} is the temperature measured at the center-top of the device package

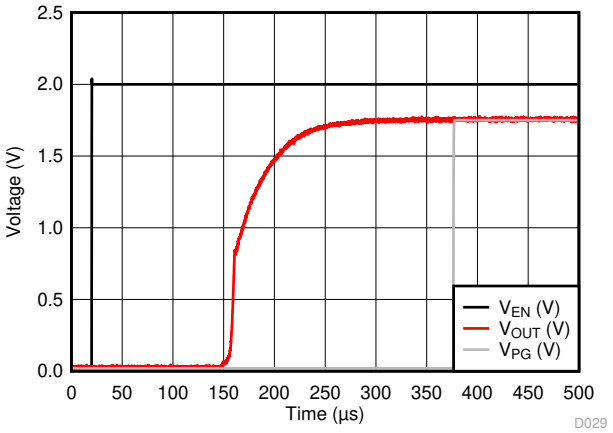
$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where:

- $P_{D(MAX)}$ is explained in the *Power Dissipation* section
- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

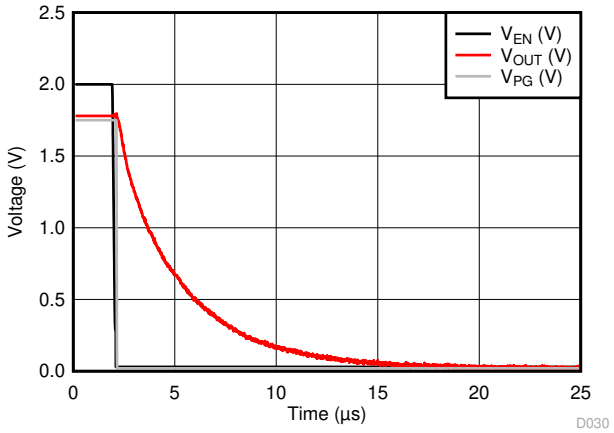
For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the *Semiconductor and IC Package Thermal Metrics* application note; for more information about measuring T_{TOP} and T_{BOARD}, see the *Using New Thermal Metrics* application note; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note. These application notes are available at www.ti.com.

8.2.3 Application Curves



V_{IN} = 2.3 V, I_{OUT} = 500 mA, C_{OUT} = 1 µF

図 8-2. LP5912-1.8 V_{OUT} vs V_{EN} (On)



V_{IN} = 2.3 V, I_{OUT} = 500 mA (3.6 Ω), C_{OUT} = 1 µF

図 8-3. LP5912-1.8 V_{OUT} vs V_{EN} (Off)

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8.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5912-EP output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 0.5 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

8.4 Layout

8.4.1 Layout Guidelines

The dynamic performance of the LP5912-EP is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs can degrade the PSRR, noise, or transient performance of the LP5912-EP.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5912-EP, and as close to the package as practical. The ground connections for C_{IN} and C_{OUT} must route back to the LP5912-EP ground pin using as wide and as short of a copper trace as practical.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. Such connections add parasitic inductances and resistance that result in inferior performance, especially during transient conditions.

8.4.2 Layout Example

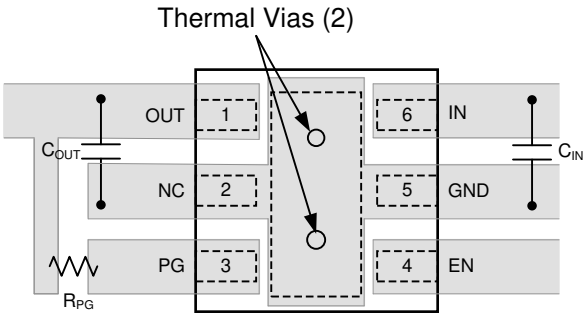

図 8-4. LP5912-EP Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For additional information, see the following:

- Texas Instruments, *AN1187 Leadless Leadframe Package (LLP)* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP591209MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2VC5	Samples
LP591212MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	12MB	Samples
LP591218MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	12MD	Samples
LP591225MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2VD5	Samples
LP591230MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	12MG	Samples
LP591233MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	12MF	Samples
LP591250MDRVREP	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	2VE5	Samples
V62/22601-04XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		12MB	Samples
V62/22601-06XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		12MD	Samples
V62/22601-07XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		2VD5	Samples
V62/22601-09XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		12MG	Samples
V62/22601-10XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		12MF	Samples
V62/22601-11XE	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		2VE5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5912-EP :

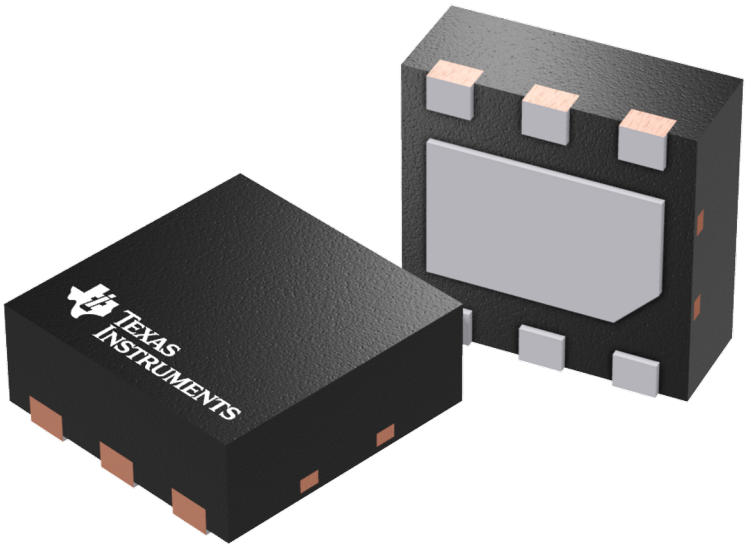
- Catalog : LP5912
- Automotive : LP5912-Q1

NOTE: Qualified Version Definitions:

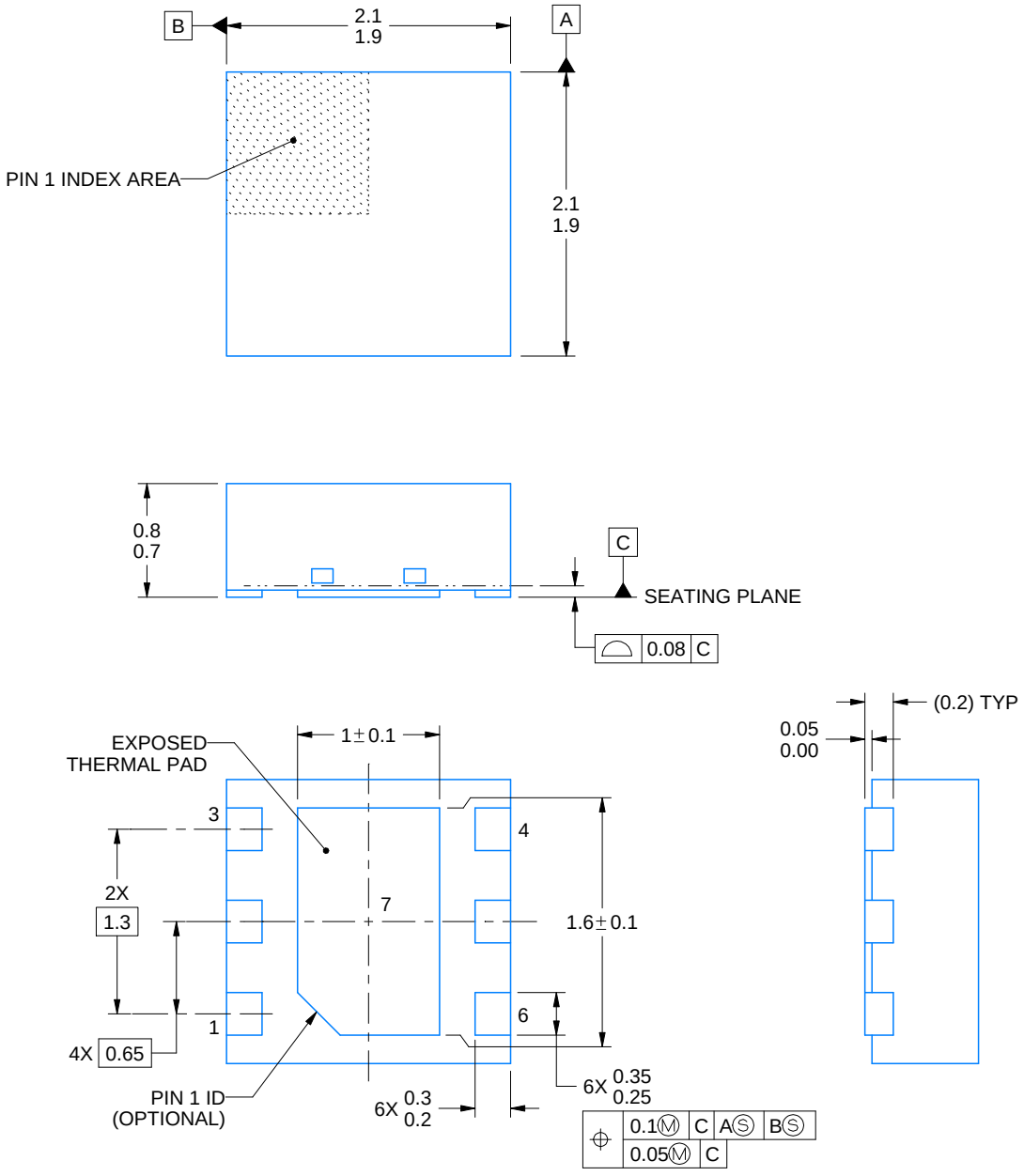
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

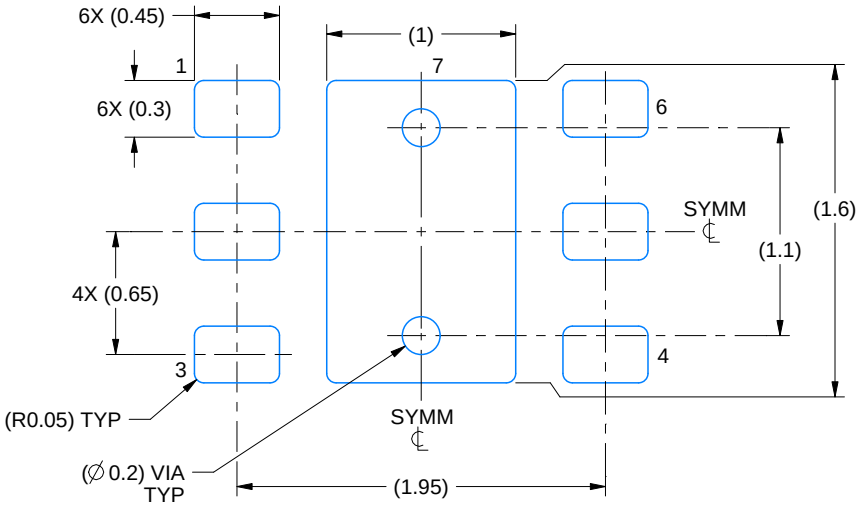


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

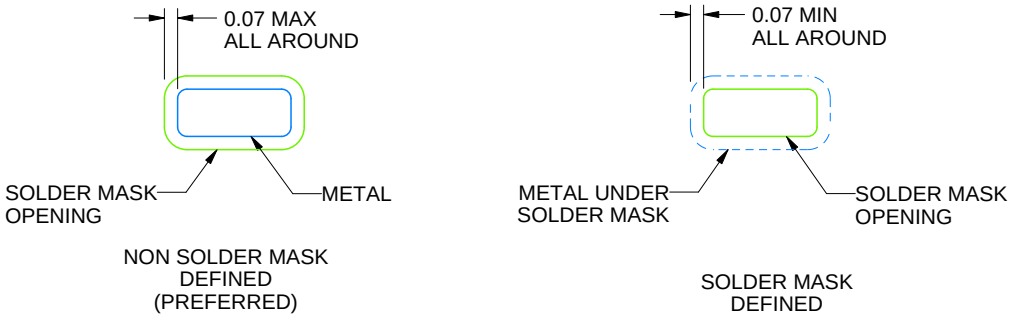


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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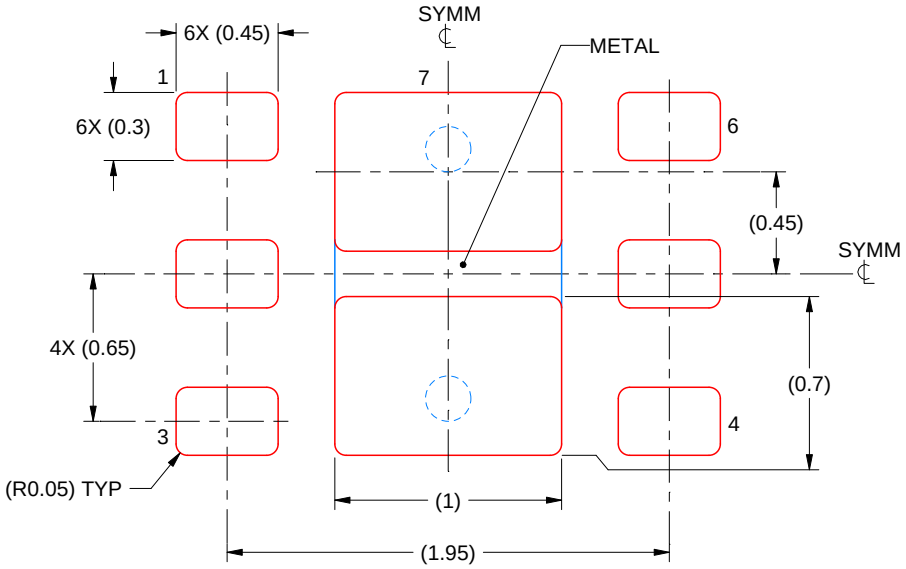
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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