

# OPAx145 高精度、低ノイズ、レール・ツー・レール出力、5.5MHz JFET オペアンプ

## 1 特長

- 最高の帯域幅とスルー・レート / 電力比:
  - ゲイン帯域幅積: 5.5MHz
  - スルーレート: 20V/μs
  - 低消費電流: 475μA (最大値)
- 高精度:
  - 非常に小さいオフセット: 150μV (最大値)
  - 非常に小さいオフセット・ドリフト: 1μV/°C (最大値)
- 低い入力バイアス電流: 2pA
- 非常に優れたノイズ性能:
  - 非常に低い電圧ノイズ: 7nV/√Hz
  - 非常に低い電流ノイズ: 0.8fA/√Hz
- 入力電圧範囲に V- 電源を含む
- 単一電源動作: 4.5V~36V
- 二重電源動作: ±2.25V~±18V

## 2 アプリケーション

- 半導体試験装置
- 実験室およびフィールド用計測機器
- ソース・メジャー・ユニット (SMU)
- 重量計
- DC (データ・センター) 内部の相互接続 (都市部)
- 商用ネットワークとサーバーの PSU (電源)
- DC 電源、AC 電源、電子負荷
- データ・アキュイジション (DAQ)

## 3 概要

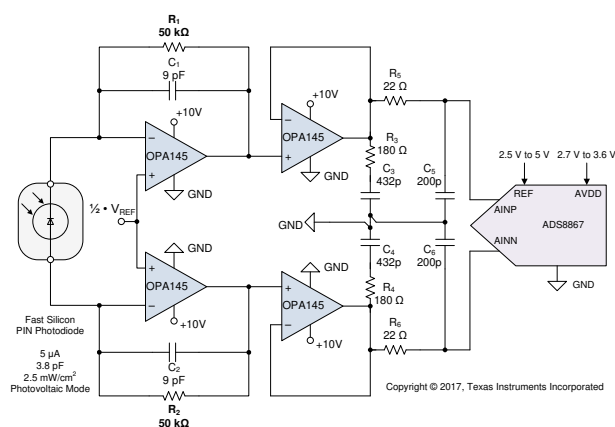
OPA145 および OPA2145 (OPAx145) デバイスは、優れたドリフト、低電流ノイズ、ピコアンペアの入力バイアス電流を持つ低消費電力 JFET 入力アンプ・ファミリの製品です。これらの特長から、OPAx145 は高インピーダンス・センサからの小さな信号を増幅するための優れた選択肢になります。

レール・ツー・レール出力のインターフェイスにより、最新の単一電源、高精度のアナログ / デジタル・コンバータ (ADC) およびデジタル / アナログ・コンバータ (DAC) に接続できます。さらに、入力範囲に V- が含まれるため、設計者は電力管理を簡素化し、単一電源、低ノイズの JFET アーキテクチャを活用できます。

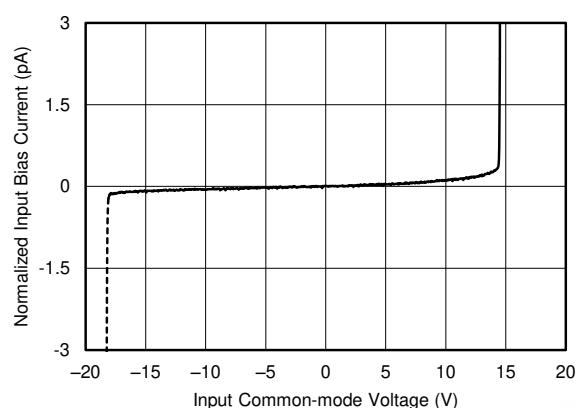
### 製品情報<sup>(1)</sup>

| 部品番号    | パッケージ      | 本体サイズ (公称)      |
|---------|------------|-----------------|
| OPA145  | SOIC (8)   | 4.90mm × 3.91mm |
|         | VSSOP (8)  | 3.00mm × 3.00mm |
|         | SOT-23 (5) | 2.90mm × 1.60mm |
| OPA2145 | SOIC (8)   | 4.90mm × 3.91mm |
|         | VSSOP (8)  | 3.00mm × 3.00mm |

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



OPAx145 は 16 ビット、100kSPS の完全差動トランスインピーダンス・イメージング・アプリケーションに最適



OPAx145 の高精度 JFET テクノロジーによる非常に優れた線形入力インピーダンス



## Table of Contents

|                                                                                                                        |           |                                                                      |           |
|------------------------------------------------------------------------------------------------------------------------|-----------|----------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                                                                                                      | <b>1</b>  | <b>8 Application and Implementation</b> .....                        | <b>23</b> |
| <b>2 アプリケーション</b> .....                                                                                                | <b>1</b>  | 8.1 Application Information.....                                     | 23        |
| <b>3 概要</b> .....                                                                                                      | <b>1</b>  | 8.2 Typical Application.....                                         | 23        |
| <b>4 Revision History</b> .....                                                                                        | <b>2</b>  | 8.3 System Examples.....                                             | 24        |
| <b>5 Pin Configuration and Functions</b> .....                                                                         | <b>3</b>  | <b>9 Power Supply Recommendations</b> .....                          | <b>26</b> |
| <b>6 Specifications</b> .....                                                                                          | <b>4</b>  | <b>10 Layout</b> .....                                               | <b>26</b> |
| 6.1 Absolute Maximum Ratings .....                                                                                     | 4         | 10.1 Layout Guidelines.....                                          | 26        |
| 6.2 ESD Ratings .....                                                                                                  | 4         | 10.2 Layout Example.....                                             | 27        |
| 6.3 Recommended Operating Conditions .....                                                                             | 4         | <b>11 Device and Documentation Support</b> .....                     | <b>28</b> |
| 6.4 Thermal Information: OPA145 .....                                                                                  | 5         | 11.1 Device Support.....                                             | 28        |
| 6.5 Thermal Information: OPA2145 .....                                                                                 | 5         | 11.2 Documentation Support.....                                      | 28        |
| 6.6 Electrical Characteristics: $V_S = 4.5\text{ V to }36\text{ V}$ ;<br>$\pm 2.25\text{ V to } \pm 18\text{ V}$ ..... | 6         | 11.3 Receiving Notification of Documentation Updates..               | 28        |
| 6.7 Typical Characteristics.....                                                                                       | 8         | 11.4 サポート・リソース.....                                                  | 29        |
| <b>7 Detailed Description</b> .....                                                                                    | <b>16</b> | 11.5 Trademarks.....                                                 | 29        |
| 7.1 Overview.....                                                                                                      | 16        | 11.6 静電気放電に関する注意事項.....                                              | 29        |
| 7.2 Functional Block Diagram.....                                                                                      | 16        | 11.7 用語集.....                                                        | 29        |
| 7.3 Feature Description.....                                                                                           | 16        | <b>12 Mechanical, Packaging, and Orderable<br/>Information</b> ..... | <b>29</b> |
| 7.4 Device Functional Modes.....                                                                                       | 22        |                                                                      |           |

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

|                                                                                               |             |
|-----------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision E (October 2020) to Revision F (February 2021)</b>                   | <b>Page</b> |
| • OPA2145 D (SOIC-8) および DGK (VSSOP-8) パッケージを事前情報 (プレビュー) から量産データ (アクティブ) に変更.....            | 1           |
| • Changed offset voltage drift specification to differentiate between OPA145 and OPA2145..... | 6           |
| • Changed PSRR specification to differentiate between OPA145 and OPA2145.....                 | 6           |
| <b>Changes from Revision D (June 2020) to Revision E (October 2020)</b>                       | <b>Page</b> |
| • 文書全体の表、図、相互参照の採番方法を更新.....                                                                  | 1           |
| • OPA2145 の事前情報 (プレビュー) DGK (VSSOP-8) パッケージと関連コンテンツを追加.....                                   | 1           |
| • Deleted <i>Operating Voltage</i> section; redundant information.....                        | 16          |
| <b>Changes from Revision C (July 2018) to Revision D (June 2020)</b>                          | <b>Page</b> |
| • OPA2145 の事前情報 (プレビュー) デバイス D (SOIC-8) パッケージと関連コンテンツを追加.....                                 | 1           |
| <b>Changes from Revision B (May 2018) to Revision C (July 2018)</b>                           | <b>Page</b> |
| • 次の情報から「プレビュー」を削除: DBV (SOT-23) パッケージ、リリース済み.....                                            | 1           |
| • データシートのステータスを量産データに変更.....                                                                  | 1           |
| <b>Changes from Revision A (March 2018) to Revision B (May 2018)</b>                          | <b>Page</b> |
| • 次の情報から「プレビュー」を削除: DGK (VSSOP) パッケージ、リリース済み.....                                             | 1           |
| <b>Changes from Revision * (June 2017) to Revision A (March 2018)</b>                         | <b>Page</b> |
| • DBV および DGK パッケージのプレビューを追加、将来のデバイスのリリースに関するコンテンツを削除.....                                    | 1           |

## 5 Pin Configuration and Functions

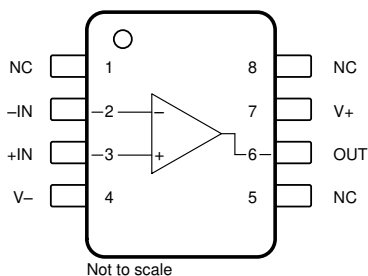


图 5-1. OPA145: D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

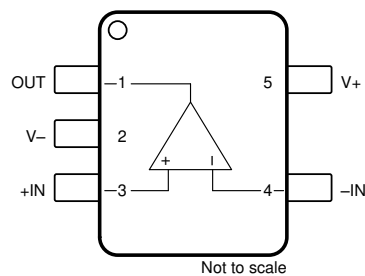


图 5-2. OPA145: DBV (5-Pin SOT-23) Package, Top View

表 5-1. Pin Functions: OPA145

| PIN  |                          |              | I/O | DESCRIPTION                                   |
|------|--------------------------|--------------|-----|-----------------------------------------------|
| NAME | OPA145                   |              |     |                                               |
|      | D (SOIC),<br>DGK (VSSOP) | DBV (SOT-23) |     |                                               |
| –IN  | 2                        | 4            | I   | Inverting input                               |
| +IN  | 3                        | 3            | I   | Noninverting input                            |
| NC   | 1, 5, 8                  | —            | —   | No internal connection (can be left floating) |
| OUT  | 6                        | 1            | O   | Output                                        |
| V–   | 4                        | 2            | —   | Negative (lowest) power supply                |
| V+   | 7                        | 5            | —   | Positive (highest) power supply               |

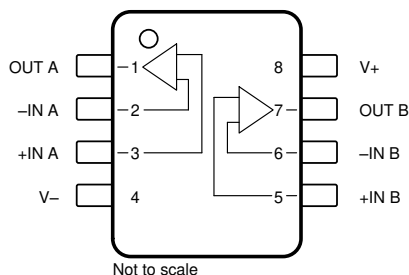


图 5-3. OPA2145: D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

表 5-2. Pin Functions: OPA2145

| PIN   |                          | I/O | DESCRIPTION                  |
|-------|--------------------------|-----|------------------------------|
| NAME  | OPA2145                  |     |                              |
|       | D (SOIC),<br>DGK (VSSOP) |     |                              |
| –IN A | 2                        | I   | Inverting input channel A    |
| +IN A | 3                        | I   | Noninverting input channel A |
| –IN B | 6                        | I   | Inverting input channel B    |
| +IN B | 5                        | I   | Noninverting input channel B |
| OUT A | 1                        | O   | Output channel A             |
| OUT B | 7                        | O   | Output channel B             |
| V–    | 4                        | —   | Negative supply              |
| V+    | 8                        | —   | Positive supply              |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                     |               | MIN        | MAX        | UNIT |
|------------------|-------------------------------------|---------------|------------|------------|------|
| V <sub>S</sub>   | Supply voltage, (V+) – (V–)         | Dual supply   |            | ±20        | V    |
|                  |                                     | Single supply |            | 40         |      |
|                  | Signal input pins <sup>(2)</sup>    | Voltage       | (V–) – 0.5 | (V+) + 0.5 | V    |
|                  |                                     | Current       |            | ±10        | mA   |
| I <sub>SC</sub>  | Output short-circuit <sup>(3)</sup> |               | Continuous | Continuous |      |
| T <sub>A</sub>   | Operating temperature               |               | –55        | 150        | °C   |
| T <sub>J</sub>   | Junction temperature                |               |            | 150        | °C   |
| T <sub>STG</sub> | Storage temperature                 |               | –65        | 150        | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to V<sub>S</sub> / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                             |               | MIN   | NOM | MAX | UNIT |
|----------------|-----------------------------|---------------|-------|-----|-----|------|
| V <sub>S</sub> | Supply voltage, (V+) – (V–) | Dual supply   | ±2.25 | ±15 | ±18 | V    |
|                |                             | Single supply | 4.5   | 30  | 36  |      |
| T <sub>A</sub> | Ambient temperature         |               | –40   | 25  | 125 | °C   |

## 6.4 Thermal Information: OPA145

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA145   |             |           | UNIT |
|-------------------------------|----------------------------------------------|----------|-------------|-----------|------|
|                               |                                              | D (SOIC) | DGK (VSSOP) | DBV (SOT) |      |
|                               |                                              | 8 PINS   | 8 PINS      | 5 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 136      | 143         | 205       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 74       | 47          | 200       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 62       | 64          | 113       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 19.7     | 5.3         | 38.2      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 54.8     | 62.8        | 104.9     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A         | N/A       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Thermal Information: OPA2145

| THERMAL METRIC <sup>(1)</sup> |                                              | OPA2145  |             | UNIT |
|-------------------------------|----------------------------------------------|----------|-------------|------|
|                               |                                              | D (SOIC) | DGK (VSSOP) |      |
|                               |                                              | 8 PINS   | 8 PINS      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 118.7    | 163.9       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 52.3     | 53.4        | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 63.5     | 85.0        | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.7     | 5.9         | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 62.4     | 83.7        | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics: $V_S = 4.5\text{ V to }36\text{ V}$ ; $\pm 2.25\text{ V to } \pm 18\text{ V}$

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)

| PARAMETER            |                              | TEST CONDITIONS                                                                                         | MIN       | TYP                     | MAX       | UNIT              |
|----------------------|------------------------------|---------------------------------------------------------------------------------------------------------|-----------|-------------------------|-----------|-------------------|
| OFFSET VOLTAGE       |                              |                                                                                                         |           |                         |           |                   |
| V <sub>OS</sub>      | Offset voltage, RTI          | V <sub>S</sub> = ±18 V                                                                                  |           | ±40                     | ±150      | μV                |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = 0°C to +85°C                                                   |           |                         | ±280      |                   |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = −40°C to +125°C                                                |           |                         | ±350      |                   |
| dV <sub>OS</sub> /dT | Drift                        | V <sub>S</sub> = ±18 V, T <sub>A</sub> = 0°C to +85°C, OPA145ID and OPA145IDGK packages                 |           | ±0.4                    | ±1        | μV/°C             |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = 0°C to +85°C, OPA145IDBV package                               |           | ±0.4                    | ±1.2      |                   |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = −40°C to +125°C, OPA145ID and OPA145IDGK packages              |           | ±0.5                    | ±1.4      |                   |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = −40°C to +125°C, OPA145IDBV package                            |           | ±0.5                    | ±1.5      |                   |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = 0°C to +85°C, OPA2145                                          |           | ±0.15                   | ±0.8      |                   |
|                      |                              | V <sub>S</sub> = ±18 V, T <sub>A</sub> = −40°C to +125°C, OPA2145                                       |           | ±0.2                    | ±1        |                   |
| PSRR                 | Power-supply rejection ratio | V <sub>S</sub> = ±2.25 V to ±18 V, OPA145ID and OPA2145 packages                                        |           | ±0.06                   | ±0.3      | μV/V              |
|                      |                              | V <sub>S</sub> = ±2.25 V to ±18 V, OPA145IDGK and OPA145IDBV packages                                   |           | ±0.06                   | ±0.5      |                   |
|                      |                              | V <sub>S</sub> = ±2.25 V to ±18 V, T <sub>A</sub> = −40°C to +125°C, OPA145                             |           |                         | ±2        |                   |
|                      |                              | V <sub>S</sub> = ±2.25 V to ±18 V, T <sub>A</sub> = −40°C to +125°C, OPA2145                            |           |                         | ±0.65     |                   |
| INPUT BIAS CURRENT   |                              |                                                                                                         |           |                         |           |                   |
| I <sub>B</sub>       | Input bias current           |                                                                                                         |           | ±2                      | ±10       | pA                |
|                      |                              | T <sub>A</sub> = 0°C to +85°C                                                                           |           |                         | ±600      |                   |
|                      |                              | T <sub>A</sub> = −40°C to +125°C                                                                        |           |                         | ±10       | nA                |
| I <sub>OS</sub>      | Input offset current         |                                                                                                         |           | ±2                      | ±10       | pA                |
|                      |                              | T <sub>A</sub> = 0°C to +85°C                                                                           |           |                         | ±600      |                   |
|                      |                              | T <sub>A</sub> = −40°C to +125°C                                                                        |           |                         | ±10       | nA                |
| NOISE                |                              |                                                                                                         |           |                         |           |                   |
|                      | Input voltage noise          | f = 0.1 Hz to 10 Hz                                                                                     |           | 320                     |           | nV <sub>PP</sub>  |
|                      |                              | f = 0.1 Hz to 10 Hz                                                                                     |           | 60                      |           | nV <sub>RMS</sub> |
| e <sub>n</sub>       | Input voltage noise density  | f = 10 Hz                                                                                               |           | 9                       |           | nV/√Hz            |
|                      |                              | f = 100 Hz                                                                                              |           | 7.2                     |           |                   |
|                      |                              | f = 1 kHz                                                                                               |           | 7                       |           |                   |
| I <sub>n</sub>       | Input current noise density  | f = 1 kHz                                                                                               |           | 0.8                     |           | fA/√Hz            |
| INPUT VOLTAGE RANGE  |                              |                                                                                                         |           |                         |           |                   |
| V <sub>CM</sub>      | Common-mode voltage range    | T <sub>A</sub> = −40°C to +125°C                                                                        | (V−) −0.1 |                         | (V+) −3.5 | V                 |
| CMRR                 | Common-mode rejection ratio  | V <sub>S</sub> = ±18 V, V <sub>CM</sub> = (V−) −0.1 V to (V+) − 3.5 V                                   | 126       | 140                     |           | dB                |
|                      |                              | V <sub>S</sub> = ±18 V, V <sub>CM</sub> = (V−) −0.1 V to (V+) − 3.5 V, T <sub>A</sub> = −40°C to +125°C | 118       |                         |           |                   |
| INPUT IMPEDANCE      |                              |                                                                                                         |           |                         |           |                   |
|                      | Differential                 |                                                                                                         |           | 10 <sup>13</sup>    5   |           | Ω    pF           |
|                      | Common-mode                  | V <sub>CM</sub> = (V−) −0.1 V to (V+) −3.5 V                                                            |           | 10 <sup>13</sup>    4.3 |           |                   |

## 6.6 Electrical Characteristics: $V_S = 4.5\text{ V to }36\text{ V}; \pm 2.25\text{ V to } \pm 18\text{ V}$ (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} = \text{midsupply}$  (unless otherwise noted)

| PARAMETER          |                                     |         | TEST CONDITIONS                                                                                                                             | MIN                     | TYP                      | MAX                     | UNIT |
|--------------------|-------------------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------|-------------------------|------|
| OPEN-LOOP GAIN     |                                     |         |                                                                                                                                             |                         |                          |                         |      |
| A <sub>OL</sub>    | Open-loop voltage gain              |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 10 kΩ, OPA145ID package only                 | 118                     | 123                      |                         | dB   |
|                    |                                     |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 10 kΩ, OPA145IDGK and<br>OPA145IDBV packages | 110                     | 123                      |                         |      |
|                    |                                     |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 10 kΩ, OPA2145                               | 114                     | 123                      |                         |      |
|                    |                                     |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 2 kΩ                                         | 106                     | 110                      |                         |      |
|                    |                                     |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 2 kΩ, OPA2145                                | 104                     | 110                      |                         |      |
|                    |                                     |         | V <sub>O</sub> = (V <sup>−</sup> ) + 0.35 V to (V <sup>+</sup> ) − 0.35 V,<br>R <sub>L</sub> = 2 kΩ, T <sub>A</sub> = −40°C to +125°C       | 104                     |                          |                         |      |
| FREQUENCY RESPONSE |                                     |         |                                                                                                                                             |                         |                          |                         |      |
| BW                 | Gain bandwidth product              |         |                                                                                                                                             |                         | 5.5                      |                         | MHz  |
| SR                 | Slew rate                           |         |                                                                                                                                             |                         | 20                       |                         | V/μs |
|                    | Settling time                       | 12 bits | 10-V step, G = +1                                                                                                                           |                         | 1.6                      |                         | μs   |
|                    |                                     | 16 bits | 10-V step, G = +1                                                                                                                           |                         | 6                        |                         |      |
| THD+N              | Total harmonic distortion and noise |         | 1 kHz, G = +1, V <sub>O</sub> = 3.5 V <sub>RMS</sub>                                                                                        |                         | 0.0001%                  |                         |      |
|                    | Overload recovery time              |         |                                                                                                                                             |                         | 600                      |                         | ns   |
| OUTPUT             |                                     |         |                                                                                                                                             |                         |                          |                         |      |
|                    | Linear output voltage swing range   |         | R <sub>L</sub> = 10 kΩ, A <sub>OL</sub> ≥ 108 dB,<br>T <sub>A</sub> = −40°C to +125°C,<br>see <a href="#">6-24</a> and <a href="#">6-25</a> | (V <sup>−</sup> ) + 0.1 |                          | (V <sup>+</sup> ) − 0.1 | V    |
|                    |                                     |         | R <sub>L</sub> = 2 kΩ, A <sub>OL</sub> ≥ 108 dB,<br>T <sub>A</sub> = −40°C to +125°C,<br>see <a href="#">6-24</a> and <a href="#">6-25</a>  | (V <sup>−</sup> ) + 0.3 |                          | (V <sup>+</sup> ) − 0.3 |      |
| V <sub>O</sub>     | Voltage output swing from rail      |         | R <sub>L</sub> = 10 kΩ                                                                                                                      |                         |                          | 75                      | mV   |
|                    |                                     |         | R <sub>L</sub> = 10 kΩ, OPA2145                                                                                                             |                         |                          | 80                      |      |
|                    |                                     |         | R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = −40°C to +125°C                                                                                    |                         |                          | 90                      |      |
|                    |                                     |         | R <sub>L</sub> = 2 kΩ                                                                                                                       |                         |                          | 210                     |      |
|                    |                                     |         | R <sub>L</sub> = 2 kΩ, OPA2145                                                                                                              |                         |                          | 230                     |      |
|                    |                                     |         | R <sub>L</sub> = 2 kΩ, T <sub>A</sub> = −40°C to +125°C,<br>OPA145ID                                                                        |                         |                          | 250                     |      |
|                    |                                     |         | R <sub>L</sub> = 2 kΩ, T <sub>A</sub> = −40°C to +125°C,<br>OPA145IDGK and OPA145IDBV<br>packages, OPA2145                                  |                         |                          | 350                     |      |
| I <sub>SC</sub>    | Short-circuit current               |         |                                                                                                                                             |                         | ±20                      |                         | mA   |
| C <sub>LOAD</sub>  | Capacitive load drive               |         |                                                                                                                                             |                         | See <a href="#">6-27</a> |                         |      |
| R <sub>O</sub>     | Open-loop output impedance          |         | f = 1 MHz, I <sub>O</sub> = 0 mA (see <a href="#">6-26</a> )                                                                                |                         | 150                      |                         | Ω    |
| POWER SUPPLY       |                                     |         |                                                                                                                                             |                         |                          |                         |      |
| I <sub>Q</sub>     | Quiescent current (per amplifier)   |         | I <sub>O</sub> = 0 mA                                                                                                                       |                         | 445                      | 475                     | μA   |
|                    |                                     |         | T <sub>A</sub> = 0°C to +85°C                                                                                                               |                         |                          | 590                     |      |
|                    |                                     |         | T <sub>A</sub> = −40°C to +125°C                                                                                                            |                         |                          | 655                     |      |

## 6.7 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

**表 6-1. Table of Graphs**

| DESCRIPTION                                                                        | FIGURE                                          |
|------------------------------------------------------------------------------------|-------------------------------------------------|
| Offset Voltage Production Distribution                                             | <a href="#">图 6-1</a>                           |
| Offset Voltage Drift Distribution From $-40^\circ\text{C}$ to $+125^\circ\text{C}$ | <a href="#">图 6-2</a>                           |
| Input Bias Current Production Distribution                                         | <a href="#">图 6-3</a>                           |
| Input Offset Current Production Distribution                                       | <a href="#">图 6-4</a>                           |
| Offset Voltage vs Temperature                                                      | <a href="#">图 6-5</a>                           |
| Offset Voltage vs Common-Mode Voltage                                              | <a href="#">图 6-6</a>                           |
| Offset Voltage vs Power Supply                                                     | <a href="#">图 6-7</a>                           |
| Open-Loop Gain and Phase vs Frequency                                              | <a href="#">图 6-8</a>                           |
| Closed-Loop Gain vs Frequency                                                      | <a href="#">图 6-9</a>                           |
| Input Bias Current vs Common-Mode Voltage                                          | <a href="#">图 6-10</a>                          |
| Input Bias Current and Offset vs Temperature                                       | <a href="#">图 6-11</a>                          |
| Output Voltage Swing vs Output Current (Maximum Supply)                            | <a href="#">图 6-12</a>                          |
| CMRR and PSRR vs Frequency                                                         | <a href="#">图 6-13</a>                          |
| CMRR vs Temperature                                                                | <a href="#">图 6-14</a>                          |
| PSRR vs Temperature                                                                | <a href="#">图 6-15</a>                          |
| 0.1-Hz to 10-Hz Voltage Noise                                                      | <a href="#">图 6-16</a>                          |
| Input Voltage Noise Spectral Density vs Frequency                                  | <a href="#">图 6-17</a>                          |
| THD+N Ratio vs Frequency                                                           | <a href="#">图 6-18</a>                          |
| THD+N vs Output Amplitude                                                          | <a href="#">图 6-19</a>                          |
| Quiescent Current vs Supply Voltage                                                | <a href="#">图 6-20</a>                          |
| Quiescent Current vs Temperature                                                   | <a href="#">图 6-21</a>                          |
| Open-Loop Gain vs Temperature (10-k $\Omega$ )                                     | <a href="#">图 6-22</a>                          |
| Open-Loop Gain vs Temperature (2-k $\Omega$ )                                      | <a href="#">图 6-23</a>                          |
| DC Open-Loop Gain vs Output Voltage Swing Relative to Supply                       | <a href="#">图 6-24</a> , <a href="#">图 6-25</a> |
| Open-Loop Output Impedance vs Frequency                                            | <a href="#">图 6-26</a>                          |
| Small-Signal Overshoot vs Capacitive Load (10-mV Step)                             | <a href="#">图 6-27</a>                          |
| No Phase Reversal                                                                  | <a href="#">图 6-28</a>                          |
| Positive Overload Recovery                                                         | <a href="#">图 6-29</a>                          |
| Negative Overload Recovery                                                         | <a href="#">图 6-30</a>                          |
| Small-Signal Step Response (10-mV Step)                                            | <a href="#">图 6-31</a> , <a href="#">图 6-32</a> |
| Large-Signal Step Response (10-V Step)                                             | <a href="#">图 6-33</a> , <a href="#">图 6-34</a> |
| Settling Time                                                                      | <a href="#">图 6-35</a>                          |
| Short-Circuit Current vs Temperature                                               | <a href="#">图 6-36</a>                          |
| Maximum Output Voltage vs Frequency                                                | <a href="#">图 6-37</a>                          |
| EMIRR vs Frequency                                                                 | <a href="#">图 6-38</a>                          |



## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

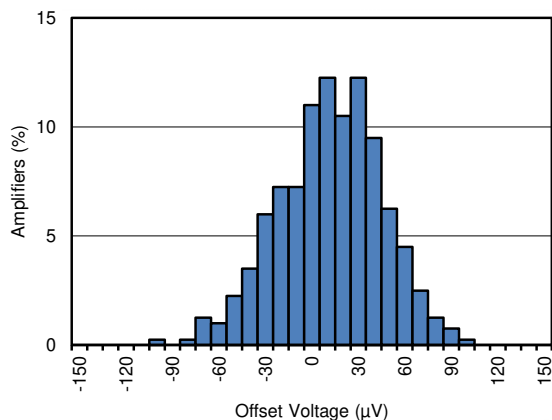


FIG 6-1. Offset Voltage Production Distribution

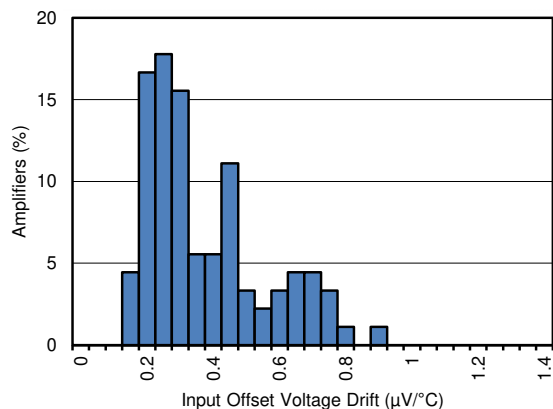


FIG 6-2. Offset Voltage Drift Distribution From  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

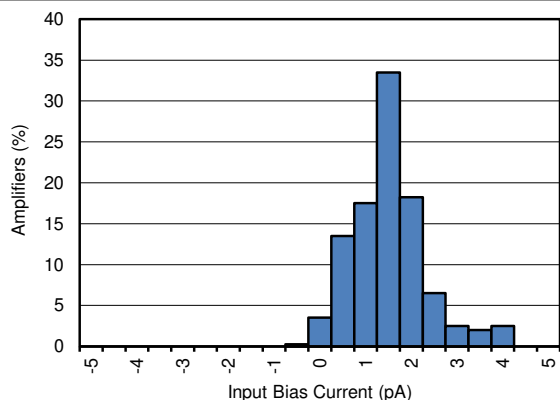


FIG 6-3. Input Bias Current Production Distribution

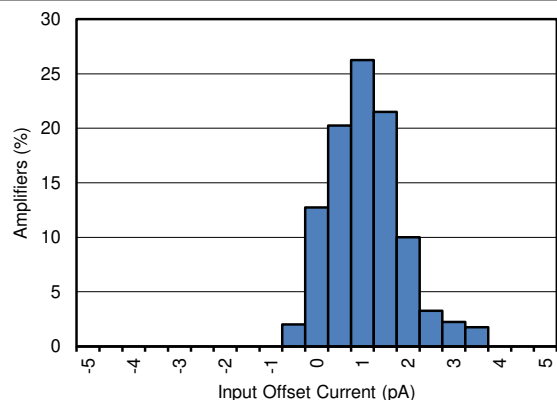


FIG 6-4. Input Offset Current Production Distribution

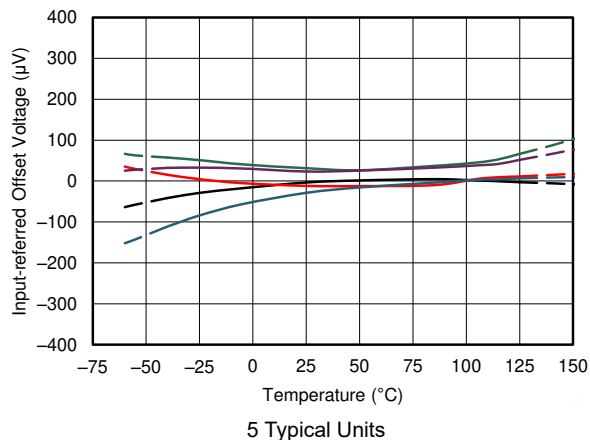


FIG 6-5. Offset Voltage vs Temperature

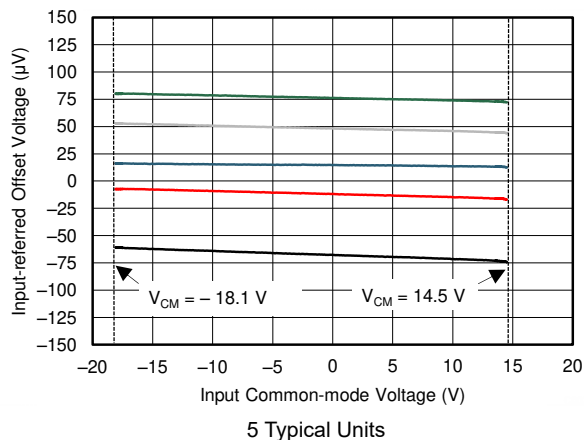


FIG 6-6. Offset Voltage vs Common-Mode Voltage

## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

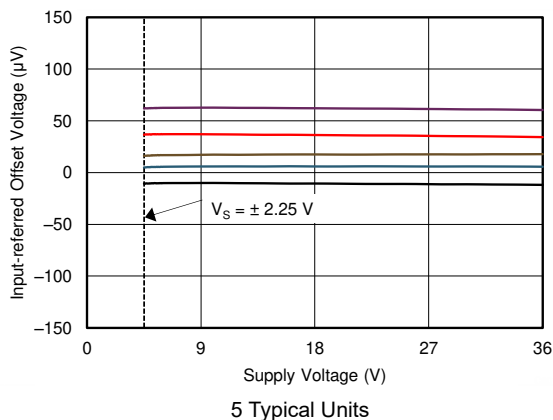


FIG 6-7. Offset Voltage vs Supply Voltage

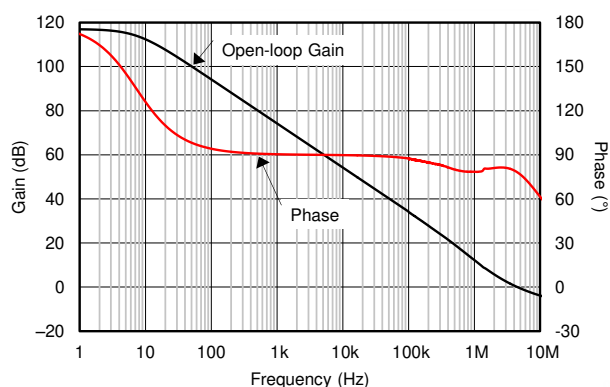


FIG 6-8. Open-Loop Gain and Phase vs Frequency

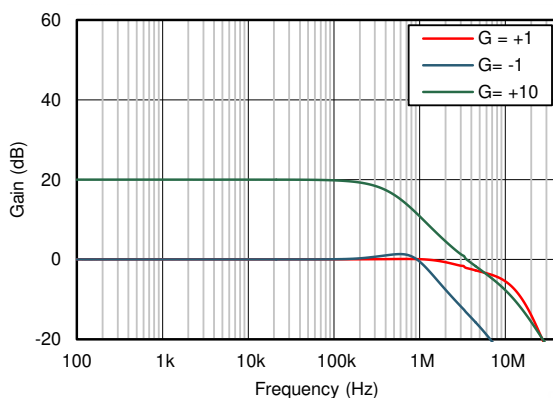


FIG 6-9. Closed-Loop Gain vs Frequency

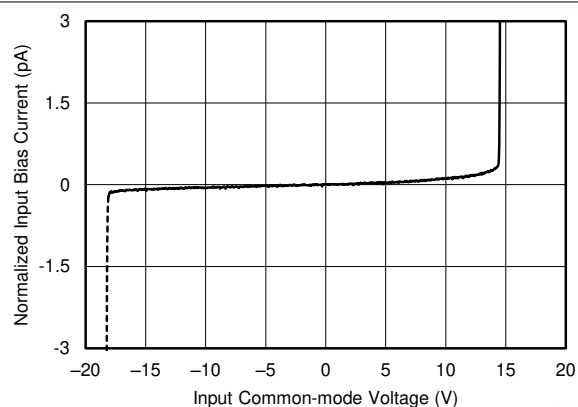


FIG 6-10. Input Bias Current vs Common-Mode Voltage

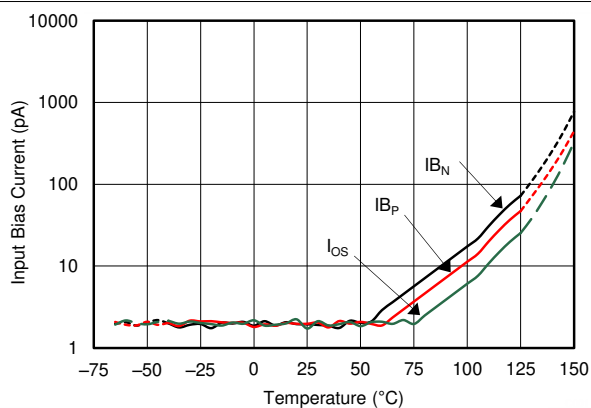


FIG 6-11. Input Bias Current and Offset vs Temperature

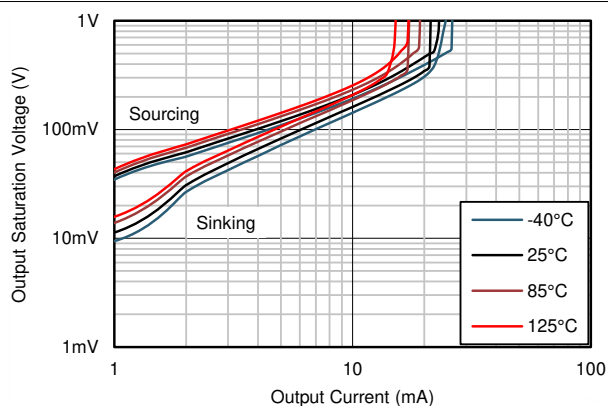
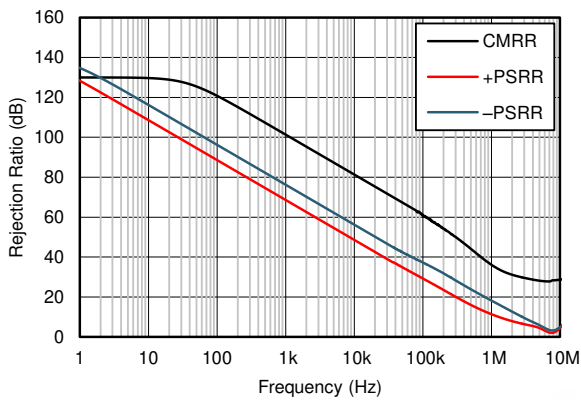


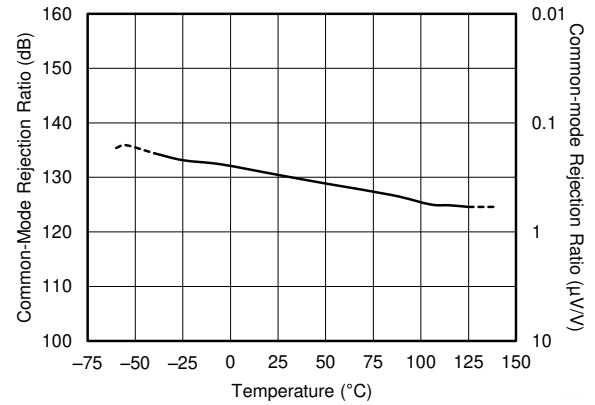
FIG 6-12. Output Voltage Swing vs Output Current (Maximum Supply)

## 6.7 Typical Characteristics (continued)

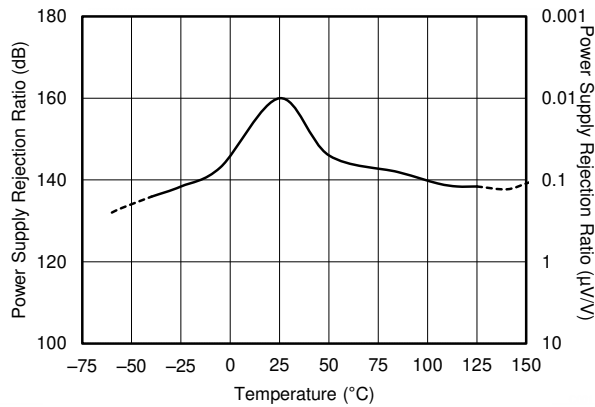
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



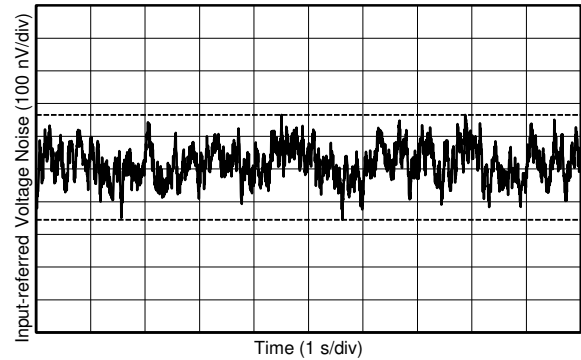
6-13. CMRR and PSRR vs Frequency



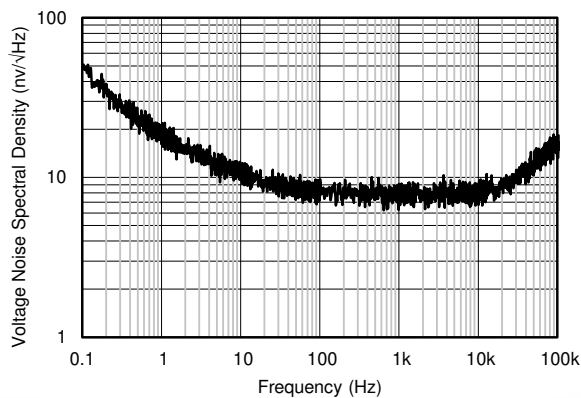
6-14. CMRR vs Temperature



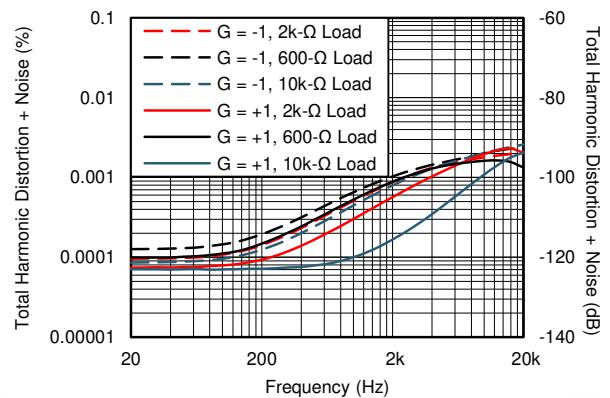
6-15. PSRR vs Temperature



6-16. 0.1-Hz to 10-Hz Voltage Noise



6-17. Input Voltage Noise Spectral Density vs Frequency



$V_{OUT} = 3.5$   $V_{RMS}, BW = 90\text{ kHz}$

6-18. THD+N Ratio vs Frequency

## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

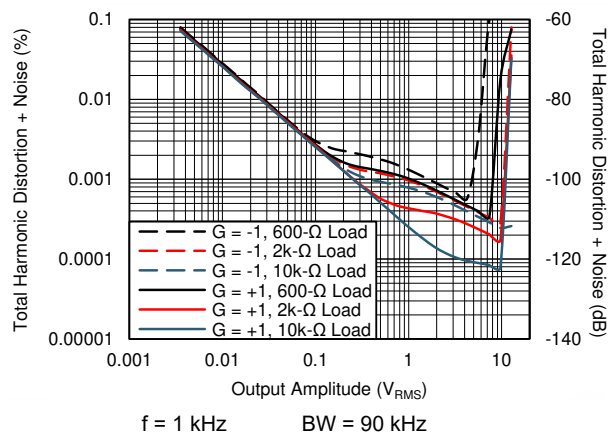


FIG 6-19. THD+N vs Output Amplitude

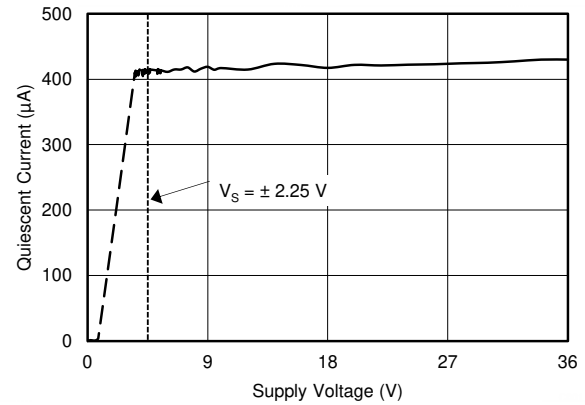


FIG 6-20. Quiescent Current vs Supply Voltage

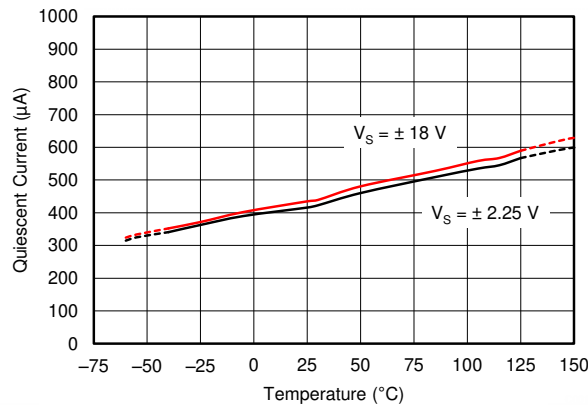


FIG 6-21. Quiescent Current vs Temperature

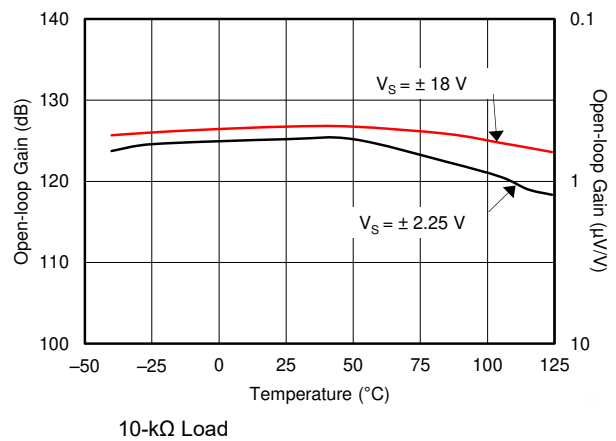


FIG 6-22. Open-Loop Gain vs Temperature

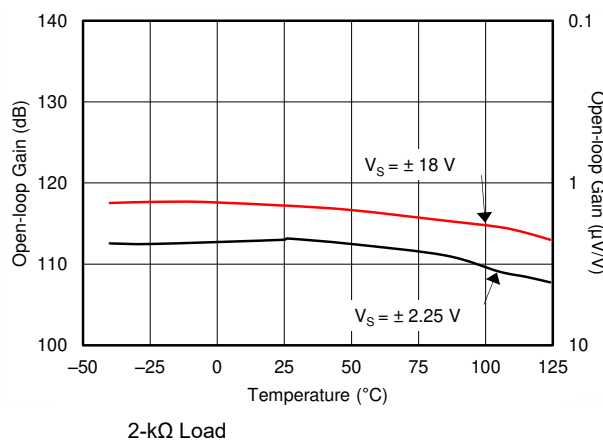


FIG 6-23. Open-Loop Gain vs Temperature

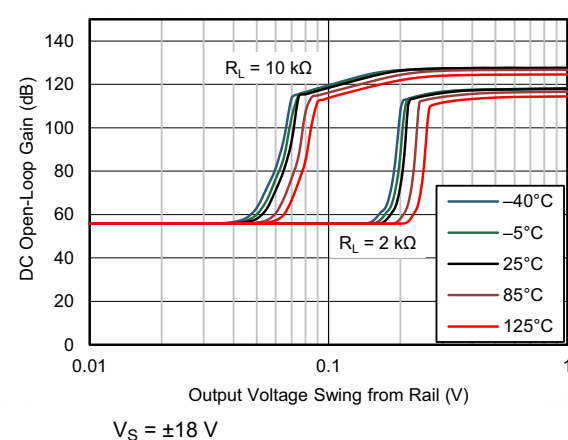


FIG 6-24. Open-Loop Gain vs Output Voltage Swing to Supply

## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

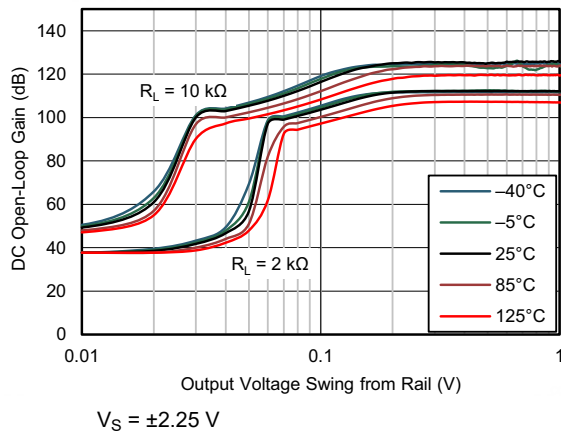


FIG 6-25. Open-Loop Gain vs Output Voltage Swing to Supply

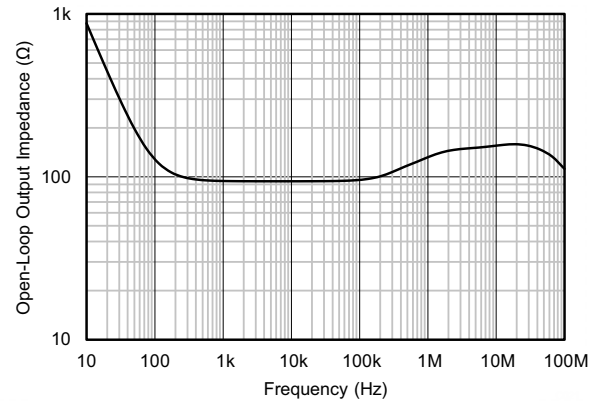


FIG 6-26. Open-Loop Output Impedance vs Frequency

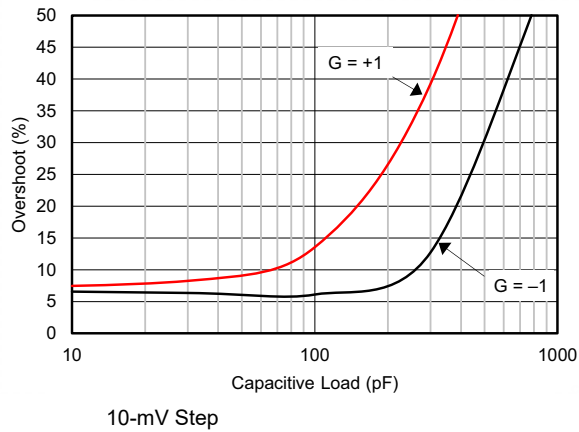


FIG 6-27. Small-Signal Overshoot vs Capacitive Load

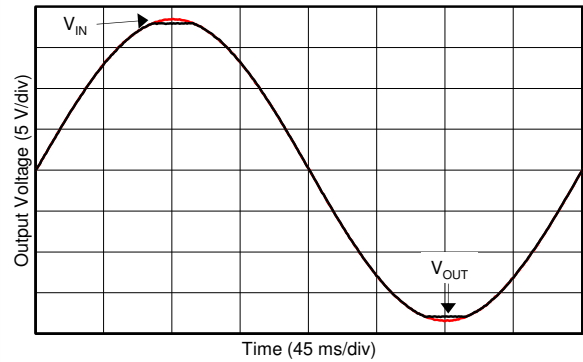


FIG 6-28. No Phase Reversal

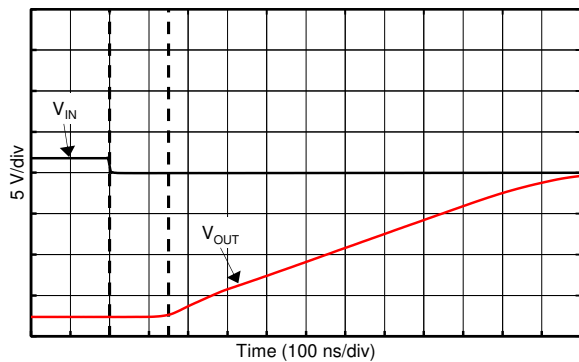


FIG 6-29. Positive Overload Recovery

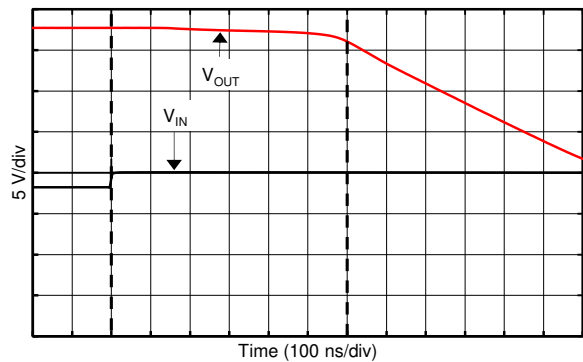
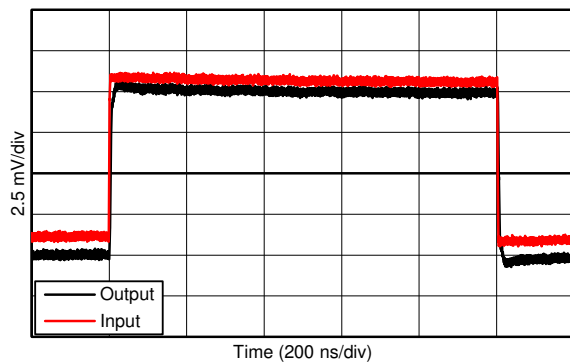


FIG 6-30. Negative Overload Recovery

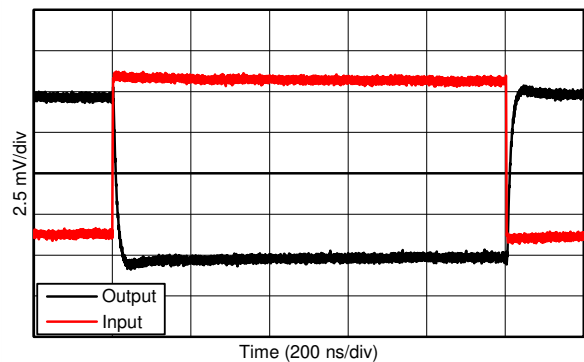
## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



$G = +1$

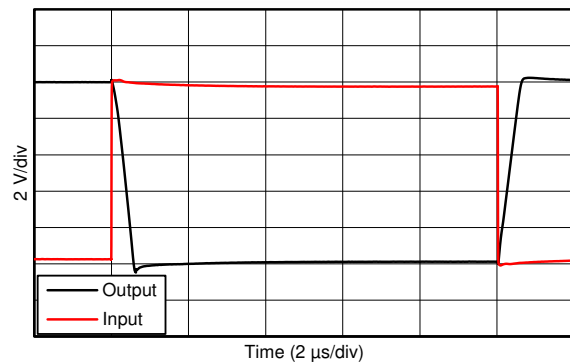
FIG 6-31. Small-Signal Step Response (10-mV Step)



10-mV Step

$G = -1$

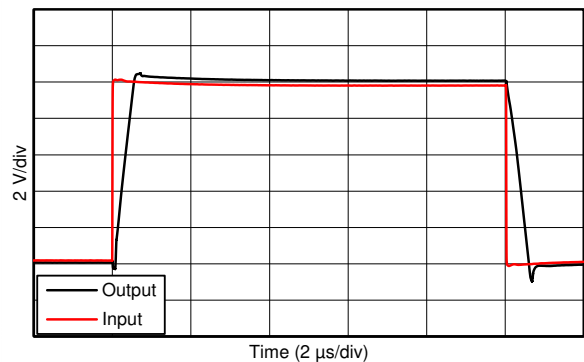
FIG 6-32. Small-Signal Step Response



10-V Step

$G = -1$

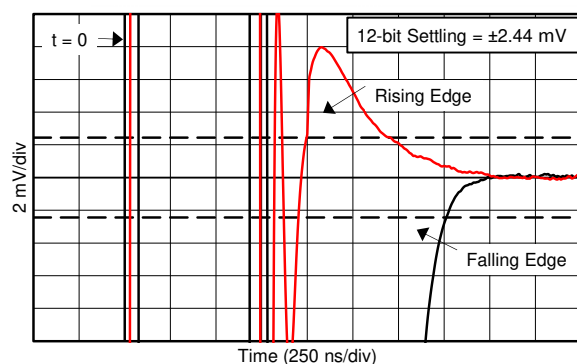
FIG 6-33. Large-Signal Step Response



10-V Step

$G = +1$

FIG 6-34. Large-Signal Step Response



12-bit settling on 10-V step =  $\pm 2.44\text{ mV}$

FIG 6-35. Settling Time (10-V Step)

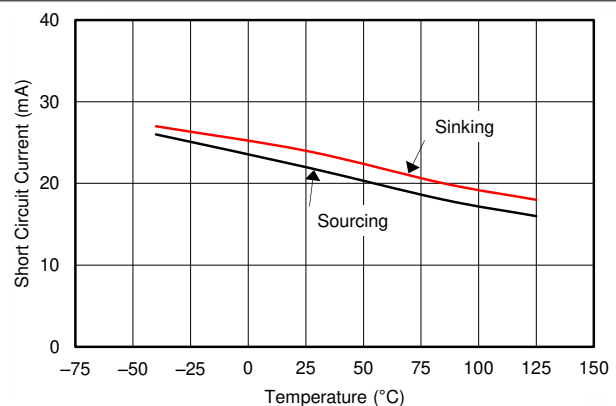
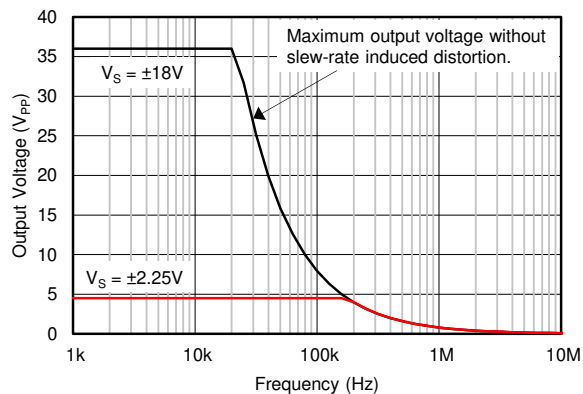


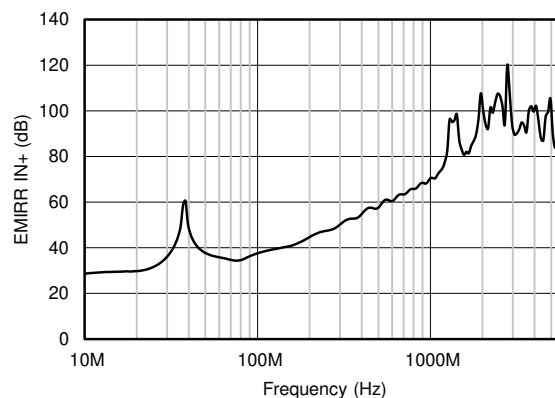
FIG 6-36. Short-Circuit Current vs Temperature

## 6.7 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



6-37. Maximum Output Voltage Amplitude vs Frequency



$P_{RF} = -10\text{ dBm}$

6-38. EMIRR vs Frequency

## 7 Detailed Description

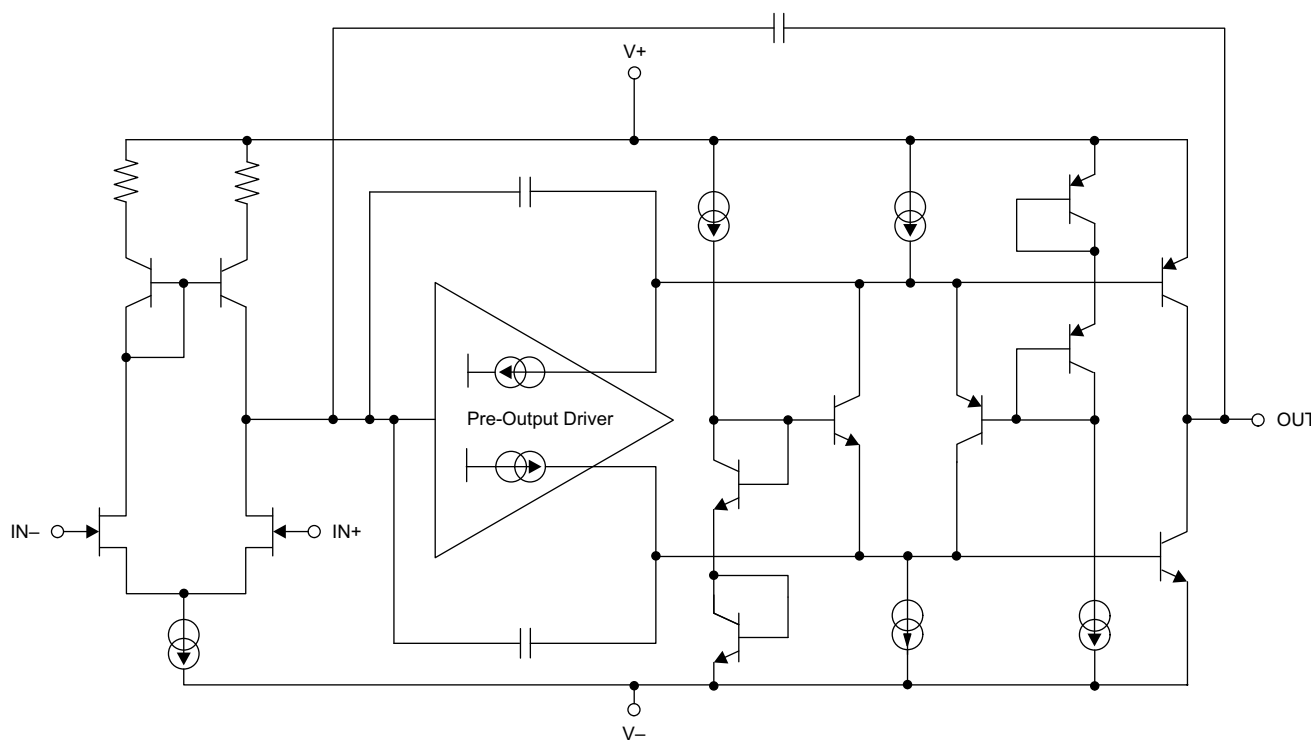
### 7.1 Overview

The OPA145 and OPA2145 (OPAx145) operational amplifiers are part of a family of low-power JFET input amplifiers that feature superior drift performance and low input bias current. The rail-to-rail output swing and input range that includes  $V^-$  allow designers to use the low-noise characteristics of JFET amplifier while also interfacing to modern, single-supply, precision, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPAx145 achieve 5.5-MHz gain-bandwidth product and 20-V/ $\mu$ s slew rate and consume only 445  $\mu$ A (typical) of quiescent current, making these devices an excellent choice for low-power applications. These devices operate on a single 4.5-V to 36-V supply or dual  $\pm 2.25$ -V to  $\pm 18$ -V supplies.

The OPAx145 are fully specified from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  for use in the most challenging environments. The single-channel OPA145 is available in 5-pin SOT-23, 8-pin SOIC, and 8-pin VSSOP packages. The dual-channel OPA2145 is available in 8-pin SOIC and 8-pin VSSOP packages.

セクション 7.2 shows the simplified diagram of the OPAx145.

### 7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

### 7.3 Feature Description

#### 7.3.1 Capacitive Load and Stability

The dynamic characteristics of the OPAx145 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ( $R_{OUT}$  equal to 50  $\Omega$ , for example) in series with the output.

Figure 6-27 illustrates the effects on small-signal overshoot for several capacitive loads. Also, see [Feedback Plots Define Op Amp AC Performance](#), available for download from the [TI website](#), for details of analysis techniques and application circuits.

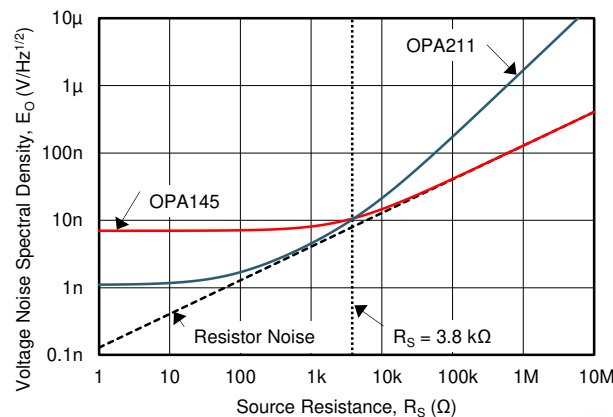


### 7.3.2 Output Current Limit

The output current of the OPAx145 is limited by internal circuitry to +20 mA (sinking) and –20 mA (sourcing) to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in [図 6-36](#).

### 7.3.3 Noise Performance

[図 7-1](#) shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPAx145 and [OPA211](#) are shown with total circuit noise calculated. The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPAx145 has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx145 is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.



NOTE: For a source resistance,  $R_S$ , greater than 3.8 kΩ, the OPAx145 is a lower-noise option compared to the OPA211, as shown in [図 7-1](#).

#### [図 7-1](#). Noise Performance of the OPAx145 and OPA211 in Unity-Gain Buffer Configuration

[式 1](#) can be used to calculate the total noise at the output of the amplifier. A plot can be created using this equation to quickly compare the noise performance of two different amplifiers when used with different source resistances, as is shown in [図 7-1](#).

$$E_O^2 = e_n^2 + (i_n \times R_S)^2 + 4kTR_S \quad (1)$$

where:

- $e_n$  = voltage noise
- $i_n$  = current noise
- $R_S$  = source impedance
- $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K
- $T$  = temperature in kelvins (K)

For more details on calculating noise, see [セクション 7.3.4](#).

### 7.3.4 Basic Noise Calculations

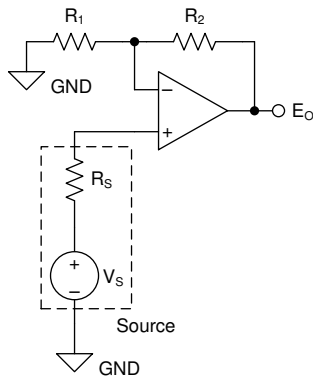
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 7-1](#). The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 7-2](#) illustrates both noninverting (**A**) and inverting (**B**) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx145 means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

#### (A) Noise in Noninverting Gain Configuration



Noise at the output is given as  $E_O$ , where

$$(1) \quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + (e_{R_1 \parallel R_2})^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

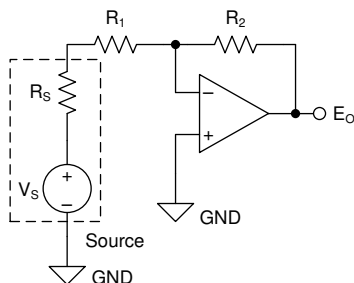
$$(2) \quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3) \quad e_{R_1 \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \parallel R_2$$

$$(4) \quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5) \quad T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

#### (B) Noise in Inverting Gain Configuration



Noise at the output is given as  $E_O$ , where

$$(6) \quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + (e_{R_1 + R_S \parallel R_2})^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

$$(7) \quad e_{R_1 + R_S \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \parallel R_2$$

$$(8) \quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9) \quad T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

Copyright © 2017, Texas Instruments Incorporated

Where:  $e_N$  is the voltage noise of the amplifier. For the OPAx145 operational amplifier,  $e_N = 7 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz.

Where:  $i_N$  is the current noise of the amplifier. For the OPAx145 operational amplifier,  $i_N = 0.8 \text{ fA}/\sqrt{\text{Hz}}$  at 1 kHz.

NOTE: For additional resources on noise calculations visit [TI's Precision Labs Series](#).

### 7-2. Noise Calculation in Gain Configurations

### 7.3.5 Phase-Reversal Protection

The OPAx145 has internal phase-reversal protection. Many FET-input and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPAx145 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see [Figure 6-28](#)).

### 7.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See [Figure 7-3](#) for an illustration of the ESD circuits contained in the OPAx145 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the power supply is connected to an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse that discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent the amplifier from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPAx145 but less than the device breakdown voltage level. After this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

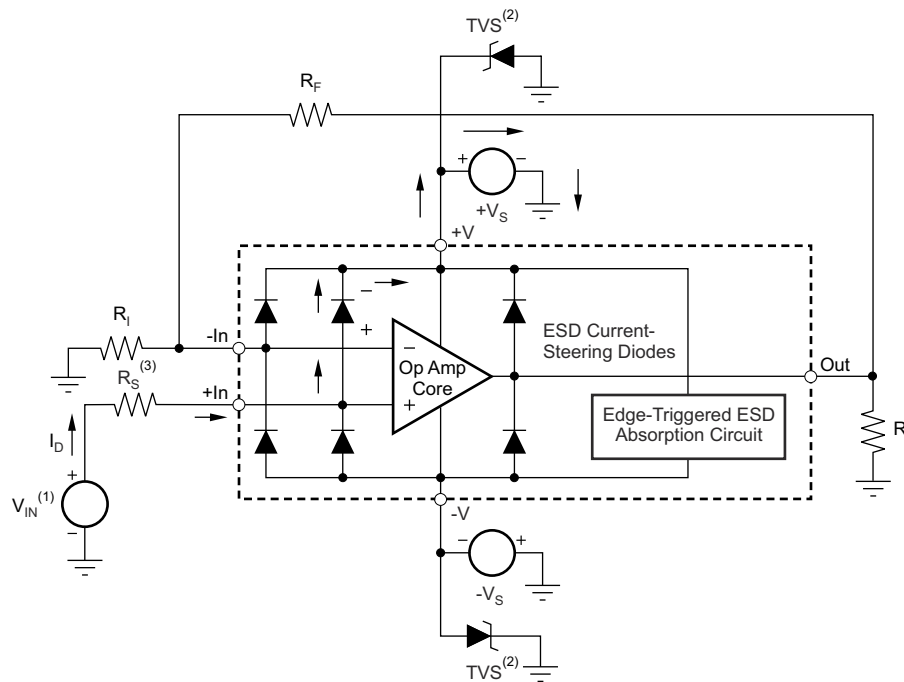
When the operational amplifier connects into a circuit, such as the one [Figure 7-3](#) shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

[Figure 7-3](#) depicts a specific example where the input voltage,  $V_{IN}$ , exceeds the positive supply voltage ( $+V_S$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $+V_S$  can sink the current, one of the upper input steering diodes conducts and directs current to  $+V_S$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies  $+V_S$  or  $-V_S$  are at 0 V. The answer depends on the supply characteristic while at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in [Figure 7-3](#). The Zener voltage must be selected so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1)  $V_{IN} = +V_S + 500 \text{ mV}$ .

(2) TVS:  $+V_{S(max)} > V_{TVSBR (Min)} > +V_S$

(3) Suggested value approximately 1 k $\Omega$ .

**Figure 7-3. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

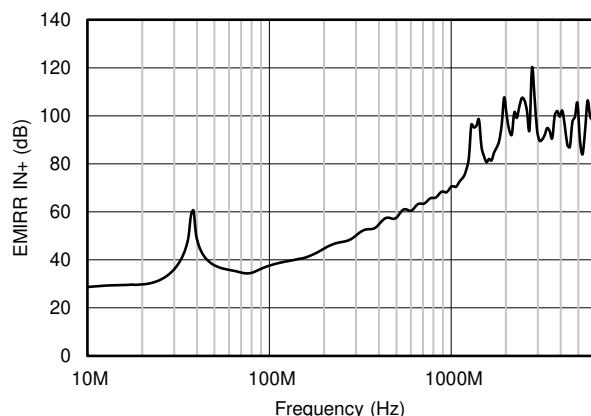
### 7.3.7 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

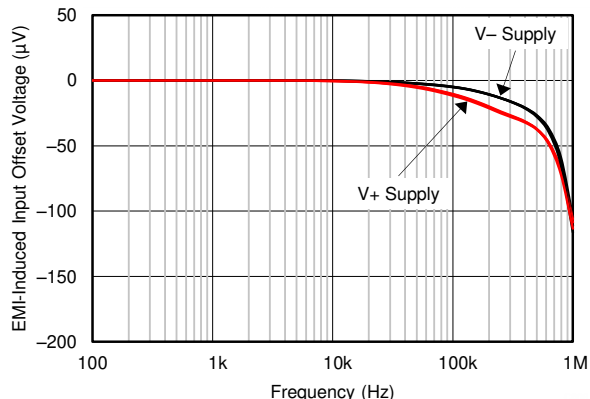
- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier result in adverse effects, as the amplifier would not have sufficient loop gain to correct for signals with spectral content outside the amplifier bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected dc offsets, transient voltages, or other unknown behavior. Be sure to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces. [Figure 7-5](#) shows the effect of conducted EMI to the power supplies on the input offset voltage of OPAx145.

The EMIRR IN+ of the OPAx145 is plotted versus frequency as shown in [Figure 7-4](#). The OPAx145 unity-gain bandwidth is 5.5 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth. See [EMI Rejection Ratio of Operational Amplifiers](#), available for download from [www.ti.com](http://www.ti.com).



**Figure 7-4. OPAx145 EMIRR IN+**



**Figure 7-5. OPAx145 EMI-Induced Input Offset Voltage (Power Supplies)**

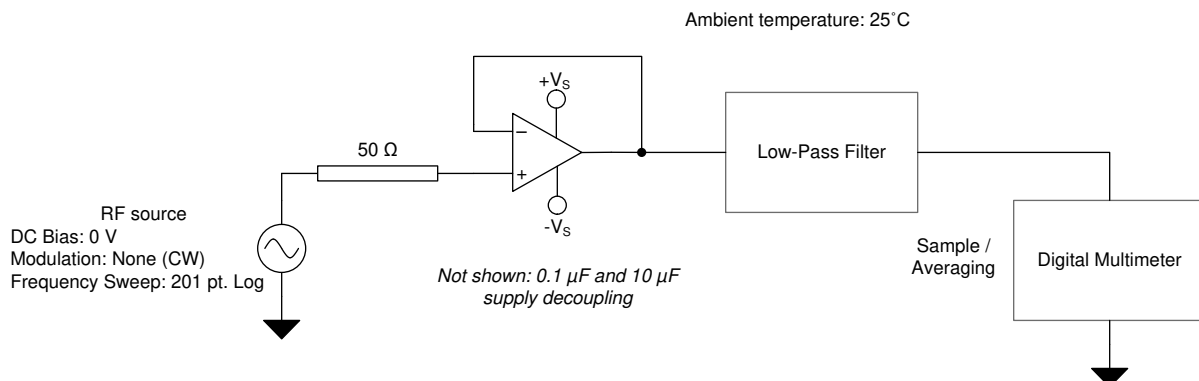
表 7-1 lists the EMIRR IN+ values for the OPAx145 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 7-1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

**表 7-1. OPAx145 EMIRR IN+ for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION                                                                                                                                                        | EMIRR IN+ |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 400 MHz   | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications                                                                         | 54 dB     |
| 900 MHz   | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications                        | 68 dB     |
| 1.8 GHz   | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)                                                                                  | 86 dB     |
| 2.4 GHz   | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 107 dB    |
| 3.6 GHz   | Radiolocation, aero communication and navigation, satellite, mobile, S-band                                                                                                      | 100 dB    |
| 5 GHz     | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)                                                | 105 dB    |

### 7.3.8 EMIRR +IN Test Configuration

图 7-6 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.



**图 7-6. EMIRR +IN Test Configuration**

## 7.4 Device Functional Modes

The OPAx145 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V ( $\pm 2.25$  V). The maximum power supply voltage for the OPAx145 is 36 V ( $\pm 18$  V).

## 8 Application and Implementation

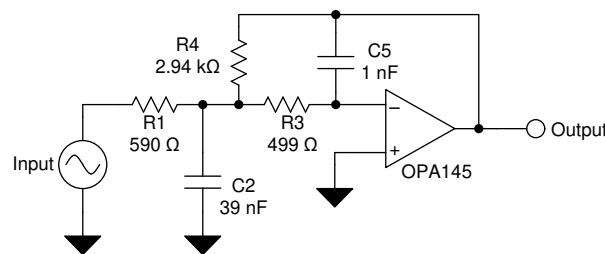
### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The OPAx145 are unity-gain stable operational amplifiers with low noise, low input-bias current, and low input-offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. Designers can easily use the rail-to-rail output swing and input range that includes V<sub>−</sub> to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

### 8.2 Typical Application



Copyright © 2017, Texas Instruments Incorporated

**8-1. 25-kHz Low-Pass Filter**

#### 8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx145 are designed to construct high-speed, high-precision active filters. 8-1 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

#### 8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 8-1. Use 式 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (2)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by 式 3:

$$\begin{aligned} \text{Gain} &= \frac{R_4}{R_1} \\ f_c &= \frac{1}{2\pi} \sqrt{1/R_3 R_4 C_2 C_5} \end{aligned} \quad (3)$$

For systems which have different filter parameters or require specific system optimization, such as minimizing the system noise, an alternative device may be desired. A list of recommended alternatives can be found in 表 8-1.

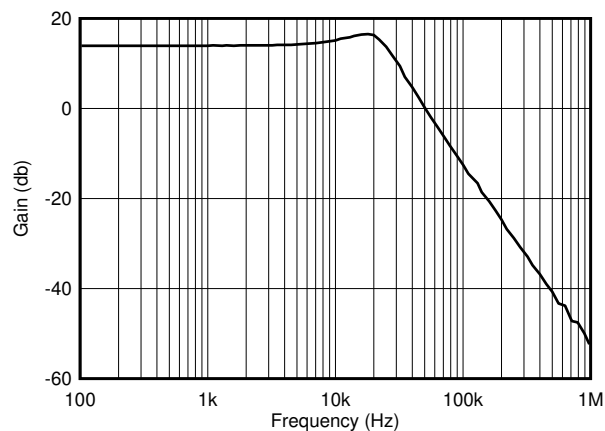
**表 8-1. Alternative Devices**

| FEATURES                                                                           | PRODUCT                |
|------------------------------------------------------------------------------------|------------------------|
| Low-power, 10-MHz FET input industrial op amp                                      | <a href="#">OPA140</a> |
| 2.2-nV/√ Hz, low-power, 36-V op amp in SOT-23 package                              | <a href="#">OPA209</a> |
| Low-noise, high-precision, 22-MHz, 4-nV/√ Hz JFET-input op amp                     | <a href="#">OPA827</a> |
| Low-noise, low I <sub>Q</sub> precision CMOS op amp                                | <a href="#">OPA376</a> |
| Low-power, precision, CMOS, rail-to-rail input/output, low-offset, low-bias op amp | <a href="#">OPA191</a> |

Software tools are readily available to simplify filter design. [WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets designers create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows designers to design, optimize, and simulate complete multistage active filter solutions within minutes.

### 8.2.3 Application Curve



**图 8-2. OPAx145 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter**

## 8.3 System Examples

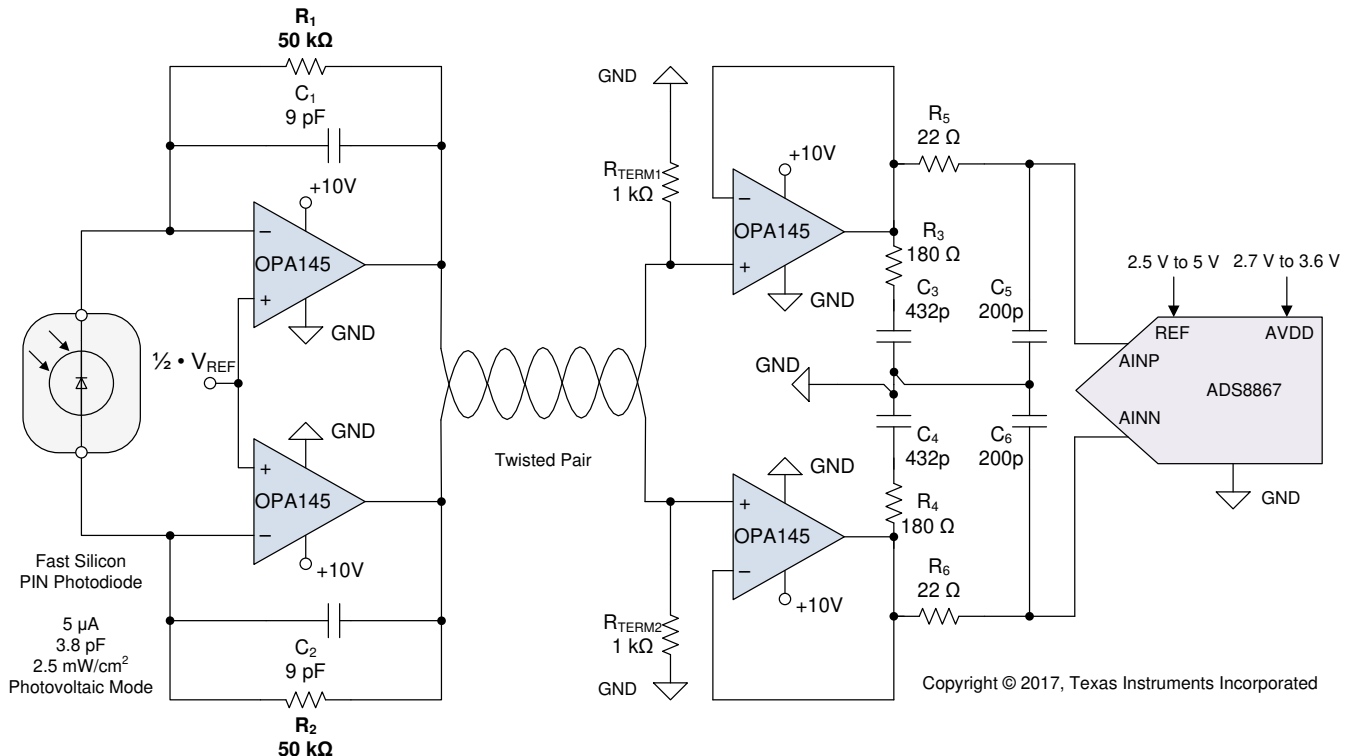
### 8.3.1 16-Bit, 100-kSPS, Fully Differential Transimpedance Imaging and Measurement

The OPAx145 are used in a differential transimpedance (I-V) measurement application capable of driving the [ADS8867](#), a 16-bit, microPower, truly-differential ADC, at its maximum conversion rate of 100 kSPS with an acquisition time of 1200 ns and conversion time of 8800 ns. The first stage supports a forward bandwidth of 493.5 kHz with 100 kΩ of transimpedance gain, enabling the photodiode to fully charge and settle to ±38 μV (±1/2 LSB on 5-V ADC reference voltage) within the conversion time of the ADC. The differential nature of the system provides several advantages such as double the transimpedance gain compared to a single-ended system, improved signal-to-noise ratio, easy interfacing to high-precision, fully-differential ADCs, and additional protection against inductively-coupled noise and interference. Additionally, capacitively-coupled common-mode transients can be minimized using low-impedance termination resistors R<sub>TERM1</sub> and R<sub>TERM2</sub>.

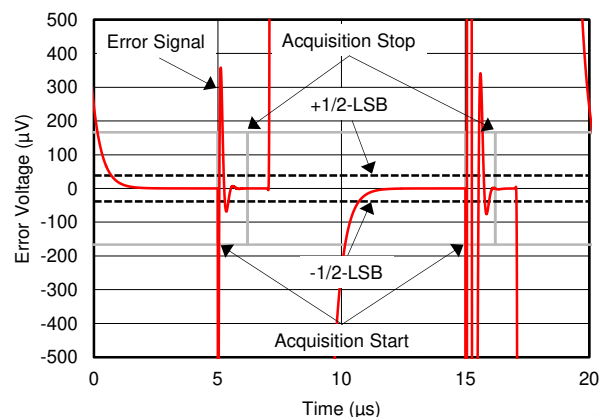
The second stage provides the reverse bandwidth required for settling to 16-bit accuracy after the internal sampling capacitor of the successive-approximation-register (SAR) ADC is connected to the second stage. The two OPAx145 amplifiers in the second stage are configured as buffers for maximum closed-loop bandwidth, and their stability is optimized using R3, C3 and R4, C4 by creating a snubber that reduces the open-loop output impedance (see 图 6-26). C5 and C6 are provided as a charge reservoir for the internal sampling capacitor of the ADC, and R5 and R6 are tuned to optimize the phase margin of the second stage to drive the output



capacitance. This two-stage approach enables compatibility with a wide selection of high output-impedance sensors while still maintaining 16-bit settling performance. Furthermore, the first stage can be designed with sufficient phase margin to drive twisted-pair transmission lines in remote measurement systems. Proper design of the transmission line reduces the interference of other signals over long distances. [Figure 8-4](#) shows the settling performance of the system described previously and in [Figure 8-3](#) — the settling time during the acquisition cycle is shown for settling successfully to 0  $\mu\text{A}$  from 5  $\mu\text{s}$  to 6.2  $\mu\text{s}$ . At 6.3  $\mu\text{s}$ , the photodiode current is changed to 5  $\mu\text{A}$  (full-scale) and settles during the conversion cycle of the ADC (6.2  $\mu\text{s}$  to 15  $\mu\text{s}$ ), and is then acquired successfully from 15  $\mu\text{s}$  to 16.2  $\mu\text{s}$ .



**Figure 8-3. 16-bit, 100-kSPS, Fully Differential Transimpedance Schematic**



**Figure 8-4. 16-bit, 100-kSPS, Fully Differential Transimpedance Settling Performance**

## 9 Power Supply Recommendations

The OPAx145 are specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [セクション 6.7](#).

### 注意

Supply voltages larger than 40 V can permanently damage the device; see [セクション 6.1](#)

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [セクション 10](#).

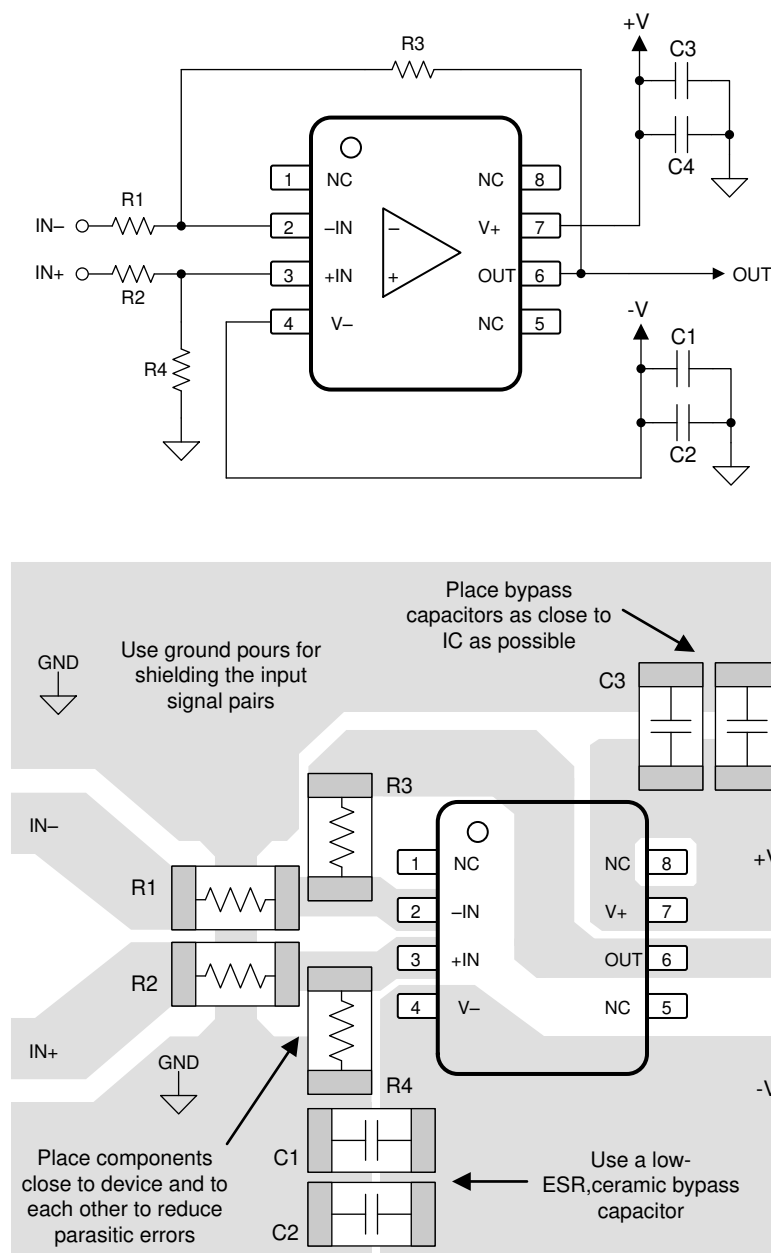
## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see [The PCB is a component of op amp design technical brief](#).
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in [図 10-1](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example



Copyright © 2017, Texas Instruments Incorporated

**FIG 10-1. Operational Amplifier Board Layout for Difference Amplifier Configuration**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

---

#### 注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

---

##### 11.1.1.2 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

##### 11.1.1.3 TI Precision Designs

TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [The PCB is a component of op amp design](#)
- Texas Instruments, [OPA140, OPA2140, OPA4140 EMI Immunity Performance](#)
- Texas Instruments, [Compensate Transimpedance Amplifiers Intuitively](#)
- Texas Instruments, [Operational amplifier gain stability, Part 3: AC gain-error analysis](#)
- Texas Instruments, [Operational amplifier gain stability, Part 2: DC gain-error analysis](#)
- Texas Instruments, [Using infinite-gain, MFB filter topology in fully differential active filters](#)
- Texas Instruments, [Op Amp Performance Analysis](#)
- Texas Instruments, [Single-Supply Operation of Operational Amplifiers](#)
- Texas Instruments, [Tuning in Amplifiers](#)
- Texas Instruments, [Shelf-Life Evaluation of Lead-Free Component Finishes](#)
- Texas Instruments, [Feedback Plots Define Op Amp AC Performance](#)
- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#)を参照してください。

## 11.5 Trademarks

TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.  
TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.  
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.  
WEBENCH® is a registered trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

## 11.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.7 用語集

**TI 用語集** この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| OPA145ID         | ACTIVE        | SOIC         | D                  | 8    | 75             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | OPA145                  | <a href="#">Samples</a> |
| OPA145IDBVR      | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 1IB2                    | <a href="#">Samples</a> |
| OPA145IDBVT      | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 1IB2                    | <a href="#">Samples</a> |
| OPA145IDGKR      | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | RoHS & Green    | NIPDAUAG   SN                        | Level-2-260C-1 YEAR  | -40 to 125   | 1I4Q                    | <a href="#">Samples</a> |
| OPA145IDGKT      | ACTIVE        | VSSOP        | DGK                | 8    | 250            | RoHS & Green    | NIPDAUAG   SN                        | Level-2-260C-1 YEAR  | -40 to 125   | 1I4Q                    | <a href="#">Samples</a> |
| OPA145IDR        | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | OPA145                  | <a href="#">Samples</a> |
| OPA2145IDGKR     | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 2BQJ                    | <a href="#">Samples</a> |
| OPA2145IDGKT     | ACTIVE        | VSSOP        | DGK                | 8    | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 2BQJ                    | <a href="#">Samples</a> |
| OPA2145IDR       | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | OP2145                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

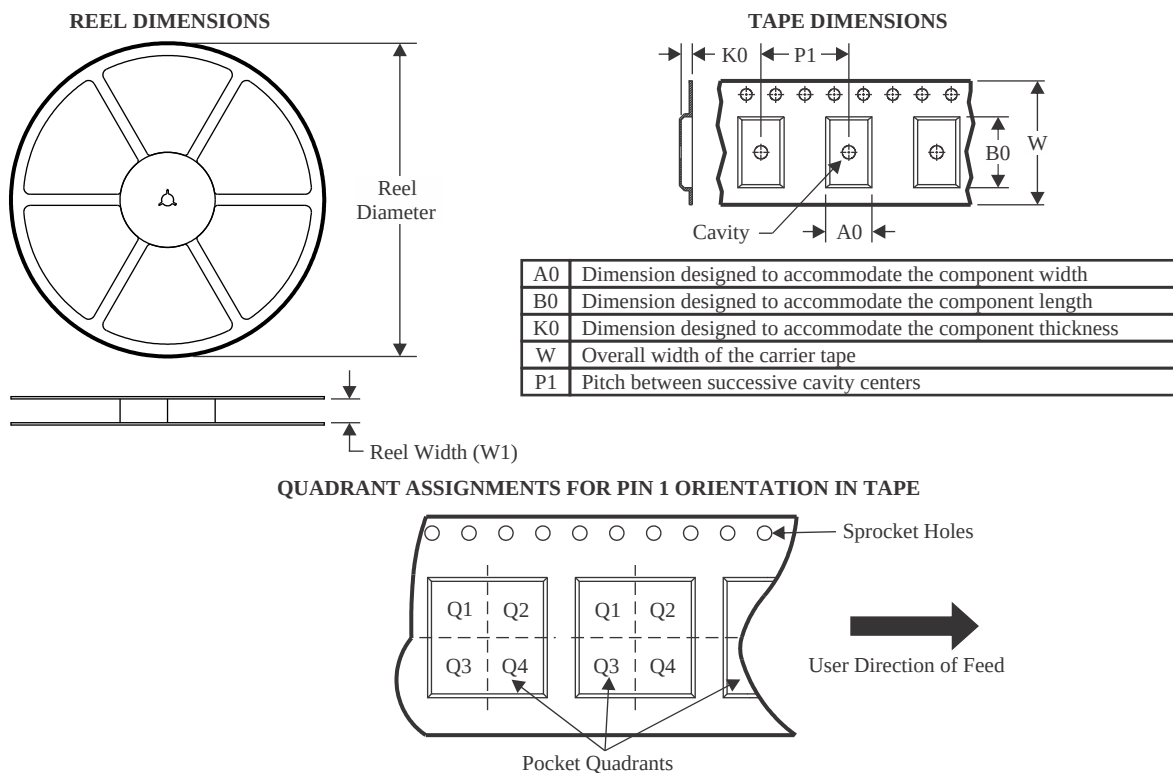
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA145IDBVR  | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA145IDBVT  | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA145IDGKR  | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA145IDGKT  | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA145IDR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA2145IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2145IDGKT | VSSOP        | DGK             | 8    | 250  | 180.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2145IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA145IDBVR  | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA145IDBVT  | SOT-23       | DBV             | 5    | 250  | 213.0       | 191.0      | 35.0        |
| OPA145IDGKR  | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| OPA145IDGKT  | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| OPA145IDR    | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA2145IDGKR | VSSOP        | DGK             | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| OPA2145IDGKT | VSSOP        | DGK             | 8    | 250  | 210.0       | 185.0      | 35.0        |
| OPA2145IDR   | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device   | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA145ID | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |

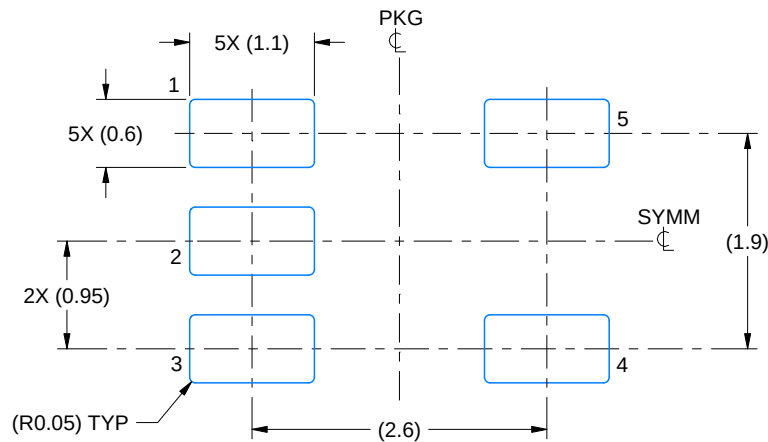


# EXAMPLE BOARD LAYOUT

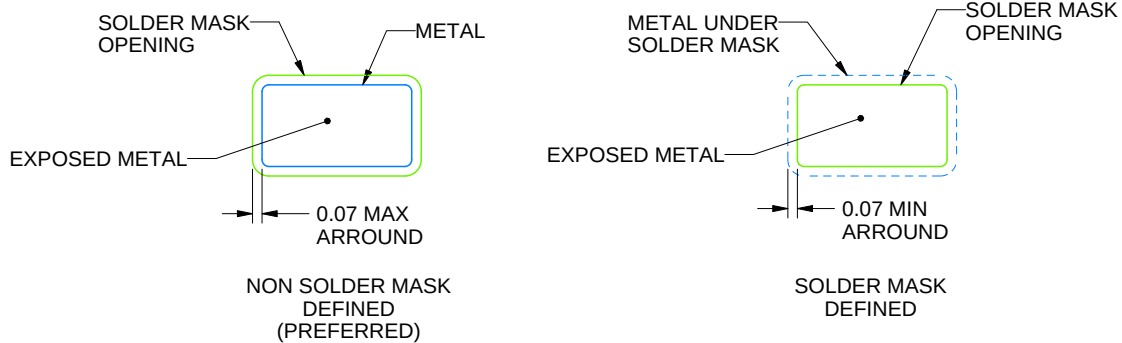
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

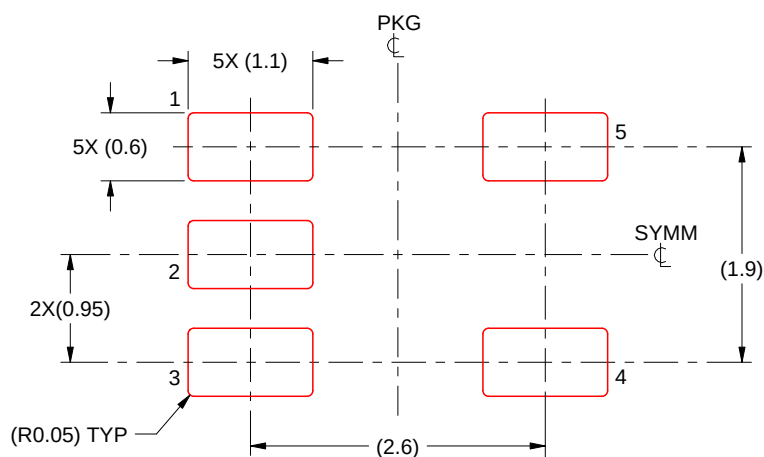
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

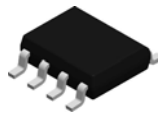


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

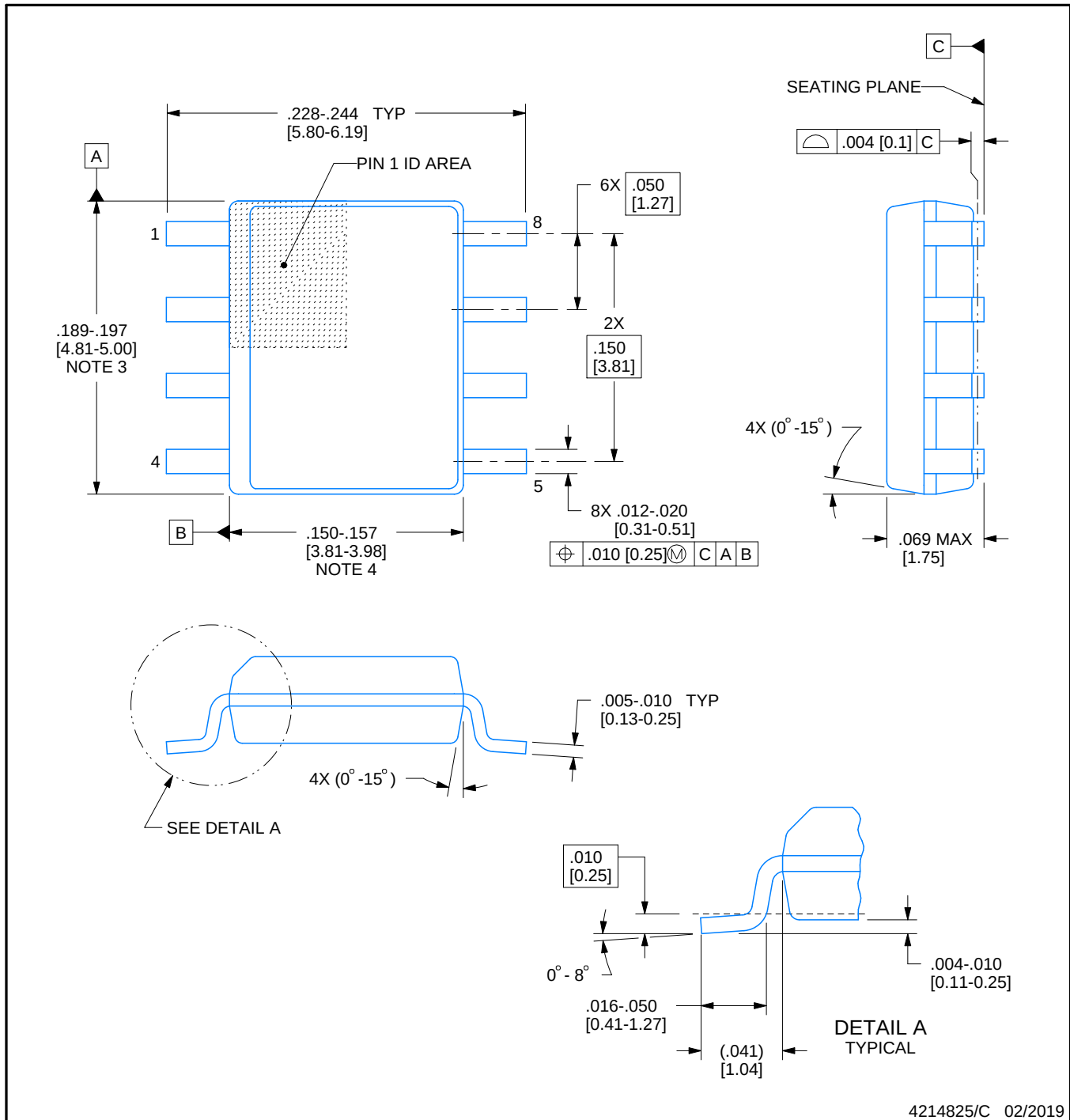


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

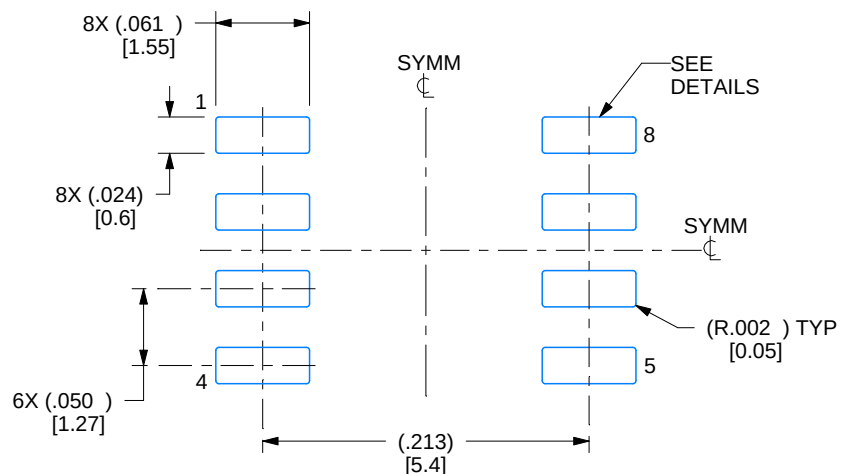
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

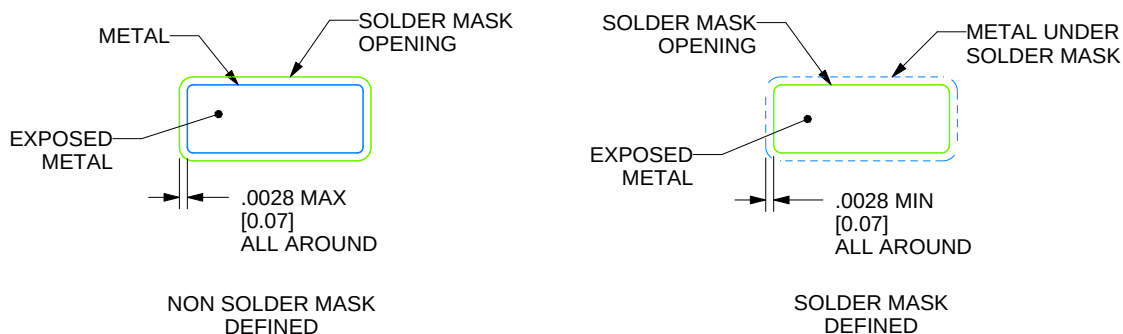
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

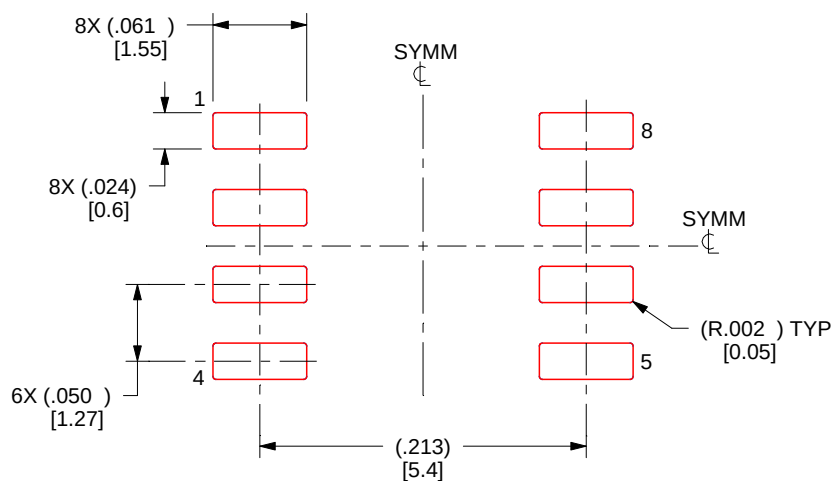
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

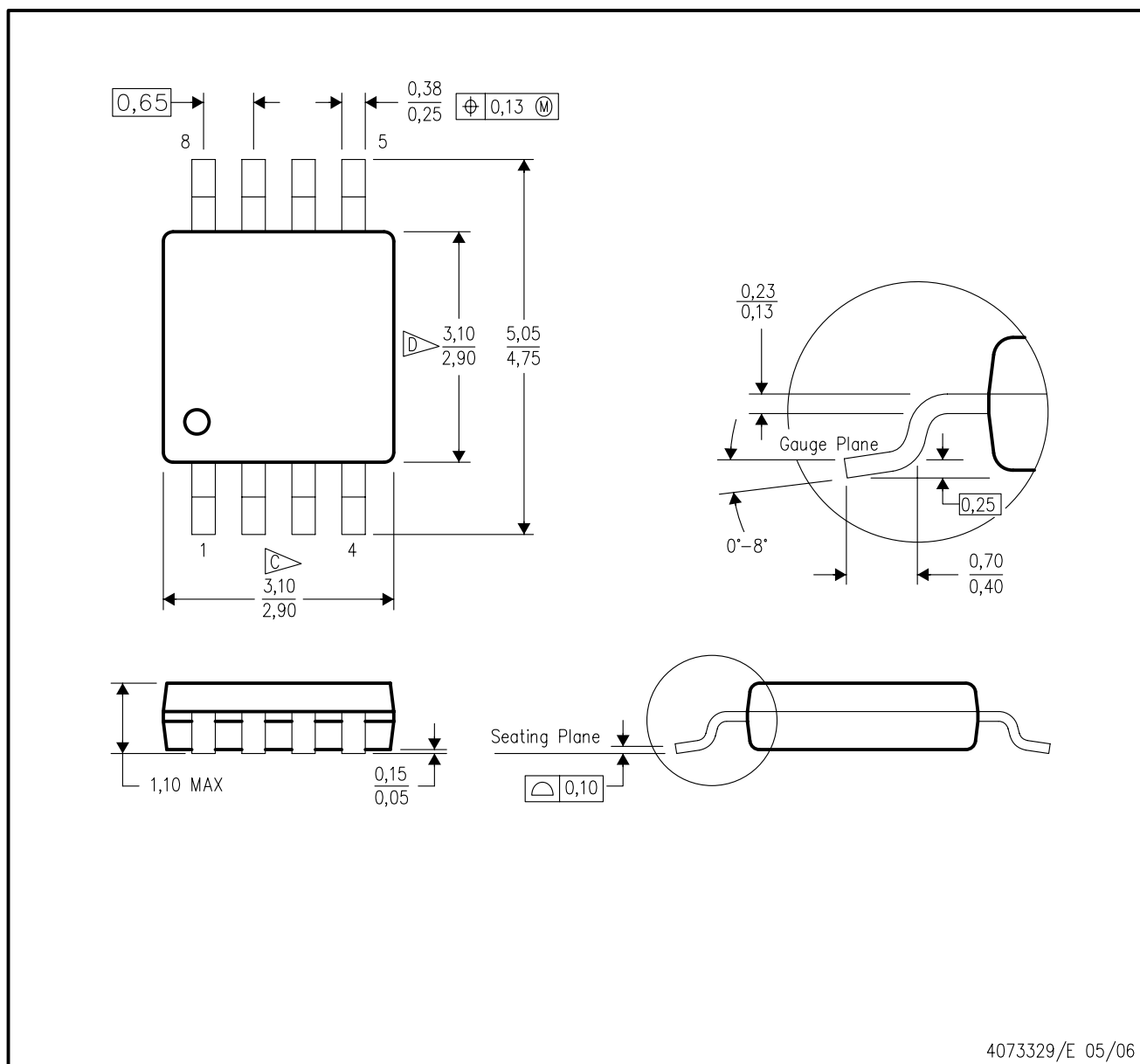
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DGK (S-PDSO-G8)

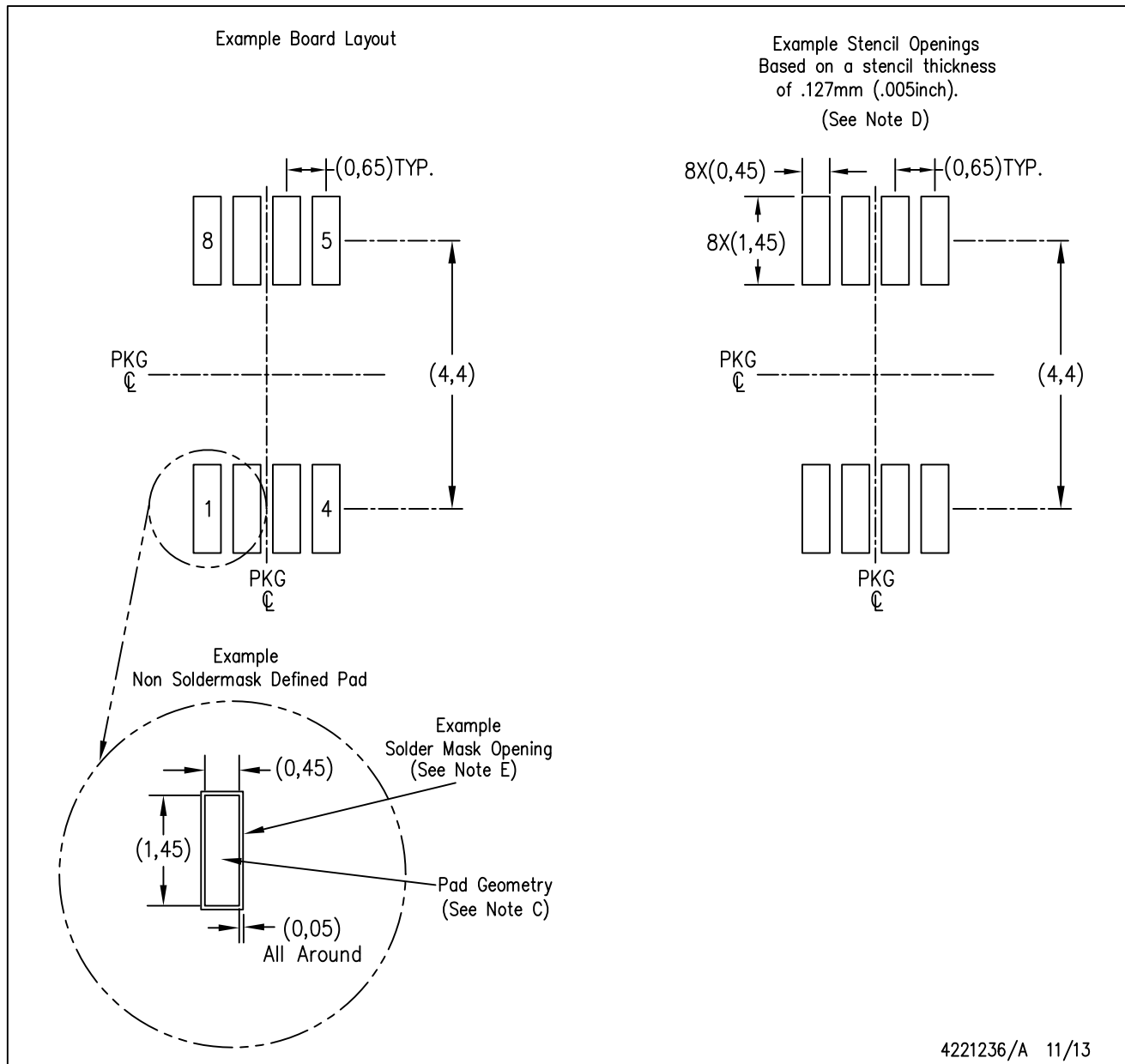
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

## D GK (S-PDSO-G8)

# PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated