

OPAx187 0.001 μ V/°Cドリフト、低消費電力、レール・ツー・レール出力、36Vオペアンプ、ゼロ・ドリフト・シリーズ

1 特長

- 低いオフセット電圧: 10 μ V (最大値)
- ゼロ・ドリフト: 0.001 μ V/°C
- 低ノイズ: 15nV/ $\sqrt{\text{Hz}}$
- PSRR: 160dB
- CMRR: 140dB
- AOL: 160dB
- 静止電流: 100 μ A
- 広い電源電圧範囲: $\pm 2.25\text{V} \sim \pm 18\text{V}$
- レール・ツー・レール出力動作
- 入力に負のレールも含む
- 低いバイアス電流: 100pA (標準値)
- EMIフィルタ付き入力
- Microsizeパッケージ

2 アプリケーション

- ブリッジ・アンプ
- 歪みゲージ
- テストおよび計測機器
- トランスデューサ・アプリケーション
- 温度測定
- 電子計測器
- 医療用計測機器
- RTDアンプ
- 高精度アクティブ・フィルタ
- ローサイド電流監視

3 概要

OPAx187シリーズのオペアンプは、オートゼロ方式を採用して、低いオフセット電圧(1 μ V)と、時間や温度の変化に対してほぼゼロのドリフト係数を同時に実現しています。これらのアンプは小型、高精度で、静止電流が低く、入力インピーダンスが高く、高インピーダンスの負荷に対してレールの5mV以内のレール・ツー・レール出力を供給します。入力同相範囲には、負のレールも含まれます。4.5V $\sim$ 36Vの範囲($\pm 2.25\text{V}$ から $\pm 18\text{V}$ まで)の単一電源またはデュアル電源を使用できます。

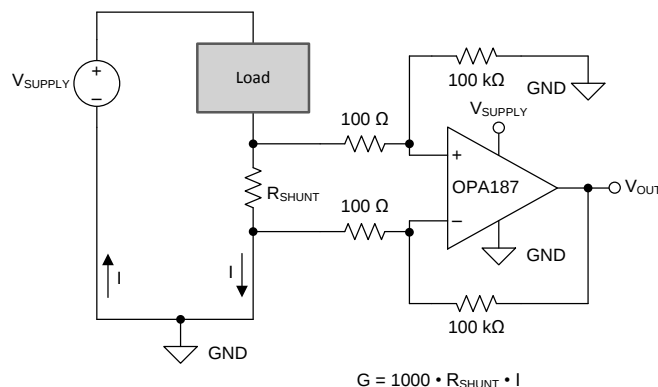
OPAx187 デバイスのシングル・バージョンは、Microsize 8ピン VSSOP、5ピン SOT-23、8ピン SOIC のパッケージで供給されます。デュアル・バージョンは、8ピン VSSOP および 8ピン SOIC のパッケージで供給されます。クワッド・バージョンは、14ピン SOIC、14ピン TSSOP、16ピン WQFNパッケージで供給されます。どのバージョンも、-40°C $\sim$ +125°Cでの動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
OPA187	SOIC (8)	4.90mm $\times$ 3.91mm
	SOT-23 (5)	2.90mm $\times$ 1.60mm
	VSSOP (8)	3.00mm $\times$ 3.00mm
OPA2187	SOIC (8)	4.90mm $\times$ 3.91mm
	VSSOP (8)	3.00mm $\times$ 3.00mm
OPA4187	SOIC (14)	8.70mm $\times$ 3.90mm
	TSSOP (14)	5.00mm $\times$ 4.40mm
	WQFN (16) (プレビュー)	4.00mm $\times$ 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

OPAx187による高精度のローサイド電流測定



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (December 2018) から Revision D に変更	Page
• OPA4187 の SOIC および TSSOP パッケージを製品プレビューから量産データに 変更	1
• Changed offset drift (high and low supply) max to $\pm 15 \text{ nV}/^\circ\text{C}$	8

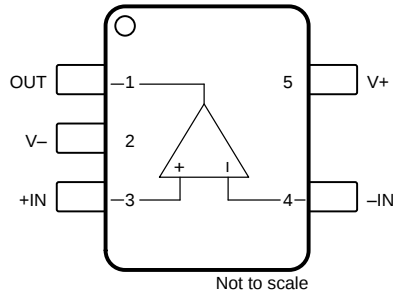
Revision B (October 2018) から Revision C に変更	Page
• 量産 OPA187 SOIC デバイスの最初のリリース	1

Revision A (July 2017) から Revision B に変更	Page
• OPA187 SOIC のステータスをプレビューに 変更	1
• OPA4187 の SOIC、TSSOP、WQFN のステータスをプレビューに 変更	1
• Changed offset drift (high supply) typical from $\pm 5 \text{ nV}/^\circ\text{C}$ to $\pm 1 \text{ nV}/^\circ\text{C}$ and max from $\pm 50 \text{ nV}/^\circ\text{C}$ to $\pm 20 \text{ nV}/^\circ\text{C}$	7
• Changed input bias current max (high supply) from $\pm 5 \text{ nA}$ to $\pm 7.5 \text{ nA}$	7
• Changed input offset current max (high supply) from $\pm 5 \text{ nA}$ to $\pm 14.5 \text{ nA}$	7
• Changed offset drift (low supply) typical from $\pm 5 \text{ nV}/^\circ\text{C}$ to $\pm 1 \text{ nV}/^\circ\text{C}$ and max from $\pm 50 \text{ nV}/^\circ\text{C}$ to $\pm 20 \text{ nV}/^\circ\text{C}$	8
• 変更 Offset Voltage Production Distribution figure	10

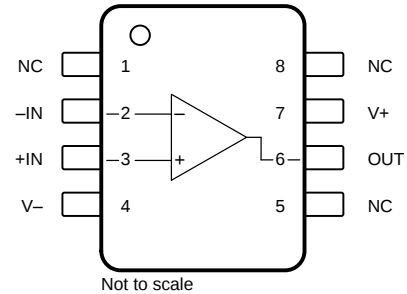
2016年12月発行のものから更新	Page
• 「概要」から VSON パッケージ・オプションを 削除	1
• 「製品情報」表から VSON パッケージ・オプションを 削除	1
• 「製品情報」表に WQFN パッケージ・オプションを 追加	1
• Deleted OPA187 DRG package option from <i>Pin Configuration and Functions</i>	3
• Added WQFN package to <i>Pin Configuration and Functions</i>	4

5 Pin Configuration and Functions

**OPA187: DBV Package
5-Pin SOT-23
Top View**



**OPA187: D and DGK Packages
8-Pin SOIC and 8-pin VSSOP
Top View**

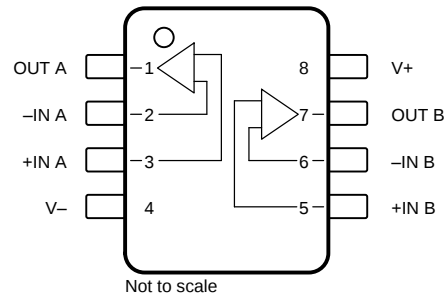


(1) NC denotes no internal connection.

Pin Functions: OPA187

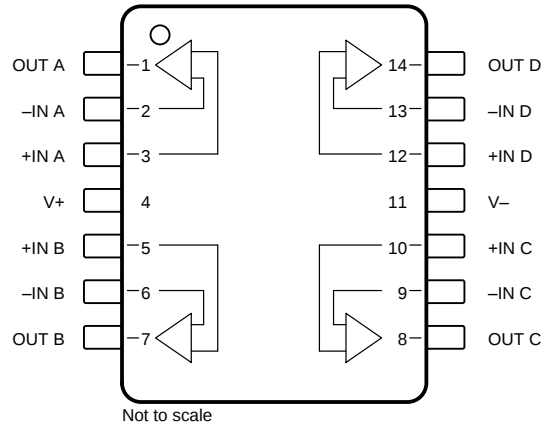
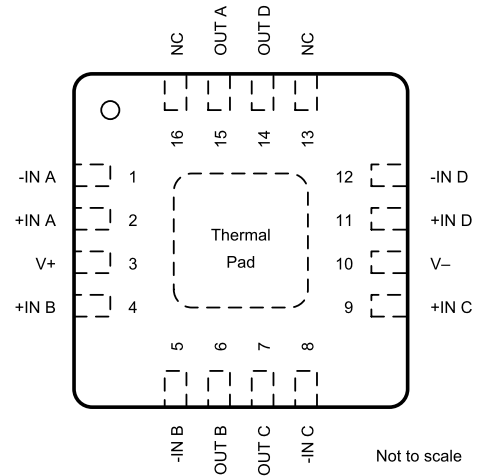
PIN			I/O	DESCRIPTION
NAME	DBV	D and DGK		
+IN	3	3	I	Non-inverting input
-IN	4	2	I	Inverting input
NC	—	1, 5, 8	—	No connection (can be left floating)
OUT	1	6	O	Output signal
V+	5	7	—	Positive (highest) supply voltage
V-	2	4	—	Negative (lowest) supply voltage

**OPA2187: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View**



Pin Functions: OPA2187

PIN		I/O	DESCRIPTION
NAME	D and DGK		
+IN A	3	I	Non-inverting input, channel A
-IN A	2	I	Inverting input, channel A
+IN B	5	I	Non-inverting input, channel B
-IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) supply voltage
V-	4	—	Negative (lowest) supply voltage

**OPA4187: D and PW Packages
14-pin SOIC and 14-Pin TSSOP
Top View**

**OPA4187: RUM Package (Preview)
16-pin WQFN
Top View**

Pin Functions: OPA4187

PIN			I/O	DESCRIPTION
NAME	D and PW	RUM		
+IN A	3	2	I	Non-inverting input, channel A
-IN A	2	1	I	Inverting input, channel A
+IN B	5	4	I	Non-inverting input, channel B
-IN B	6	5	I	Inverting input, channel B
+IN C	10	9	I	Non-inverting input, channel C
-IN C	9	8	I	Inverting input, channel C
+IN D	12	11	I	Non-inverting input, channel D
-IN D	13	12	I	Inverting input, channel D
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
V+	4	3	—	Positive (highest) supply voltage
V-	11	10	—	Negative (lowest) supply voltage
NC	—	13, 16	—	No internal connection (can be left floating)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V^+) - (V^-)$		40	V
	Signal input pin ⁽²⁾	$(V^-) - 0.5$	$(V^+) + 0.5$	
	Signal output pin ⁽³⁾	$(V^-) - 0.5$	$(V^+) + 0.5$	
Current	Signal input pin ⁽²⁾	–10	10	mA
	Signal output pin ⁽³⁾	–55	55	mA
	Output short-circuit ⁽⁴⁾	Continuous	Continuous	Continuous
Temperature	Operating range, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to ± 10 mA or less.
- (3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5 V beyond the supply rails should be current limited to ± 55 mA or less.
- (4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$(V^+) - (V^-)$	Supply voltage	4.5 (± 2.25)		36 (± 18)	V
T_A	Operating temperature	–40		150	°C

6.4 Thermal Information: OPA187

THERMAL METRIC ⁽¹⁾		OPA187			UNIT
		5 PINS	8 PINS		
		DBV (SOT-23)	DGK (VSSOP)	D (SOIC)	
R _{θJA}	Junction-to-ambient thermal resistance	273.8	159	100.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	126.8	37	42.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.9	49	41.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.9	1.2	4.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	84.9	77.1	40.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: OPA2187

THERMAL METRIC ⁽¹⁾		OPA2187		UNIT
		8 PINS		
		DGK (VSSOP)	D (SOIC)	
R _{θJA}	Junction-to-ambient thermal resistance	159	100.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	37	42.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	49	41.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.2	4.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	77.1	40.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: OPA4187

THERMAL METRIC ⁽¹⁾		OPA4187			UNIT
		14 PINS		16 PINS	
		PW (TSSOP)	D (SOIC)	RUM (WQFN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	83.8	35.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	70.7	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	59.5	12.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	11.6	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.6	37.7	12.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics: High-Voltage Operation

at $T_A = +25^\circ\text{C}$, $V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$ ($V_S = +8\text{ V}$ to $+36\text{ V}$), $R_L = 10\text{ k}\Omega$ connected to $V_S / 2^{(1)}$, and $V_{CM} = V_{OUT} = V_S / 2^{(1)}$ (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±1	±10		μV
			T _A = −40°C to +125°C	±0.001	±0.015		μV/°C
PSRR	Power-supply rejection ratio		V _S = 4.5 V to 36 V, T _A = −40°C to +125°C	±0.01	±1		μV/V
INPUT BIAS CURRENT							
I _B	Input bias current		V _{CM} = V _S / 2	±100	±350		pA
			T _A = −40°C to +125°C			±7.5	
I _{OS}	Input offset current			±100	±500		pA
			T _A = −40°C to +125°C			±14.5	
NOISE							
e _n	Input voltage noise		f = 0.1 Hz to 10 Hz	0.4			μV _{pp}
			f = 0.1 Hz to 10 Hz	60			nV _{rms}
	Input voltage noise density		f = 1 kHz	20			nV/√Hz
i _n	Input current noise density		f = 1 kHz	160			fA/√Hz
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range			(V−) − 0.1		(V+) − 2	V
CMRR	Common-mode rejection ratio		(V−) − 0.1 V < V _{CM} < (V+) − 2 V, V _S = ±18 V	126	140		dB
			(V−) < V _{CM} < (V+) − 2 V, V _S = ±18 V, T _A = −40°C to +125°C	130	145		dB
INPUT IMPEDANCE							
Z _{ID}	Differential			100 6			MΩ pF
Z _{IC}	Common-mode			6 4.2			10 ¹² Ω pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain		T _A = −40°C to +125°C, V _S = ±4 V to ±18 V, (V−) + 0.3 V < V _O < (V+) − 0.3 V, R _L = 10 kΩ	132	160		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			550			kHz
SR	Slew rate		V _O = 10-V step, G = +1	0.2			V/μs
t _S	Settling time	0.1%	V _S = ±18 V, G = 1, 10-V step	46			μs
		0.01%	V _S = ±18 V, G = 1, 10-V step	48			μs
t _{OR}	Overload recovery time		V _{IN} × G = V _S	8			μs
THD+N	Total harmonic distortion + noise		1 kHz, G = +1, V _{OUT} = 3.5 V _{RMS} , No Load	0.035%			
OUTPUT							
	Voltage output swing from rail		V _S = ±4 V to ±18 V, No Load	5	15	mV	
			V _S = ±4 V to ±18 V, R _L = 10 kΩ	75	100		
			V _S = ±4 V to ±18 V, R _L = 10 kΩ, T _A = −40°C to +125°C	100	125		
I _{SC}	Short-circuit current		V _S = ±18 V, Sinking	−30		mA	
			V _S = ±18 V, Sourcing	+30		mA	
R _O	Open-loop output resistance		f = 550 kHz, I _O = 0, See Figure 21	1.4		kΩ	
C _{LOAD}	Capacitive load drive			See Typical Characteristics			
POWER SUPPLY							
I _Q	Quiescent current (per amplifier)		V _S = ±4 V to V _S = ±18 V	100	145	μA	
			I _O = 0 mA, T _A = −40°C to +125°C		150	μA	

(1) $V_S / 2 = \text{midsupply}$.

6.8 Electrical Characteristics: Low-Voltage Operation

at $T_A = +25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $< \pm 4\text{ V}$ ($V_S = +4.5\text{ V}$ to $< +8\text{ V}$), $R_L = 10\text{ k}\Omega$ connected to $V_S / 2^{(1)}$, and $V_{CM} = V_{OUT} = V_S / 2^{(1)}$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage			±1	±15	μV
		T _A = −40°C to +125°C		±0.001	±0.015	μV/°C
PSRR	Power-supply rejection ratio	V _S = 4.5 V to 36 V, T _A = −40°C to +125°C		±0.01	±1	μV/V
INPUT BIAS CURRENT						
I _B	Input bias current	V _{CM} = V _S / 2		±100	±350	pA
		T _A = −40°C to +125°C			±5	nA
I _{OS}	Input offset current			±100	±500	pA
		T _A = −40°C to +125°C			±5	nA
NOISE						
e _n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.4		μV _{PP}
		f = 0.1 Hz to 10 Hz		60		nV _{rms}
	Input voltage noise density	f = 1 kHz		20		nV/√Hz
i _n	Input current noise density	f = 1 kHz		160		fA/√Hz
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range		(V [−]) − 0.1		(V ⁺) − 2	V
CMRR	Common-mode rejection ratio	(V [−]) − 0.1 V < V _{CM} < (V ⁺) − 2 V, V _S = ±2.25 V	114	130		dB
		(V [−]) < V _{CM} < (V ⁺) − 2 V, V _S = ±2.25 V, T _A = −40°C to +125°C	120	137		dB
INPUT IMPEDANCE						
Z _{ID}	Differential			100 6		MΩ pF
Z _{IC}	Common-mode			6 4.2		10 ¹² Ω pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	T _A = −40°C to +125°C, V _S = ±2.25 V to ±4 V, (V [−]) + 0.3 V < V _O < (V ⁺) − 0.3 V, R _L = 10 kΩ	120	140		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			550		kHz
SR	Slew rate	V _O = 1-V step, G = +1		0.2		V/μs
t _{OR}	Overload recovery time	V _{IN} × G = V _S		8		μs
THD+N	Total harmonic distortion + noise	1 kHz, G = +1, V _{OUT} = 1 V _{rms} , No Load		0.05%		
OUTPUT						
	Voltage output swing from rail	V _S = ±2.25 V to ±4 V, No Load		5	15	mV
		V _S = ±2.25 V to ±4 V, R _L = 10 kΩ		15	25	
		V _S = ±2.25 V to ±4 V, R _L = 10 kΩ, T _A = −40°C to +125°C		15	30	
I _{SC}	Short-circuit current	V _S = ±2.25, Sinking		−20		mA
		V _S = ±2.25, Sourcing		+20		mA
R _O	Open-loop output resistance	f = 550 kHz, I _O = 0, See Figure 21		1.4		kΩ
C _{LOAD}	Capacitive load drive			See Typical Characteristics		
POWER SUPPLY						
I _Q	Quiescent current (per amplifier)	V _S = ±2.25 V to V _S = ±4 V		100	145	μA
		I _O = 0 mA, T _A = −40°C to +125°C			150	μA

(1) $V_S / 2 = \text{midsupply}$.

6.9 Typical Characteristics

表 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4
Offset Voltage vs Power Supply	Figure 5
Open-Loop Gain and Phase vs Frequency	Figure 6
Closed-Loop Gain vs Frequency	Figure 7
I_B vs Common-Mode Voltage	Figure 8
Input Bias Current vs Temperature	Figure 9
Output Voltage Swing vs Output Current	Figure 10
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 11
CMRR vs Temperature	Figure 12
PSRR vs Temperature	Figure 13
0.1-Hz to 10-Hz Noise	Figure 14
Input Voltage Noise Spectral Density vs Frequency	Figure 15
THD+N Ratio vs Frequency	Figure 16
THD+N vs Output Amplitude	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Quiescent Current vs Temperature	Figure 19
Open-Loop Gain vs Temperature	Figure 20
Open-Loop Output Impedance vs Frequency	Figure 21
Small-Signal Overshoot vs Capacitive Load ($G = 1$) (10-mV Output Step)	Figure 22
No Phase Reversal	Figure 23
Positive Overload Recovery	Figure 24
Negative Overload Recovery	Figure 25
Small-Signal Step Response (10 mV)	Figure 26 , Figure 27
Large-Signal Step Response	Figure 28 , Figure 29
Large-Signal Settling Time (10-V Positive Step)	Figure 30
Large-Signal Settling Time (10-V Negative Step)	Figure 31
Short-Circuit Current vs Temperature	Figure 32
Maximum Output Voltage vs Frequency	Figure 33
Crosstalk vs Frequency	Figure 34
EMIRR IN+ vs Frequency	Figure 35

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

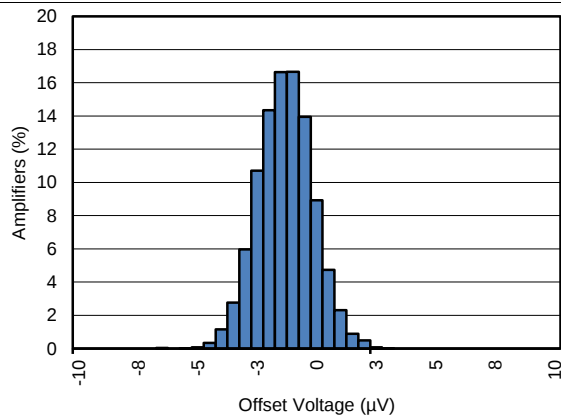


图 1. Offset Voltage Production Distribution

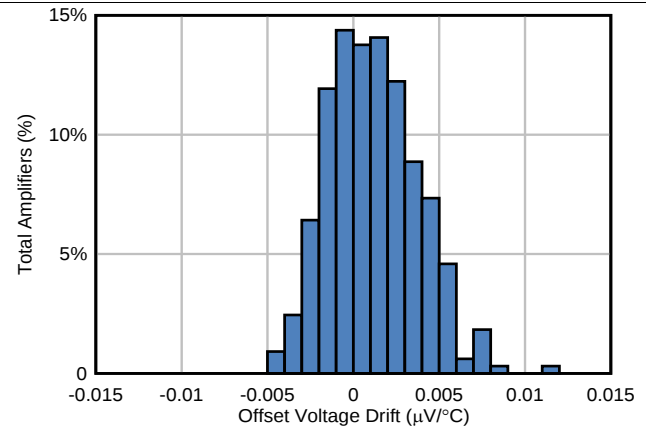


图 2. Offset Voltage Drift Distribution

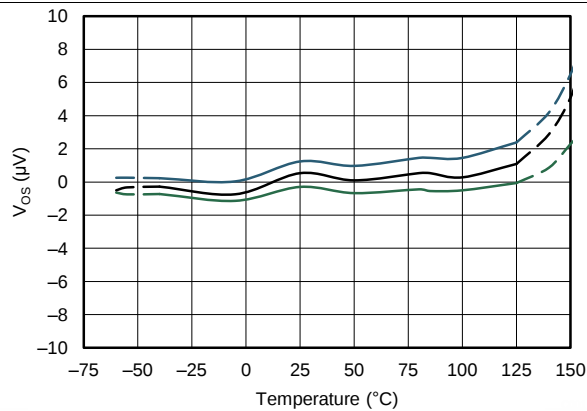


图 3. Offset Voltage vs Temperature

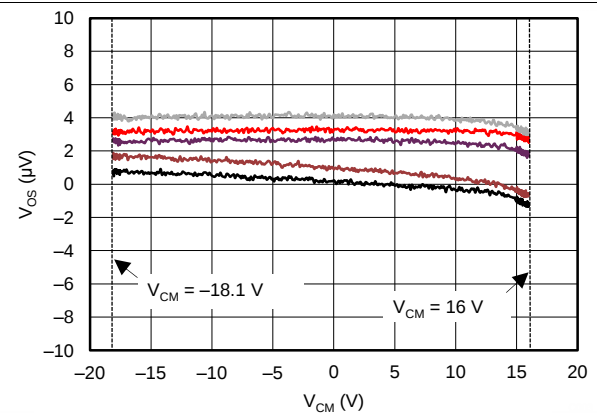


图 4. Offset Voltage vs Common-Mode Voltage

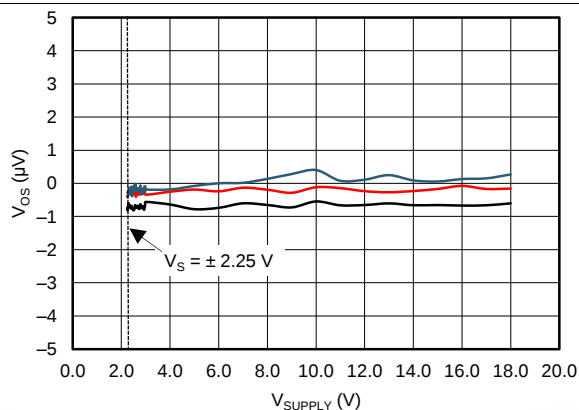


图 5. Offset Voltage vs Power Supply

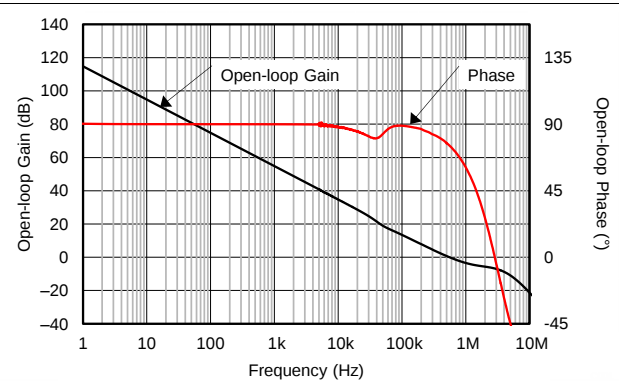


图 6. Open-Loop Gain and Phase vs Frequency

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

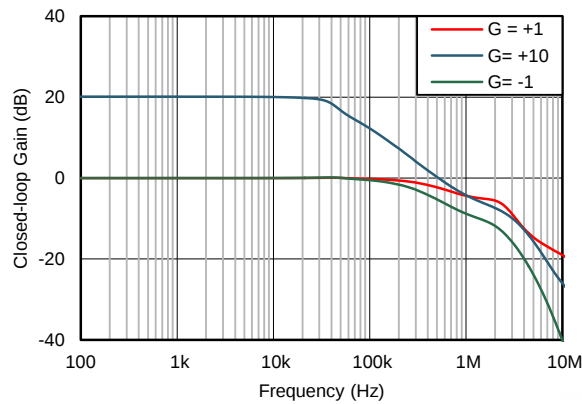


Figure 7. Closed-Loop Gain vs Frequency

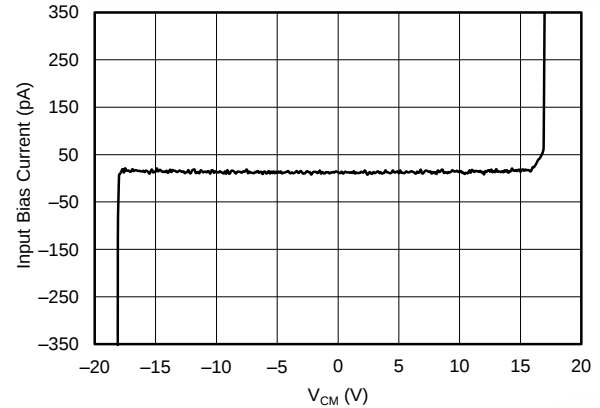


Figure 8. I_B vs Common-Mode Voltage

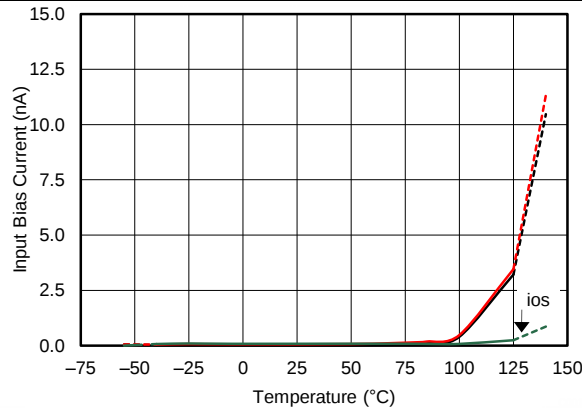


Figure 9. Input Bias Current vs Temperature

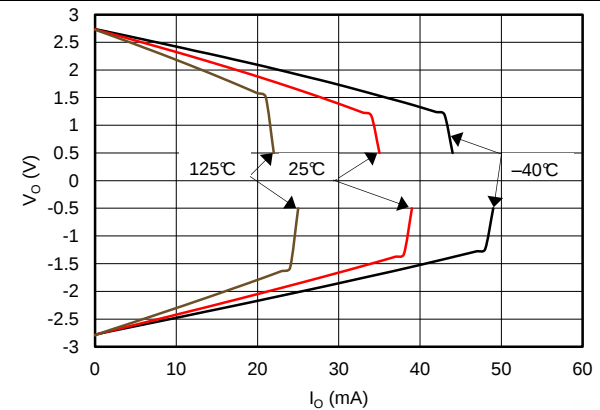


Figure 10. Output Voltage Swing vs Output Current

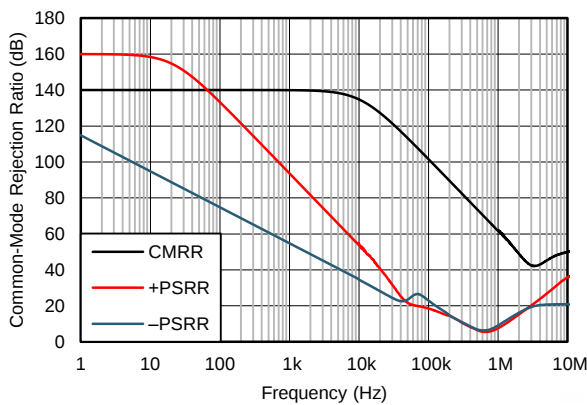


Figure 11. CMRR and PSRR vs Frequency (Referred-to-Input)

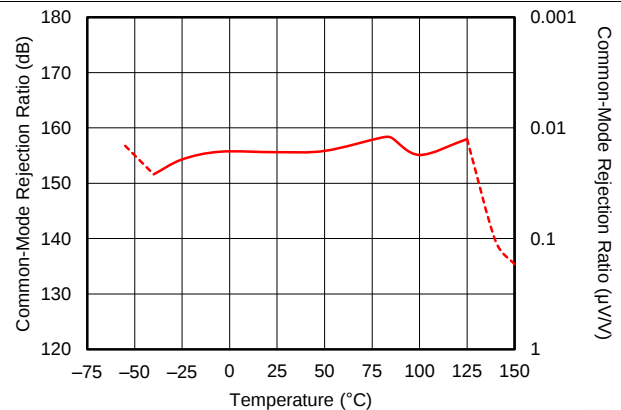


Figure 12. CMRR vs Temperature

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

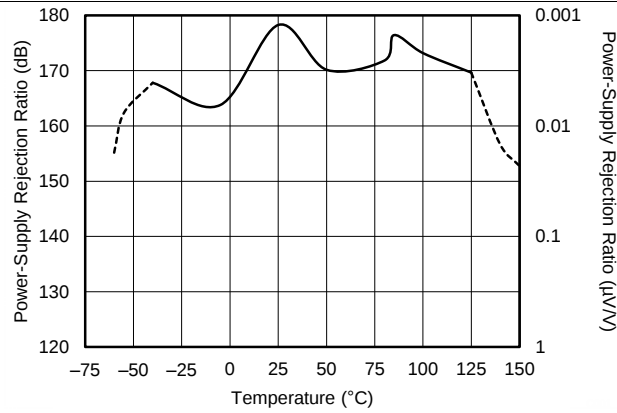


FIG 13. PSRR vs Temperature

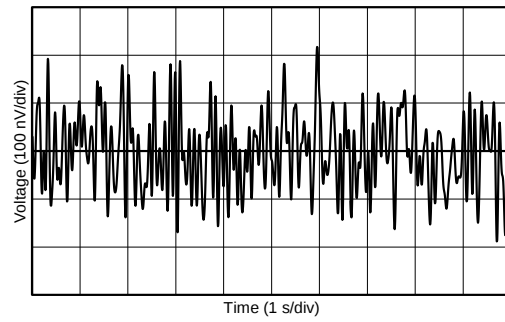


FIG 14. 0.1-Hz to 10-Hz Noise

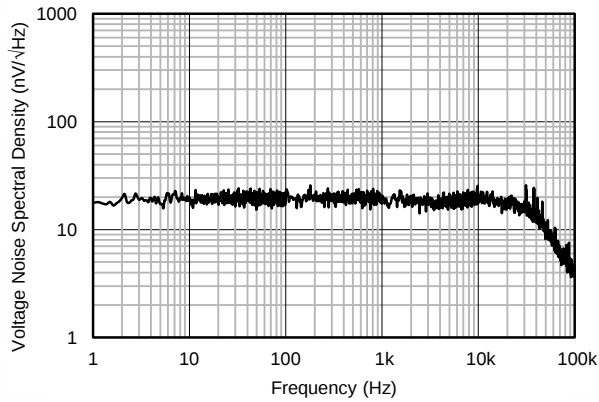


FIG 15. Input-Referred Voltage Noise Spectral Density vs Frequency ($G = +101$)

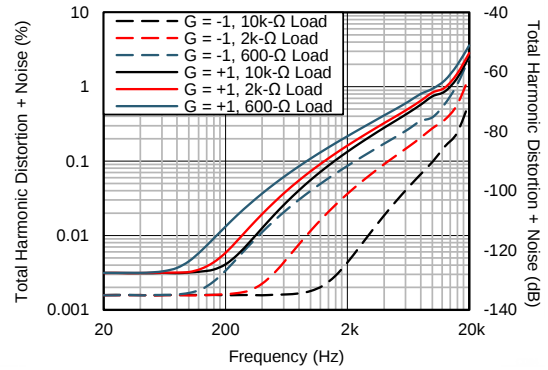


FIG 16. THD+N Ratio vs Frequency

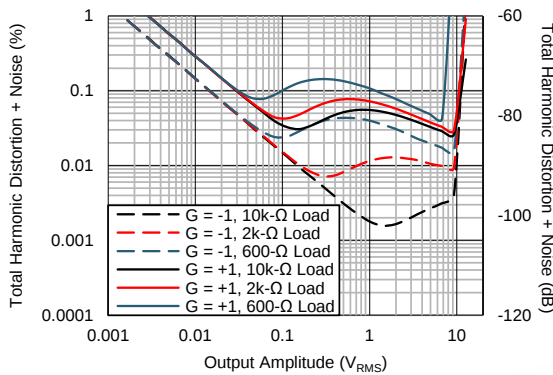


FIG 17. THD+N vs Output Amplitude

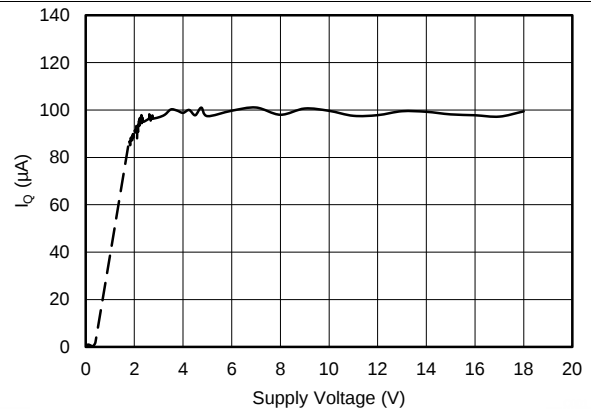


FIG 18. Quiescent Current vs Supply Voltage

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

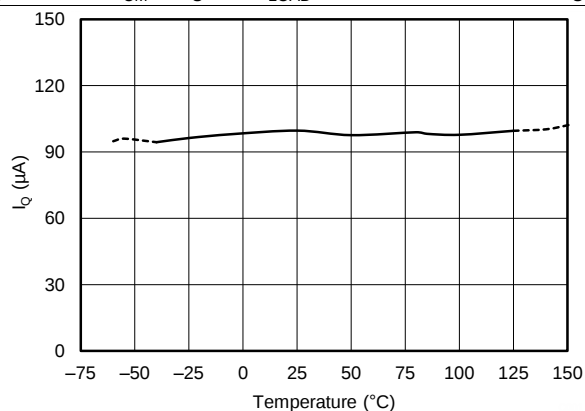


Figure 19. Quiescent Current vs Temperature

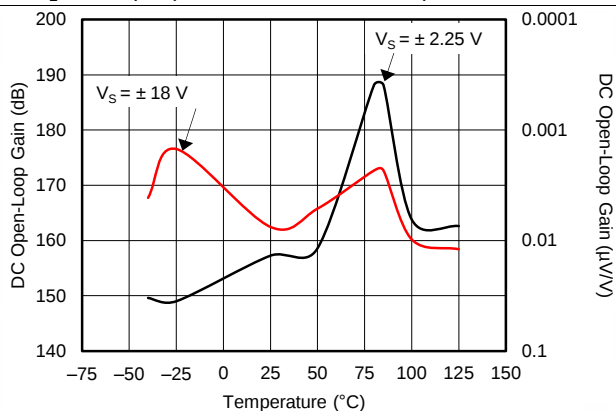


Figure 20. Open-Loop Gain vs Temperature

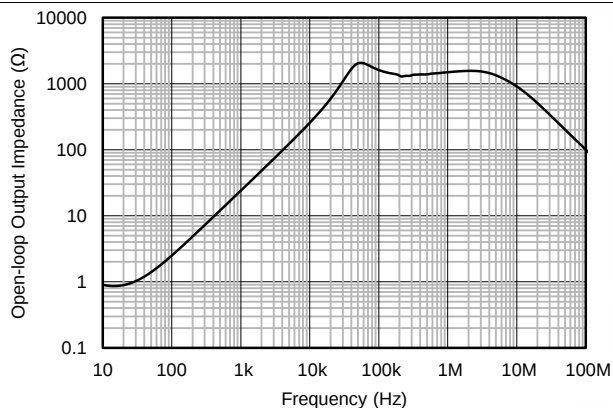


Figure 21. Open-Loop Output Impedance vs Frequency

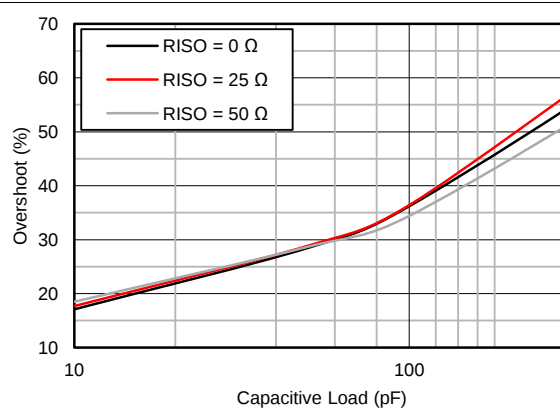


Figure 22. Small-Signal Overshoot vs Capacitive Load ($G = +1$) (10-mV Output Step)

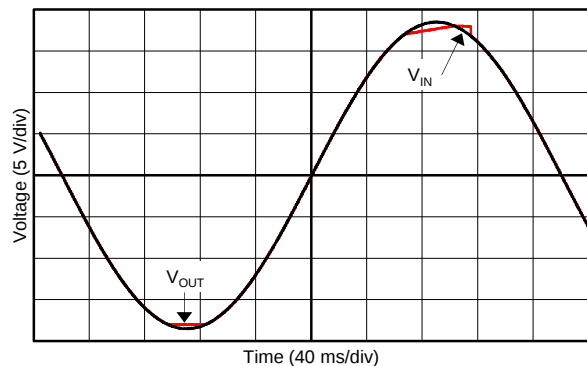


Figure 23. No Phase Reversal

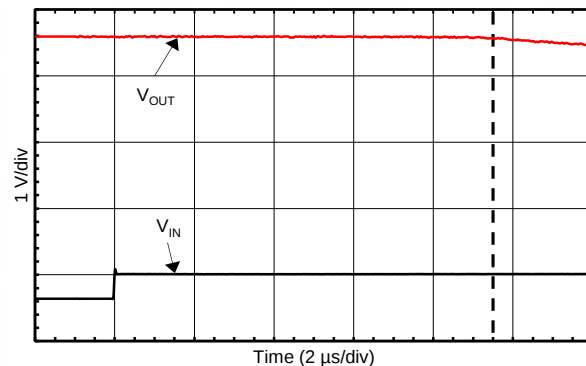


Figure 24. Positive Overload Recovery

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

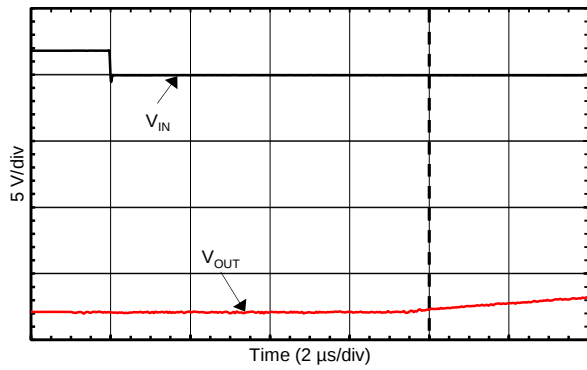


Figure 25. Negative Overload Recovery

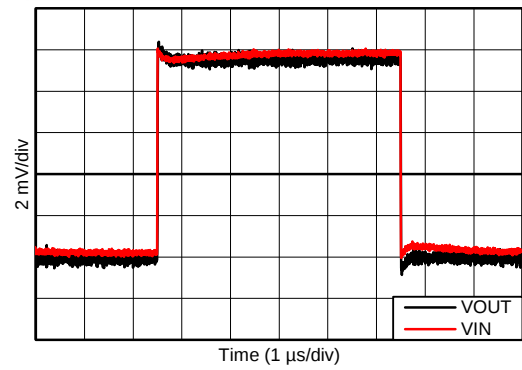


Figure 26. Small-Signal Step Response (100 mV)

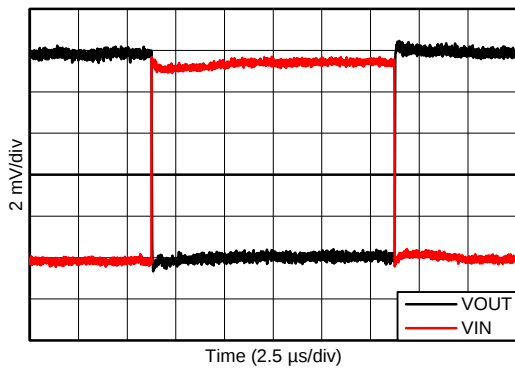


Figure 27. Small-Signal Step Response (100 mV)

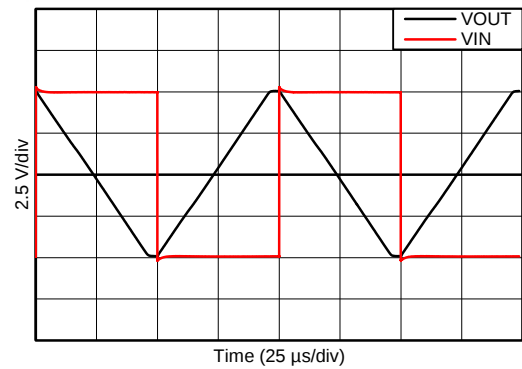


Figure 28. Large-Signal Step Response

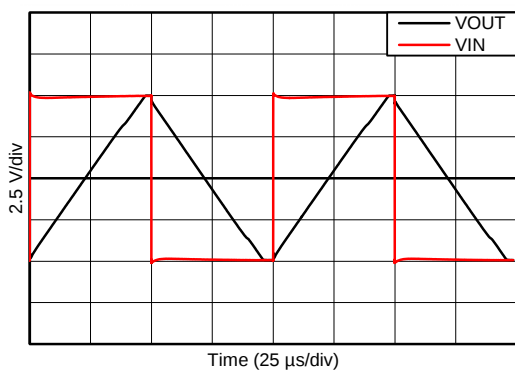


Figure 29. Large-Signal Step Response

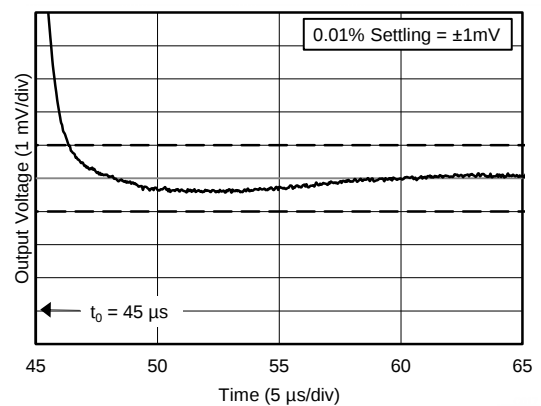


Figure 30. Large-Signal Settling Time (10-V Positive Step)

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

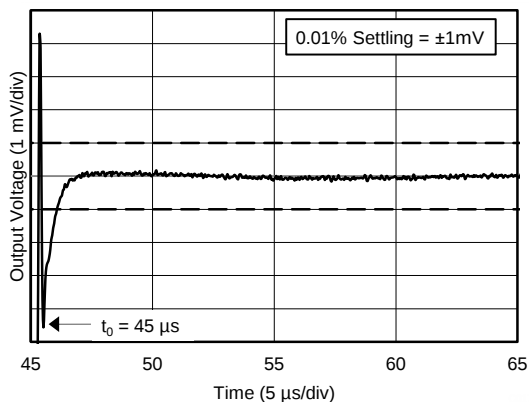


Figure 31. Large-Signal Settling Time (10-V Negative Step)

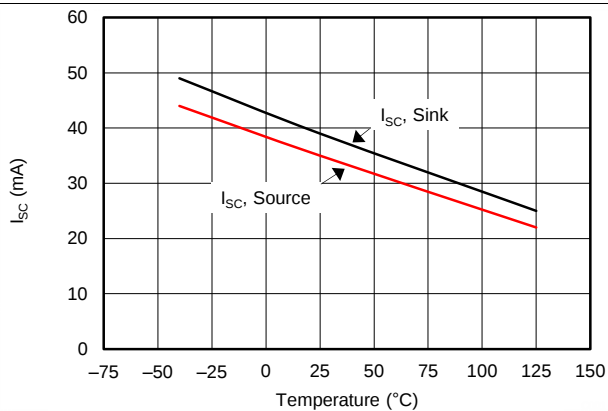


Figure 32. Short-Circuit Current vs Temperature

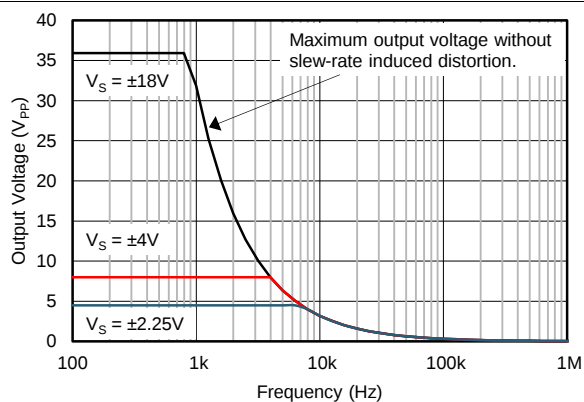


Figure 33. Maximum Output Voltage vs Frequency

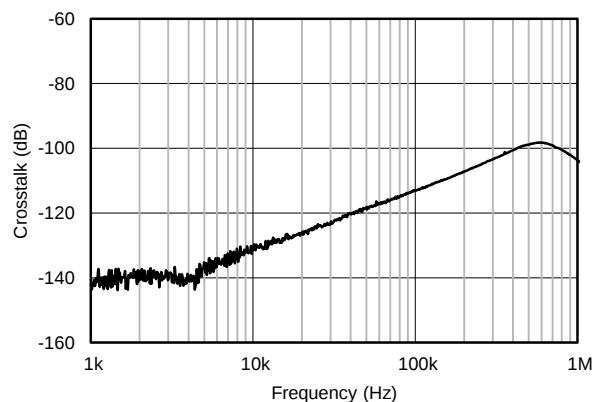


Figure 34. Crosstalk vs Frequency

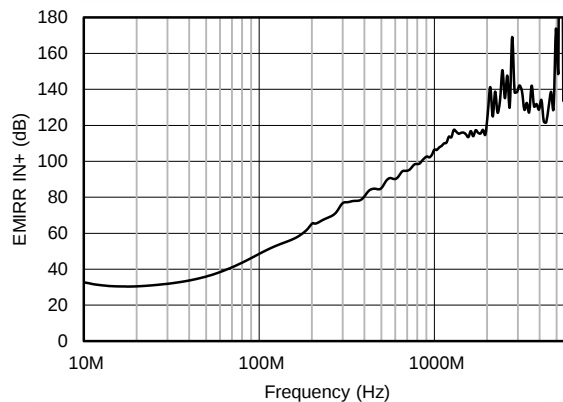


Figure 35. EMIRR IN+ vs Frequency

7.3 Feature Description

The OPAx187 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic autocalibration technique to provide ultra-low input offset voltage and near zero input offset voltage drift over temp and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure they are equal on both input pins. Other layout and design considerations include:

Use low thermoelectric-coefficient conditions (avoid dissimilar metals).

Thermally isolate components from power supplies or other heat sources.

Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 $\mu\text{V}/^\circ\text{C}$ or higher, depending on the materials used.

7.3.1 Operating Characteristics

The OPAx187 device is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V). Many specifications apply from -40°C to $+125^\circ\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

7.3.2 Phase-Reversal Protection

The OPAx187 device has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx187 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. [Figure 37](#) shows this performance.

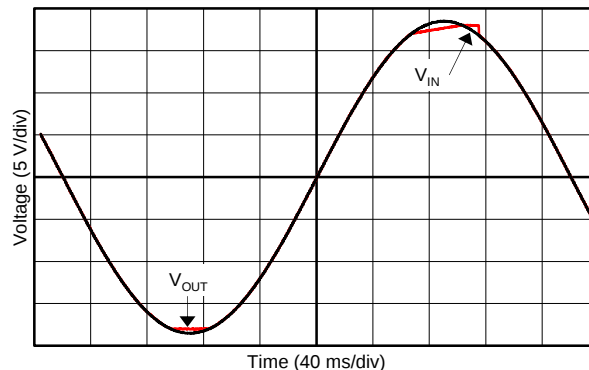


Figure 37. No Phase Reversal

7.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers, such as the OPAx187, use switching on their inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents them from being amplified, however they may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

7.3.4 Internal Offset Correction

The OPAx187 op amp uses an auto-calibration technique with a time-continuous 125-kHz op amp in the signal path. This amplifier is zero-corrected every 22 μs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 μs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Feature Description (continued)

7.3.5 EMI Rejection

The OPAx187 device uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx187 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 38](#) shows the results of this testing on the OPAx187. [Table 2](#) lists the EMIRR IN+ values for the OPAx187 at particular frequencies commonly encountered in real-world applications. Applications listed in [Table 2](#) may be centered on or operated near the particular frequency shown. Detailed information can also be found in [EMI Rejection Ratio of Operational Amplifiers](#), available for download from www.ti.com.

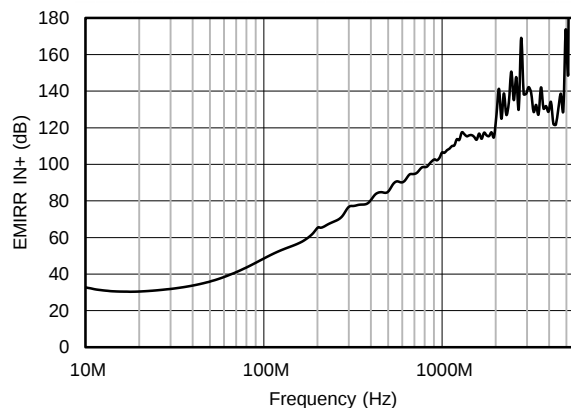


Figure 38. EMIRR Testing

Table 2. OPAx187 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	81.8 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	102.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	115.4 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	150.7 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	142.0 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	173.8 dB

7.3.6 Capacitive Load and Stability

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. [Figure 39](#) illustrates small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, for details of analysis techniques and application circuits, refer to [Feedback Plots Define Op Amp AC Performance](#), available for download from www.ti.com.

$G = 1$, $R_L = 10\text{ k}\Omega$, 10-mV Output Step

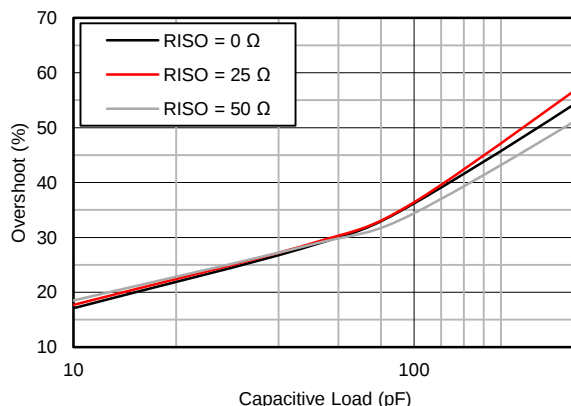


FIG 39. Small-Signal Overshoot Versus Capacitive Load

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See [FIG 40](#) for an illustration of the ESD circuits contained in the OPAX187 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAX187 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

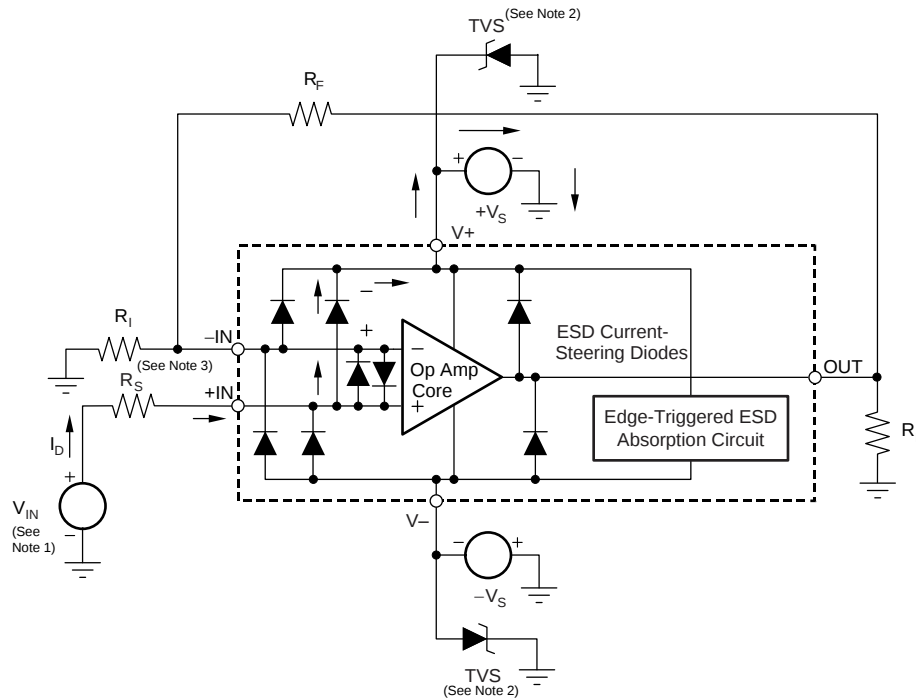
When the operational amplifier connects into a circuit (as shown in [FIG 40](#)), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[FIG 40](#) shows a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $-V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external TVS (Transient Voltage Suppressor) diodes may be added to the supply pins, as shown in [Figure 40](#). The TVS voltage must be selected such that the diode does not turn on during normal operation. However, the TVS voltage should be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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 NOTE 1: $V_{IN} = +V_S + 500 \text{ mV}$.

 NOTE 2: TVS: $+V_{S(max)} > V_{TVSBR(min)} > +V_S$.

 NOTE 3: Suggested value is approximately 1 k Ω .

Figure 40. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPAx187 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in [Figure 40](#). In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx187. [Figure 40](#) shows an example configuration that implements a current-limiting feedback resistor.

7.4 Device Functional Modes

The OPAx187 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (± 2.25 V). The maximum power supply voltage for the OPAx187 is 36 V (± 18 V).

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

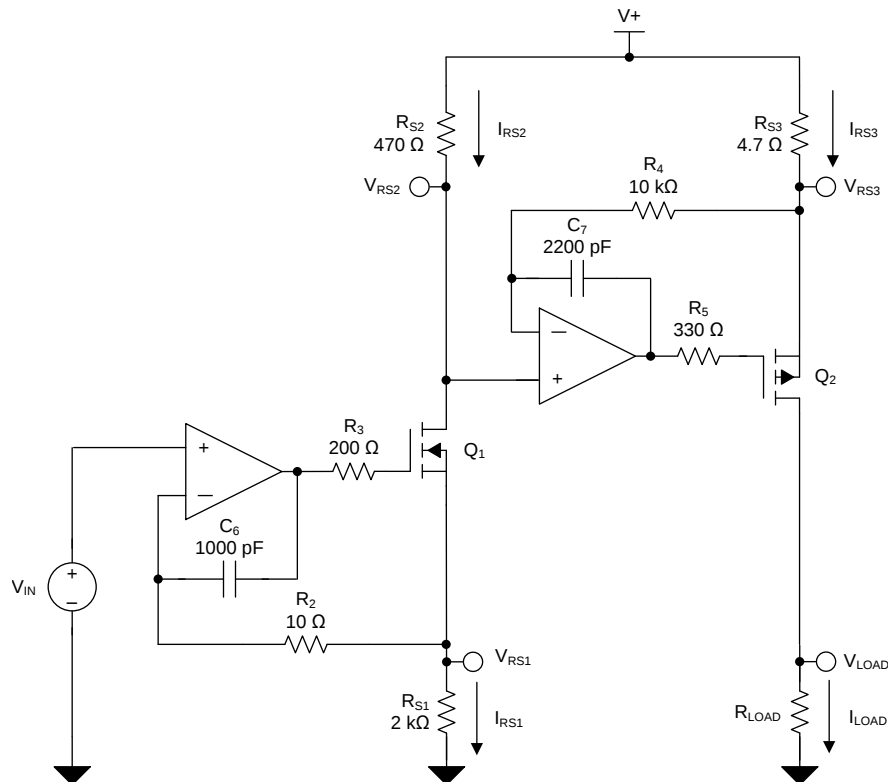
The OPAx187 operational amplifier combines precision offset and drift with excellent overall performance, making it ideal for many precision applications. The precision offset drift of only $0.001 \mu\text{V}/^\circ\text{C}$ provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, $0.1\text{-}\mu\text{F}$ capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx187 can be used.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in [Figure 41](#) is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V into an output current of 0 mA to 100 mA . [Figure 42](#) shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2187 facilitate excellent dc accuracy for the circuit.



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Figure 41. High-Side Voltage-to-Current (V-I) Converter

8.2.1.1 Design Requirements

The design requirements are:

Typical Applications (continued)

- Supply voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN} , and the three current sensing resistors, R_{S1} , R_{S2} , and R_{S3} . The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3} .

This application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPAx187 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier, optimized for wide-voltage, single-supply operation, with an output swing to within 5 mV of the positive rail. The OPAx187 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPAx187 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a [High-Side Voltage-to-Current \(V-I\) Converter](#).



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIPD102, High-Side Voltage-to-Current \(V-I\) Converter](#) (SLAU502).

8.2.1.3 Application Curve

Figure 42 shows the measured transfer function for the high-side voltage-to-current converter shown in Figure 41.

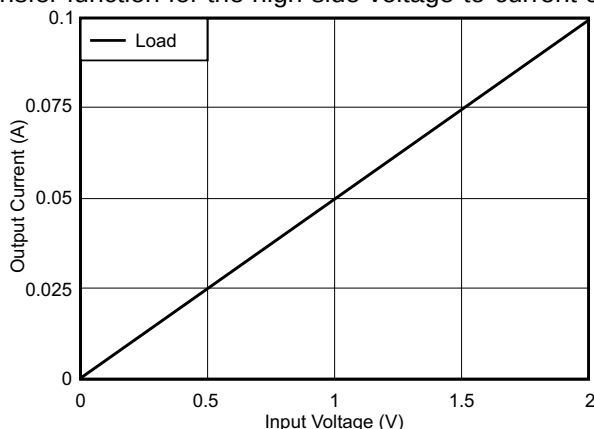


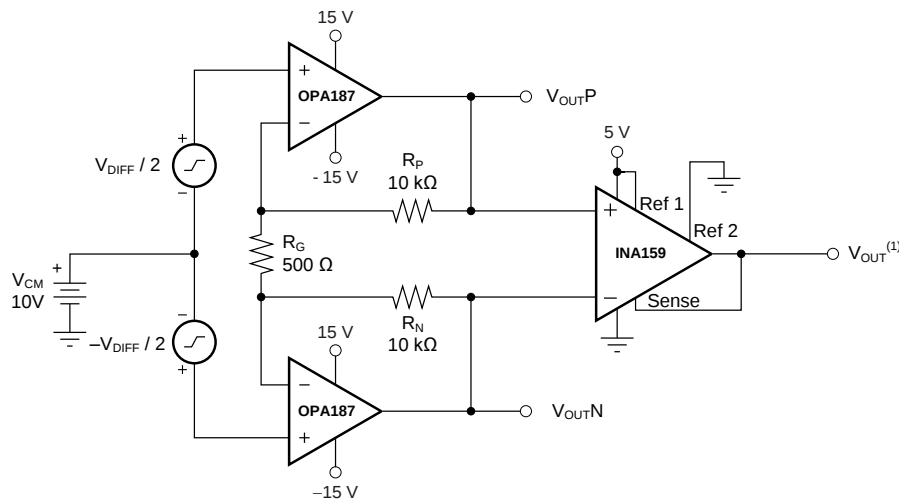
Figure 42. Measured Transfer Function for High-Side V-I Converter

8.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

注

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

Figure 43 shows an example of how the OPAx187 is used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link to download the TINA-TI file: [Discrete INA](#).



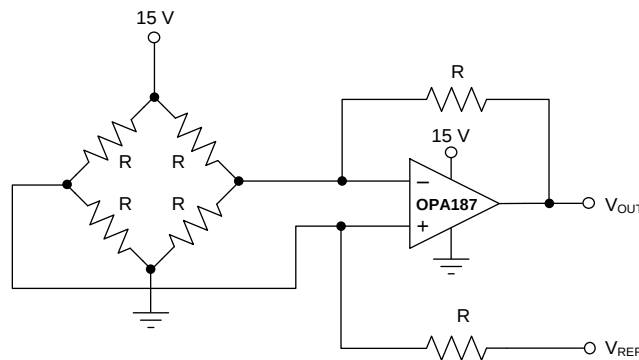
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$$(1) \quad V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref\ 1) / 2.$$

Figure 43. Discrete INA + Attenuation for ADC With 3.3-V Supply

8.2.3 Bridge Amplifier

Figure 44 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: [Bridge Amplifier Circuit](#).



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Figure 44. Bridge Amplifier

8.2.4 Low-Side Current Monitor

Figure 45 shows the OPAx187 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPAx187, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: [Current-Sensing Circuit](#).

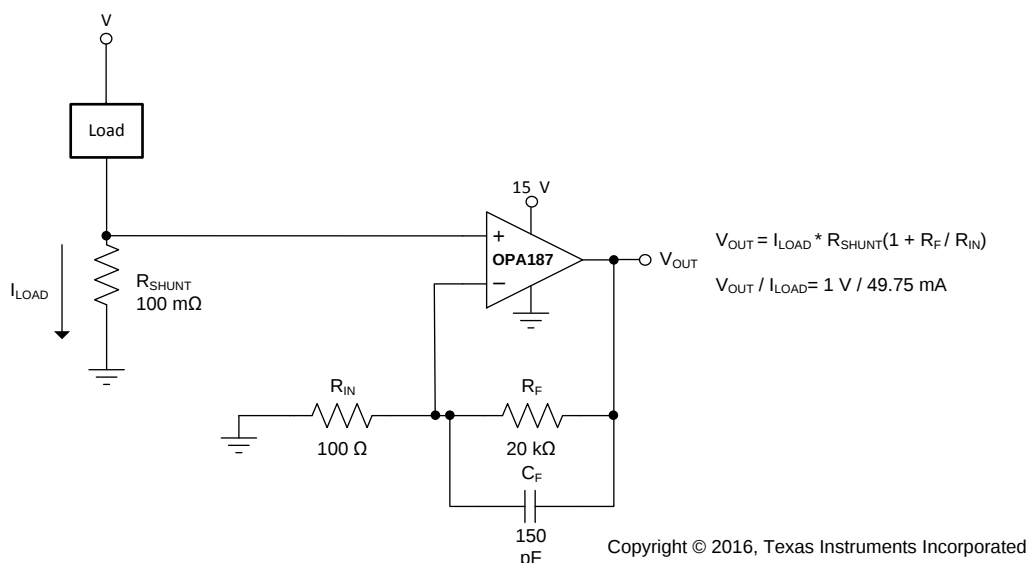
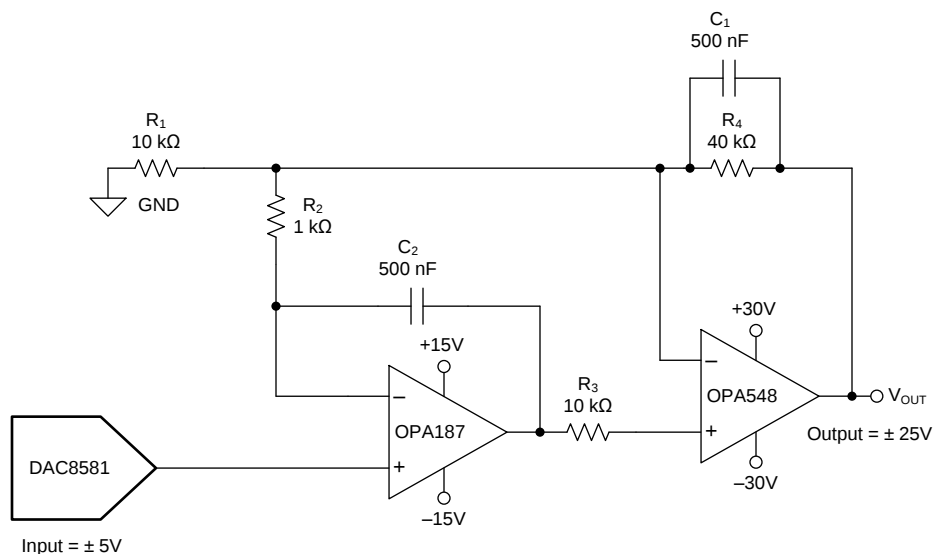


FIG 45. Low-Side Current Monitor

8.2.5 Programmable Power Supply

FIG 46 shows the OPAx187 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPAx187 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: [Programmable Power-Supply Circuit](#).

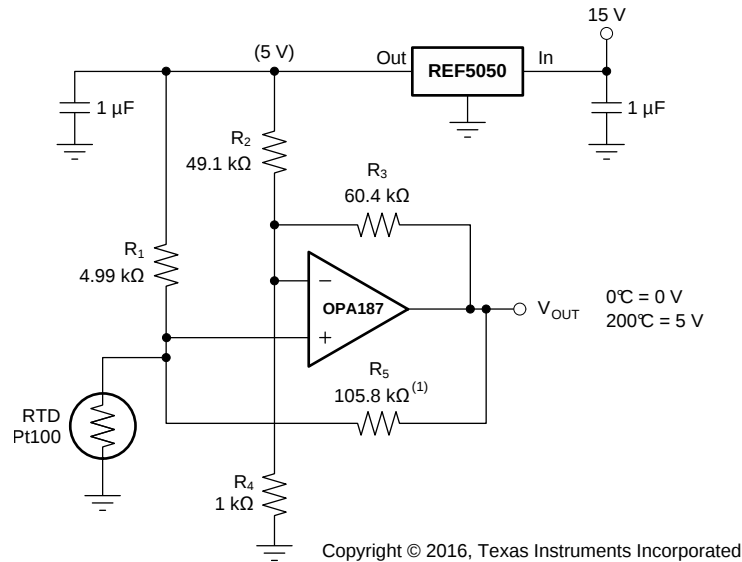


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FIG 46. Programmable Power Supply

8.2.6 RTD Amplifier With Linearization

See [Analog Linearization Of Resistance Temperature Detectors](#), for an in-depth analysis of [Figure 47](#). Click the following link to download the TINA-TI file: [RTD Amplifier With Linearization](#).



(1) R_5 provides positive-varying excitation to linearize output.

Figure 47. RTD Amplifier With Linearization

9 Power Supply Recommendations

The OPAx187 is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V); many specifications apply from -40°C to $+125^\circ\text{C}$. The [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 40 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

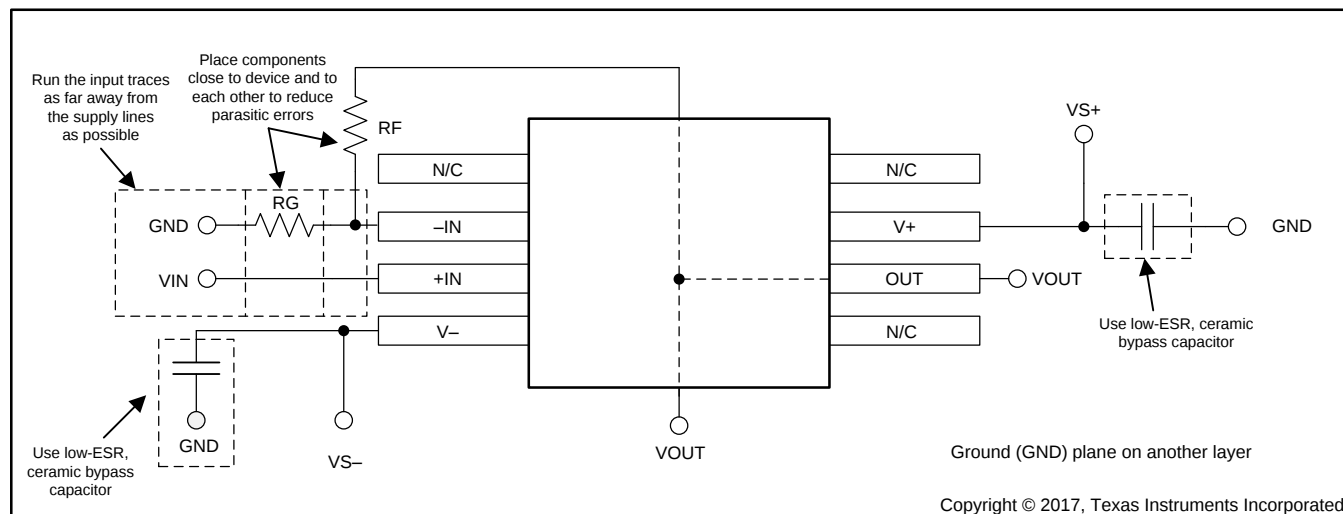
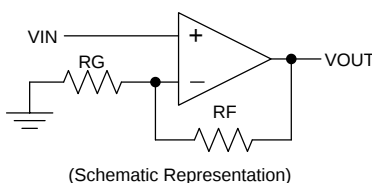
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Low-ESR, 0.1- μF ceramic bypass capacitors must be connected between each supply pin and ground; place the capacitors as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



✎ 48. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方の広範なモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.2 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designs は、<http://www.ti.com/ww/en/analog/precision-designs/> からオンラインで入手できます。

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH Design CenterからWebベースのツールとして利用でき、完全な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『オペアンプのゲイン安定性、第3部: ACゲイン誤差の解析』
- テキサス・インスツルメンツ、『オペアンプのゲイン安定性、第2部: DCゲイン誤差の解析』
- テキサス・インスツルメンツ、『完全差動アクティブ・フィルタにおける無限ゲイン、MFBフィルタ・トポロジの使用』
- テキサス・インスツルメンツ、『オペアンプの性能分析』
- テキサス・インスツルメンツ、『オペアンプの単一電源動作』
- テキサス・インスツルメンツ、『アンプのチューニング』
- テキサス・インスツルメンツ、『鉛フリー仕上げ部品の保管寿命評価』

11.3 関連リンク

表 3 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルと購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA187	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2187	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4187	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.6 商標

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11.7 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	Samples
OPA187IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	Samples
OPA187IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	Samples
OPA187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	1D96	Samples
OPA187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	1D96	Samples
OPA187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	Samples
OPA2187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	Samples
OPA2187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	Samples
OPA2187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	Samples
OPA2187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	Samples
OPA4187ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IRUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	Samples
OPA4187IRUMT	ACTIVE	WQFN	RUM	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA187IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4187IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4187IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4187IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA4187IRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA187IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA187IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA187IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA187IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA187IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2187IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2187IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2187IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4187IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4187IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4187IRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
OPA4187IRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4187ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4187IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

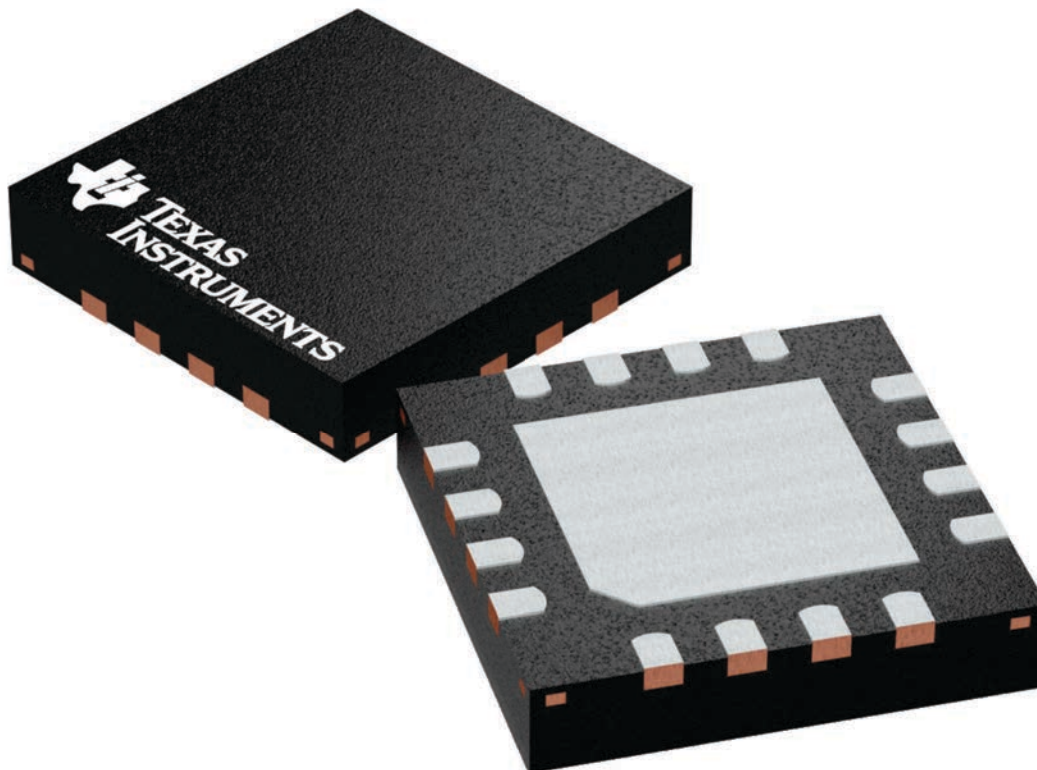
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

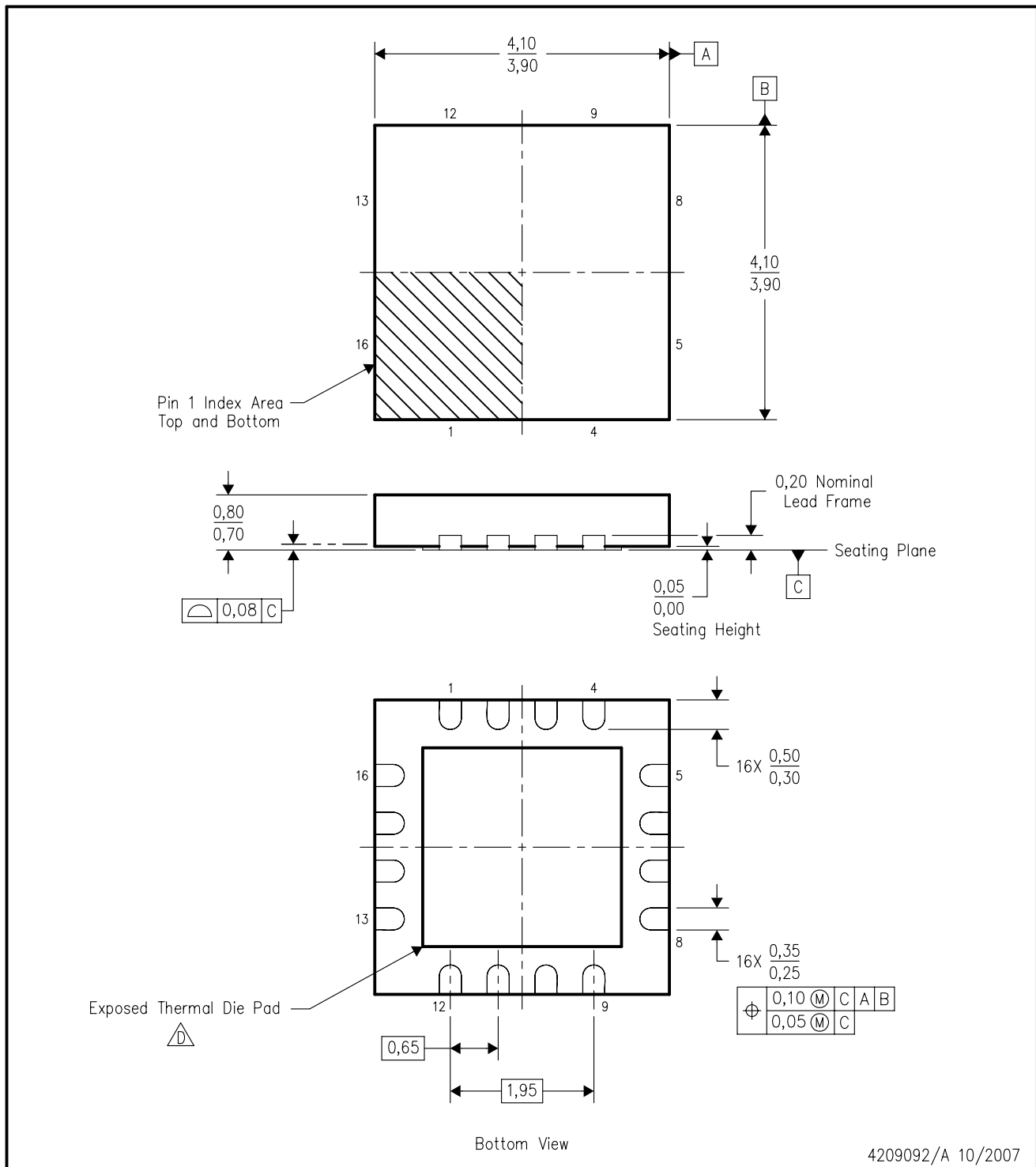
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4209092/A 10/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-220 variation WGGC-3.

RUM (S-PWQFN-N16)

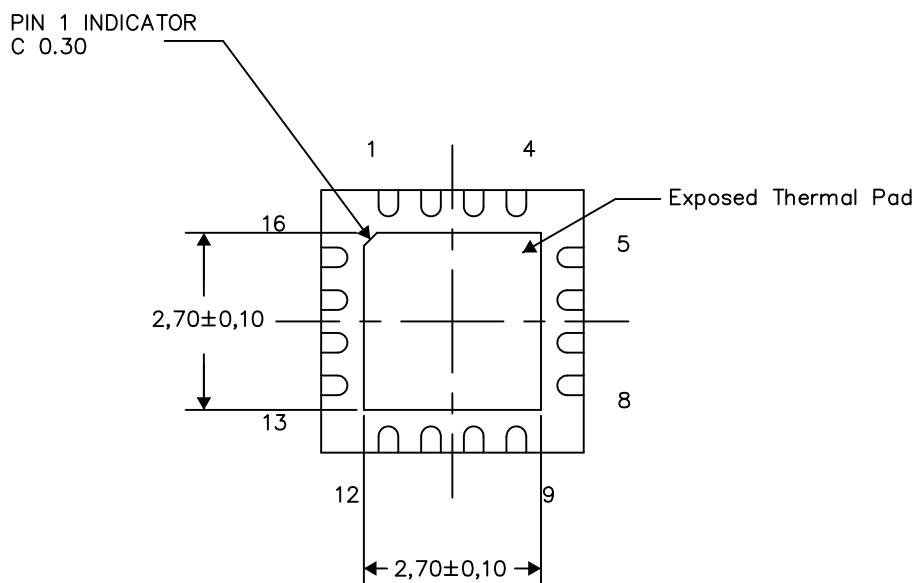
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

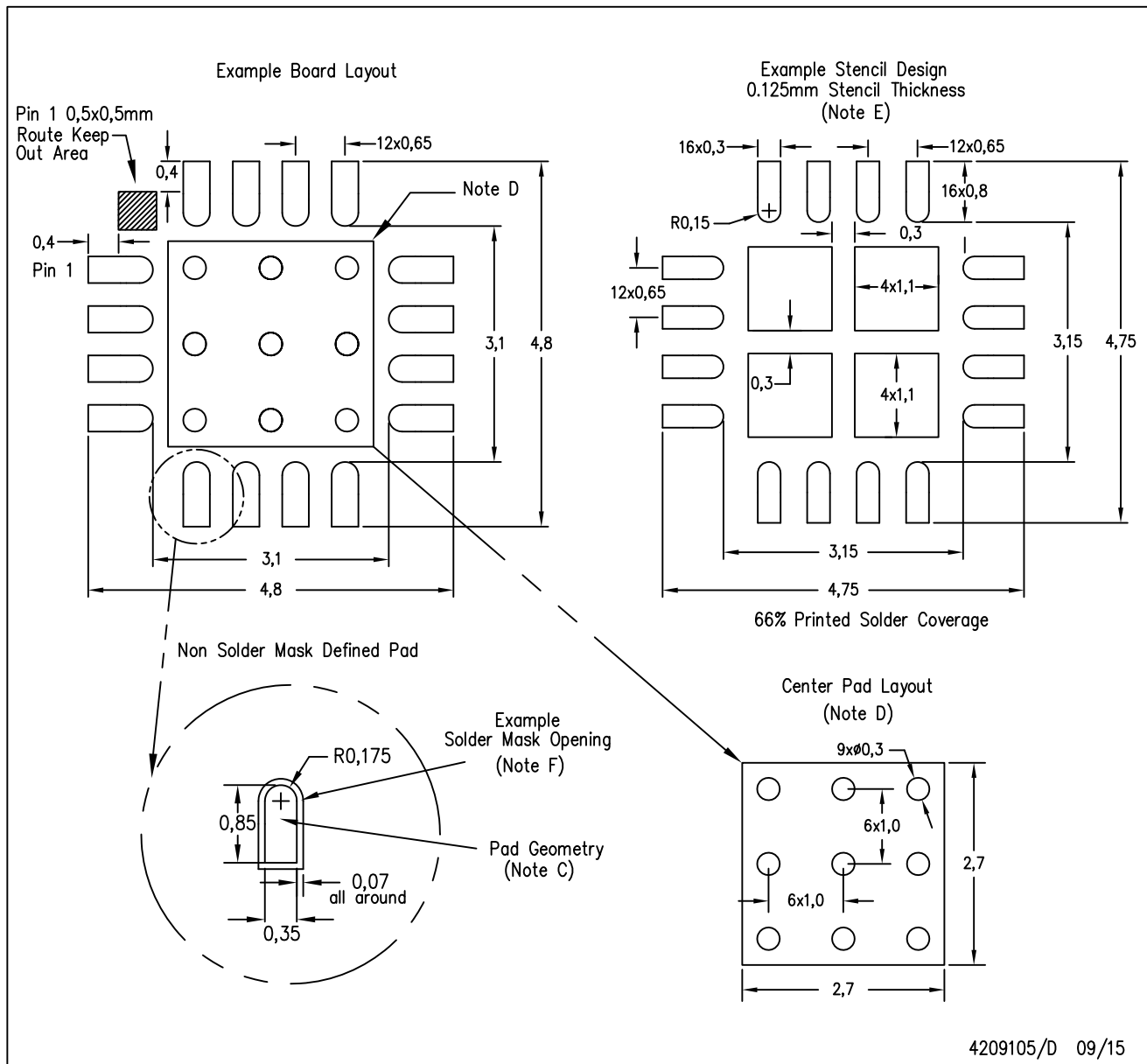
Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4209105/D 09/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.



SOT-23 - 1.45 mm max height

PIN 1 INDEX AREA

1.75
1.45

3.0
2.6

1.9

2X 0.95

1.9

3.05
2.75

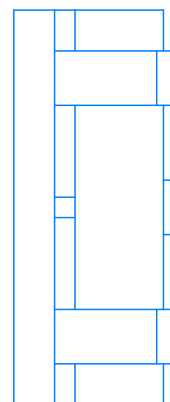
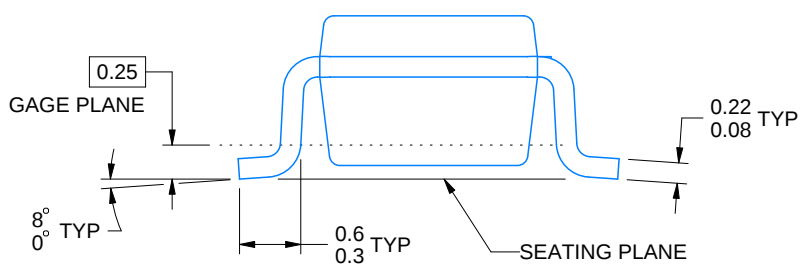
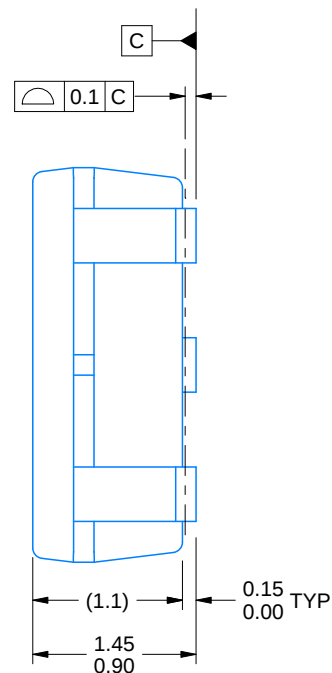
0.1

0.15

NOTE 5

5X 0.5
0.3

⊕ 0.2 M C A B



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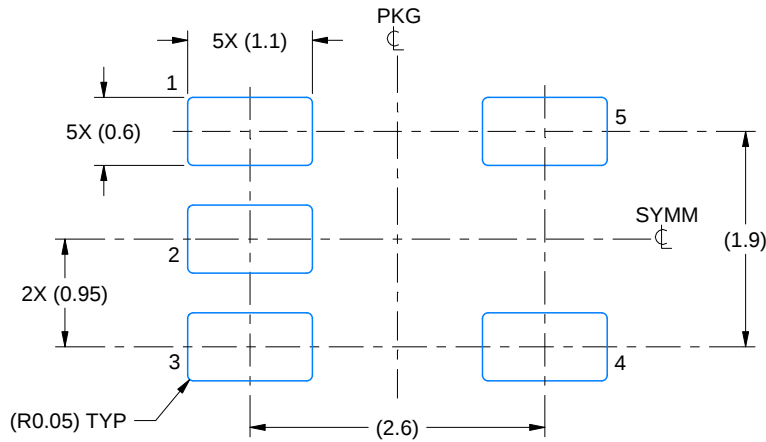
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

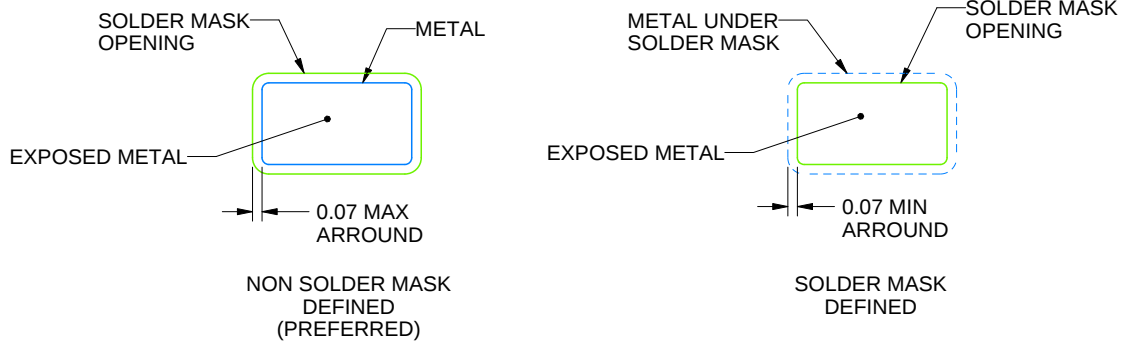
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

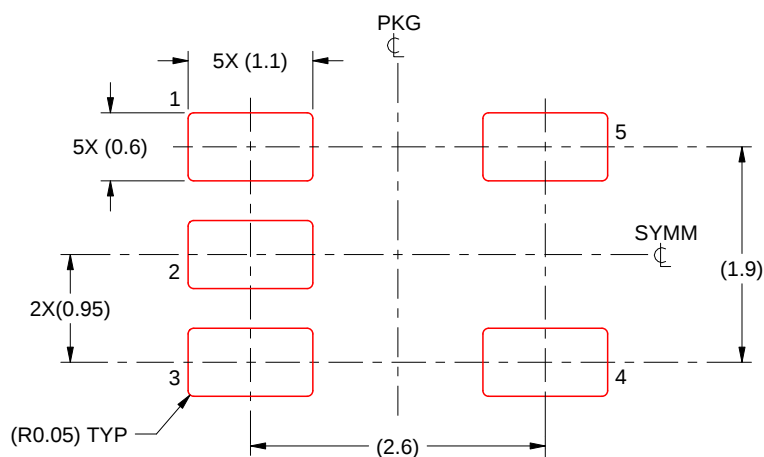
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

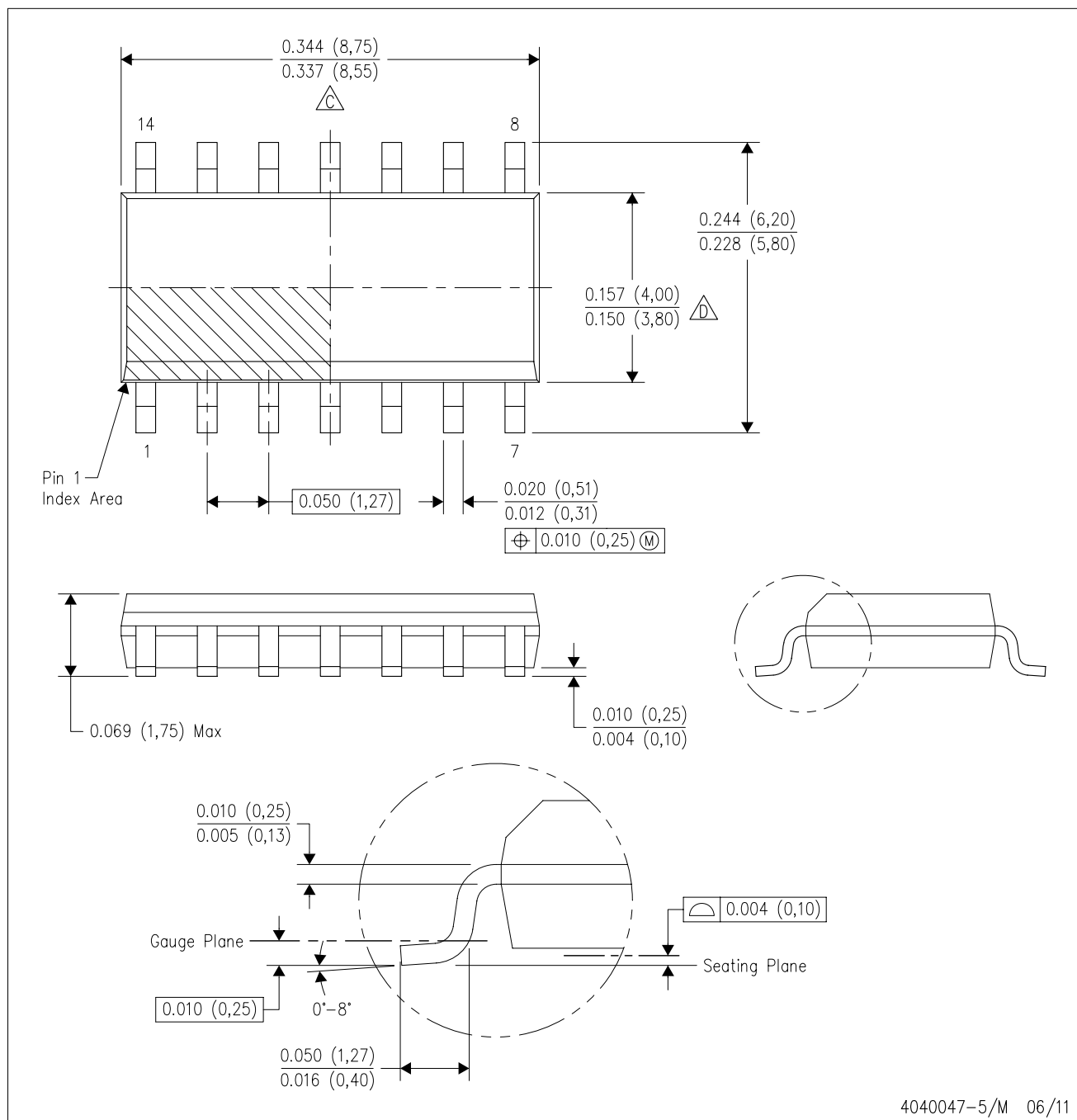
4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

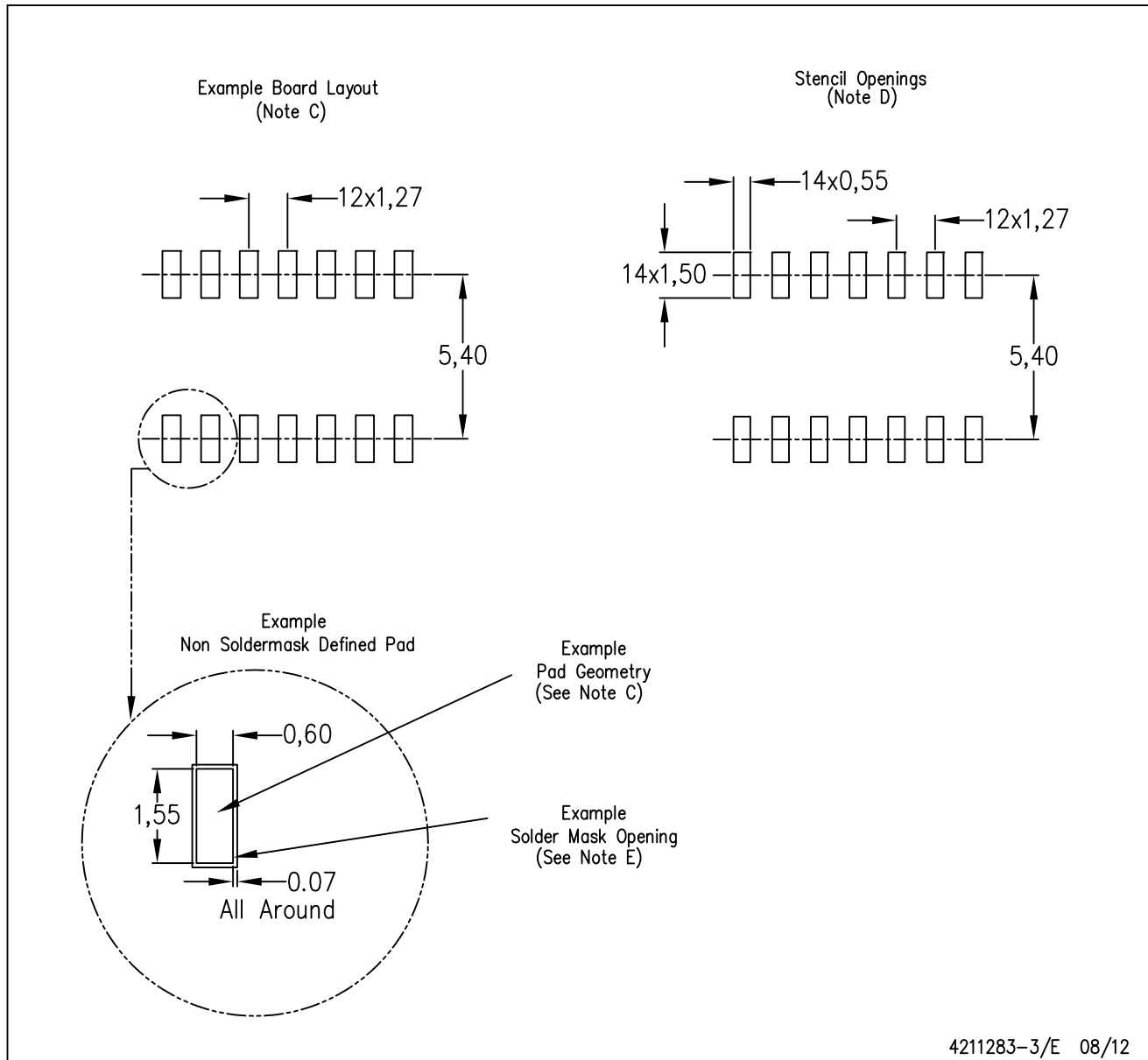


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

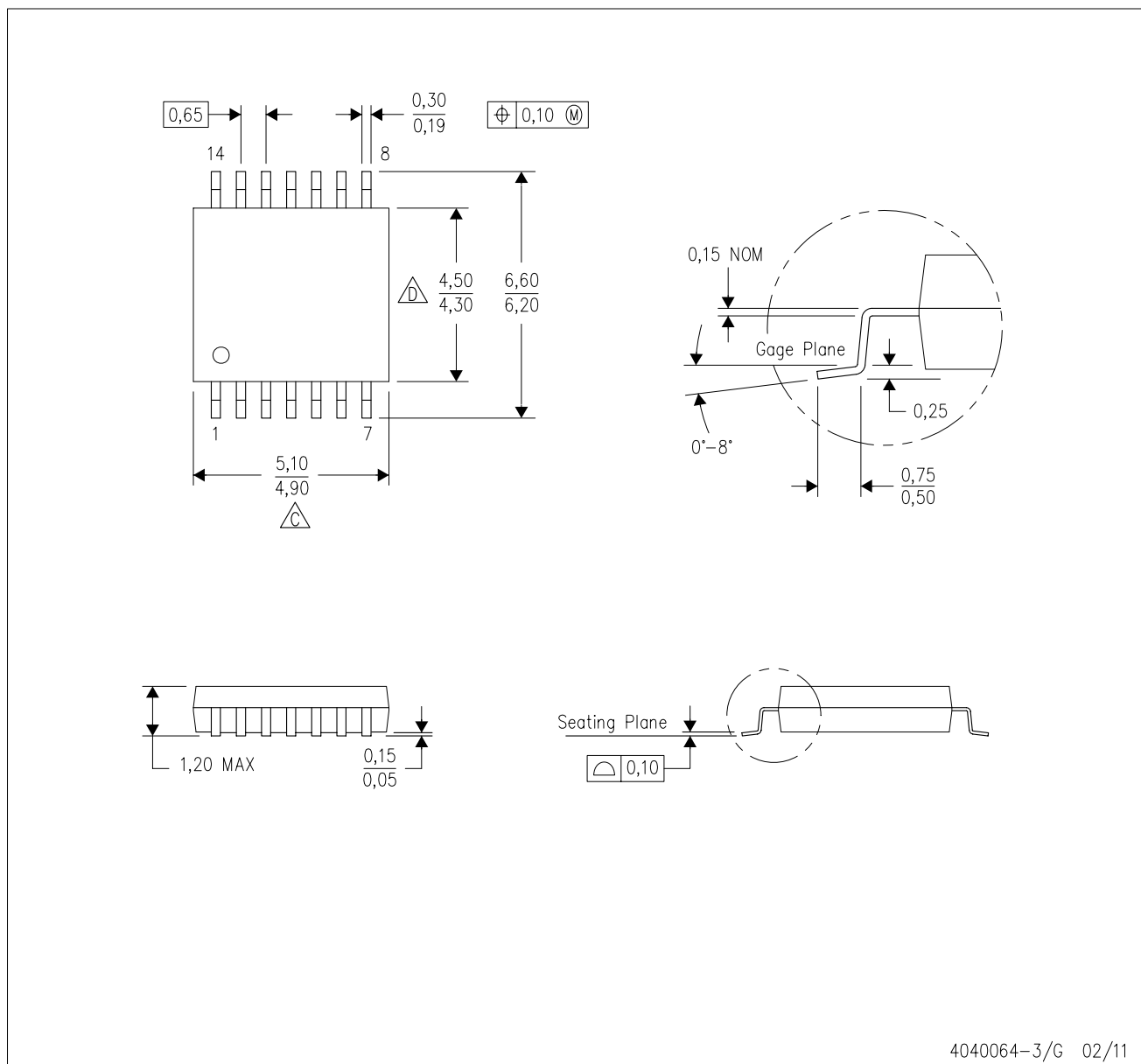
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

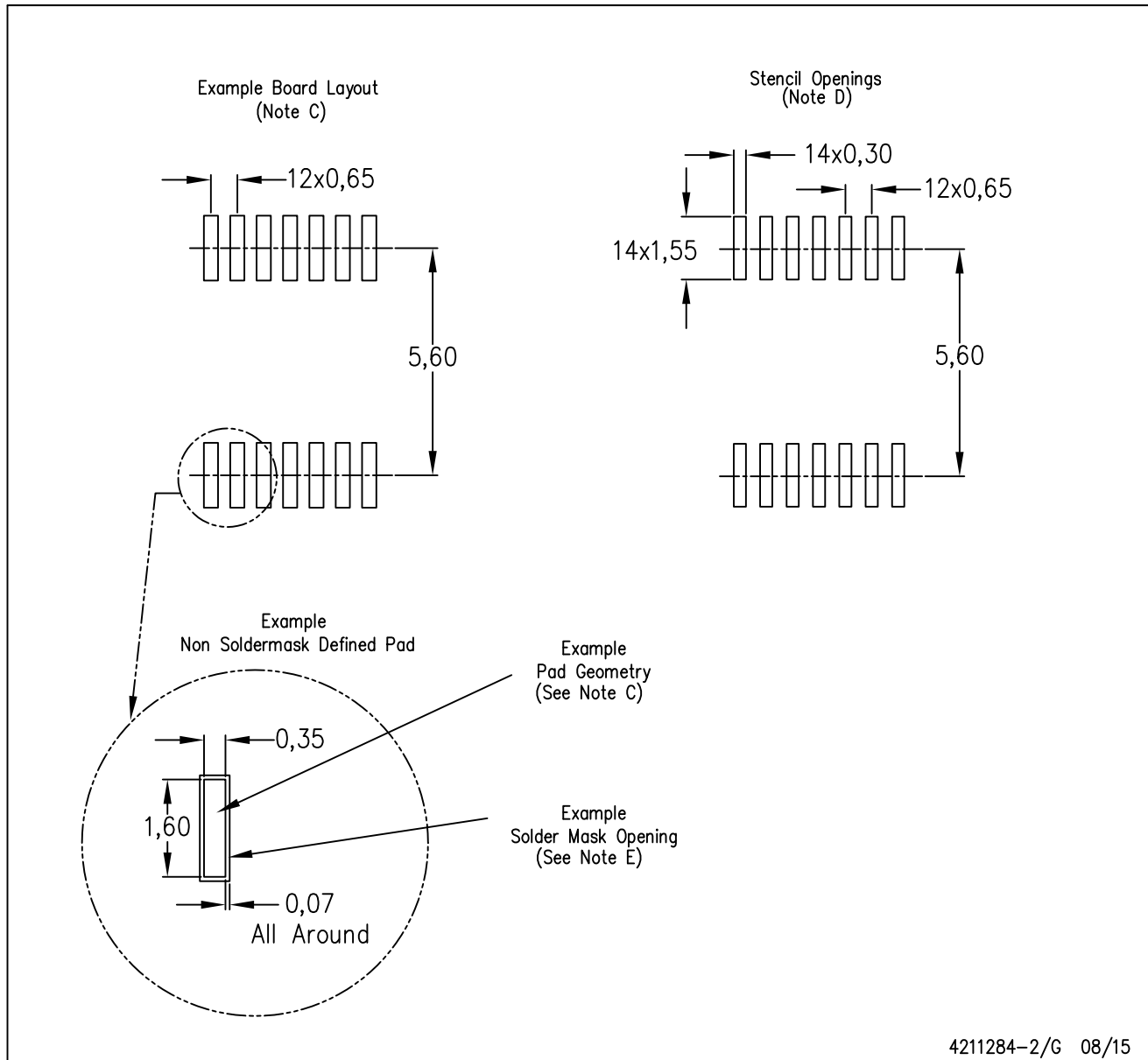
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

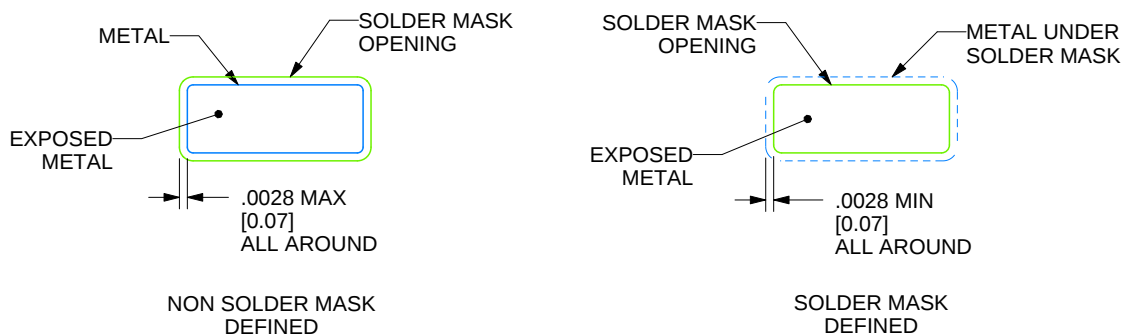
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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