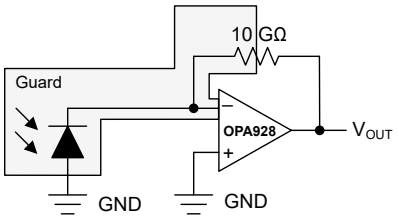
OPA928 16V 対応、フェムトアンペア入力バイアス、高精度、レール・ツー・レール I/O、e-trim™ オペアンプ

1 特長

- 超低入力バイアス電流:
  - 25℃と 85℃で 20fA (最大テスト値)
- 低ノイズ:
  - 0.1Hz 時に 0.05fA/√Hz
  - 1kHz 時に 15nV/√Hz
- 高い DC 精度:
  - ±5μV の入力オフセット電圧
  - ±0.1μV/℃のオフセット電圧ドリフト
- 広い帯域幅:2.5MHz GBW
- 低い静止電流:275μA
- EMI および RFI フィルタ入力
- 高精度ガード・バッファ
- 広い電源範囲:±2.25V～±8V、+4.5V～16V
- レール・ツー・レール入出力
- 高い容量性負荷駆動能力:1nF
- 動作温度範囲:-40℃～+125℃
- 業界標準のパッケージ:
  - 8 ピン SOIC

2 アプリケーション

- 電気化学メーター - pH メーター
- 実験室およびフィールド用計測機器
- 質量分光器
- イオン・クロマトグラフィー (IC) 装置
- 分光光度計



高ゲイン・トランスインピーダンス・アンプ

3 説明

OPA928 は、新世代の 16V、フェムトアンペア入力バイアスの e-trim™ オペアンプです。このデバイスは、25℃および 85℃で 20fA (最大) という超低入力バイアス電流を提供します。OPA928 の入力バイアス性能は、両方の温度で製造時にテストされています。

このデバイスは、入力バイアスがゼロに近いほか、レール・ツー・レール入出力、低いオフセット電圧 (代表値 ±5μV)、低いオフセット・ドリフト (代表値 ±0.1μV/℃)、低い電流ノイズ (0.1Hz で 0.05fA/√Hz) など、優れた DC 精度と AC 性能を備えています。これらの特長から、OPA928 は低光フォトダイオードおよび高ソース・インピーダンスのアプリケーションに最適です。

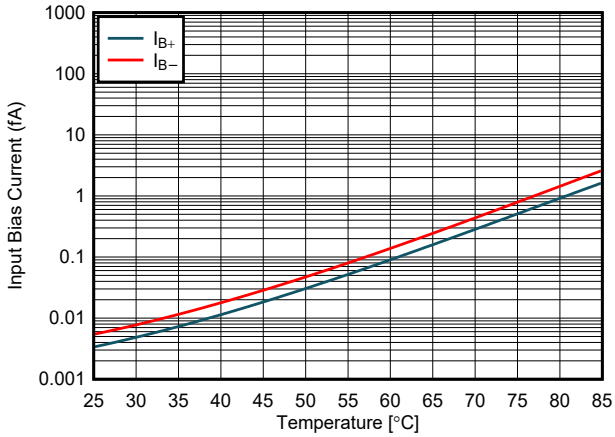
OPA928 には高精度のガード・バッファが内蔵されており、高インピーダンスの入力パターンを、感受性が高いアプリケーションでの望ましくない電流リークから保護します。OPA928 のパッケージとピン配置は、低リークの回路設計をサポートするように設計されています。

OPA928 は -40℃～+125℃で動作が規定されています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
OPA928	D (SOIC、8)	4.90mm × 3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



入力バイアス電流と温度との関係
(V_S = 16V、V_{CM} = 中電力)

ADVANCE INFORMATION

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
March 2023	*	Initial release.

5 Pin Configuration and Functions

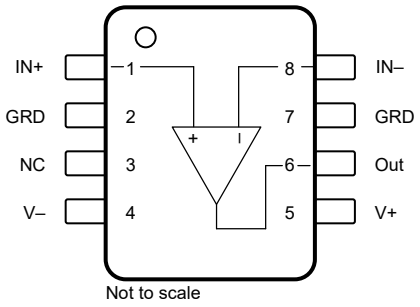

図 5-1. D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GRD	2, 7	—	Guard buffer
IN+	1	Input	Noninverting input
IN–	8	Input	Inverting input
DNC	3	—	Do not connect (leave floating)
OUT	6	Output	Output
V+	5	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply		±20	V
		Single supply		40	
	Signal input pin voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(2)		±0.5	
	Signal input pin current			±10	mA
I_{SC}	Output short circuit(3)		Continuous		
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001((1))	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002((2))	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Dual supply	±2.25		±8	V
		Single supply	4.5		16	
RH	Relative humidity				50	%
T_A	Ambient temperature		–40		125	°C

Thermal Information

THERMAL METRIC(1)		OPA928 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V to 16 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±20	fA
		T_A = –40°C to +85°C				±20	
I_{OS}	Input offset current				±1	±20	fA
		T_A = –40°C to +85°C				±20	
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±8	±75	
		V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = –40°C to +125°C		±25	±150	
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V			See *Typical Characteristics*		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.8	µV/°C
			V_{CM} = (V+) – 1.5 V		±0.5		
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		1.4		$µV_{PP}$
			(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V		7		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		18		$nV/\sqrt{Hz}$
			f = 1 kHz		15		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		53		
			f = 1 kHz		24		
i_n	Input current noise density	f = 0.1 Hz			0.05		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
			T_A = –40°C to +125°C	114	126		
		(V+) – 1.5 V < V_{CM} < (V+)		96	120		
			T_A = –40°C to +125°C	86	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		124	134		dB
			T_A = –40°C to +125°C	114	126		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		126	140		
			T_A = –40°C to +125°C	120	134		

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6.4 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 4.5 V to 16 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	Gain = 1, 10-V step	Falling		7.5		V/µs
			Rising		5.5		
t_s	Settling time	To 0.01%, C_L = 20 pF	Gain = 1, 2-V step		0.7		µs
			Gain = 1, 5-V step		1		
		To 0.001%, C_L = 20 pF	Gain = 1, 2-V step		1.8		
			Gain = 1, 5-V step		3.7		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0012%		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			700		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			275	400	µA
			T_A = –40°C to +125°C			500	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C
INTERNAL GUARD BUFFER							
V_{OSG}	Guard input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±8	±75	
dV_{OSG}/dT	Guard input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.8	µV/°C
			V_{CM} = (V+) – 1.5 V		±0.5		
BW	Bandwidth				2.5		MHz
	Guard output impedance	I_O = 0 A			1		kΩ

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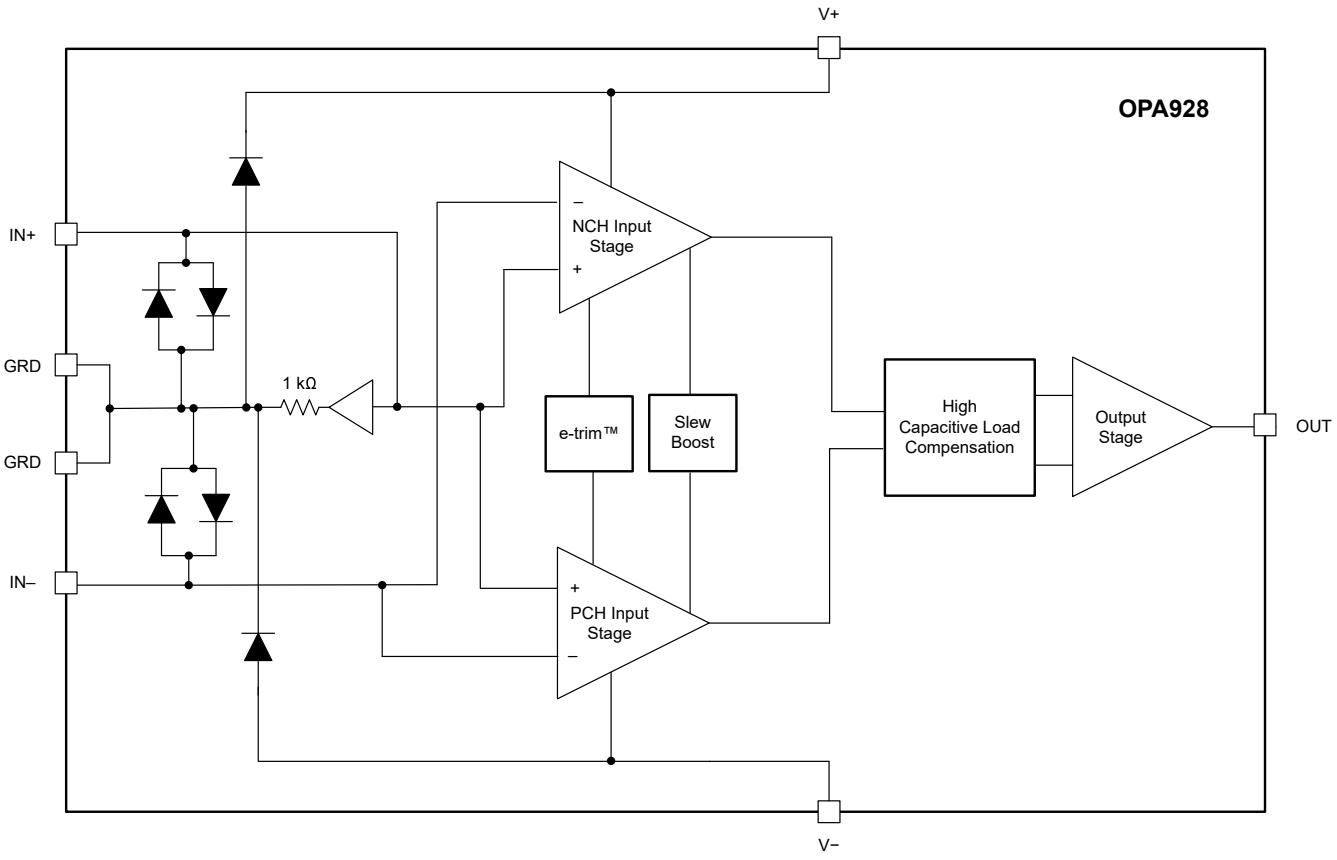
7 Detailed Description

7.1 Overview

The OPA928 op amp is an ultra-low input bias current, high-precision, low-power, e-trim operational amplifier. This op amp provides extremely low input bias current (< 20 fA) across the entire industrial temperature range of −40ºC to 85ºC. In addition, the OPA928 operates from 4.5 V to 16 V, is unity-gain stable, and post-package trimmed to achieve very low offset and offset drift performance.

The amplifier features state-of-the art CMOS technology and advanced design features to achieve extremely low input bias current across a wide temperature range, wide input and output voltage ranges, high loop gain, and low, flat output impedance. The OPA928 strengths include a wide bandwidth of 2.5 MHz, low noise spectral density of 15 nV/$\sqrt{\text{Hz}}$, low 1/f noise of 1.4 μV_{PP}, and low quiescent current of 400 µA. This combination of features make the OPA928 an excellent choice for interfacing very high impedance sensors, and photodiodes.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Guard Buffer

The OPA928 uses input protection diodes to limit the input differential voltage range and protect the device against transient currents. The back-to-back, or antiparallel, input protection diodes can be activated by fast transient step responses and cause relatively large amounts of current to flow through the inputs. The inrush current is routed through the antiparallel diodes and to the power supplies to avoid internal damage to the OPA928.

To achieve a femtoampere-level input bias current, the OPA928 uses an internal, high-precision, rail-to-rail guard buffer connected to the noninverting input. The guard buffer drives the voltage at the input of the OPA928 to the guard pins (pins 2 and 7) and sets a 0-V differential voltage across the antiparallel diodes, greatly reducing leakage current though the diodes. The guard buffer is isolated from large capacitive loads at the guard pins by a nominal 1-kΩ resistor. Use the guard pins to guard external components and input traces from possible current leakage paths. For more on guarding, see セクション 8.1.2.

7.3.2 Thermal Protection

The internal power dissipation of any amplifier causes the junction temperature (T_J) to rise. This phenomenon is called *self heating*. To prevent damage from overheating, the OPA928 has a thermal protection feature.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 180°C. Thermal protection forces the output to a high-impedance state. The OPA928 is also designed with approximately 30°C of thermal hysteresis. The OPA928 returns to normal operation when the output stage temperature reaches a safe operating temperature of approximately 150°C.

> **注意**
> The absolute maximum T_J of the OPA928 is 150°C. Exceeding the limits shown in the *Absolute Maximum Ratings* can cause damage to the device. Thermal protection triggers at approximately 180°C and does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

7.3.3 Capacitive Load and Stability

The OPA928 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 図 7-1. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

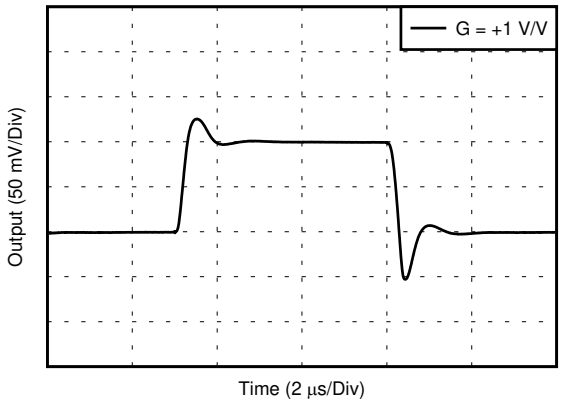

図 7-1. Transient Response With a Purely Capacitive Load of 1 nF

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For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small, 10-Ω to 20-Ω isolation resistor (R_{ISO}) in series with the output; 図 7-2 shows this resistor. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

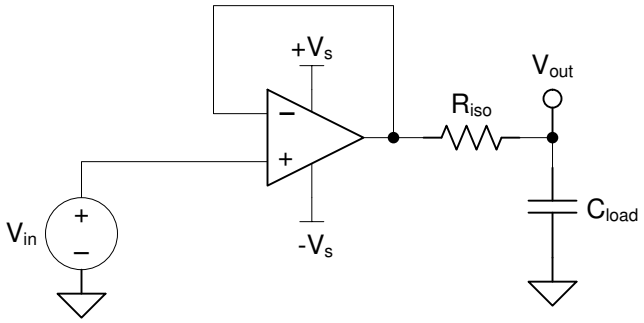

図 7-2. Extending Capacitive Load Drive With the OPA928

7.3.4 EMI Rejection

The OPA928 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. The OPA928 features improved design techniques to enhance EMI immunity.

7.3.5 Common-Mode Voltage Range

The OPA928 is a 16-V, true rail-to-rail input/output operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.

The OPA928 uses a precision trim for both the N-channel and P-channel regions enabling significantly lower levels of offset than previous-generation devices. In inverting configurations, such as with a transimpedance amplifier, the common-mode voltage is constant and set by the voltage at the noninverting pin. Therefore, in inverting configurations, the transition region can be easily avoided and is typically not a problem. In noninverting configurations, such as with a buffer, the common-mode voltage can vary widely; take care to avoid the transition region when possible.

The OPA928 guard buffer features the same complementary input stage. The input bias performance of the OPA928 is sensitive to small shifts in offset voltage. The shift in offset in the transition region is presented across the internal protection diodes and causes increased leakage. The increase in leakage can be significant and degrade the input bias performance of the OPA928. Avoid operating in the transistion region when possible to achieve specified input bias current performance.

7.4 Device Functional Modes

The OPA928 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPA928 is 16 V (±8 V).

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8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The OPA928 offers femtoampere level input bias current, and excellent dc precision and ac performance. This device provides 2.5-MHz bandwidth and very low noise, 15 nV/√Hz and 0.05 fA/√Hz. The OPA928 can operate with a 16-V supply and offers true rail-to-rail input/output performance to allow for a wide linear output voltage swing. The ultra-low input bias, low noise and wide output voltage swing capability make this device an excellent choice for low-light photodiode applications.

8.1.1 Contamination Considerations

Applications requiring femtoampere-level performance are extremely sensitive to contamination. Contaminants in the form of solder flux, salts, oils, organic acids, and more can form conductive paths over PCB traces and allow small currents to leak into input traces or other sensitive nodes, severely degrading performance. Proper handling and cleaning is required to achieve femtoampere level input bias performance in a PCB featuring the OPA928.

The following list of best practices helps prevent a PCB from contamination:

- Always wear a pair of clean, powder-free gloves or finger cots when handling the PCB.
- Always hold the PCB by the edges when handling is required.
- Avoid touching the surface of the PCB and other component packages, especially near sensitive nodes or input traces.
- Be cautious when breathing, speaking, and sneezing to prevent moisture or saliva from contacting the PCB.
- Do not allow direct airflow onto the board. Moving air can blow dust and moisture onto sensitive nodes. Airflow also introduces moving charges that manifest as a small current at the input.
- When not in use, place the PCB in an ESD bag or other enclosure to prevent dust and other contaminants from settling on the board.
- If configuring through-hole components in sensitive nodes, handle the components by the wire leads only.

A rigorous cleaning protocol is required after PCB assembly to remove all contaminants that can degrade input bias performance of the OPA928. Repeat the cleaning procedure any time the board is soldered or modified near sensitive nodes, or if contamination of these nodes is suspected.

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8.1.2 Guarding Considerations

図 8-1 details how to implement a guard in printed circuit board (PCB) layout. This section explores considerations for driving the PCB guard with the OPA928 internal guard buffer, an external guard driver, or by connecting the guard copper directly to the analog ground.

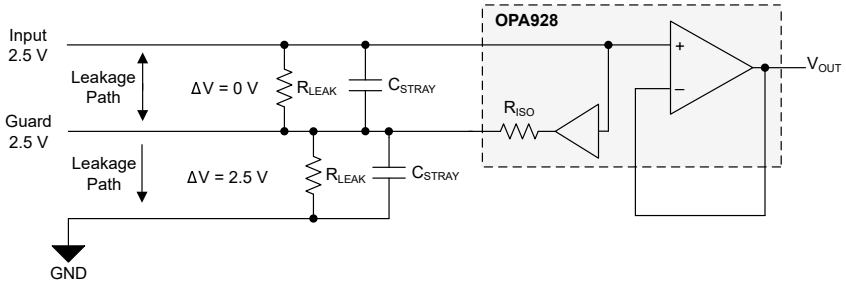

図 8-1. Driving the Guard, Internal Guard Buffer

The guard presents a low-impedance path for leakage currents of equal potential to the high-impedance node that is being guarded. For a noninverting configuration, the common-mode changes with the input signal and the guard must be actively driven by a voltage follower that tracks the input signal. Choose a low-offset, low-noise amplifier for the guard driver because any voltage potential between guard and input causes current to leak into the high-impedance trace. The OPA928 features a high-performance internal guard buffer that can be accessed at pin 2 and pin 7 to drive the PCB guard copper; see the *Electrical Characteristics*. The internal guard buffer tracks the voltage of the OPA928 input signal and is isolated from capacitive loads through a 1-kΩ isolation resistor, R_{ISO}.

図 8-2 shows how the PCB guard is driven with an external guard driver instead of the OPA928 internal guard buffer. To prevent the input bias current of the external guard driver from degrading the input signal, track the low-impedance input of the OPA928. If an external guard driver is used, the OPA928 guard pins can be left unconnected or can be overdriven by the external guard driver. Include an isolation resistor at the output of the guard driver to prevent gain peaking due to capacitive loading and to provide short-circuit protection. Make sure that the guard driver is stable and capable of driving the capacitive load presented by the guard, including long cable lengths, if applicable.

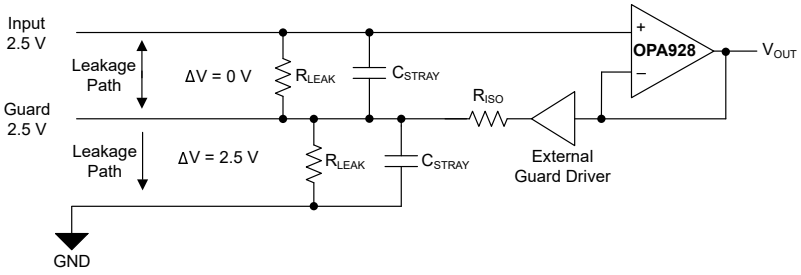

図 8-2. Driving the Guard, External Guard Driver

For inverting configurations, the input common-mode voltage is fixed to the analog ground or some dc reference voltage applied to the noninverting input. In this case, tie the PCB guard directly to the ground or low-impedance reference of the signal amplifier. Tying the PCB guard makes sure that the guard potential is always equal to the input common-mode voltage, without the additional offset and noise of an active guard driver. If the PCB guard is connected to the analog ground of the circuit, make sure to ground return paths in the PCB. Keep power and digital grounds separate from the guard and prevent ground loops from occurring. For inverting configurations, the OPA928 internal guard buffer or an external guard driver can be used to drive the PCB guard, and the same considerations apply as discussed for noninverting configurations.

ADVANCE INFORMATION

8.1.3 Humidity Considerations

The resistance of insulators is substantially affected by both temperature and humidity. Humidity can significantly lower the effective resistance of insulators and cause an increase in leakage current around the affected material. When water molecules settle on the surface of a given material, such as the plastic packaging and PCB, a parallel and more electrically conductive path is created. Effective guarding techniques and appropriate materials can help mitigate this behavior in the sensitive applications.

In some cases, water molecules can also penetrate the surface of a given material. The water molecules in the material increase the conductivity of the body of the material and a reduction of resitance is established across all adjacent nodes. Contrary to surface level leakge paths, leakage through the material cannot me mitigated with guarding techniques. Use PCB materials with low humidity absorption properties to reduce moisture related errors.

8.1.4 Dielectric Relaxation

All materials are prone to polarization in the presence of an electric field. The molecules of the given material within the electric field become aligned at varying rates; a phenomena known as polarization. The rate depends on the strength of the electric field and the susceptibility of the material. When the electric field is removed, the molecules in the material return to the original alignment and random distribution, a phenomena known as relaxation. The rate at which the molecules return to normal alignment depends on the permittivity and resistivity of the material. In conductors, polarization and relaxation happens nearly instantaneously. In dielectrics, the time delay for polarization and relaxation can be significant.

In most applications, dielectric relaxation is not a major design concern. However, for femtoampere leakage current, dielectric relaxation becomes a major concern. The realignment of molecules causes a small displacement current to appear across the material. The displacement current from the dielectric relaxation is often greater than the input bias current level of the OPA928. The time required for the displacement current in common FR-4 PCB materials to dissipate under the input bias current level of the OPA928 can take well over an hour. To minimize the dielectric relaxation time and the leakage effects, use ceramic-based PCB materials such as Rogers 4350B.

8.2 Typical Applications

8.2.1 High-Impedance (Hi-Z) Amplifier

The OPA928 behaves very close to an ideal op amp in regards to the input current. The near-zero input bias current performance enables applications with extremely high impedance signal sources. For example, pH probes can have an output impedance of up to 10 GΩ. Most op amps are inadequate to use with this kind of sensor impedance. For example, a CMOS op amp with 1 pA of input bias current loads the sensor and causes a large, and unacceptable, 10-mV error at the input. In 図 8-3, the OPA928 is used to gain up the small signal from the pH probe sensor. The large input impedance and ultra-low bias current into the positive input pin of the OPA928 does not load the sensor and minimizes the input bias current error.

ADVANCE INFORMATION

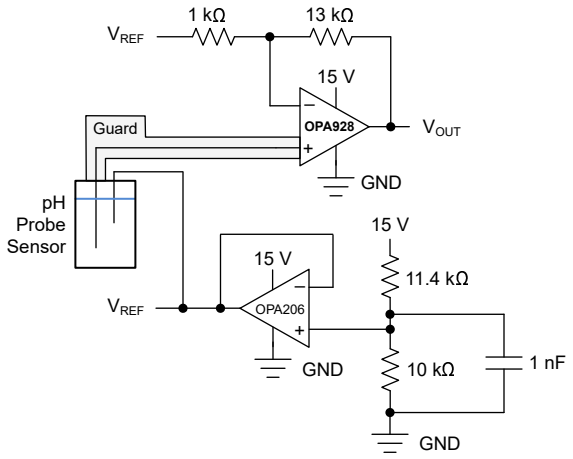

図 8-3. High Impedance pH Probe Amplifier Circuit

8.2.1.1 Design Requirements

The primary objective is to design a single-supply, pH-probe gain amplifier.

- Supply voltage: 15 V
- pH-probe sensor impedance: 10 GΩ
- Temperature range: 25ºC to 85ºC

8.2.1.2 Detailed Design Procedure

In the 図 8-3 example, the pH-probe sensor is assumed to produce an output of ±59 mV/pH at room temperature, or 25°C, and ±71 mV/pH at 85°C. The pH probe can be modeled as a small, variable battery in series with a 10-GΩ resistor. As a result of the intrinsic characteristics of the pH probe, a near 0-V output is produced for a neutral pH value of 7. A gain of 14 V/V provides a wide output swing of approximately ±7 V. To enable single supply operation, a 7-V reference voltage (V_{REF}) is created using the 15-V supply voltage and a simple voltage divider. The output swing is shifted to 0 V to 14 V, and is conveniently proportional to the approximately 1 V/pH at 85°C. Temperature calibration of the pH sensor (not shown) is necessary for accurate results when wide temperature variation is expected.

8.2.1.3 Application Curve

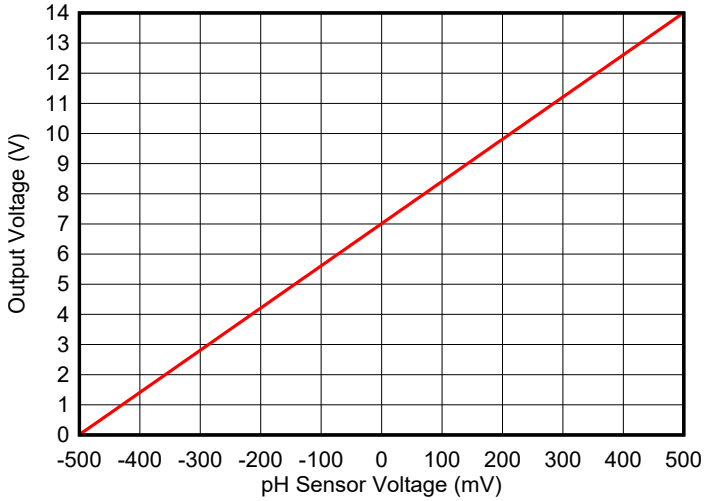

図 8-4. Single Supply, pH-Probe Sensor Transfer Function

ADVANCE INFORMATION

8.2.2 Transimpedance Amplifier

図 8-5 shows the OPA928 configured as a transimpedance amplifier (TIA) for a low-light photodiode. TIAs are needed to amplify the light-dependent current of the photodiode. In low-light conditions, photodiodes produce a very small current and ultra-low input bias current and large gain in excess of 10^9 V/A is required. For a full analysis of the TIA circuit, including theory, calculations, and measured data, see the *Transimpedance Amplifiers (TIA): Choosing the Best Amplifier for the Job* application brief.

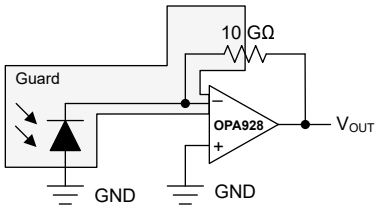

図 8-5. OPA928 Simplified Photodiode Transimpedance Amplifier

8.2.2.1 Design Requirements

The design requirements for this design are:

- Transimpedance gain: 10,000,000,000 A/V
- Supply voltage rail: 5 V
- Photodiode shunt resistance: 5 GΩ
- Photodiode shunt capacitance: 35 pF

8.2.2.2 Detailed Design Procedure

Some photodiode applications operate in dark conditions and require low-light detection. In these cases, the current output from the photodiode can be miniscule. To make the small diode current measurable, a transimpedance amplifier (TIA) with a very large gain is required. The ideal transfer function of a resistive transimpedance amplifier is given by 式 1:

$$V_{OUT} = I_{PD} \times R_F \tag{1}$$

The photodiode current (I_{PD}) flows through the feedback resistor (R_F) and forces an output voltage (V_{OUT}) equal to the voltage drop across R_F. The ideal transfer function gives an intuitive understanding of TIA operation. In practice, however, nonidealities must be taken into consideration to achieve desirable performance. 図 8-6 illustrates important nonidealities of the transimpedance amplifier circuit.

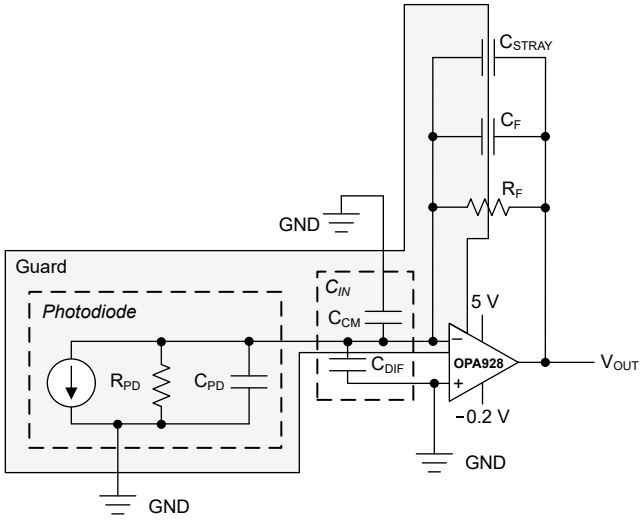

図 8-6. Transimpedance Photodiode Application

ADVANCE INFORMATION

One very important consideration, is the input bias current of the op amp. The input bias current directly adds to I_{PD} and creates an undesired error. The input bias current typically determines the minimum measurable I_{PD} within a given error tolerance. For example, a 1-pA input bias current yields a 20% error when measuring a 5-pA photodiode current. A 1% error target requires a 50-fA input bias current maximum specification. The ultra-low input bias current of the OPA928 enables accurate, extremely low I_{PD} measurements. For information on how to maintain the specified input bias performance, see セクション 8.4.

The input offset voltage (V_{OS}) of the op amp is another significant source of error. The input offset voltage forces a voltage across the effective shunt resistance of the diode (R_D) and creates an error current (I_{RPD}) equal to V_{OS} / R_{PD}. In many cases, V_{OS} can be a major source of error. For example, a V_{OS} of 25 µV and an R_{PD} of 1 GΩ creates an I_{RPD} of 25 fA. Take into consideration offset voltage variation with temperature and common-mode voltage.

In low-light applications, a very large R_F is needed to provide the required gain, giving rise to potential stability problems. R_F interacts with the input capacitance (C_{IN}) of the op amp, the photodiode capacitance (C_{PD}), and stray PCB capacitance to create a low-frequency zero in the noise gain transfer function (1/β). Remember that C_{IN} includes the differential (C_{DF}) and common-mode (C_{CM}) capacitance of the op amp. The value of C_{DF} and C_{CM} are found in the *Electrical Characteristics*. The zero in 1/β causes the gain to increase over frequency and is the basis for instability problems. To counteract the zero, create a pole by adding a compensation capacitor (C_F) in the feedback loop. The optimal value selection of C_F depends on several parameters and extensive literature exists on this topic. One approach is to equate two expressions of noise gain. 式 2 makes the assumption that the noise gain only depends on the capacitance of the circuit at a high enough frequency; a reasonable approximation.

$$\frac{GBW}{2\pi R_F C_F} = \frac{C_{IN} + C_F}{C_F} \tag{2}$$

Solving 式 2 for C_F yields a quadratic equation with one real solution. The quadratic equation is given by 式 3:

$$C_F = \frac{1 \pm \sqrt{1 + 8\pi GBW R_F C_I}}{4\pi GBW R_F} \tag{3}$$

式 3 yields more than 45° of phase margin and some amount of gain peaking. Increasing the value of C_F yields a higher phase margin and limits the peaking response at the expense of signal bandwidth, given by 式 4. For a flat frequency response, use a compensation capacitor calculator. For a very large R_F, a very small capacitor (< 0.5 pA) is required to maintain stability, and stray capacitance in the feedback loop can be sufficient.

$$f_{-3dB} = \frac{1}{2\pi R_F C_F} \tag{4}$$

Another issue arises when using a very large R_F. All resistors are sources of thermal noise. The magnitude of noise density contribution from a resistor is directly correlated to the square root of the resistance value. In a gain configuration, the feedback resistance and input resistance contribute to the total noise of the circuit. The thermal noise resistance value in 図 8-6 is given by the parallel combination of R_F and R_{PD}. 式 5 shows the input-referred-resistor noise-density equation. The low voltage noise of the OPA928 is not a significant contributor of noise because R_F and R_{PD} are typically very large.

$$e_{n\_R} = \sqrt{4kT\frac{R_{PD}R_F}{(R_{PD} + R_F)}} \tag{5}$$

In this application, a 5-V output is required from the 500-pA current input from a Si photodiode. A 10-GΩ resistor is used to achieve the required gain of 10,000,000,000 V/A. R_{PD} and C_{PD} of the photodiode is assumed to be 5 GΩ and 35 pF, respectively. Using the specifications of the OPA928 and the aforementioned photodiode specifications, 式 3 calculates C_F to be approximately 0.017 pF. The value obtained by calculation is impractical; therefore, the smallest standard capacitor available is used (1 pF). If settling time is a major concern, consider making the required small-value capacitor using PCB traces.

ADVANCE INFORMATION

8.3 Power-Supply Recommendations

The OPA928 is specified for operation from 4.5 V to 16 V (±2.25 V to ±8 V). The OPA928 features a high power-supply rejection ratio (PSRR) and significantly reduces power supply errors at dc. However, a decreasing PSRR at high frequencies means that high-frequency components in the power supply, such as noise, can be coupled to the output. Use a linear, low-noise power supply to optimize noise performance. Place 0.1-µF bypass capacitors close to the power-supply pins to further reduce errors coupling in from the power supplies. For more detailed information on bypass capacitor placement, see セクション 8.4. Switching power supplies generate switching noise that can manifest at the output of the OPA928. When switching power supplies cannot be avoided, use proper filtering and a low-dropout regulator to attenuate the switching noise and respective harmonics to an acceptable level.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, follow PCB layout best practices, including:

- Connect 0.1-µF ceramic bypass capacitors with low equivalent series resistance (ESR) between each supply pin and ground. Place the capacitors as close to the device as possible. For single-supply applications, use a single bypass capacitor from V+ to ground. Bypass capacitors are used to reduce coupled noise by providing low-impedance power sources local to the analog circuitry.
- Physically separate digital and analog grounds, paying attention to the flow of the ground current. Separate grounding for analog and digital circuitry is one of the simplest and most effective methods for noise suppression. A ground plane helps distribute heat and reduces EMI noise pickup.
- Place external components as close to the device as possible.
- Keep the length of input traces as short as possible. Input traces are the most sensitive part of the circuit.

In addition to general PCB layout considerations, specific layout techniques must be implemented to achieve femtoampere-level input bias current. Every insulator, including PCB material, has a finite resistance that can become a path for current to leak into input traces and degrade input bias performance. To minimize leakage current paths, implement a guard in the PCB layout. The guard presents a low-impedance path equipotential to the input traces. Leakage current toward the high impedance input path can be diverted to the low-impedance guard path. The guard is driven to a potential equal to the input common-mode voltage (see guarding considerations). Current flowing between the input and guard traces is negligible because both traces are ideally at the same potential.

Surround all high-impedance input traces with copper guard traces all the way from the source to the input pins of the OPA928. For inverting configurations, extend the guard copper to the middle of the feedback components, separating the low-impedance output from the high-impedance input node. Remove all solder mask and silkscreen from the guard area to reduce surface-charge accumulation and prevent surface-level leakage paths to the input.

Leakage currents can flow between layers vertically or diagonally through the PCB, as well as horizontally on the surface layer. The guard must be implemented in a three-dimensional scheme to prevent leakage currents originating in other layers from flowing into the signal path. Place the guard copper on the next layer directly below the surface-level signal and guard traces to protect from vertical leakage paths. Surround the sensitive input traces with a via fence connecting the guard copper on different layers to complete the three-dimensional guard enclosure. 図 8-9 shows the internal copper layers of a four-layer PCB using a three-dimensional guarding scheme.

A copper ground pour around the OPA928 and guard area is recommended to reduce noise and EMI. In addition to noise and EMI benefits, this ground pour presents another low-impedance path for leakage currents to take. Keep voltage potentials other than guard and ground as far as possible from sensitive nodes. The OPA928 SOIC pinout places the input and power supply pins at opposite ends of the amplifier package to reduce leakage currents across the package and PCB material. If the power supplies (or other voltages) are present in vias or through-holes near the OPA928, a ground-potential via fence can be applied locally to these through-holes to provide a low-impedance path for leakage currents in the direction of sensitive nodes.

High-impedance, femtoampere-level circuits are highly sensitive to electromagnetic interference (EMI). Ground planes and ground pours in the PCB layout can help reduce the effects of EMI. During operation, a femtoampere-level PCB is commonly placed within a shielded enclosure tied to ground for further EMI rejection. In layout, consider enclosing the OPA928 and all high-impedance traces within a local grounded RF shield. An example of localized RF shielding for high-impedance nodes is available in the OPA928EVM user's guide.

8.4.2 Layout Examples

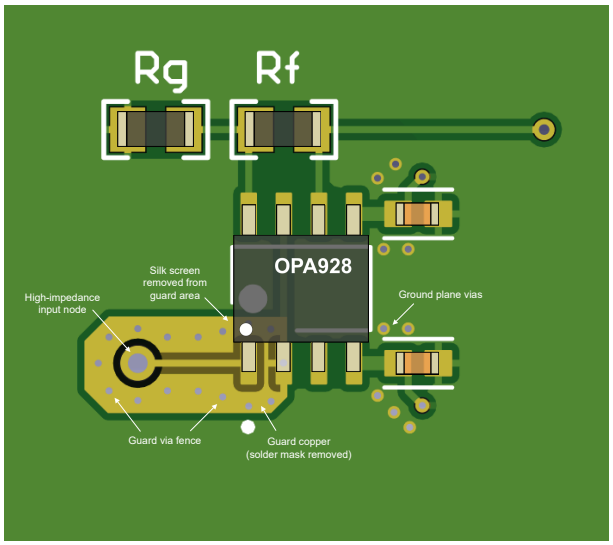

図 8-7. Layout Example: Noninverting Configuration

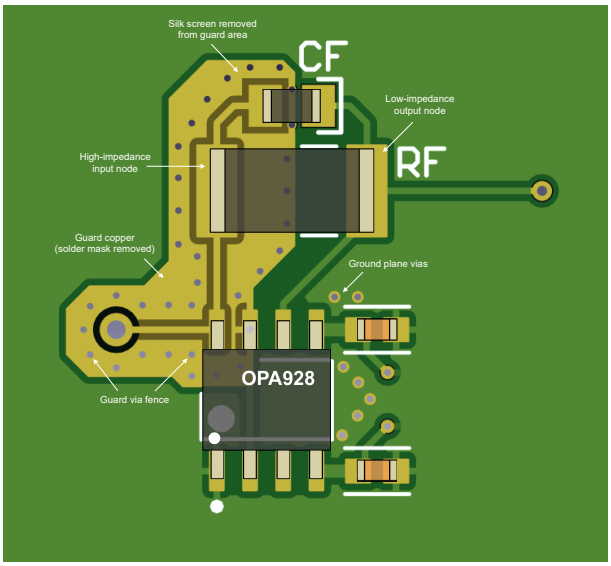

図 8-8. Layout Example: Inverting Configuration

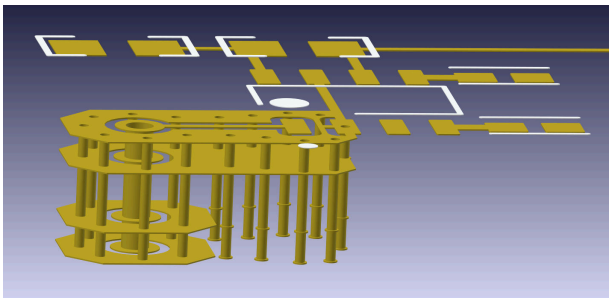

図 8-9. Layout Example: Three-Dimensional Guard (4-Layer PCB)

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

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9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, *OPA928EVM User's Guide*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA928DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	OPA928	Samples
OPA928DT	ACTIVE	SOIC	D	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	OPA928	Samples
POPA928DR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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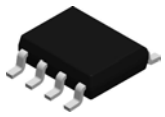
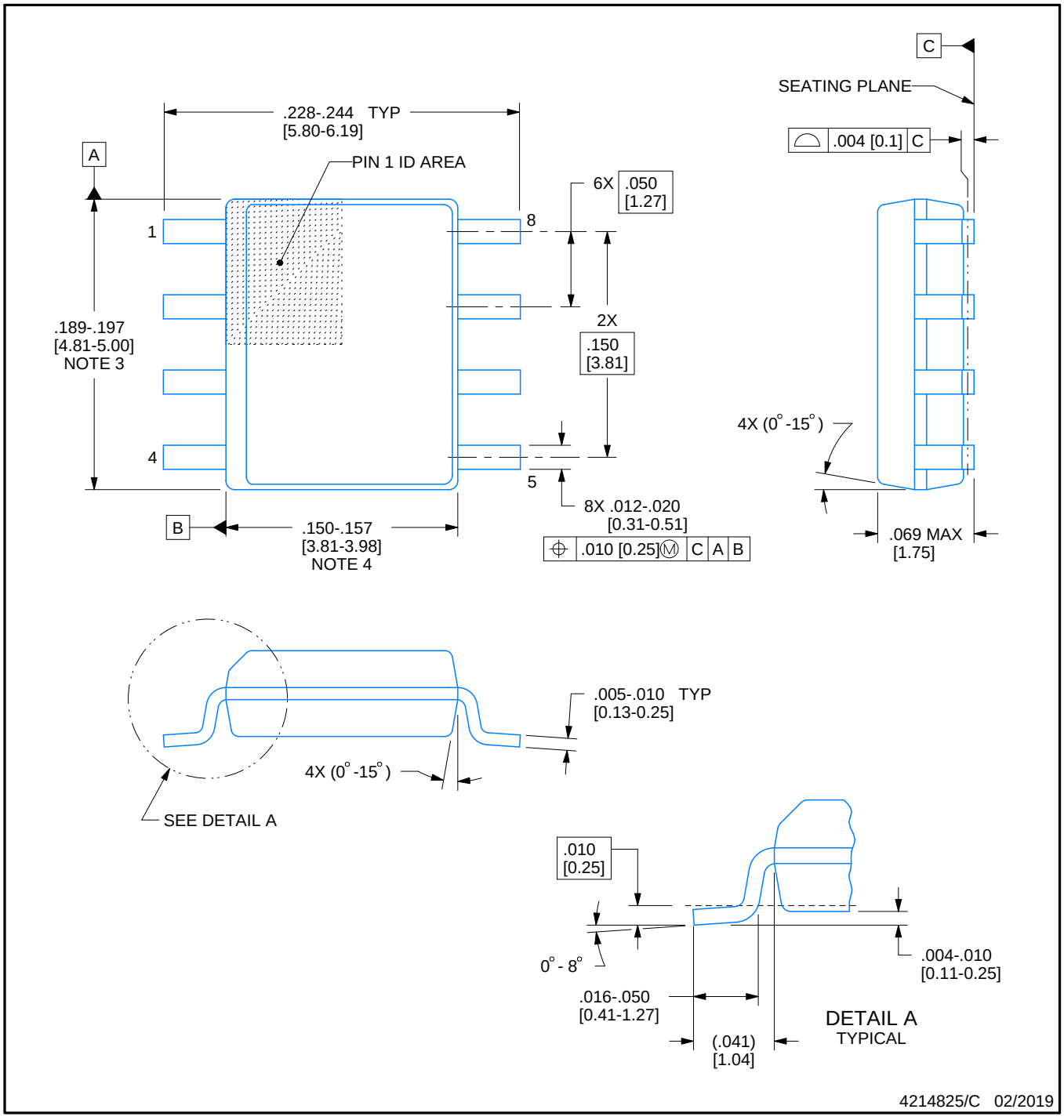


PACKAGE OUTLINE

D0008A

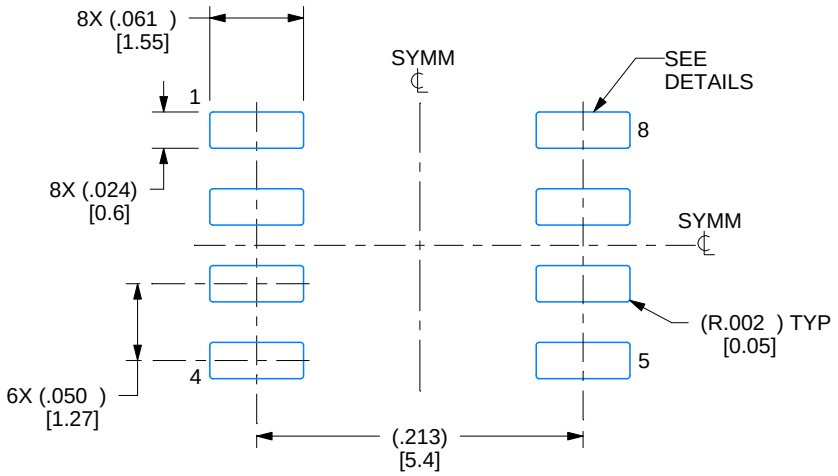
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

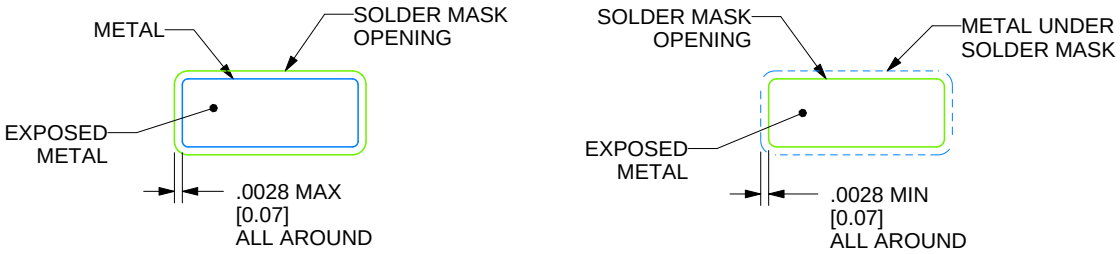


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

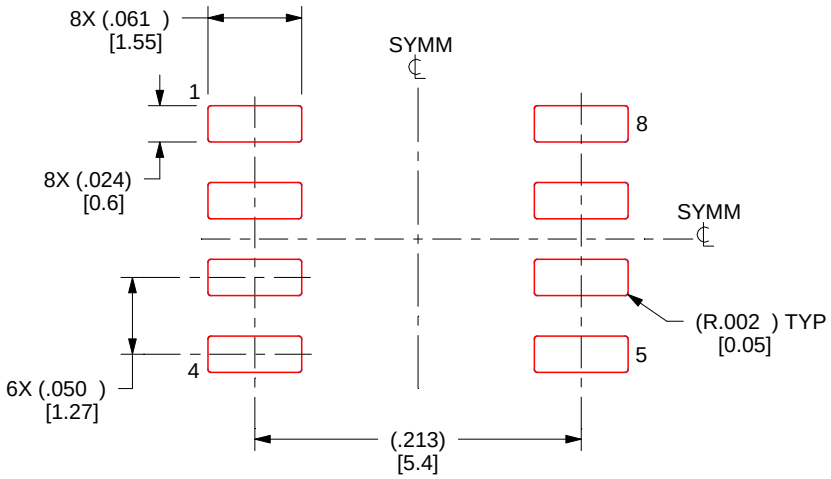
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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