TEXAS INSTRUMENTS
PCA9534A
JAJSLF1J – SEPTEMBER 2006 – REVISED MARCH 2021

PCA9534A 割り込み出力および構成レジスタ付き、リモート 8 ビット I²C/SMBus 低消費電力 I/O エクスパンダ

1 特長

- 低いスタンバイ消費電流：1μA 以下
- I²C からパラレル・ポートへのエクスパンダ
- オープン・ドレインのアクティブ LOW 割り込み出力
- 2.3V～5.5V の動作電源電圧範囲
- 5V 許容の I/O ポート
- 400kHz の高速 I²C バス
- 3 本のアドレス・ピンにより、最大 8 個のデバイスを I²C/SMBus に接続可能
- PCA9534 と組み合わせて使用した場合、最大 16 のデバイスを I²C/SMBus に接続可能
  I²C エクスパンダ製品については、*セクション 5* を参照してください。
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- パワー・オン・リセット機能を内蔵
- 電源投入時はすべてのチャネルが入力に構成された状態
- 電源オン時のグリッチなし
- SCL/SDA 入力でのノイズ・フィルタ
- 大電流の最大駆動能力を持つラッチ付き出力により、LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 概要

この 2 線式双方向バス (I²C) 用 8 ビット I/O エクスパンダは、2.3V～5.5V の V_{CC} で動作するように設計されています。I²C インターフェイス [シリアル・クロック (SCL)、シリアル・データ (SDA)] により、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

PCA9555 は、構成 (入力 / 出力選択)、入力ポート、出力ポート、極性反転 (アクティブ HIGH またはアクティブ LOW 動作) 用の 8 ビット・レジスタをそれぞれ 2 個ずつ搭載しています。電源オン時に、I/O は入力として構成されます。しかし、システム・マスタは、I/O 構成ビットに書き込むことで、I/O を入力または出力として有効にできます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されます。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。すべてのレジスタをシステム・マスタで読み出すことができます。

タイムアウトまたはその他の不適切な動作が発生した場合、システム・マスタはパワーオン・リセット機能を利用して PCA9534A をリセットできます。これにより、レジスタはデフォルト状態になり、I²C/SMBus ステート・マシンは初期化されます。

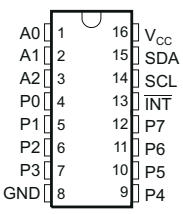
PCA9534A のオープン・ドレイン割り込み ($\overline{INT}$) 出力は、いずれかの入力の状態が、対応する入力ポート・レジスタの状態と異なっている場合にアクティブになるため、入力状態が変化したことをシステム・マスタに示すために使用されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
PCA9534A	SSOP (16)	6.20mm × 5.30mm
	VQFN (16)	4.00mm × 4.00mm
	QFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGV PACKAGE
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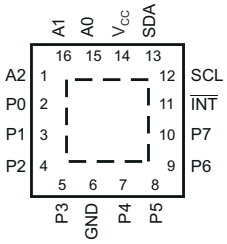

RGT PACKAGE
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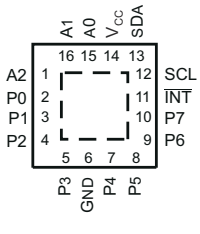

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3 Revision History

Changes from Revision I (June 2014) to Revision J (March 2021)	Page
• Moved the "Storage temperature range" to the *Absolute Maximum Ratings*	6
• Moved the "Package thermal impedance" to the *Thermal Resistance Characteristic*	6
• Changed the V_{IH} High-level input voltage (SDL, SDA) Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions*	6
• Changed the V_{IH} High-level input voltage (A0, A1, A2, P7–P0) MIN value From: 2 V To: V_{CC} in the *Recommended Operating Conditions*	6
• Changed the V_{IL} Low-level input voltage (A0, A1, A2, P7–P0) MAX value From: 0.8 V To: 0.3 x V_{CC} in the *Recommended Operating Conditions*	6
• Added the *Thermal Resistance Characteristics*	6
• Changed the V_{PORR} row in the *Electrical Characteristics*	7
• Added the V_{PORF} row in the *Electrical Characteristics*	7
• Changed the I_{CC} Standby mode values in the *Electrical Characteristics*	7
• Changed the C_i SCL Max value From: 5 pF To: 8 pF in the *Electrical Characteristics*	7
• Changed the C_{io} SDA Max value From:6.5 pF To: 9.5 pF in the *Electrical Characteristics*	7
• Changed the t_{pv} Output data valid MAX values From: 200 ns To 350 ns in the *Swirtching Characteristics*	8
• Changed the *Typical Characteristics* graphs	9
• Changed the *Power Supply Recommendations*	25

Changes from Revision H (June 2010) to Revision I (June 2014)	Page
• Added Interrupt Errata section.	17
• Deleted the 100 kΩ resistor at V_{CC}	23

4 概要 (続き)

PCA9534A と PCA9534 は、固定 I^2C アドレスを除くと同じです。そのため、これらのデバイス最大 16 個 (各 8 個) を同じ I^2C バスに接続できます。

$\overline{INT}$ はマイクロコントローラの割り込み入力に接続できます。この配線で割り込み信号を送ることでリモート I/O は、I^2C バス経由で通信しなくてもポート上に受信データが存在するかどうかをマイクロコントローラに通知できます。そのため、PCA9534A はシンプル・スレーブ・デバイスとして機能できます。

本デバイスの出力 (ラッチ付き) は大電流駆動能力を備えているため、LED を直接駆動できます。本デバイスは低消費電流です。

3 本のハードウェア・ピン (A0、A1、A2) を使って固定 I^2C アドレスをプログラムおよび変更することで、最大 8 つのデバイスが同じ I^2C バスまたは SMBus を共有できます。

PCA9534A は PCF8574A とピン互換、I^2C アドレス互換です。しかし PCA9534A では、PCF8574A に対して機能が拡張されているため、ソフトウェアを変更する必要があります。

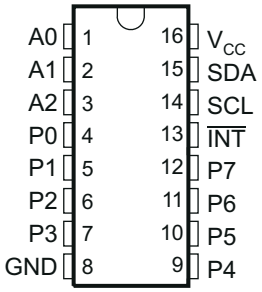
PCA9534A は PCA9554A の低消費電力バージョンです。PCA9534A と PCA9554A の唯一の違いは、PCA9534A では内部 I/O プルアップ抵抗が除去されていることです。そのため、I/O を LOW に保持する際のスタンバイ・モードの消費電力が大幅に低減されています。

5 Device Comparison Table

DEVICE	MAX FREQUENCY	I^2C ADDRESS	V_{CC} RANGE	NO. OF GPIOs	INTERRUPT OUTPUT	RESET INPUT	CONFIGURATION REGISTERS	5-V TOLERANT	PUSH-PULL I/O TYPE	OPEN-DRAIN I/O TYPE	COMMENT
TCA6408	400	0100 00x	1.65 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and t_r (ramp time) < 10 ms
TCA6408	400	0100 00x	1.65 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000 ms
TCA6416	400	0100 00x	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA6416A	400	0100 00x	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000ms
TCA6424	400	0100 00x	1.65 to 5.5	24	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA9535	400	0100 xxx	1.65 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
TCA9539	400	1110 1xx	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	
TCA9555	400	0100 xxx	1.65 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA6107	400	0011 xxx	2.3 to 5.5	8	Yes	Yes	Yes	Yes	Yes P1—P7 bits	Yes P0 bit	One open drain output; eight push pull outputs
PCA9534	400	0100 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	PCA9534 has a different slave address as the PCA9534A, allowing up to 16 devices '9534 type devices on the same I^2C bus
PCA9534A	400	0111 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	PCA9534A has a different slave address as the PCA9534, allowing up to 16 devices '9534 type devices on the same I^2C bus
PCA9535	400	0100 xxx	2.3 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA9536	400	1000 001	2.3 to 5.5	4	No	No	Yes	Yes	Yes	No	
PCA9538	400	1110 0xx	2.3 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	
PCA9539	400	1110 1xx	2.3 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	
PCA9554	400	0100 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	
PCA9554A	400	0111 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	
PCA9555	400	0100 xxx	2.3 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA9557	400	0011 xxx	2.3 to 5.5	8	No	Yes	Yes	Yes	Yes	Yes	
PCF8574	400	0100 xxx	2.5 to 6.0	8	Yes	No	No	Yes	Yes	No	PCA8574 has a different slave address as the PCA8574A, allowing up to 16 devices '9534 type devices on the same I^2C bus
PCF8574A	400	0111 xxx	2.5 to 6.0	8	Yes	No	No	Yes	Yes	No	PCA8574A has a different slave address as the PCA8574, allowing up to 16 devices '9534 type devices on the same I^2C bus
PCF8575	400	0100 xxx	2.5 to 5.5	16	Yes	No	No	Yes	Yes	No	
PCF8575C	400	0100 xxx	4.5 to 5.5	16	Yes	No	No	Yes	No	Yes	

6 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGV PACKAGE
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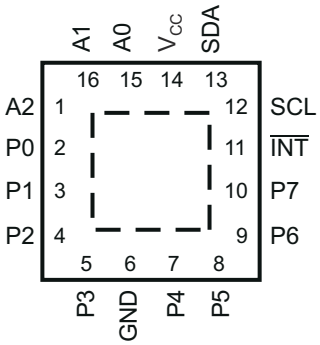


RGT PACKAGE
(TOP VIEW)

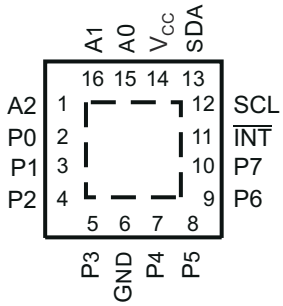


表 6-1. Pin Functions

PIN			DESCRIPTION
NAME	QSOP (DBQ), SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT) AND QFN (RGV)	
A0	1	15	Address input. Connect directly to V_{CC} or ground.
A1	2	16	Address input. Connect directly to V_{CC} or ground.
A2	3	1	Address input. Connect directly to V_{CC} or ground.
P0	4	2	P-port input/output. Push-pull design structure.
P1	5	3	P-port input/output. Push-pull design structure.
P2	6	4	P-port input/output. Push-pull design structure.
P3	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P4	9	7	P-port input/output. Push-pull design structure.
P5	10	8	P-port input/output. Push-pull design structure.
P6	11	9	P-port input/output. Push-pull design structure.
P7	12	10	P-port input/output. Push-pull design structure.
$\overline{INT}$	13	11	Interrupt output. Connect to V_{CC} through a pullup resistor.
SCL	14	12	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	15	13	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	16	14	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		A2–A0, P7–P0	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A2–A0, P7–P0	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P7–P0		–10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

7.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		PCA9535							UNIT
		DB (SSOP)	DBQ (SSOP)	DVG (TVSOP)	DW (SOIC)	PW (TSSOP)	RGT (VQFN)	RVE (VQFN)	
		16 Pins	16 Pins	16 Pins	16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82	90	86	92.2	122	63.2	51	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	8		mA
	P port(3)	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	V_I = V_{CC} or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	V_I = V_{CC}	2.3 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			–1	µA
I_{CC}	Operating mode	V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{scl} = 400 kHz	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{scl} = 100 kHz	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		1.5	8.7	
			3.6 V		0.9	4	
			2.7 V		0.6	3	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		All LED I/Os at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			1	
C_I	SCL	V_I = V_{CC} or GND	2.3 V to 5.5 V		4	8	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	2.3 V to 5.5 V		5.5	9.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P0) must be limited to a maximum current of 200 mA.

7.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see 図 8-1)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I²C bus capacitive load			400		400	ns

(1) C_b = total capacitive of one bus in pF

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see 図 8-2 and 図 8-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		350		350	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

7.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

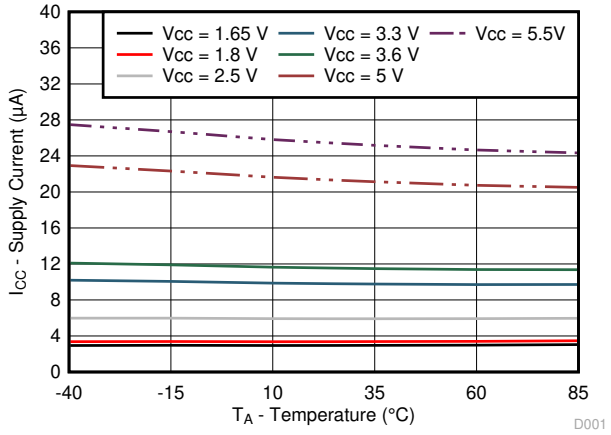


図 7-1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

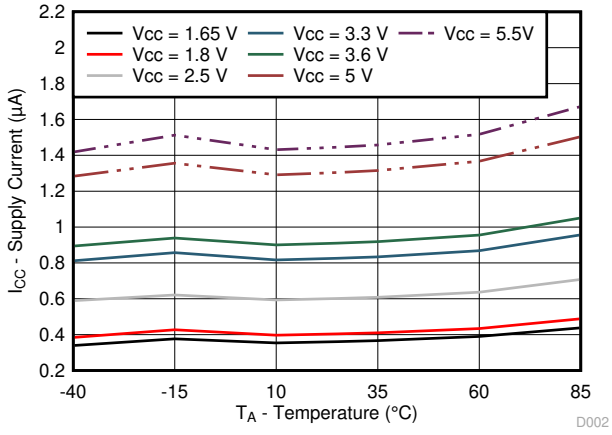


図 7-2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

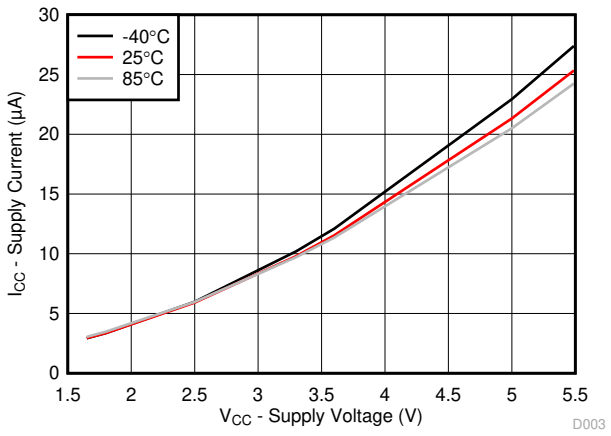


図 7-3. Supply Current vs Supply Voltage for Different Temperature (T_A)

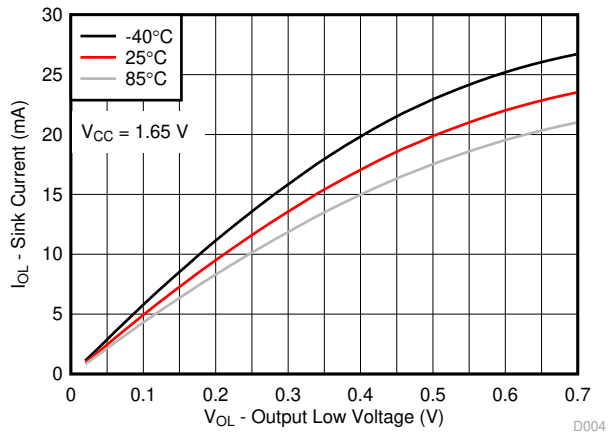


図 7-4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

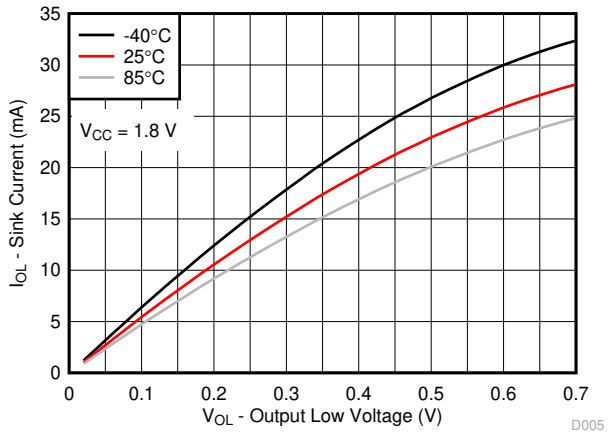


図 7-5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

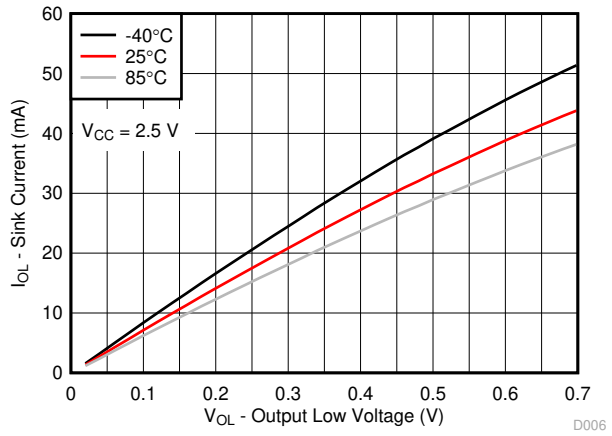


図 7-6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

7.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

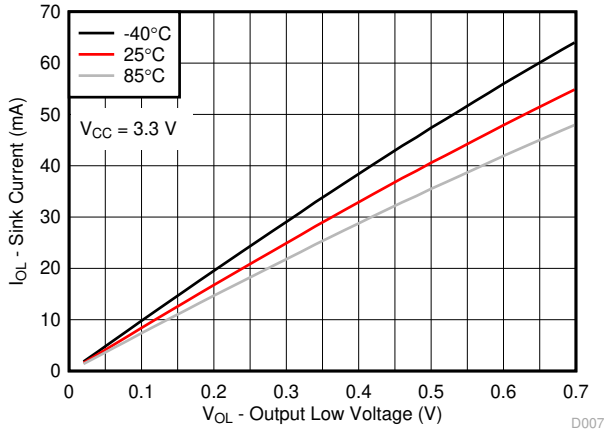


図 7-7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

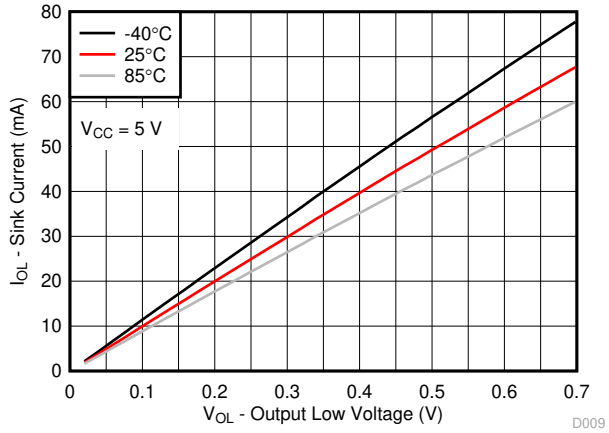


図 7-8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

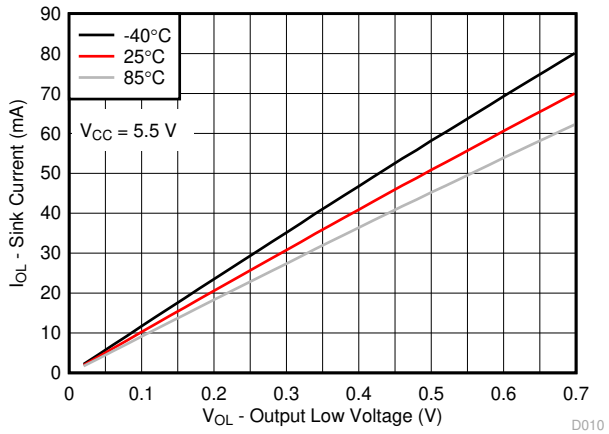


図 7-9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

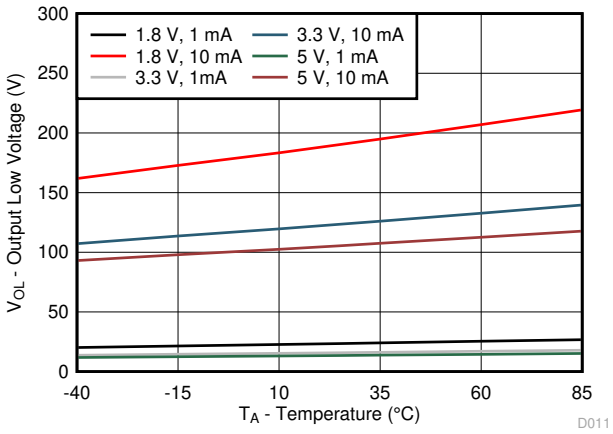


図 7-10. II/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

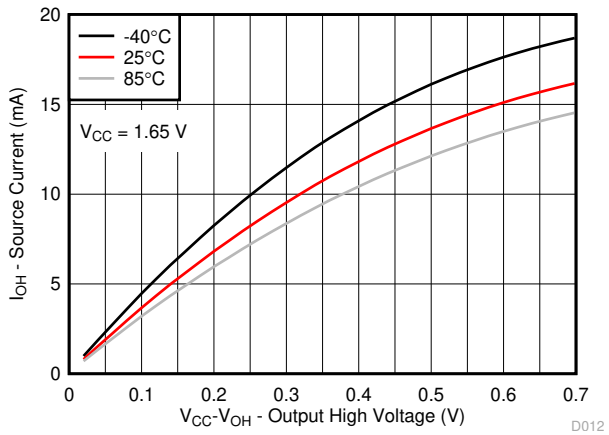


図 7-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

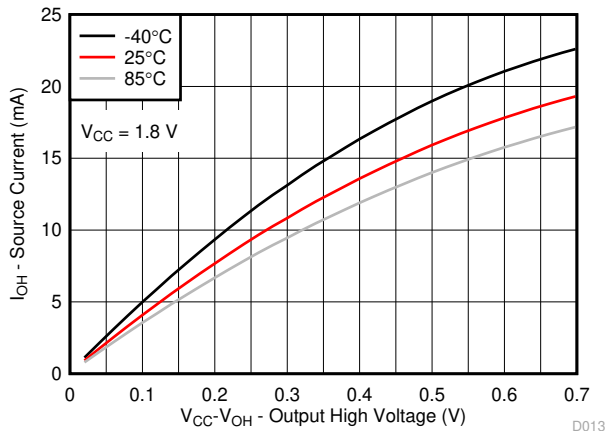


図 7-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

7.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

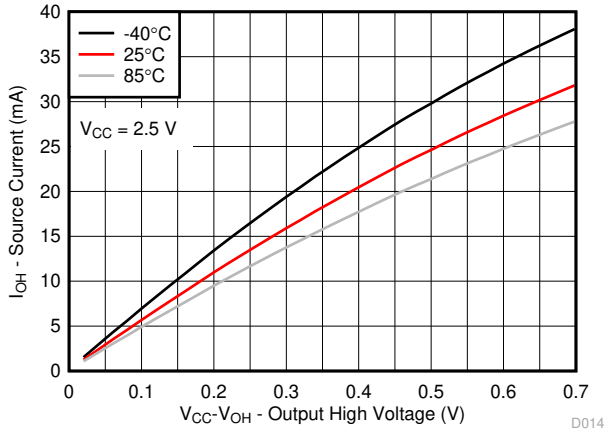


図 7-13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

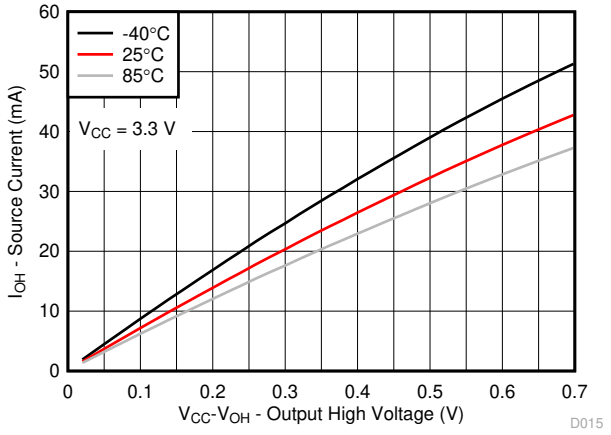


図 7-14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

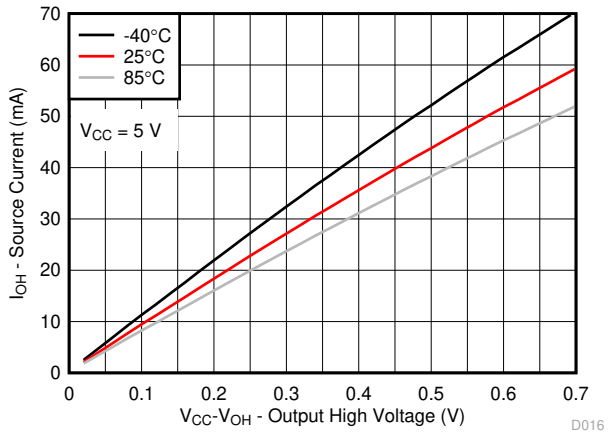


図 7-15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

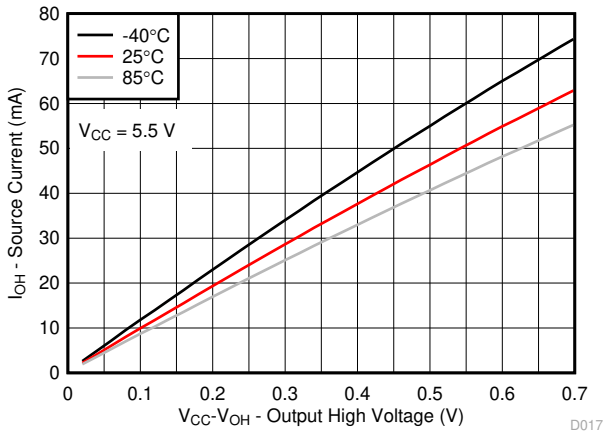


図 7-16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

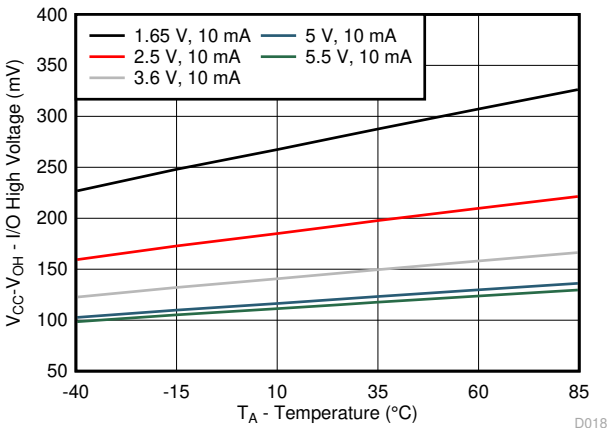


図 7-17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

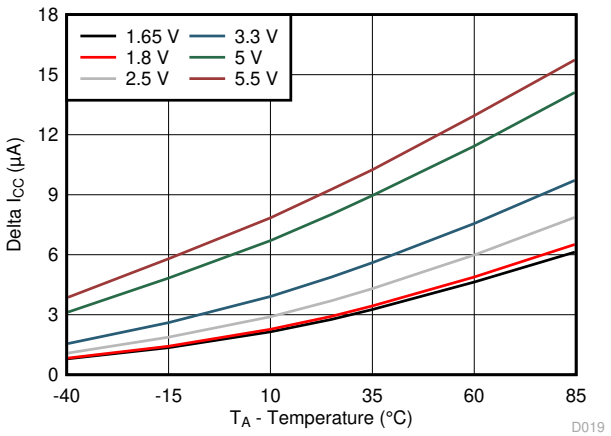
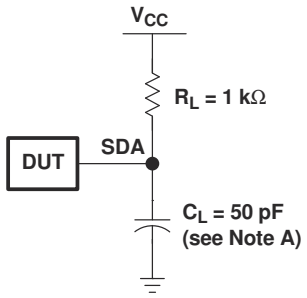
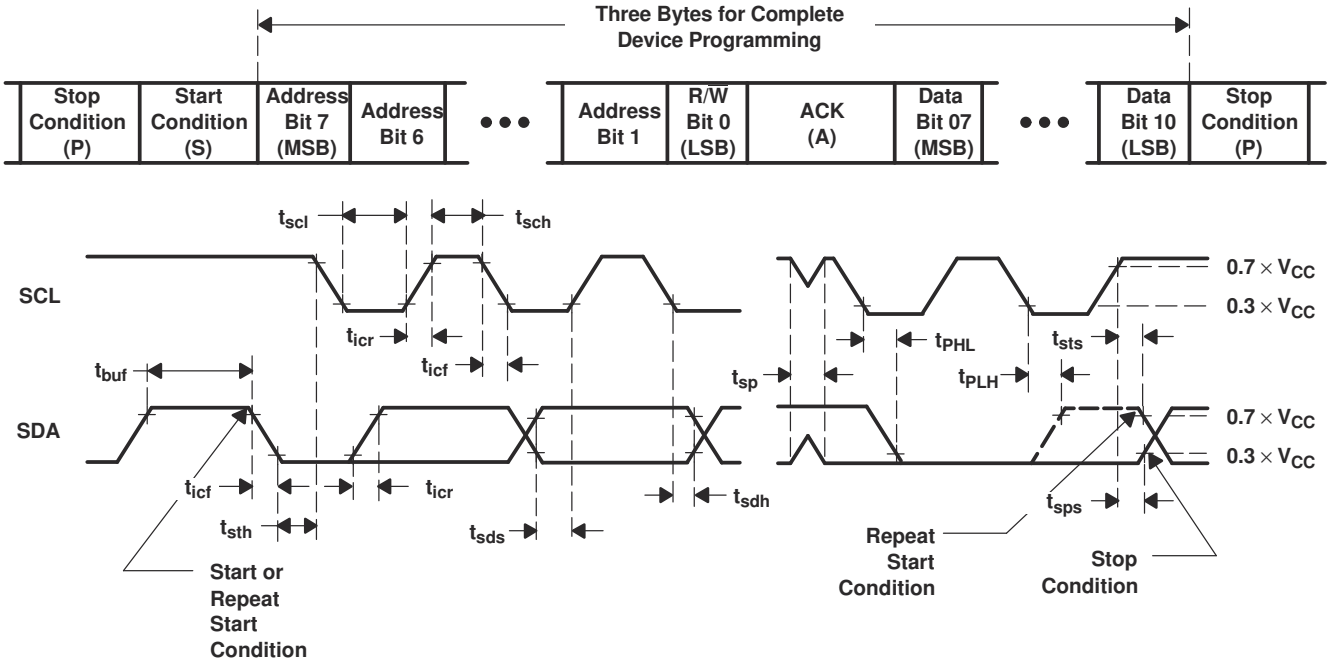


図 7-18. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

8 Parameter Measurement Information



SDA LOAD CONFIGURATION

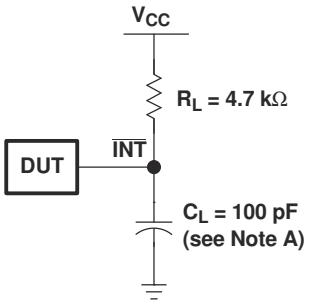


VOLTAGE WAVEFORMS

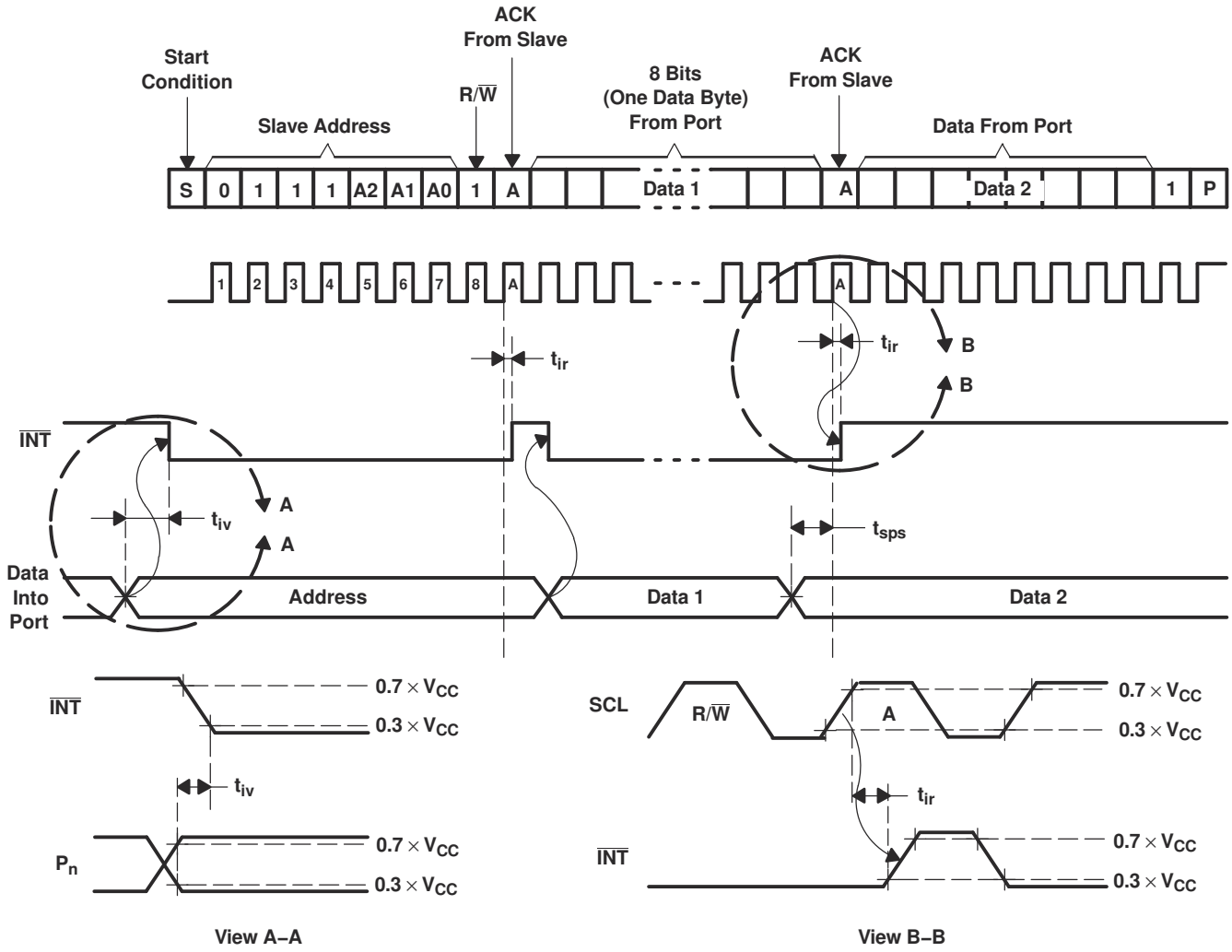
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 8-1. I^2C Interface Load Circuit And Voltage Waveforms

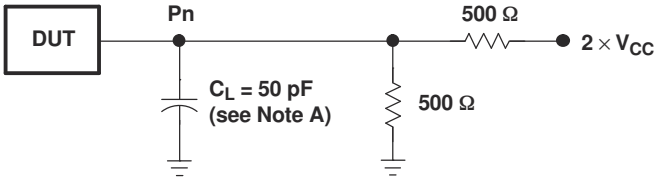


INTERRUPT LOAD CONFIGURATION

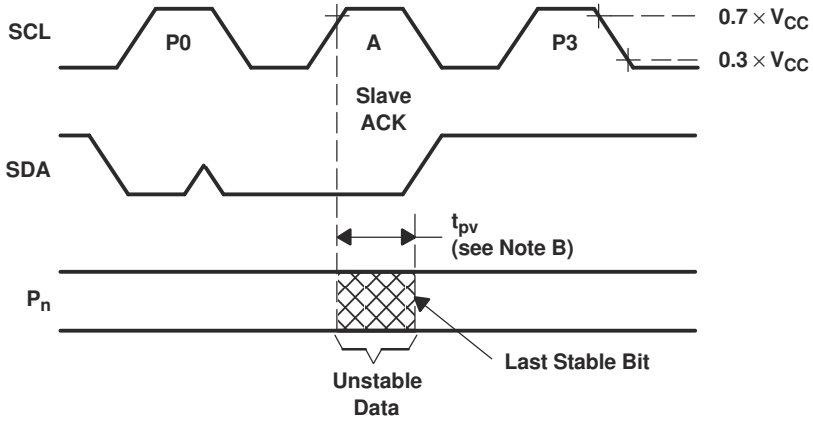


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

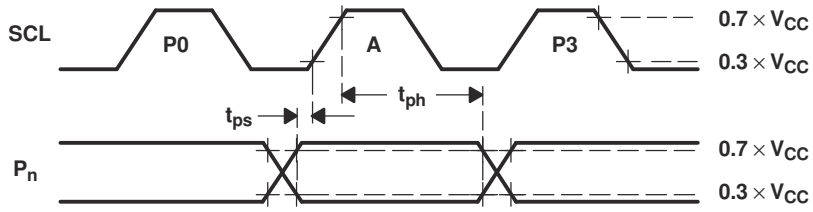
図 8-2. Interrupt Load Circuit And Voltage Waveforms



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



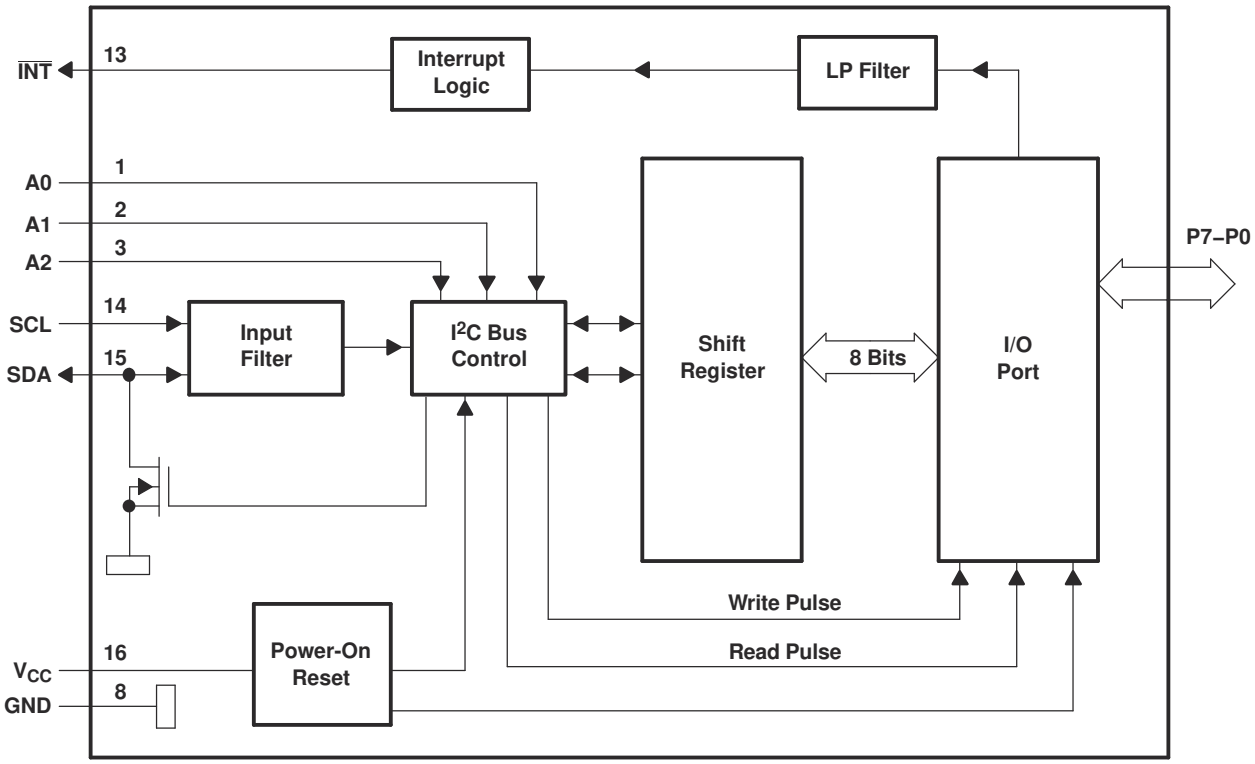
READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 8-3. P-Port Load Circuit And Voltage Waveforms

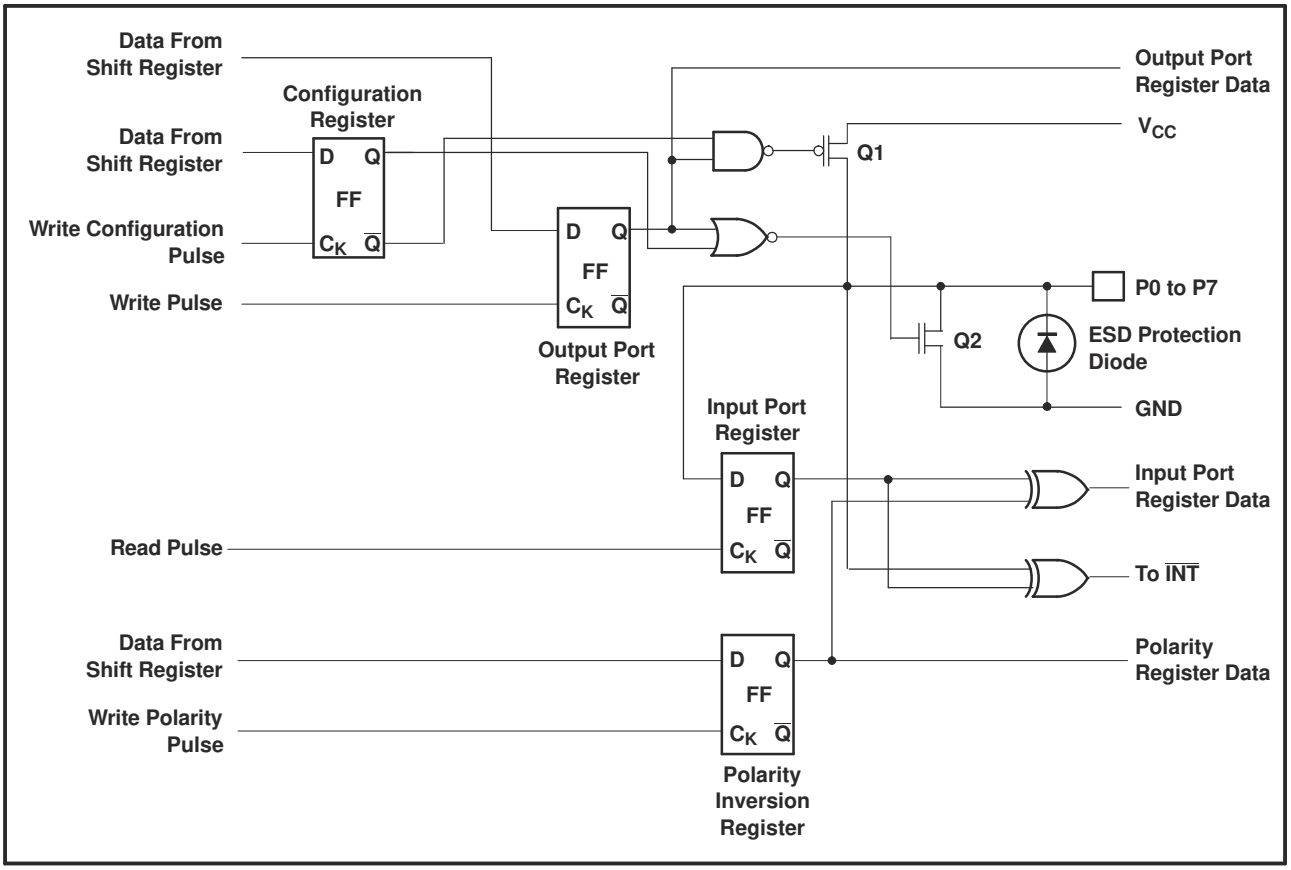
9 Detailed Description

9.1 Functional Block Diagram



A. Pin numbers shown are for DB, DBQ, DGV, DW, or PW package.
B. All I/Os are set to inputs at reset.

図 9-1. Logic Diagram (Positive Logic)



A. At power-on reset, all registers return to default values.

図 9-2. Simplified Schematic Of P0 To P7

9.2 Device Functional Modes

9.2.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9534A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9534A registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

9.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 図 9-2) are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

9.2.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an

interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

9.2.3.1 Interrupt Errata

9.2.3.1.1 Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^2C command byte (register pointer) written to the device was 00h.

Note

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^2C bus acknowledges an address byte with the R/W bit set high

9.2.3.1.2 System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

9.2.3.1.3 System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9534A device or before reading from another slave device.

Note

Software change will be compatible with other versions (competition and TI redesigns) of this device.

9.3 Programming

9.3.1 I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 図 9-3). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see 図 9-4).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 図 9-3).

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 9-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

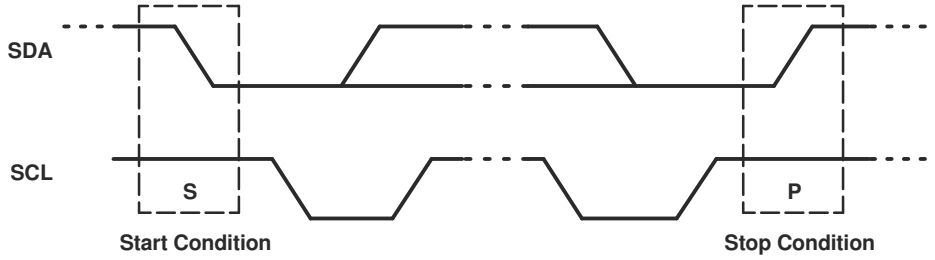


図 9-3. Definition Of Start And Stop Conditions

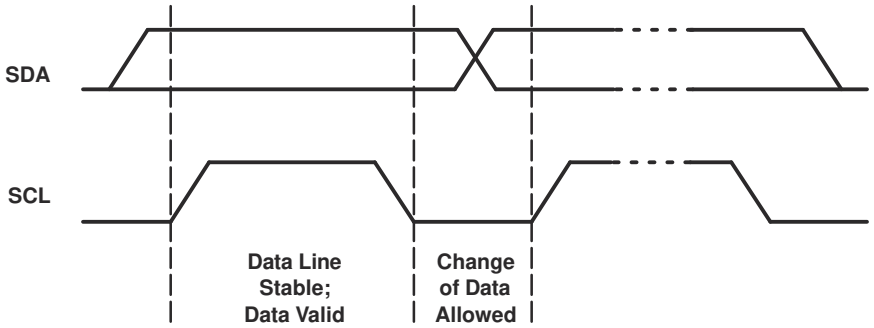


図 9-4. Bit Transfer

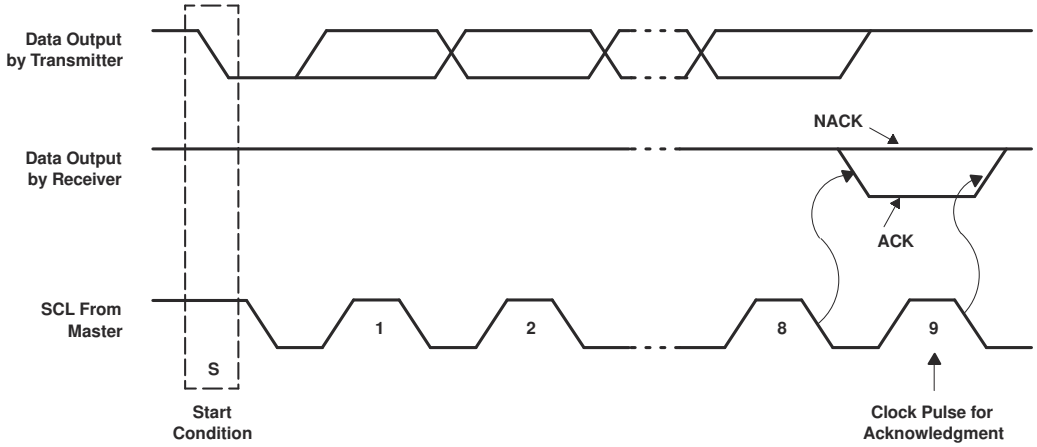


図 9-5. Acknowledgment On I^2C Bus

9.3.2 Register Map

表 9-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	H	H	A2	A1	A0	R/ $\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

9.3.2.1 Device Address

図 9-6 shows the address byte of the PCA9534A.

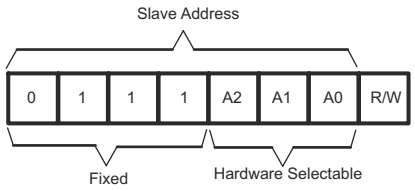


図 9-6. Pca9534a Address

表 9-2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

9.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte which is stored in the control register in the PCA9534A. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	0	B1	B0

図 9-7. Control Register Bits

表 9-3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

9.3.2.3 Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the input port register will be accessed next.

表 9-4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

表 9-5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

表 9-6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

表 9-7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

9.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9534A through write and read commands.

9.3.2.4.1 Writes

Data is transmitted to the PCA9534A by sending the device address and setting the least-significant bit to a logic 0 (see 図 9-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see 図 9-8 and 図 9-9). There is no limitation on the number of data bytes sent in one write transmission.

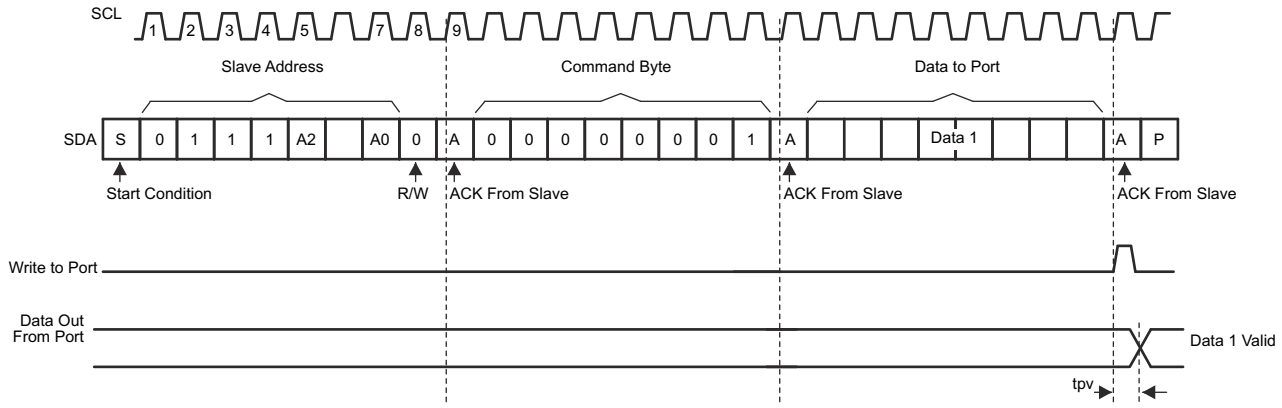


図 9-8. Write To Output Port Register

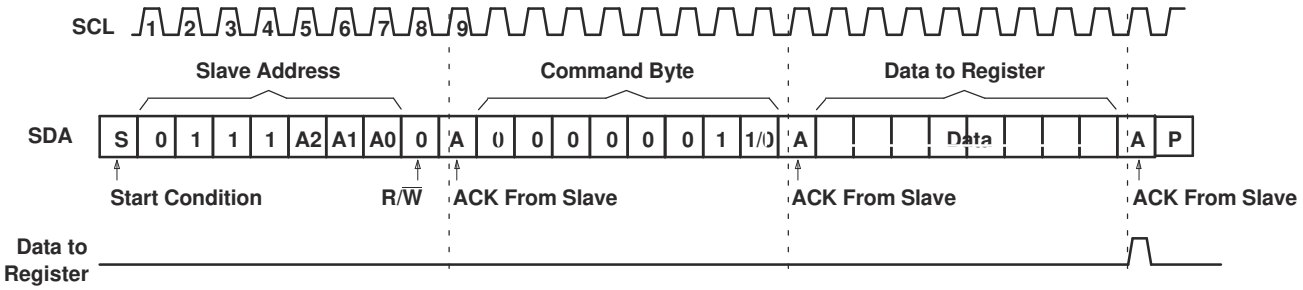


図 9-9. Write To Configuration Or Polarity Inversion Registers

9.3.2.4.2 Reads

The bus master first must send the PCA9534A address with the least-significant bit set to a logic 0 (see 図 9-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9534A (see 図 9-10 and 図 9-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

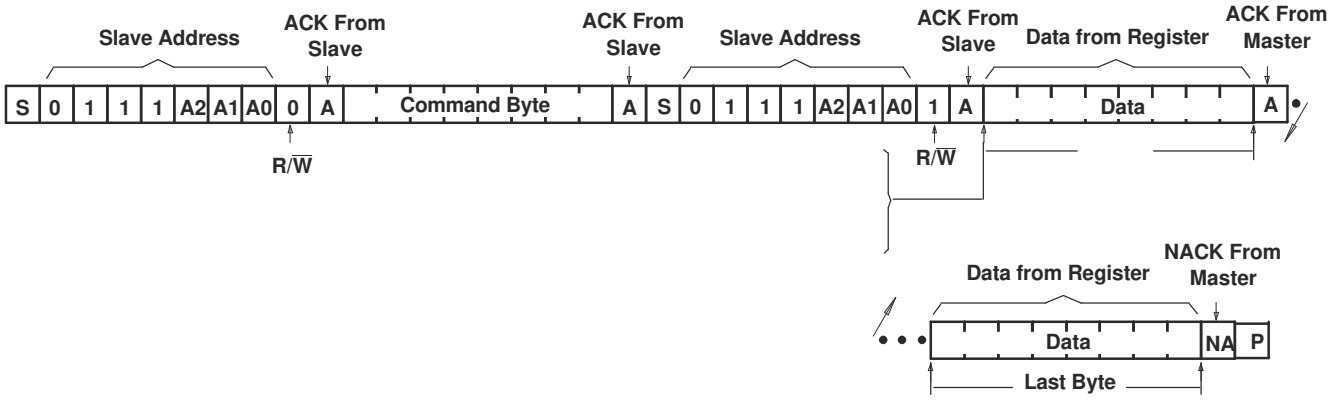
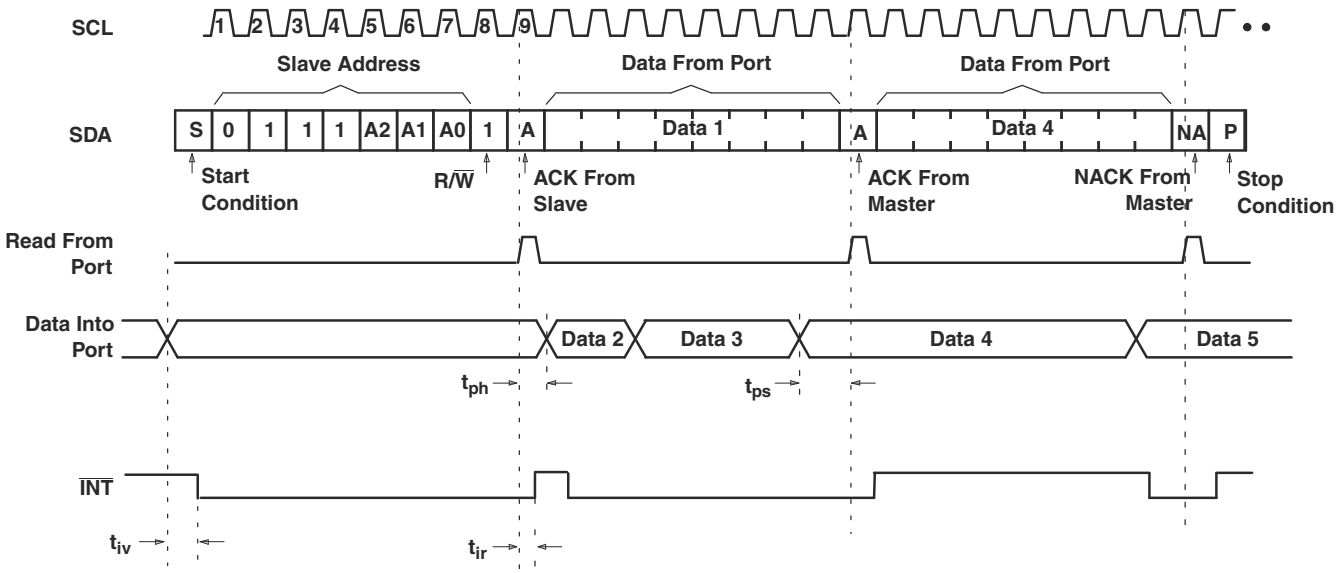


図 9-10. Read From Register



A. This figure assumes that the command byte has previously been programmed with 00h.
B. Transfer of data can be stopped at any moment by a stop condition.
C. This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and the actual data transfer from the P Port. See 図 9-10 for these details.

図 9-11. Read Input Port Register

10 Application Information Disclaimer

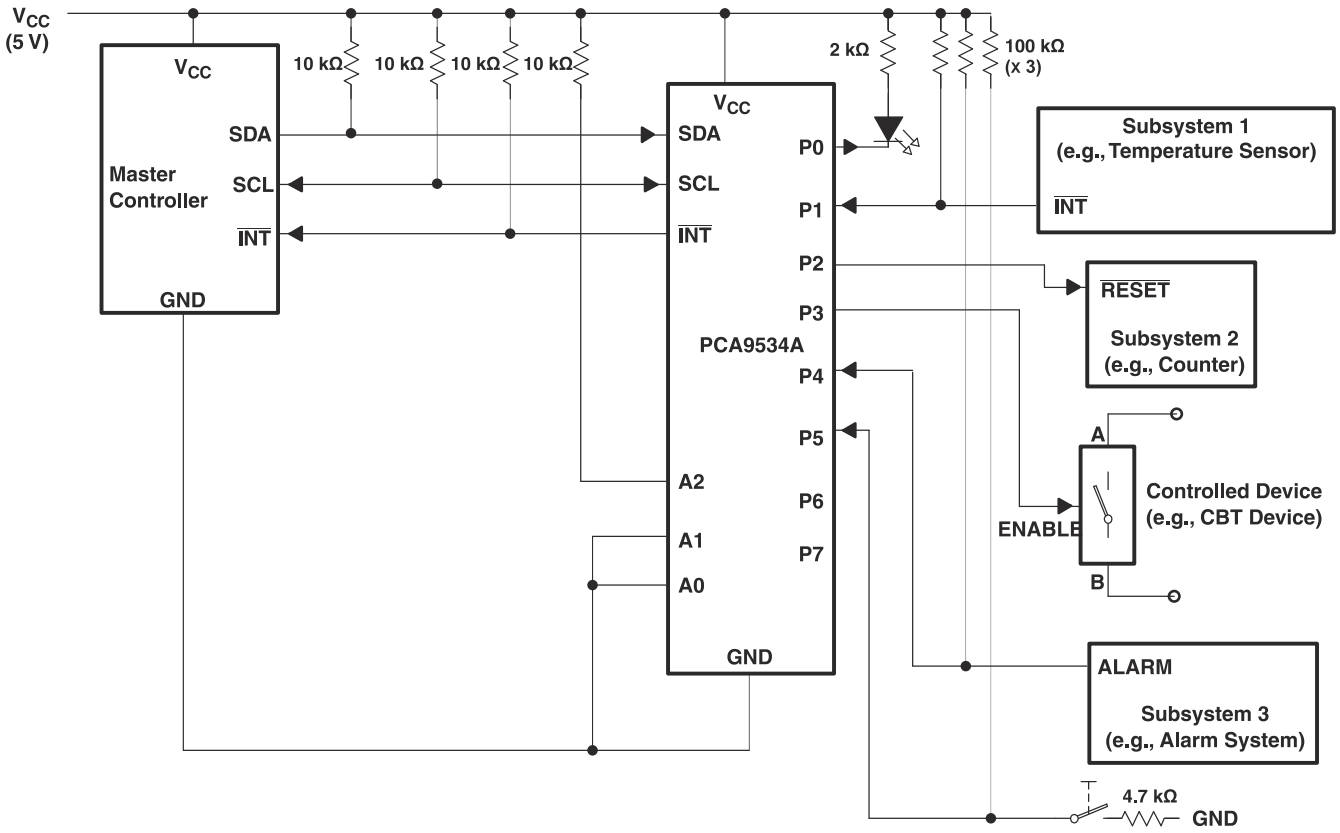
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Typical Application

図 10-1 shows an application in which the PCA9534A can be used.



A. Device address is configured as 0111100 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and must be configured as outputs.

図 10-1. Typical Application

10.1.1.1 Design Requirements

10.1.1.1.1 Minimizing I_{CC} When The I/O Controls Leds

When the I/Os are used to control LEDs, they normally are connected to V_{CC} through a resistor as shown in 図 10-1. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of the I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. 図 10-2 shows a high-value resistor in parallel with the LED. 図 10-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

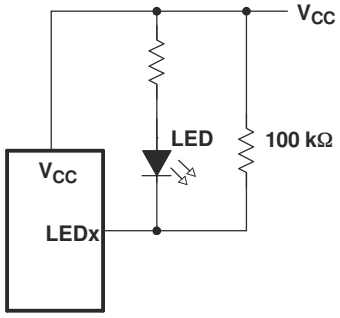


図 10-2. High-Value Resistor In Parallel With The Led

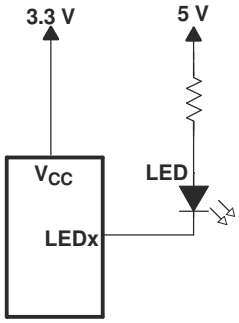


図 10-3. Device Supplied By A Lower Voltage

11 Power Supply Recommendations

11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9534A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 図 11-1 and 図 11-2.

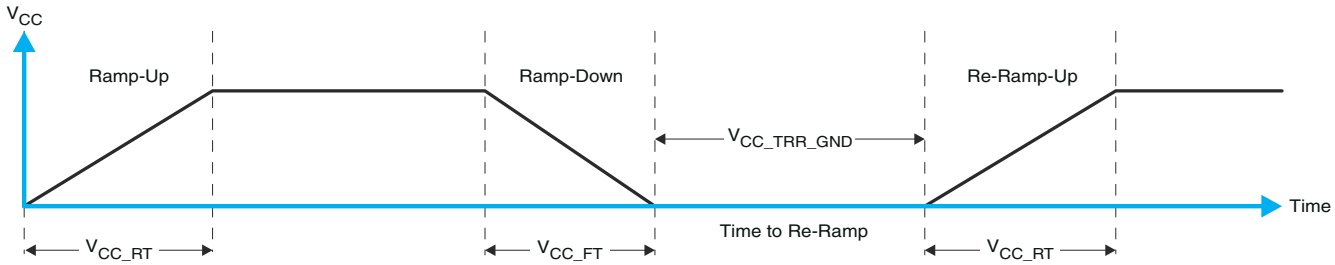


図 11-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

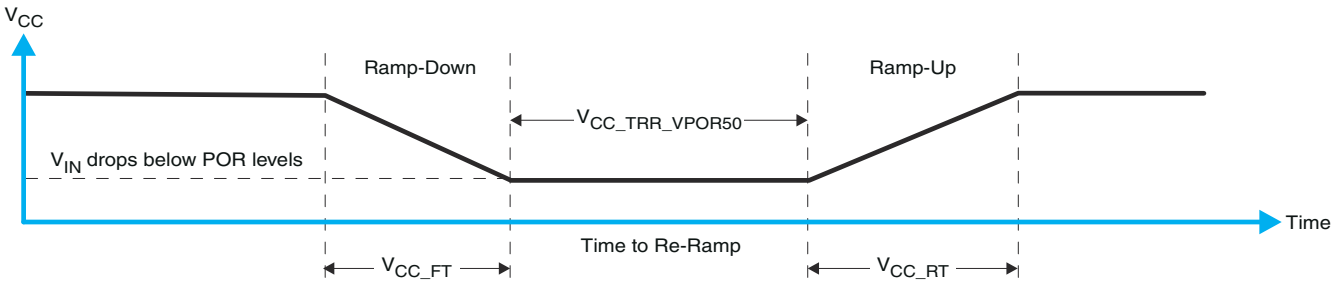


図 11-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 11-1 specifies the performance of the power-on reset feature for PCA9534A for both types of power-on reset.

表 11-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 11-1	1		100	ms
V_{CC_RT}	Rise rate	See 図 11-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 11-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 11-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See 図 11-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 11-3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 図 11-3 and 表 11-1 provide more information on how to measure these specifications.

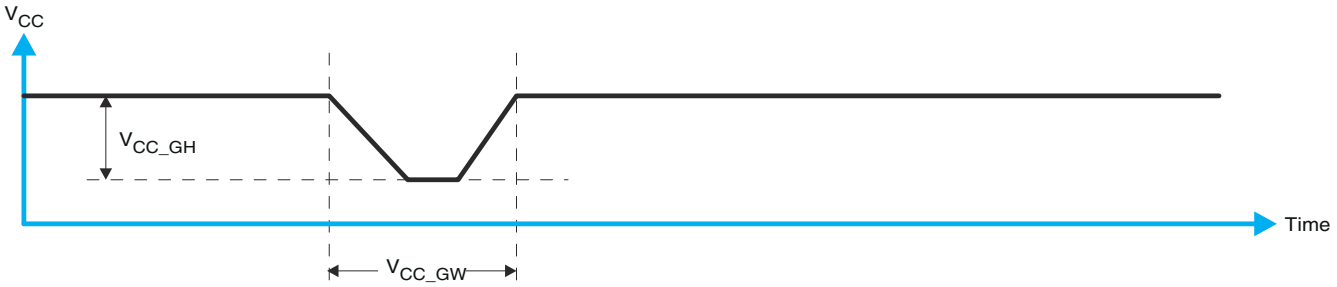


図 11-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 11-4 and 表 11-1 provide more details on this specification.

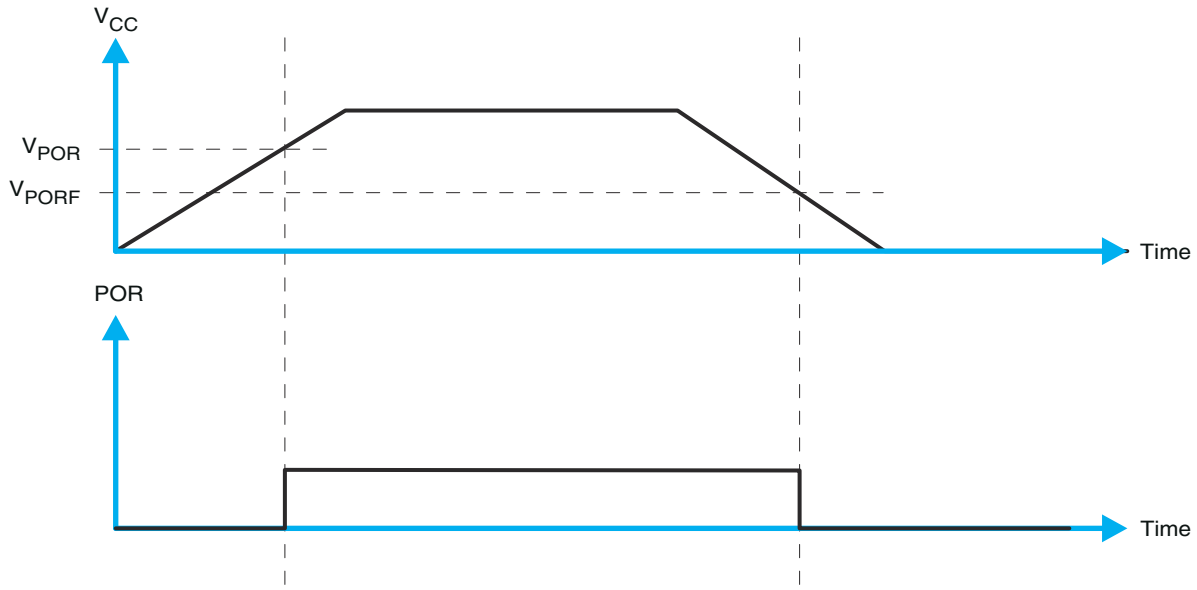


図 11-4. V_{POR}

12 Device and Documentation Support

12.1 Trademarks

すべての商標は、それぞれの所有者に帰属します。

12.2 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.3 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9534ADB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	
PCA9534ADWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	
PCA9534APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVJ	Samples
PCA9534ARGTRG4	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVJ	Samples
PCA9534ARGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD534A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

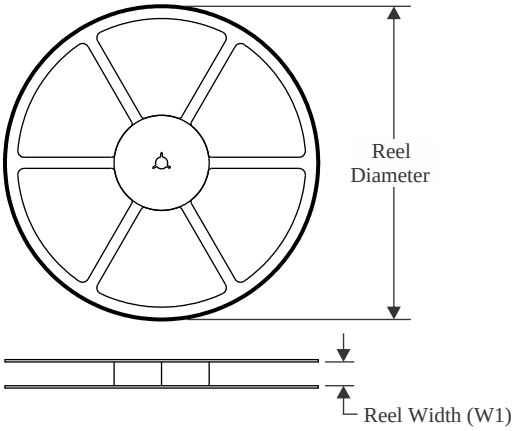
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

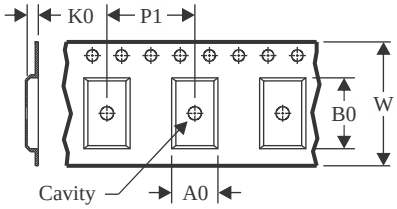
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

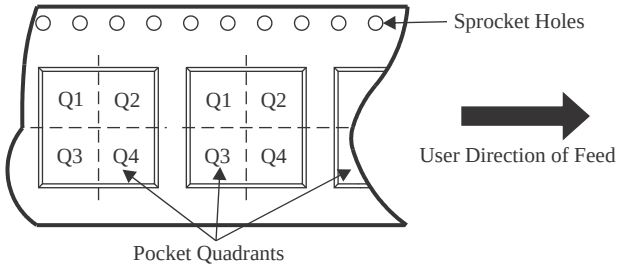


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

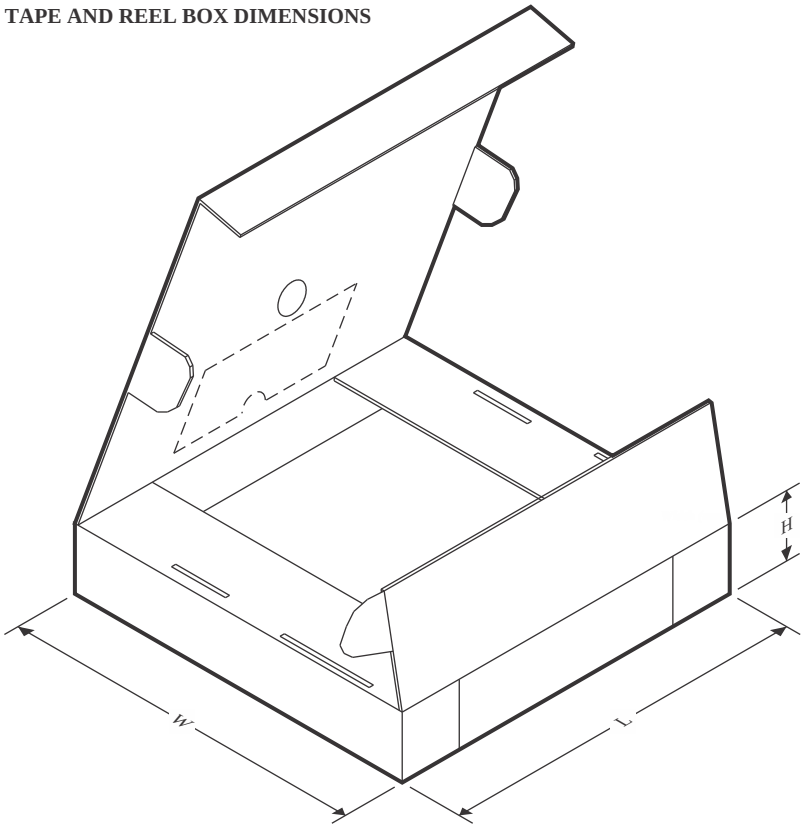
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9534ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
PCA9534ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9534ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9534APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9534APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9534ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9534ARGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

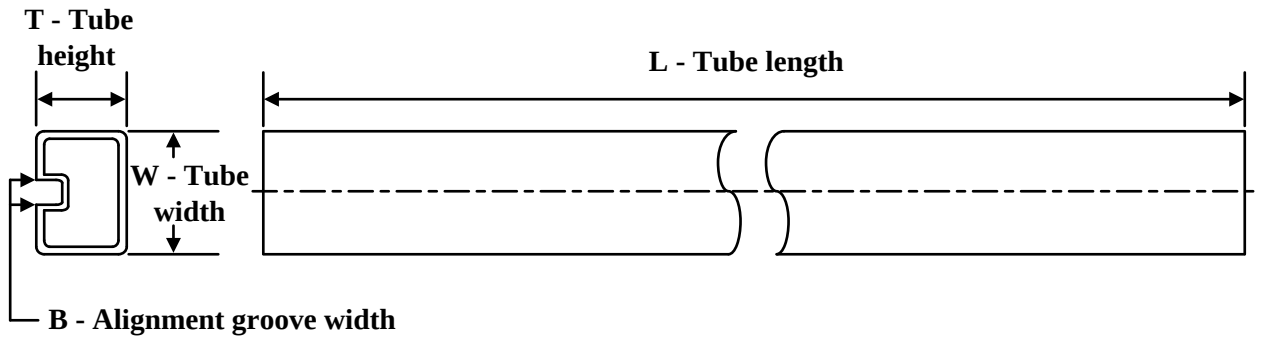
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9534ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
PCA9534ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
PCA9534ADWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCA9534APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9534APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9534ARGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
PCA9534ARGVR	VQFN	RGV	16	2500	356.0	356.0	35.0

TUBE

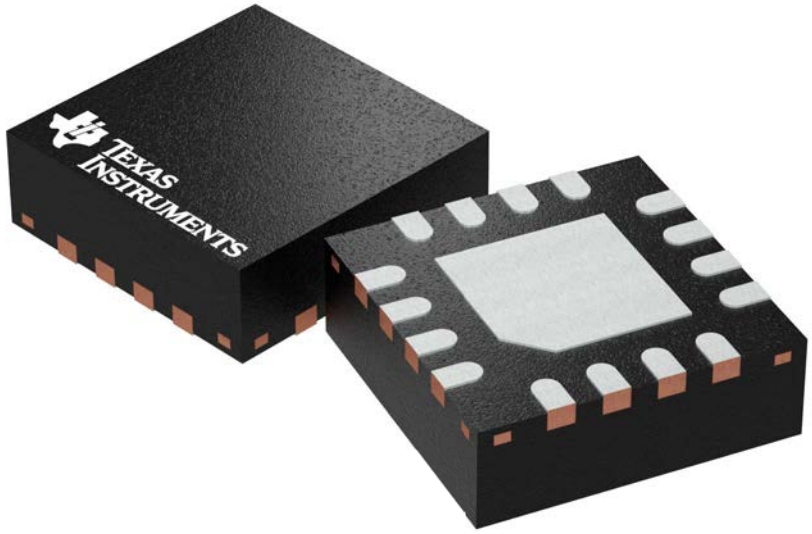


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9534ADB	DB	SSOP	16	80	530	10.5	4000	4.1
PCA9534ADW	DW	SOIC	16	40	506.98	12.7	4826	6.6

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



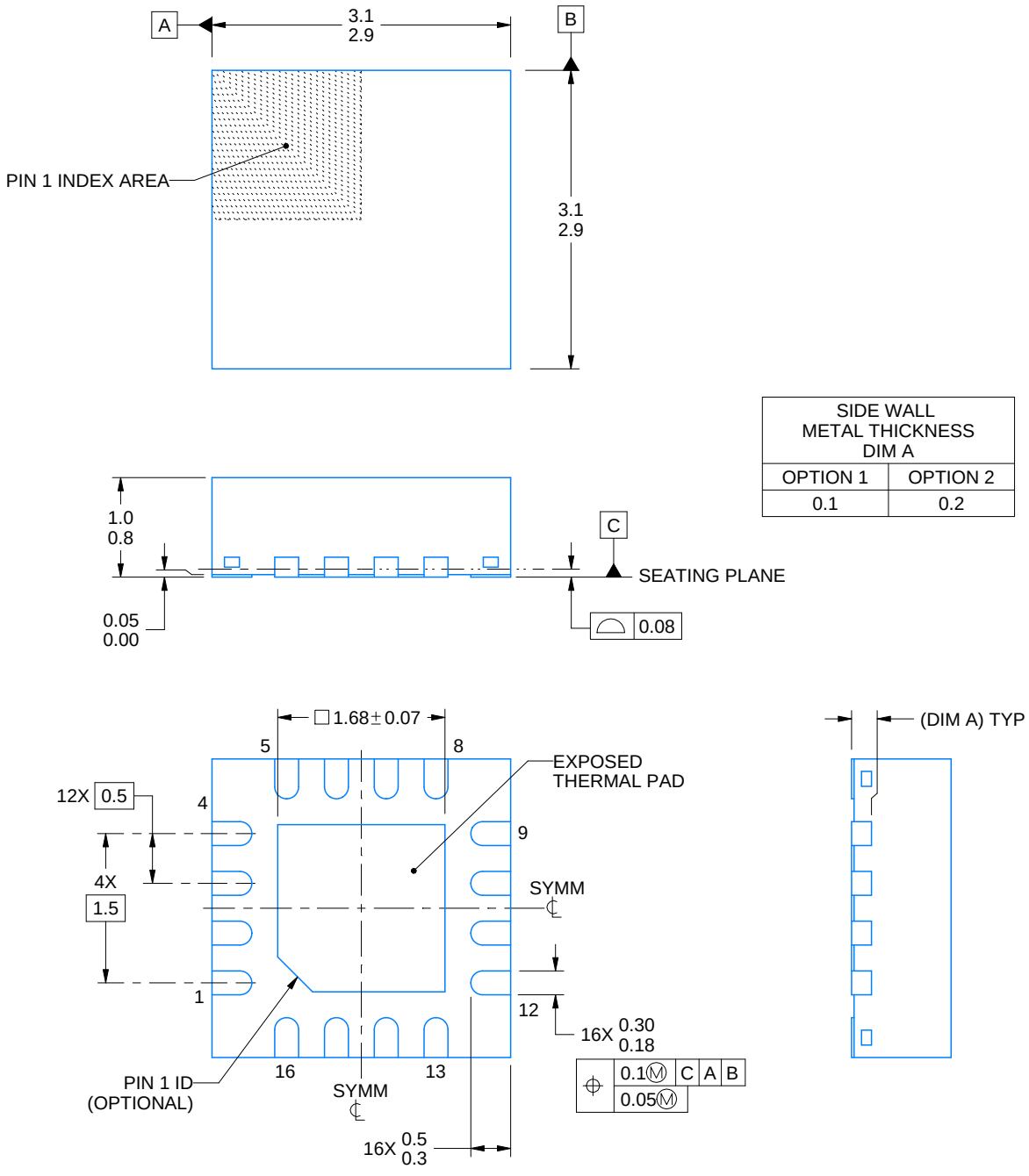
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

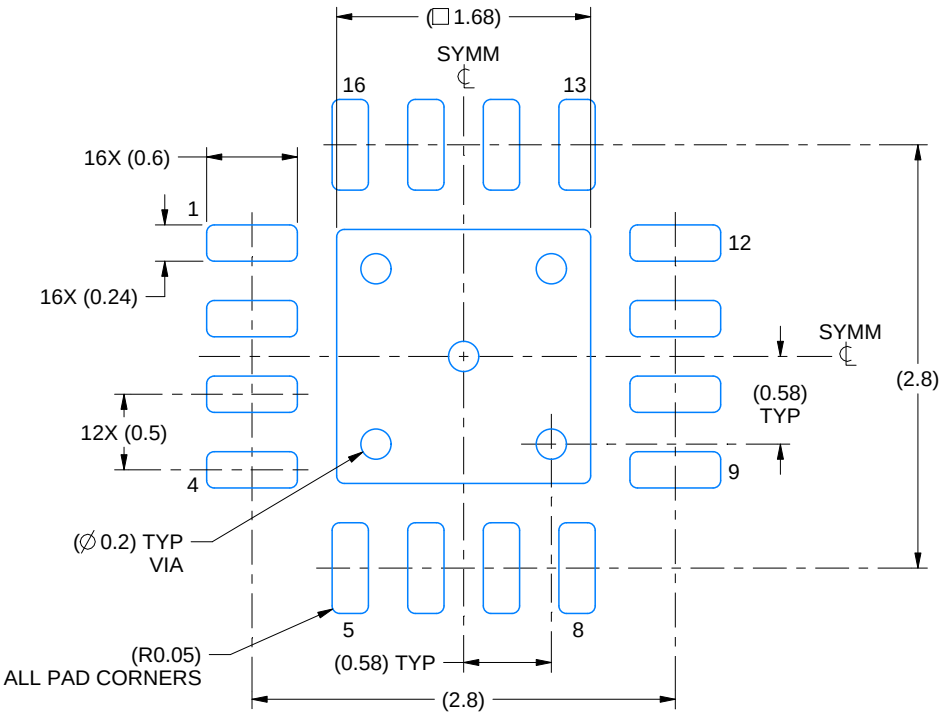
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

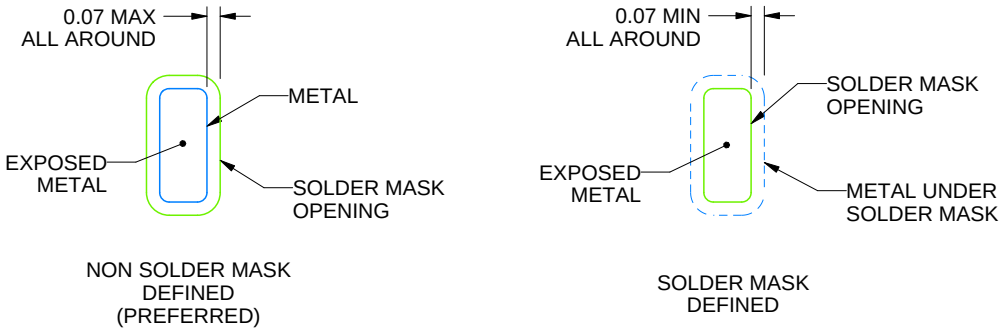


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

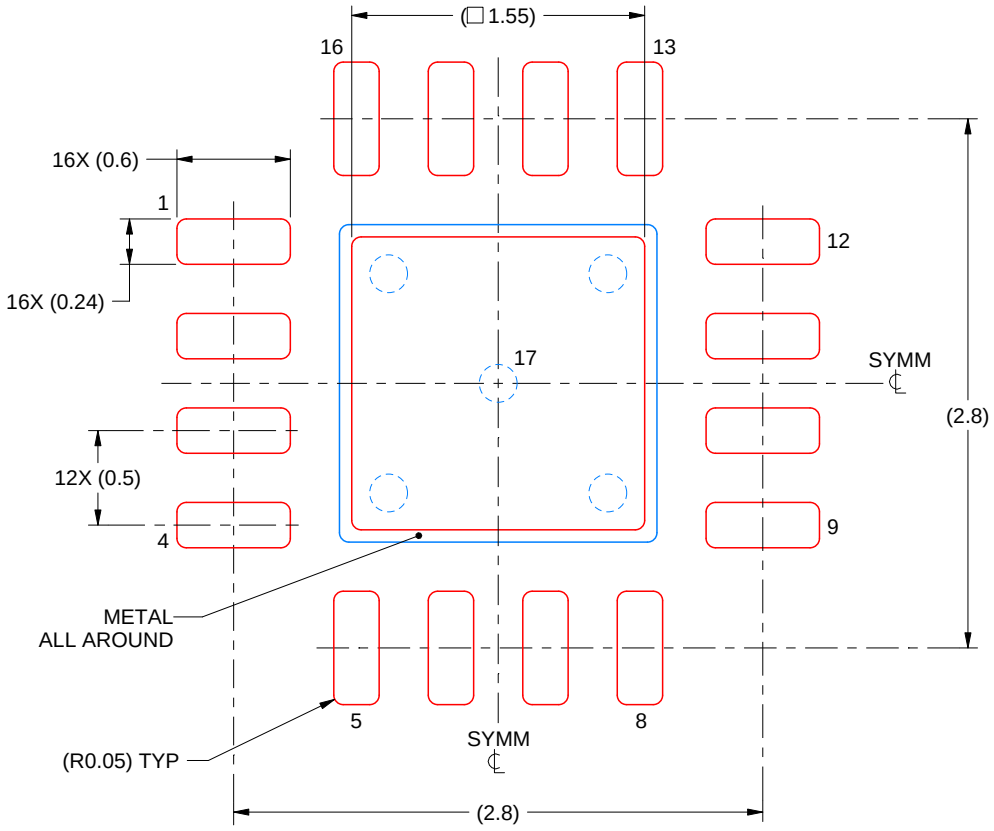


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

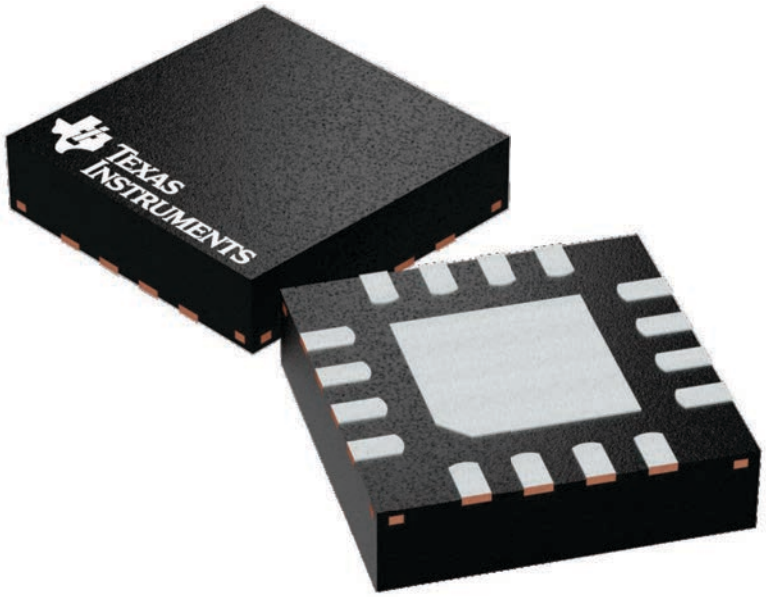
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

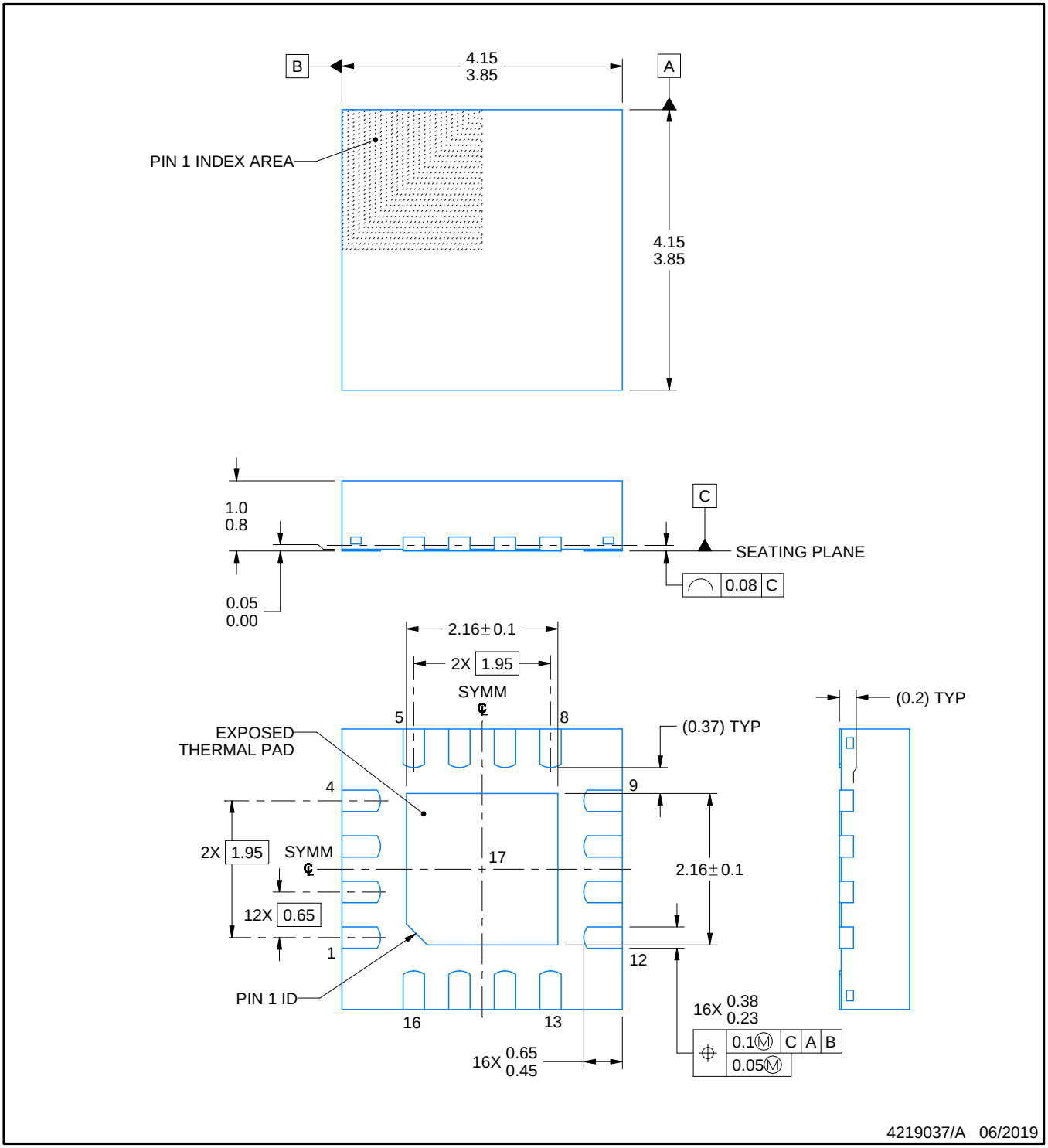
4224748/A

RGV0016A

PACKAGE OUTLINE

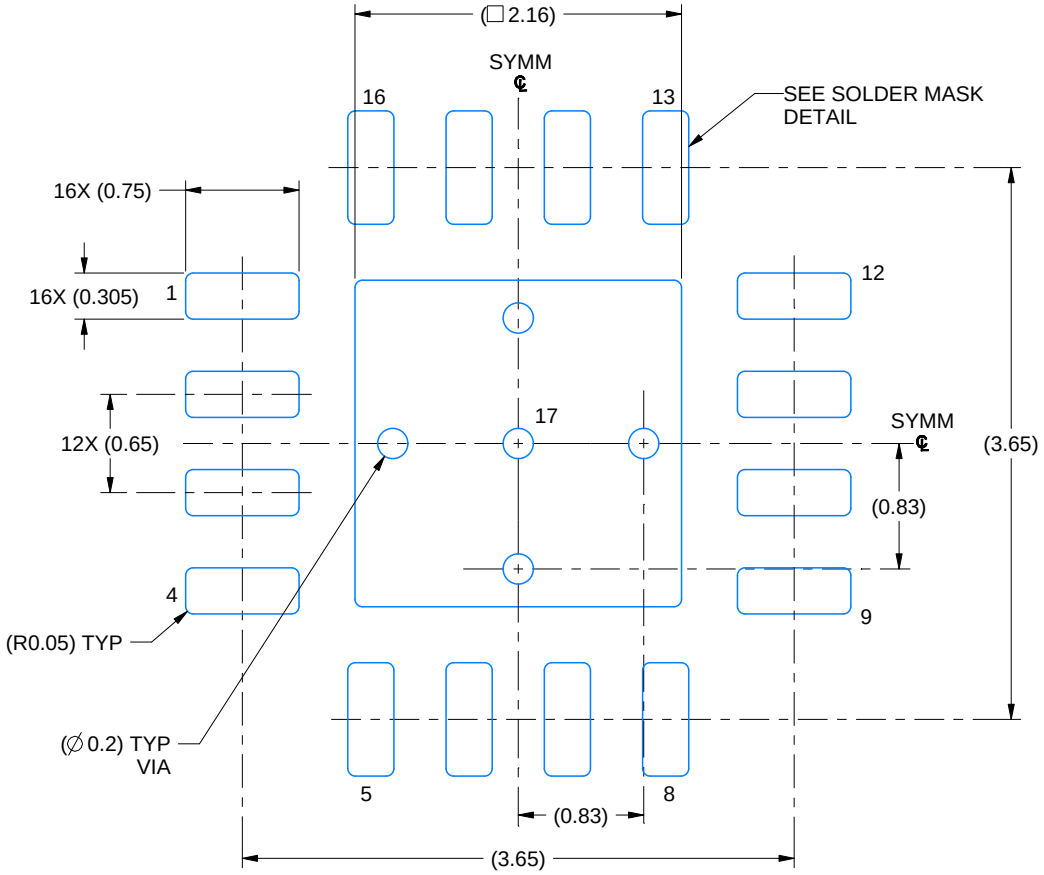
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

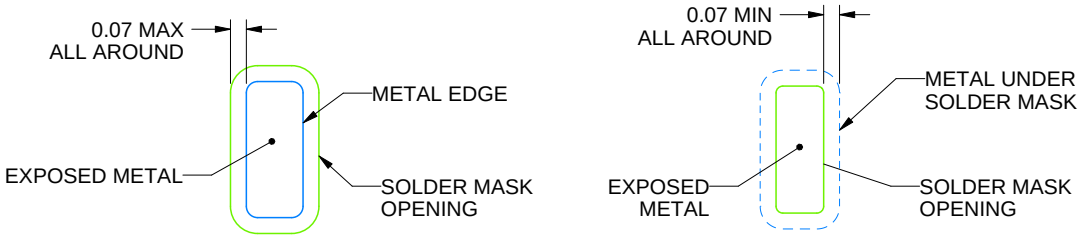


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

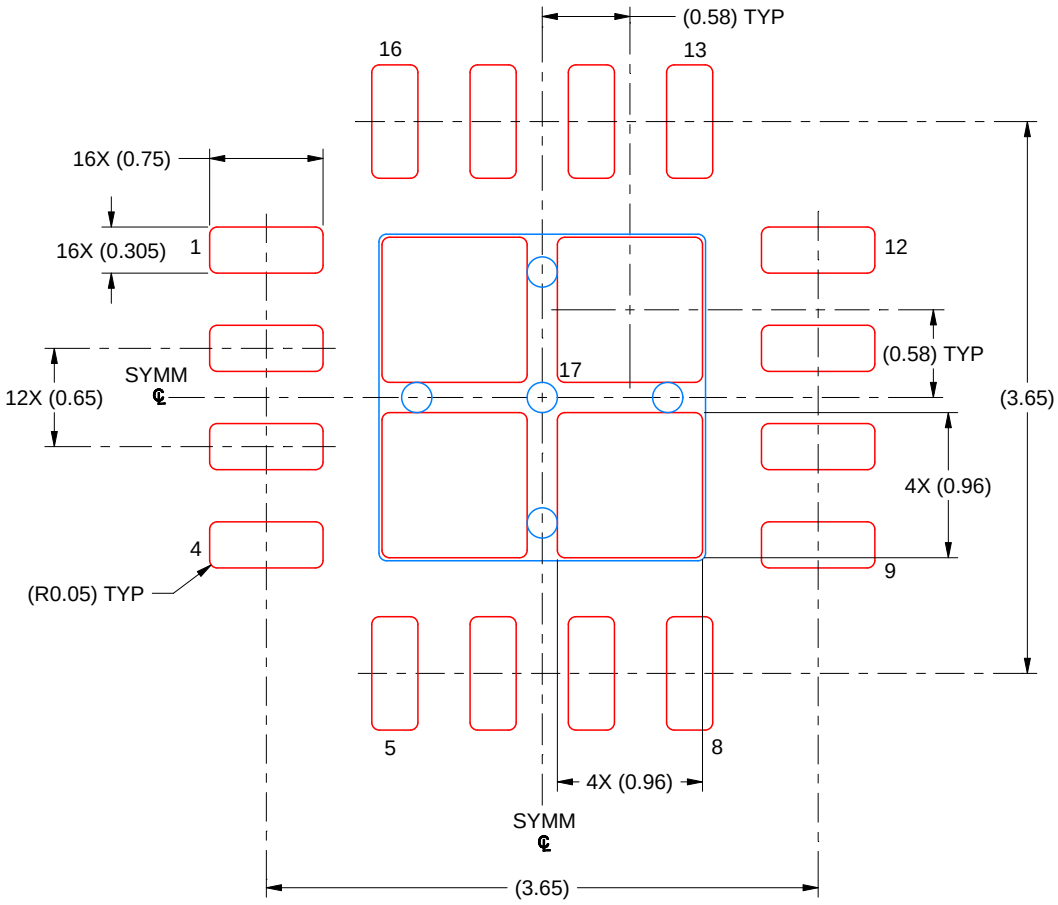
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

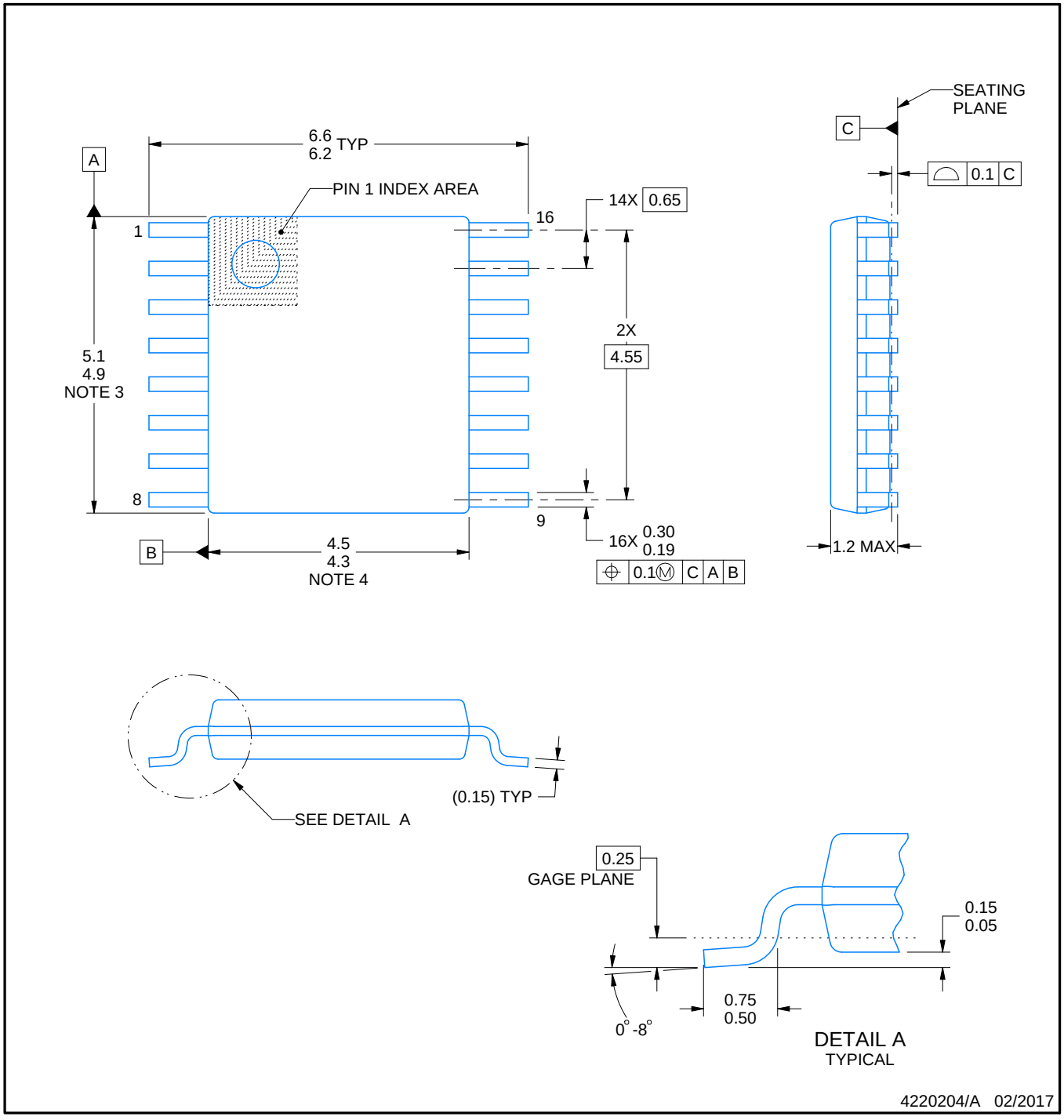
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

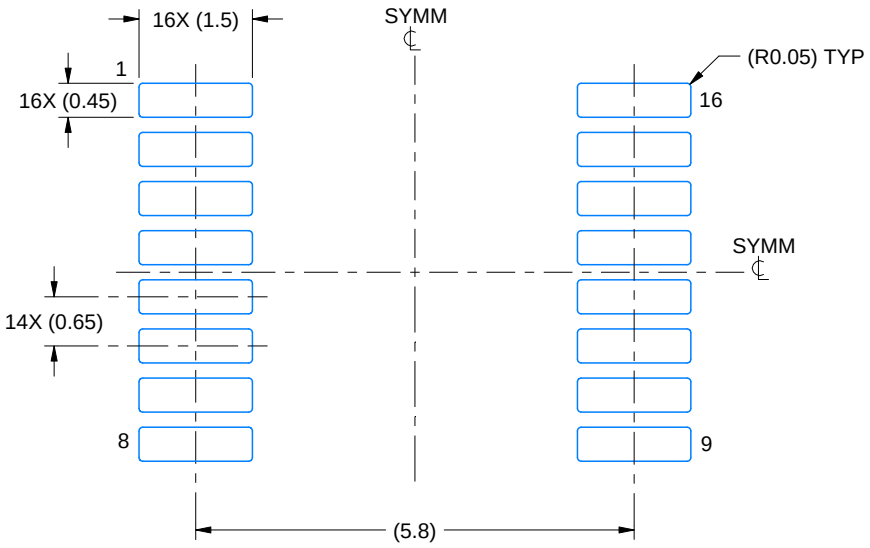
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

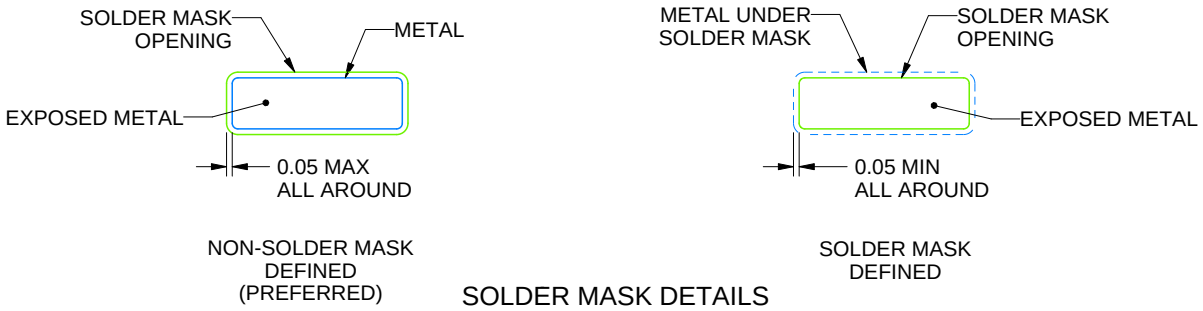


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

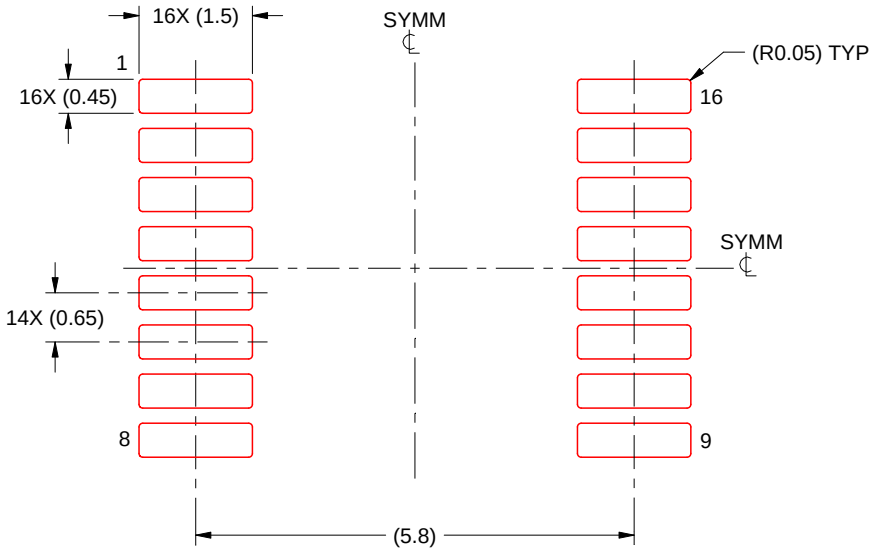


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

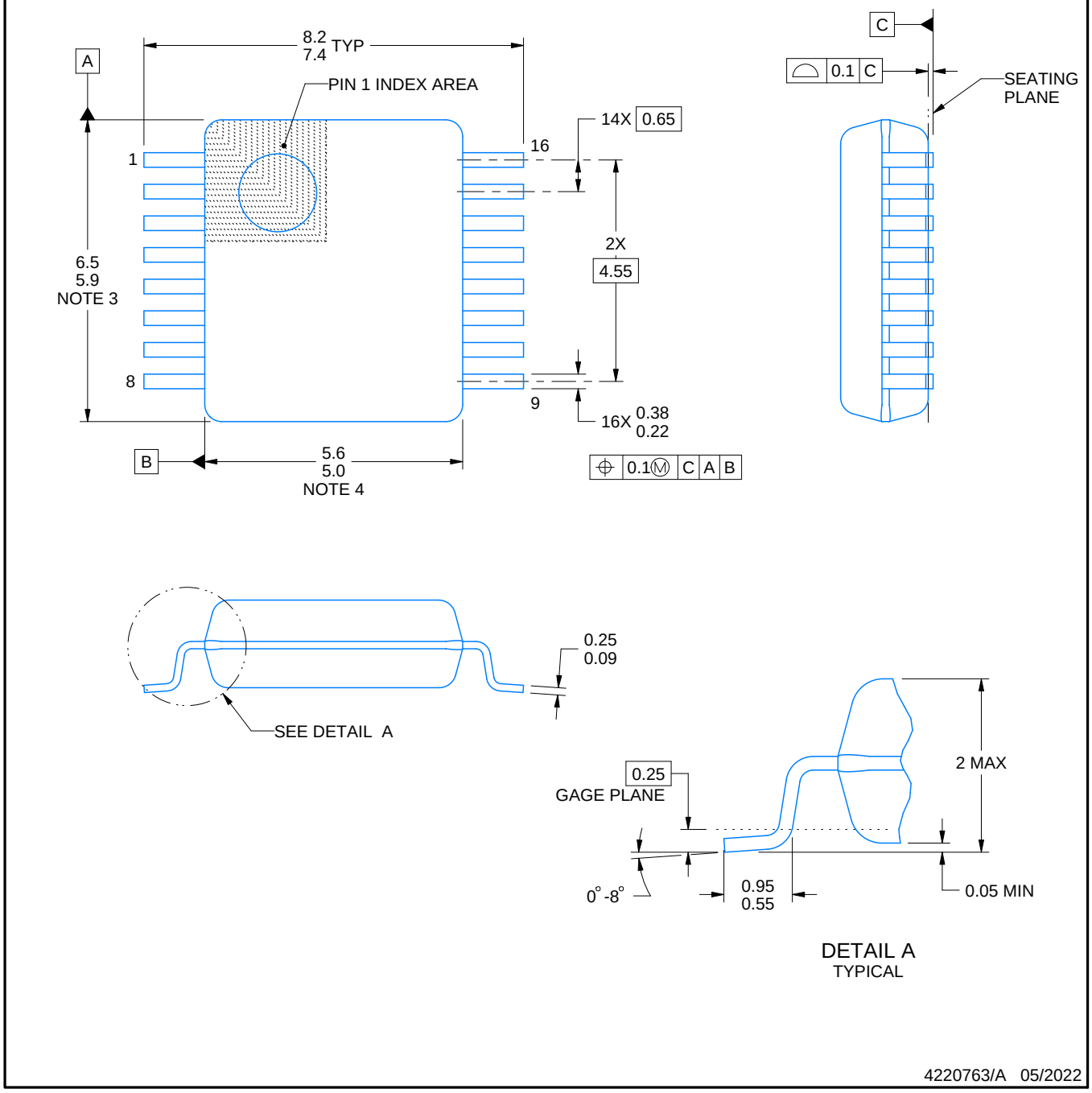
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

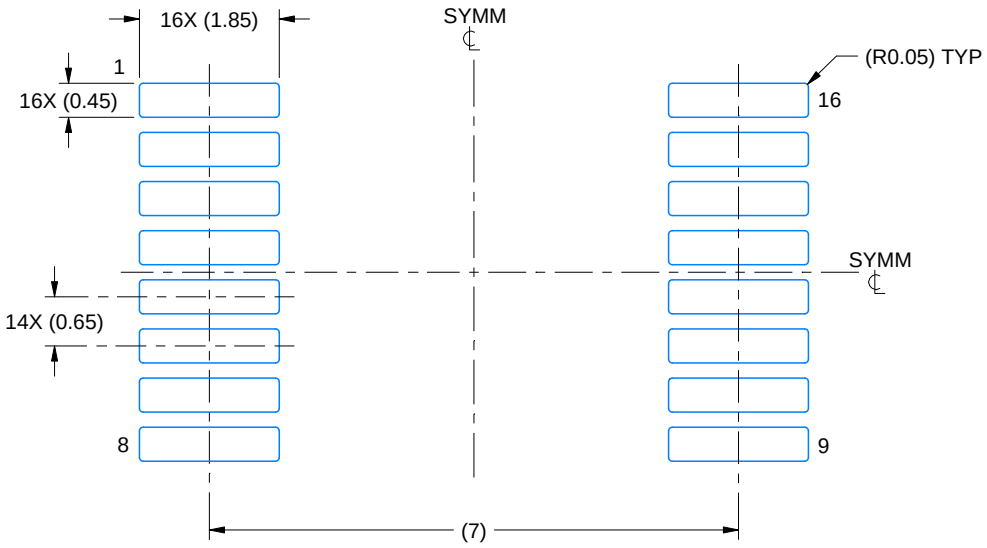
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

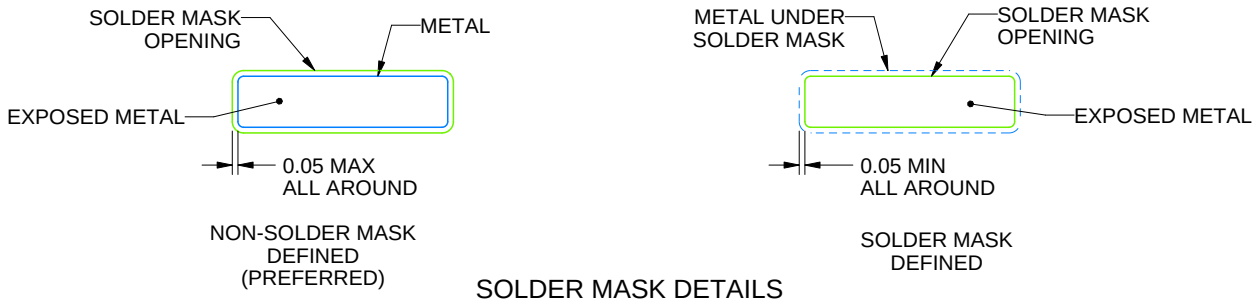


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

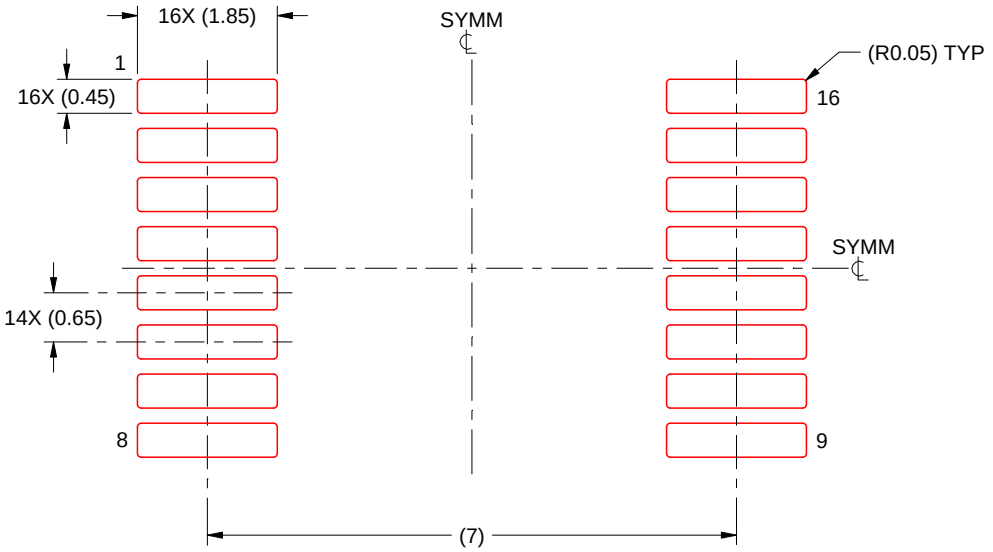


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

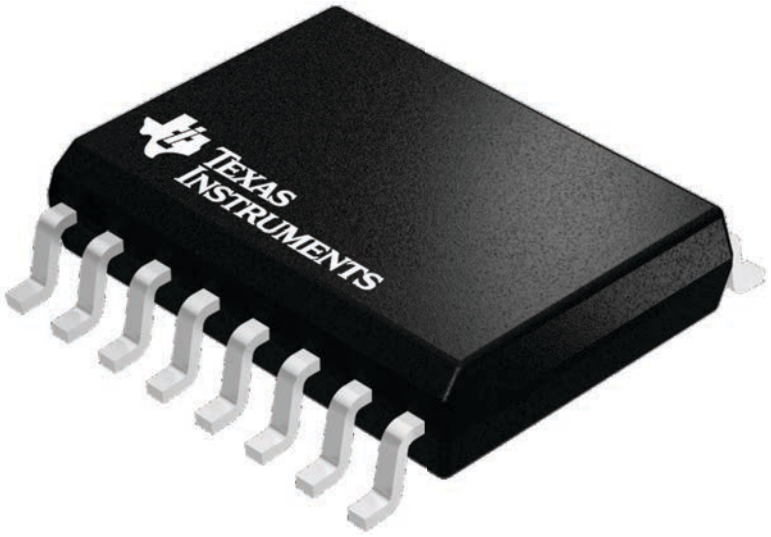
DW 16

SOIC - 2.65 mm max height

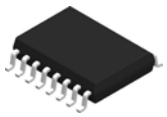
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

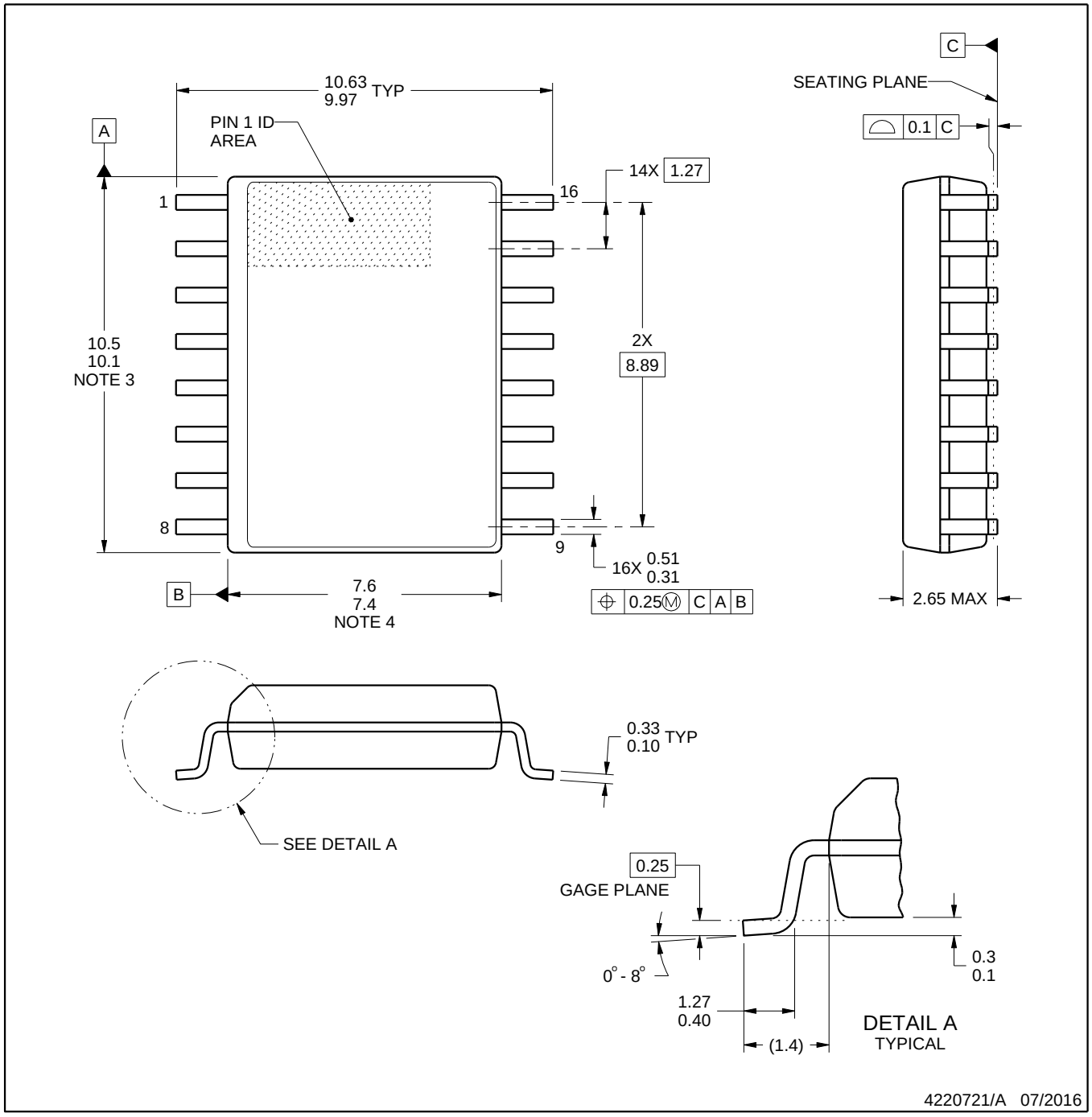


PACKAGE OUTLINE

DW0016A

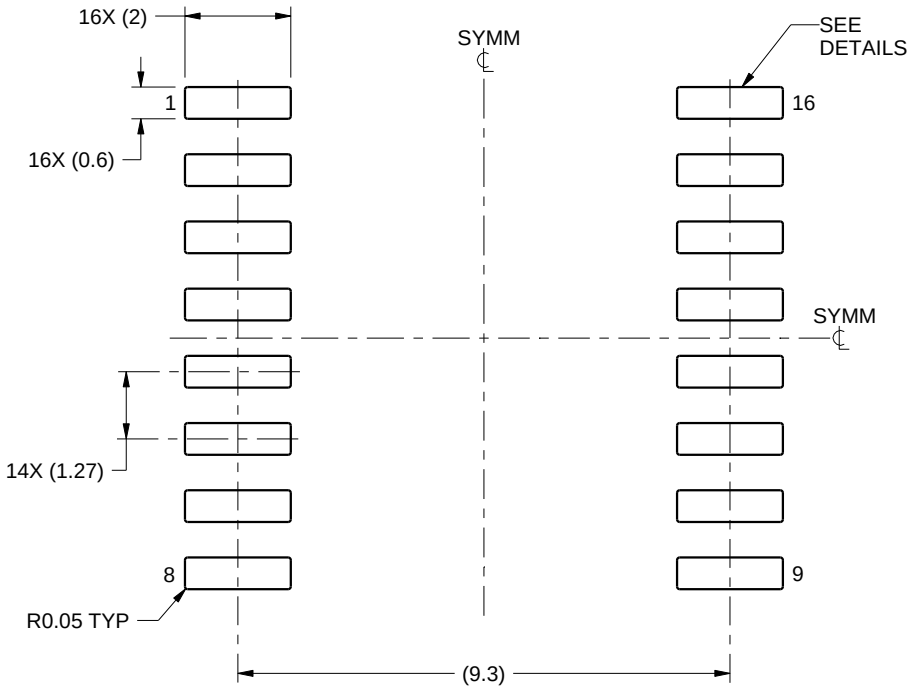
SOIC - 2.65 mm max height

SOIC

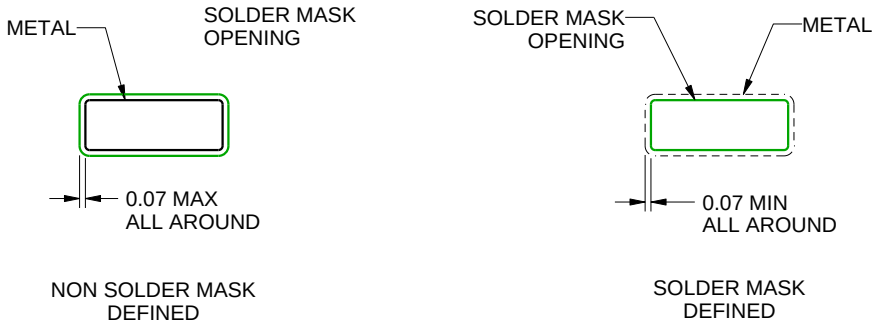


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

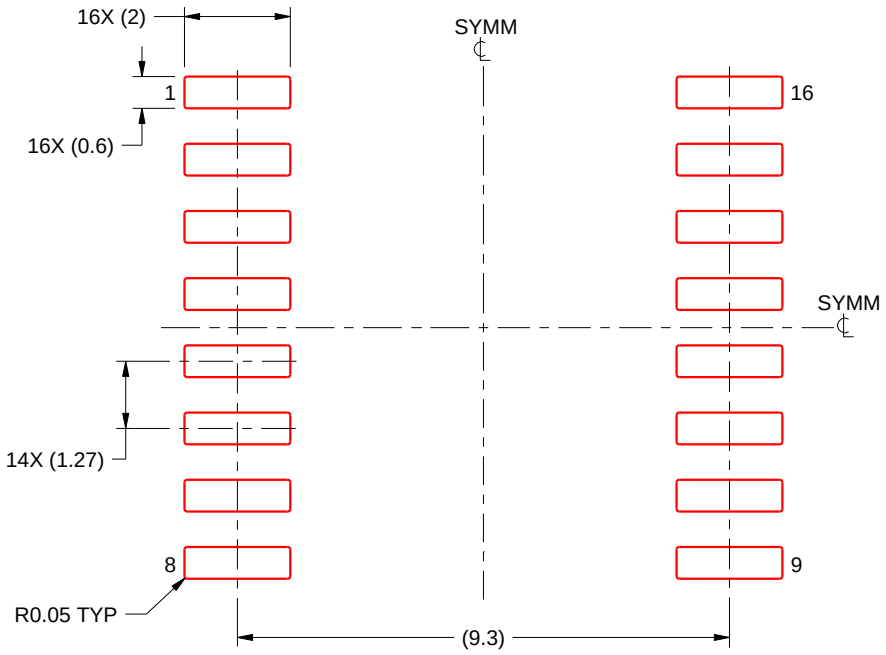


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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