RES11A マッチング済み、薄膜分割抵抗、1kΩ 入力

1 特長

- 広い温度範囲：-40℃～+125℃
- 高比率マッチング精度：±0.05% (最大値)
- 低いドリフト：±2ppm/℃ TCR (最大値)

2 アプリケーション

- 高精度電圧分割器、高精度レベル変換
- ゲインおよび減衰アンプ
- CMRR の高い差動アンプ
- ゲイン精度の高いディスクリート計測アンプ
- ゲイン精度の高い完全差動アンプ
- ピンポイントのコンパレータ スレッショルド設定

3 概要

RES11A は、マッチングされた抵抗分割器のペアで、テキサス・インスツルメンツの最新の高性能アナログ CMOS プロセスで薄膜 SiCr に実装されています。このデバイスは、熱および電流ノイズを低減するための公称入力抵抗が 1kΩ であり、幅広いシステムの要求を満たすため、いくつかの公称比率で供給されます。RES11A は、デバイスの配置を 180° 回転させるだけで、ゲインを反転した構成で使用できます。この機能により、レイアウトの再利用がサポートされ、ディスクリート計測機器や差動アンプの実装などのアプリケーションで柔軟性が向上します。

RES11A シリーズは高い比率マッチング精度を特長としており、各分割器の測定比率は公称値の ±120 ppm (標準値) 以内です。この精度は温度範囲全体にわたって維持され、最大比ドリフトはわずか ± 2ppm/℃です。さらに、デバイスのバイアスされた長期安定性は、徹底的な特性評価によって証明されています。

RES11A は、-40℃～+125℃の温度範囲で動作が規定されています。このデバイスは 8 ピンの SOT-23-THIN パッケージで供給され、本体サイズは 2.9mm × 1.6mm です (本体サイズは公称値であり、ピンは含まれていません)。

パッケージ情報

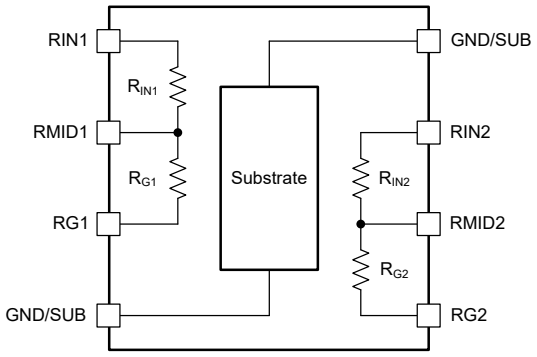
部品番号	パッケージ (1)	パッケージ サイズ (2)
RES11A	DDF (SOT-23-THIN、8)	2.9mm × 2.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

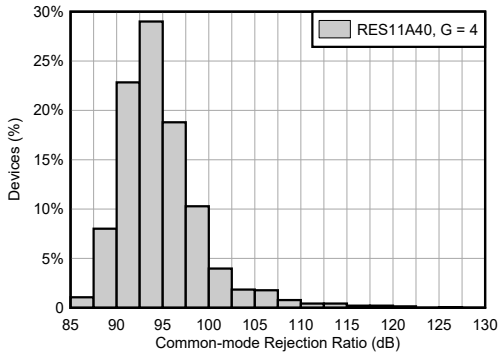
製品情報

部品番号	公称比
RES11A10	1：1
RES11A15 (1)	1：1.5
RES11A16 (1)	1：1.667
RES11A20 (1)	1：2
RES11A25 (1)	1：2.5
RES11A30 (1)	1：3
RES11A40	1：4
RES11A50 (1)	1：5
RES11A90	1：9
RES11A00	1：10

(1) プレビュー情報 (事前情報ではありません)。



機能ブロック図



最高の CMRR を実現する優れた比率マッチング

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4 Pin Configuration and Functions

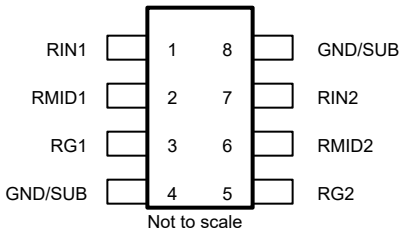


図 4-1. DDF Package, 8-Pin SOT-23-THN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND/SUB	4, 8	Ground	Substrate bias connection. Only bias one GND/SUB pin. Float the other GND/SUB pin to prevent current return paths from forming through the substrate. See also セクション 7.4.
RG1	3	Input	Gain resistor connection for divider 1
RG2	5	Input	Gain resistor connection for divider 2
RIN1	1	Input	Input resistor connection for divider 1
RIN2	7	Input	Input resistor connection for divider 2
RMID1	2	Output	Center tap of divider 1
RMID2	6	Output	Center tap of divider 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CM}	Maximum common mode voltage (any pin to GND/SUB)			±135	V
ΔV_{DMAX}	Maximum instantaneous overload voltage per divider (RINx pin to RGx pin) (2)	RES11A10		±77.0	V
		RES11A15		±64.2	
		RES11A16		±63.0	
		RES11A20		±57.8	
		RES11A25		±89.9	
		RES11A30		±102.7	
		RES11A40		±96.3	
		RES11A50		±94.6	
		RES11A90		±128.4	
		RES11A00		±135	
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	175	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum instantaneous voltage permitted under transient conditions. Avoid sustained operation at these voltage levels because the resulting self-heating causes T_J to exceed 150°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1200	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Maximum common-mode voltage (any pin to GND/SUB)				±120	V
	Maximum sustained current through R_{INx} (RINx pin to RMIDx pin, 10 years at T_A = 25°C) (1)	RES11A10		±8.93	±12.2	mA
		RES11A15		±8.93	±12.2	
		RES11A16		±8.93	±12.5	
		RES11A20		±8.93	±12.2	
		RES11A25		±7.44	±10.2	
		RES11A30		±8.93	±12.2	
		RES11A40		±8.93	±12.2	
		RES11A50		±8.93	±12.5	
		RES11A90		±8.93	±12.2	
		RES11A00		±7.44	±10.2	
	Maximum sustained current through R_{Gx} (RGx pin to RMIDx pin, 10 years at T_A = 25°C) (1)	RES11A10		±8.93	±12.2	mA
		RES11A15		±5.95	±8.14	
		RES11A16		±5.36	±7.49	
		RES11A20		±4.47	±6.11	
		RES11A25		±5.95	±8.14	
		RES11A30		±5.95	±8.14	
		RES11A40		±4.47	±6.11	
		RES11A50		±3.57	±5.00	
		RES11A90		±2.98	±4.07	
		RES11A00		±2.98	±4.07	
T_A	Ambient temperature		–40		125	°C

(1) Assumes $R_{\theta JA}$ = 156.2 °C/W. Applies whether the specified current is applied across a *single* divider, or *both* dividers simultaneously. For long-term use under static dc biases, keep the current less than or equal to the nominal value. For long-term use under dynamic conditions, keep the RMS current less than or equal to the maximum value. Adhere to the limitations in *Absolute Maximum Ratings*.

5.4 Thermal Information

THERMAL METRIC(1)		RES11A DDF (SOT-23-THIN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INITIAL RESISTANCE							
G_{nom}	Nominal ratio (R_{Gx} / R_{INx})	RES11A10			1		V/V
		RES11A15			1.5		
		RES11A16			1.667		
		RES11A20			2		
		RES11A25			2.5		
		RES11A30			3		
		RES11A40			4		
		RES11A50			5		
		RES11A90			9		
		RES11A00			10		
t_{D1}	Ratio tolerance of divider 1 (1)	(R_{G1} / R_{IN1}) / G_{nom} – 1	RES11A10			±500	ppm
			RES11A15			±500	
			RES11A16			±500	
			RES11A20			±500	
			RES11A25			±500	
			RES11A30			±500	
			RES11A40		±120	±500	
			RES11A50			±500	
			RES11A90			±500	
			RES11A00			±500	
	Voltage-divider circuit tolerance of divider 1	(1 + G_{nom}) × (R_{IN1} / (R_{IN1} + R_{G1})) – 1	RES11A10			±500	ppm
			RES11A15			±500	
			RES11A16			±500	
			RES11A20			±500	
			RES11A25			±500	
			RES11A30			±500	
			RES11A40		±100	±500	
			RES11A50			±500	
			RES11A90			±500	
			RES11A00			±500	
t_{D2}	Ratio tolerance of divider 2 (1)	(R_{G2} / R_{IN2}) / G_{nom} – 1	RES11A10			±500	ppm
			RES11A15			±500	
			RES11A16			±500	
			RES11A20			±500	
			RES11A25			±500	
			RES11A30			±500	
			RES11A40		±120	±500	
			RES11A50			±500	
			RES11A90			±500	
			RES11A00			±500	

5.5 Electrical Characteristics (続き)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Voltage-divider circuit tolerance of divider 2	$(1 + G_{nom}) \times (R_{IN2} / (R_{IN2} + R_{G2})) - 1$	RES11A10			±500	ppm
			RES11A15			±500	
			RES11A16			±500	
			RES11A20			±500	
			RES11A25			±500	
			RES11A30			±500	
			RES11A40		±100	±500	
			RES11A50			±500	
			RES11A90			±500	
			RES11A00			±500	
t_M	Matching tolerance of dividers 1 and 2	$t_{D2} - t_{D1}$	RES11A10			±1000	ppm
			RES11A15			±1000	
			RES11A16			±1000	
			RES11A20			±1000	
			RES11A25			±1000	
			RES11A30			±1000	
			RES11A40		±85	±1000	
			RES11A50			±1000	
			RES11A90			±1000	
			RES11A00			±1000	
t_{abs}	Absolute tolerance (per resistor) (2)	$(R_x / R_{xnom}) - 1$ (3)			±2	±12	%
	Absolute tolerance span	MAX ($t_{absRIN1}$, t_{absRG1}, $t_{absRIN2}$, t_{absRG2}) – MIN ($t_{absRIN1}$, t_{absRG1}, $t_{absRIN2}$, t_{absRG2})			±235		ppm
RESISTANCE DRIFT							
	Absolute temperature coefficient of resistance (per resistor) (4)	$(\Delta R_x / R_{x(25°C)}) / \Delta T_A$	T_A = –40C to +125°C		±18		ppm/°C
	Divider temperature coefficient of resistance (per divider) (4)	$\Delta t_{Dx} / \Delta T_A$	T_A = –40C to +125°C		–0.2	±2	ppm/°C
TCR	Matching temperature coefficient of resistance (4)	$\Delta t_M / \Delta T_A$	T_A = –40C to +125°C		±0.05		ppm/°C
	Absolute voltage coefficient of resistance (per resistor)(2) (4)	$\Delta R_{INx} / \Delta V_{RINx}$	V_{RINx} = 0 V to V_{RINx} = 40 V		±0.02		Ω/V
		$\Delta R_{Gx} / (\Delta V_{RGx} \times G_{nom})$	V_{RGx} = 0 V to V_{RGx} = 40 V		±0.02		
	Divider voltage coefficient of resistance (per divider) (4)	$\Delta t_{Dx} / \Delta V_{Dx}$	V_{Dx} = 0 V to V_{Dx} = 40 V		±2		ppm/V
VCR	Matching voltage coefficient of resistance (4)	$(\Delta t_{D2} - \Delta t_{D1}) / \Delta V_{Dx}$	V_{Dx} = 0 V to V_{Dx} = 40 V		±0.5		ppm/V
IMPEDANCE							
C_{IN}	Pin capacitance (4)	RINx to GND/SUB			2.2		pF
		RGx to GND/SUB			1.6		
		RMIDx to GND/SUB			3.3		

5.5 Electrical Characteristics (続き)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Crosstalk (RMID1 to RMID2) (4)	Substrate biased to GND	f = 10 kHz		–100		dB
			f = 1 MHz		–64		
		Substrate floating	f = 10 kHz		–98		
			f = 1 MHz		–56		
	–3-dB bandwidth (4)	Substrate biased to GND			35		MHz
		Substrate floating			40		
CMRR	Common-mode rejection ratio (5)	RES11A10		66.0			dB
		RES11A15		68.0			
		RES11A16		68.5			
		RES11A20		69.5			
		RES11A25		70.9			
		RES11A30		72.0			
		RES11A40		74.0	95.4		
		RES11A50		75.6			
		RES11A90		80.0			
		RES11A00		80.8			

(1) Relation of R_{G1} / R_{IN1} or R_{G2} / R_{IN2} to nominal ratio.
(2) Relation of R_{G1}, R_{IN1}, R_{G2}, or R_{IN2} to nominal resistance.
(3) The specification is the result of this expression, given as a percentage (multiplied by 100%).
(4) Specified by characterization.
(5) The specification is the calculated CMRR when implemented in a difference amplifier configuration with an ideal op-amp, such that the only source of common-mode error is the resistor network. See the *Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs* application note for more information. Effects over frequency are not included. If the circuit is configured in an attenuating gain, this result changes accordingly.

5.6 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

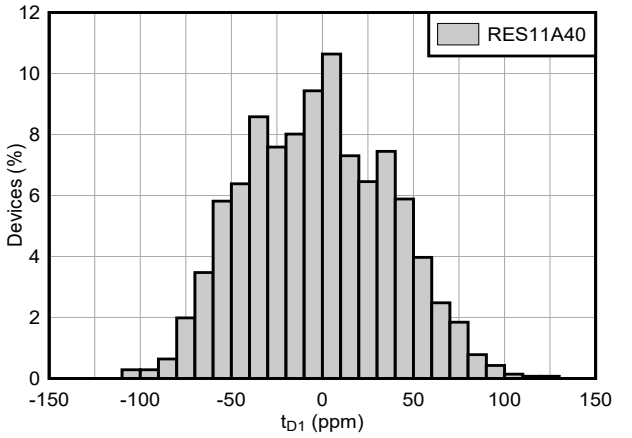


図 5-1. t_{D1} Distribution

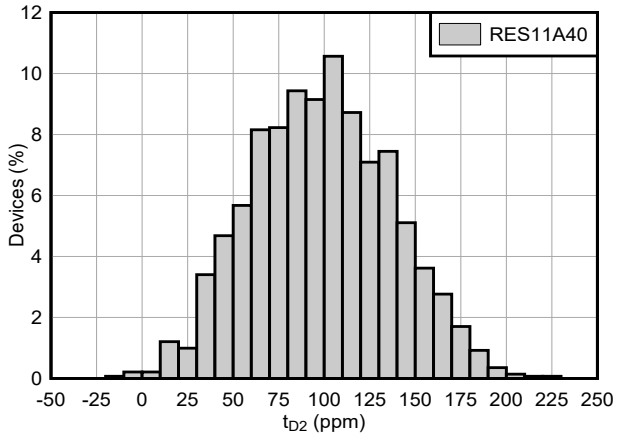


図 5-2. t_{D2} Distribution

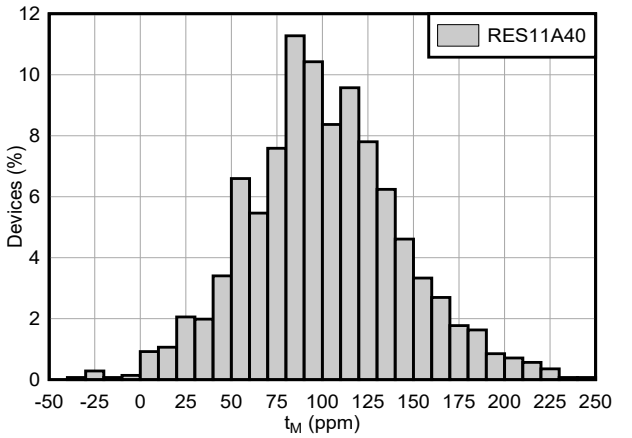


図 5-3. t_M Distribution

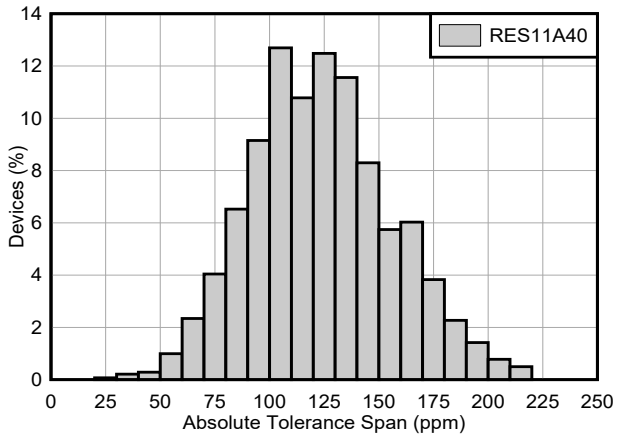


図 5-4. Absolute Tolerance Span Distribution

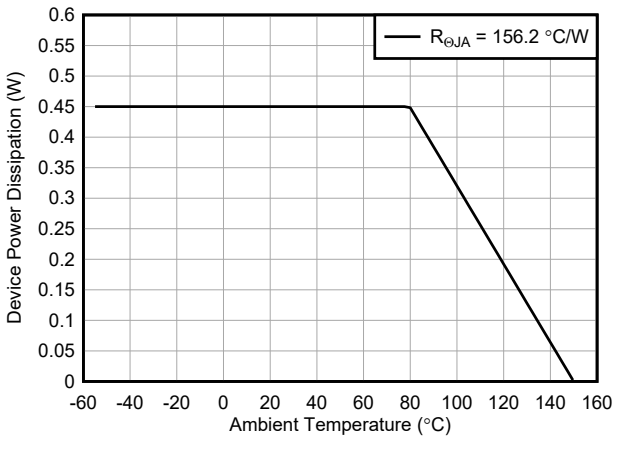


図 5-5. Maximum Power Dissipation

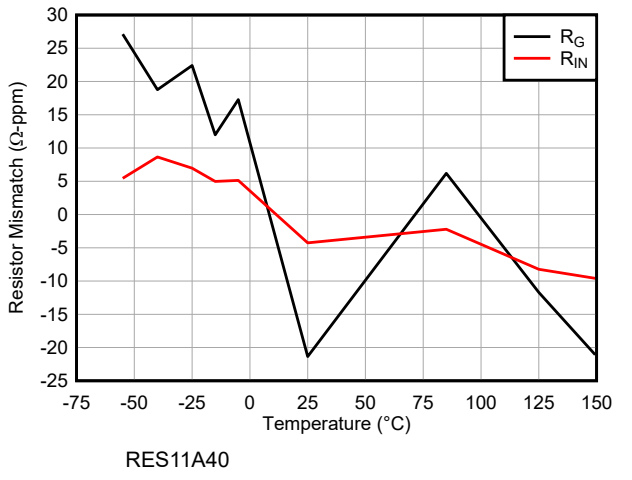


図 5-6. $R_{x2} – R_{x1}$ vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

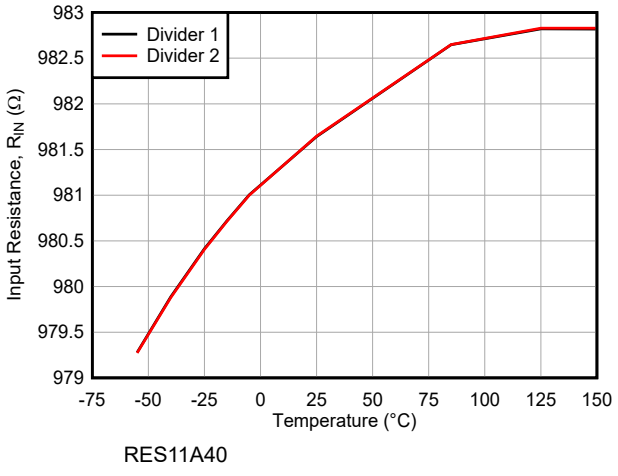


図 5-7. R_{INx} vs Temperature

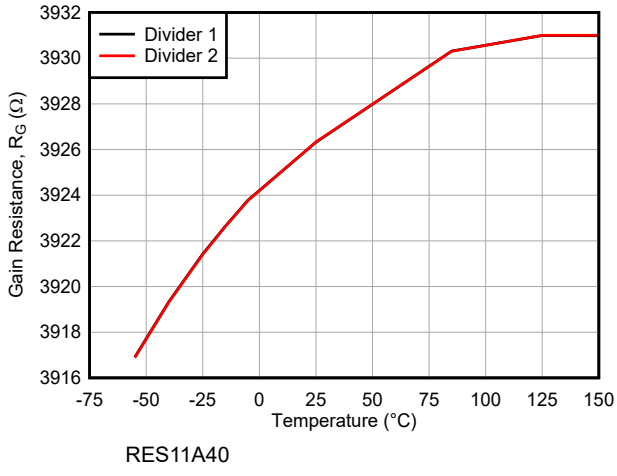


図 5-8. R_{Gx} vs Temperature

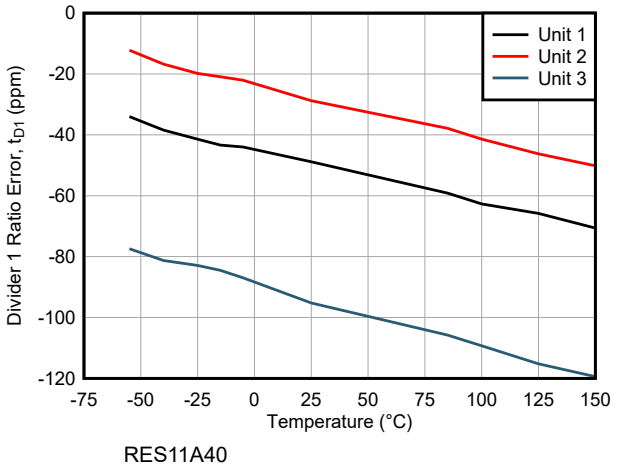


図 5-9. t_{D1} vs Temperature

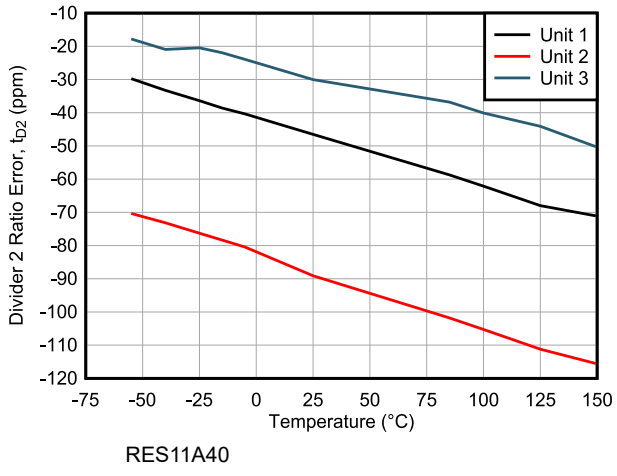


図 5-10. t_{D2} vs Temperature

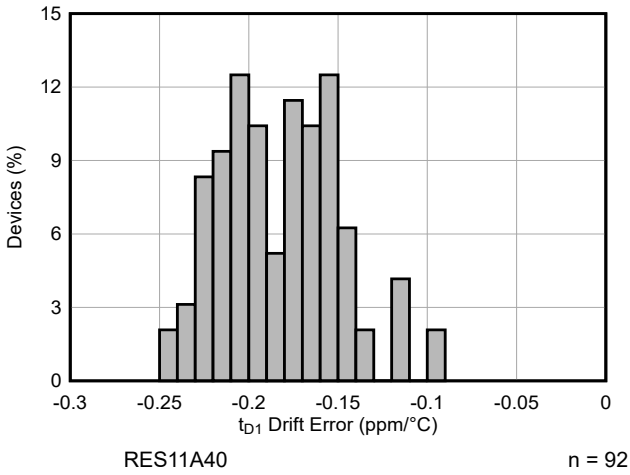


図 5-11. t_{D1} Drift Distribution

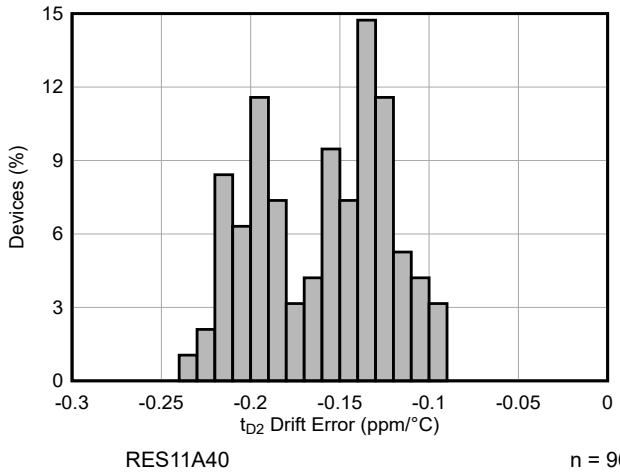


図 5-12. t_{D2} Drift Distribution

5.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

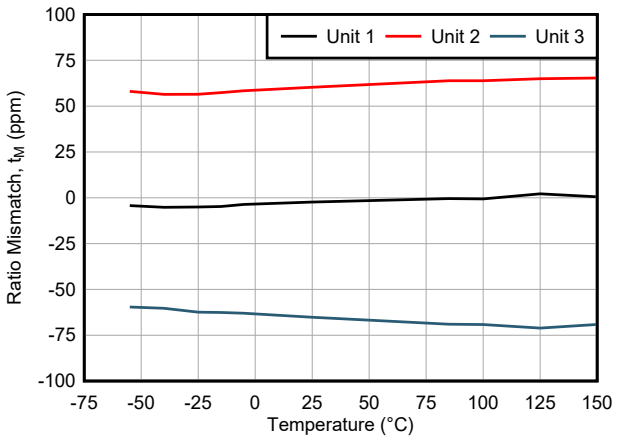


図 5-13. t_M vs Temperature

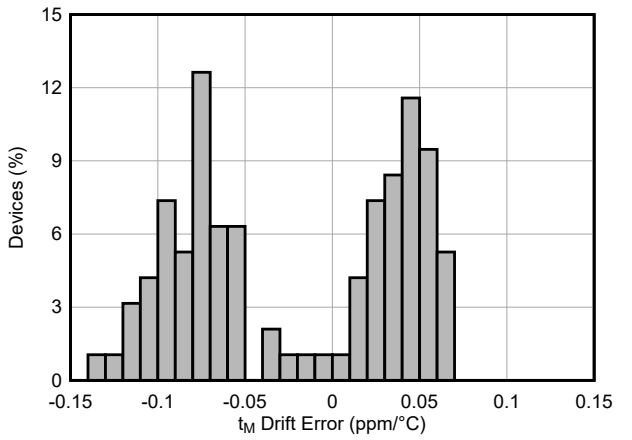


図 5-14. t_M Drift Distribution

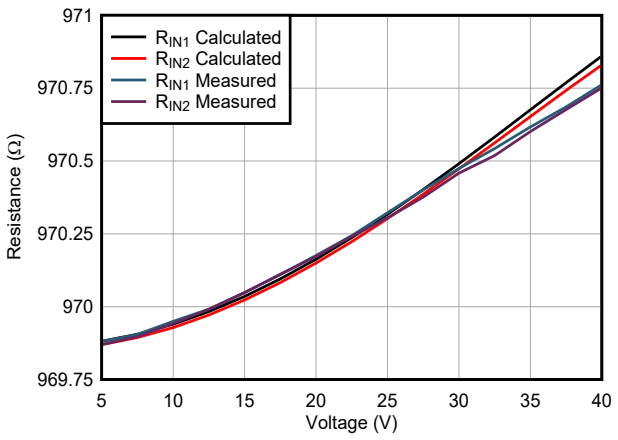


図 5-15. R_{INx} vs Bias

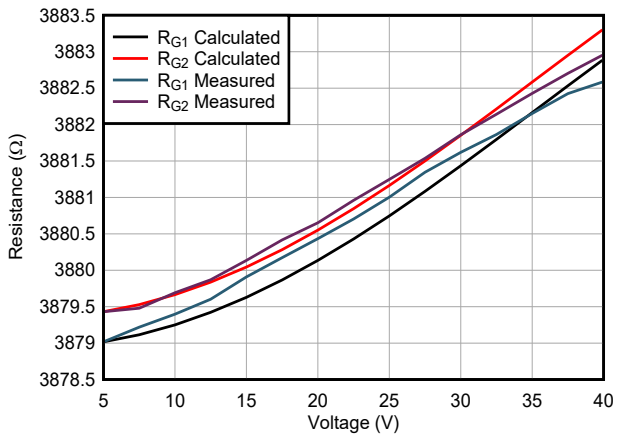


図 5-16. R_{Gx} vs Bias

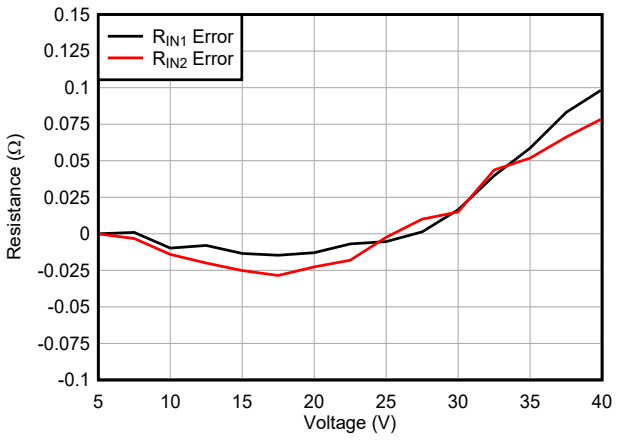


図 5-17. R_{INx} Actual-to-Expected Mismatch Error vs Bias

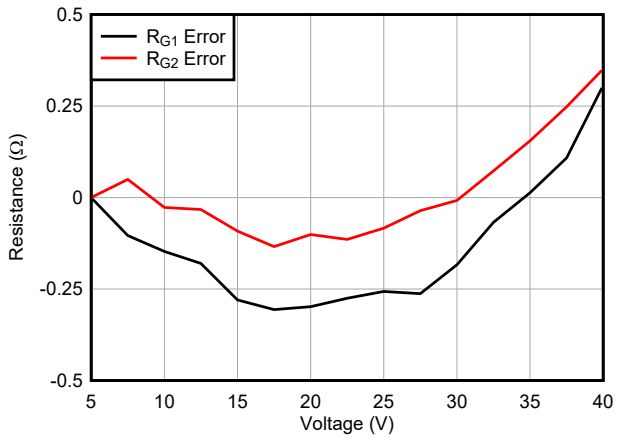


図 5-18. R_{Gx} Actual-to-Expected Mismatch Error vs Bias

5.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

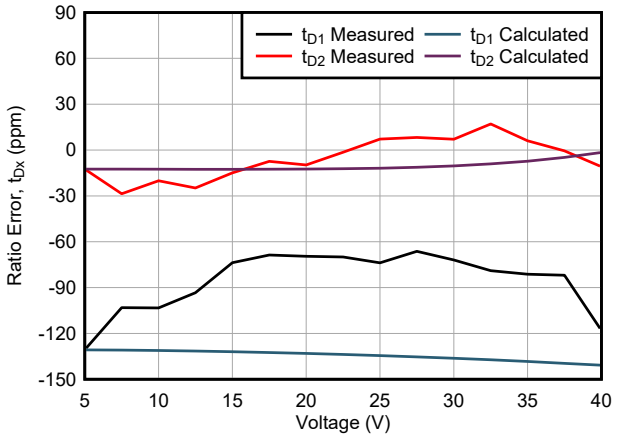


図 5-19. t_{Dx} vs Bias

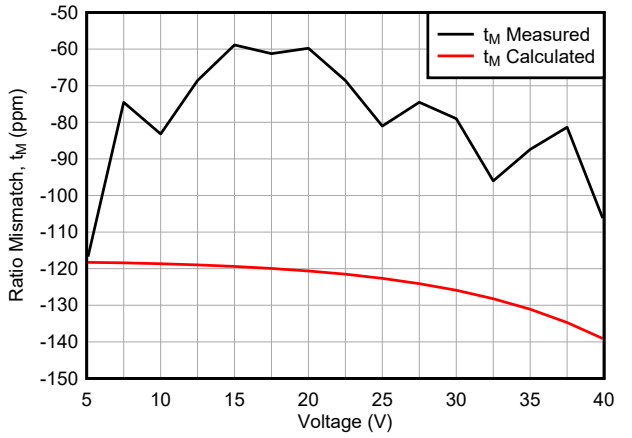


図 5-20. t_M vs Bias

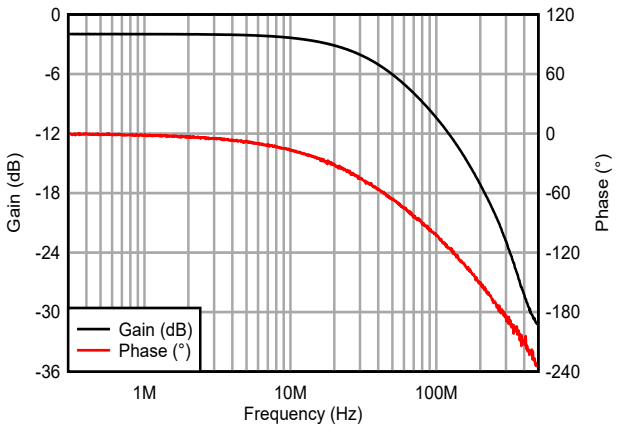


図 5-21. Bandwidth vs Frequency, R_{INx}

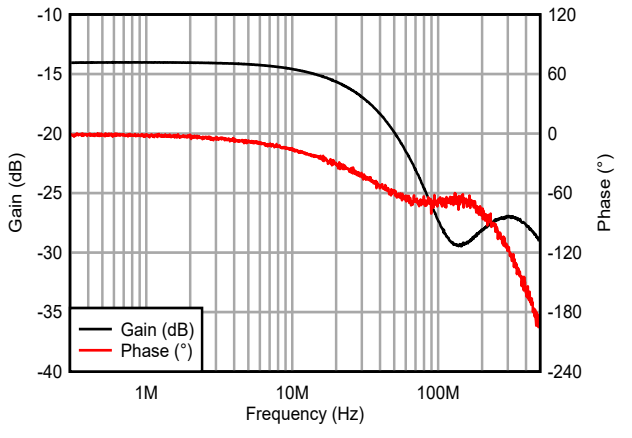


図 5-22. Bandwidth vs Frequency, R_{Gx}

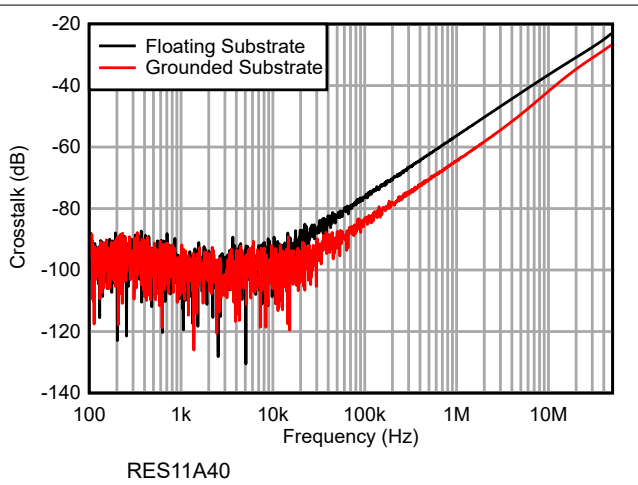


図 5-23. Crosstalk vs Frequency

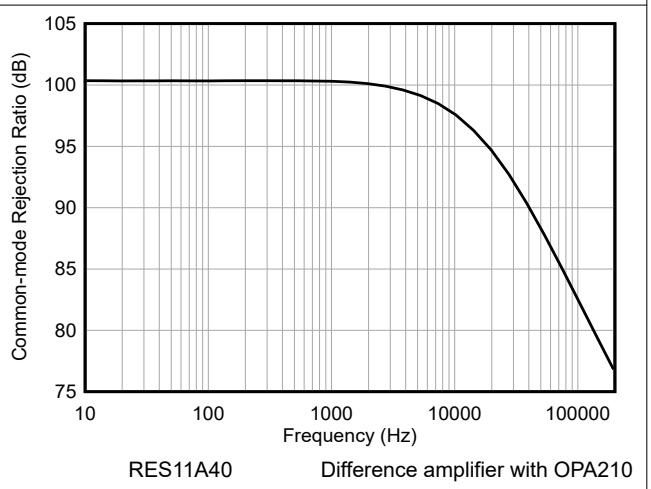


図 5-24. CMRR vs Frequency

6 Parameter Measurement Information

6.1 DC Measurement Configurations

An example of the circuit configuration used for dc measurements is shown in 図 6-1. Voltage V_{Dx} refers to the voltage across a given divider, such as V_{D1} for divider 1. Voltage V_{Rx} refers to the voltage across a given resistor, such as V_{RIN1} for R_{IN1} or V_{RG1} for R_{G1}.

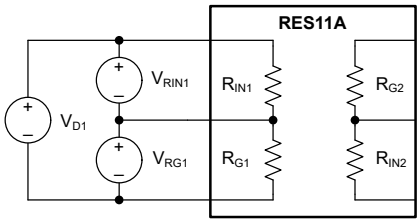


図 6-1. DC Measurement Terminology for Divider 1

When the RES11A is used to set the gain of an op amp (shown in 図 6-2), the ratio of the resistors in a divider sets the amplifier gain according to $G = R_G / R_{IN}$. Discrete-difference-amplifier and instrumentation-amplifier circuits are variations on this ratiometric use case. Typical and maximum parameter values for ratio tolerance (t_{D1}, t_{D2}) are expressed in terms of R_{Gx} / R_{INx} to simplify calculations for these circuits.

However, another valid use case of the RES11A is a simple voltage divider, where the midpoint voltage V_{MID} is equal to the input voltage V_D multiplied by $R_G / (R_{IN} + R_G)$, or by $R_{IN} / (R_{IN} + R_G)$ as shown in 図 6-3. Typical and maximum parameter values for ratio tolerance of these voltage-divider circuits, expressed in terms of $R_{INx} / (R_{INx} + R_{Gx})$, are provided.

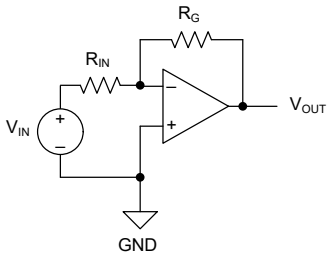


図 6-2. Amplifier Gain Circuit

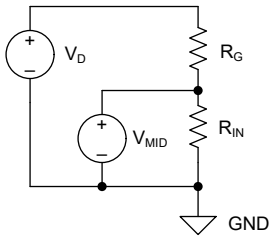


図 6-3. Voltage-divider circuit

図 6-4 shows the circuit configuration used for CMRR calculations. For an ideal amplifier with no offset and infinite CMRR, the effective circuit CMRR is entirely a function of the matching of the resistors. See セクション 8.1.1.1 and the *Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs* application note for more information.

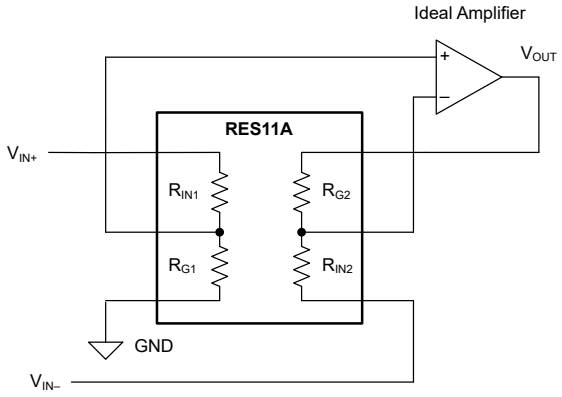


図 6-4. CMRR Calculation Reference Schematic

6.2 AC Measurement Configurations

図 6-5 shows the circuit configuration used for capacitance measurements. For the RES11A, a 1-MΩ R_{KNOWN} resistance and 10-pF C_{KNOWN} capacitance are used. The circuit creates an impedance divider; the resulting gain-vs-frequency relationship is used to calculate the parasitic capacitance in parallel with the resistor under test (in this case, R_{IN1}). Calibration with an empty socket is performed to account for board parasitics. The ac source is swept from 100 Hz to 50 MHz.

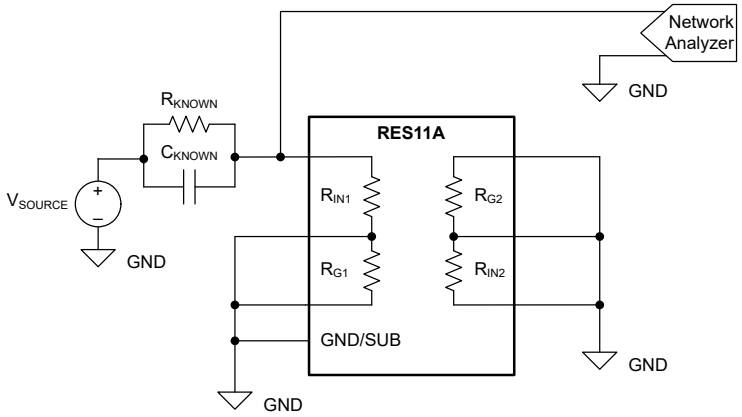


図 6-5. Capacitance Measurement Reference Schematic

図 6-6 shows the circuit configuration that is used for bandwidth measurements. The ac source is swept from 100 kHz to 500 MHz.

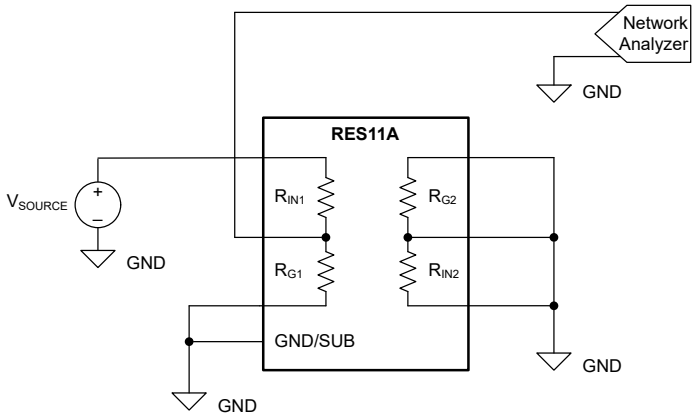


図 6-6. Bandwidth Measurement Reference Schematic

図 6-7 shows the circuit configuration used for crosstalk measurements. The ac source is swept from 100 Hz to 100 MHz.

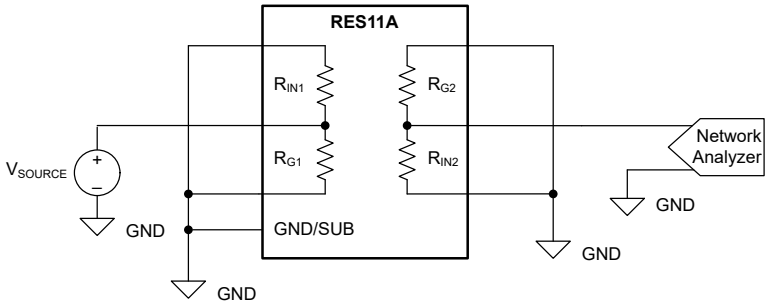


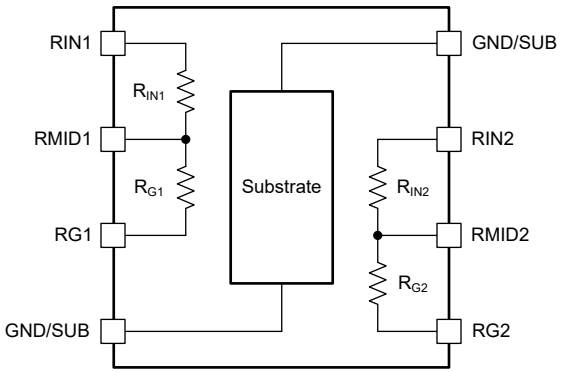
図 6-7. Crosstalk Measurement Reference Schematic

7 Detailed Description

7.1 Overview

The RES11A consists of four precision thin-film SiCr resistors, arranged to form two matched dividers. The device has two *input* resistors, R_{IN1} and R_{IN2}, both nominally 1 kΩ. The device also has two *gain* resistors, R_{G1} and R_{G2}, with values that depend on the nominal ratio (R_{Gx} / R_{INx}) of the RES11A device in question. The resistors are arranged with R_{IN1} and R_{G1} in series to form the first divider, and R_{IN2} and R_{G2} in series to form the second divider. Two GND pins are also provided to bias the device substrate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ratiometric Matching

The resistors of the RES11A are described by the following equations:

$$R_{IN1} = R_{INnom} \times (1+t_{abs}) = R_{INnom} \times (1+t_{RIN1}) \times (1+t_{SiCr}) \quad (1)$$

$$R_{IN2} = R_{INnom} \times (1+t_{RIN2}) \times (1+t_{SiCr}) \quad (2)$$

$$R_{G1} = R_{Gnom} \times (1+t_{RG1}) \times (1+t_{SiCr}) \quad (3)$$

$$R_{G2} = R_{Gnom} \times (1+t_{RG2}) \times (1+t_{SiCr}) \quad (4)$$

R_{INnom} and R_{Gnom} are the nominal values of each resistor. The parameter t_{abs} is an error term that describes the absolute tolerance of the RES11A device in question, such that $|t_{abs}| \leq 12\%$. The absolute tolerance is dominated by the variation in the SiCr resistivity, t_{SiCr}. The four resistors of a given RES11A are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for each of the four resistors, although t_{SiCr} varies on a part-to-part basis. The following examples show that when each divider is considered in ratiometric terms, these error terms drop out. Parameter t_{Rx} is an error term that describes the remaining effective tolerance of each resistor of the given RES11A device after accounting for the universal t_{SiCr}.

$$\frac{R_{Gx}}{R_{INx}} = \frac{R_{Gnom} \times (1+t_{RGx}) \times (1+t_{SiCr})}{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr})} = \frac{R_{Gnom} \times (1+t_{RGx})}{R_{INnom} \times (1+t_{RINx})} = G_{nom} \times \frac{(1+t_{RGx})}{(1+t_{RINx})} = G_x \quad (5)$$

$$\frac{R_{INx}}{R_{INx}+R_{Gx}} = \frac{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr})}{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr}) + R_{Gnom} \times (1+t_{RGx}) \times (1+t_{SiCr})} = \frac{R_{INnom} \times (1+t_{RINx})}{R_{INnom} \times (1+t_{RINx}) + R_{Gnom} \times (1+t_{RGx})} \quad (6)$$

The RES11A is specified with a maximum divider ratio tolerance of 0.05%, meaning that the relationship between the actual divider ratio G_x and nominal ratio G_{nom} of a given divider *x* is described by the following:

$$G_x = G_{nom} \times (1+t_{Dx}) \quad (7)$$

such that t_{Dx} ≤ 0.05%. Because any devices that do not meet these criteria are screened out at final test, these equations can be used with 式 5 to prove the effective bounds of t_{Rx}. Therefore, despite the device absolute end-to-end tolerance bounds of ±12%, the effective error tolerances of each resistor (for ratiometric applications) are within approximately ±0.025%, for the worst-case t_{Rx}.

The RES11A is specified with a maximum divider matching tolerance of 0.1%, meaning that the relationship between the ratio of divider 1 (G_1) and ratio of divider 2 (G_2) is described by the following:

$$t_M = t_{D2} - t_{D1} = \frac{G_2 - G_1}{G_{nom}} \quad (8)$$

By definition, $|t_M| \leq 0.1\%$. Again, the previous equations relate t_M to the parameters t_{DX} and t_{RX}. As a result of the interdigitation of the two dividers, the actual typical magnitude of t_M is significantly lower than this maximum value, depending on the specific RES11A device. This value is used to calculate the common-mode rejection ratio (CMRR) when implementing a difference amplifier circuit. For example, typical t_M for the RES11A40 is approximately 85 ppm, and the typical CMRR is 95.4 dB.

7.3.2 Ratiometric Drift

The ratiometric matching of the RES11A provides a benefit not just for initial conditions, but also when considering parametric drift. The resistors must be considered individually, in absolute terms, and ratiometrically to each other, in matched terms. The absolute temperature coefficients of each resistor show strong correlation, with the coefficient of R_{IN1} comparable to that of R_{IN2} and the coefficient of R_{G1} comparable to that of R_{G2}. The absolute temperature coefficient (in Ω/°C) of each R_G is approximately G_{nom} times greater than that of the comparable R_{IN}; hence, the normalized absolute temperature coefficient (in ppm/°C) of every resistor is about the same.

Because the resistors of the RES11A are interdigitated, and occupy a small footprint, the die temperature of the device is effectively common to each of the four resistors. As the temperature changes, each resistor experiences a similar temperature rise. Because the resistors have very similar temperature coefficients, the ratio of R_G to R_{IN} is well preserved. For example, the RES11A40 has a typical absolute temperature coefficient of approximately 18 ppm/°C for R_{IN} or R_G. When considered in ratiometric terms, the typical temperature coefficient of t_{D1} or t_{D2} is –0.2 ppm/°C, and the temperature coefficient of t_M is 0.05 ppm/°C.

7.3.3 Predictable Voltage Coefficient

The voltage coefficients of the RES11A are almost entirely related to self-heating, where the power dissipated in the device raises the die temperature. As previously mentioned, the commonality of this temperature rise leads to a comparable shift in each resistor, such that the divider ratio is well preserved.

Applying voltage *V* across resistor or divider *R* results in the loss of a corresponding power dissipation of $P = V^2 / R$, in the form of heat in the device die. This heat leads to a localized increase in the junction temperature, which in turn causes the same parametric shifts previously discussed in the context of temperature coefficients. TCR is specified as a function of ambient temperature; therefore, use the effective junction-to-ambient thermal resistance to determine the effective temperature rise and calculate the nominal or expected shift.

$$R_{expected} = \frac{V_R^2}{R} \times R_{\theta JA\ effective} \times TCR_{abs} \times R \quad (9)$$

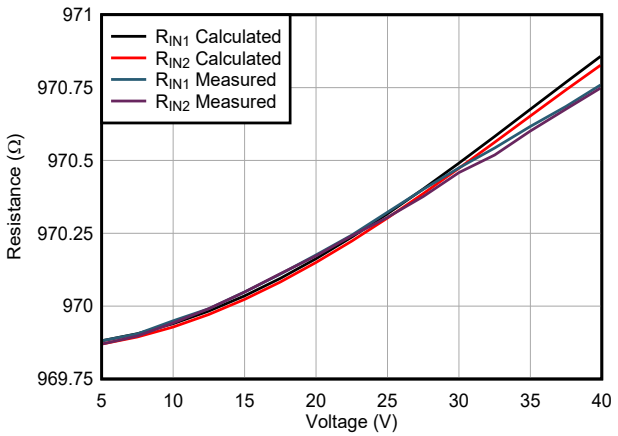


図 7-1. R_{IN} Resistance vs Voltage

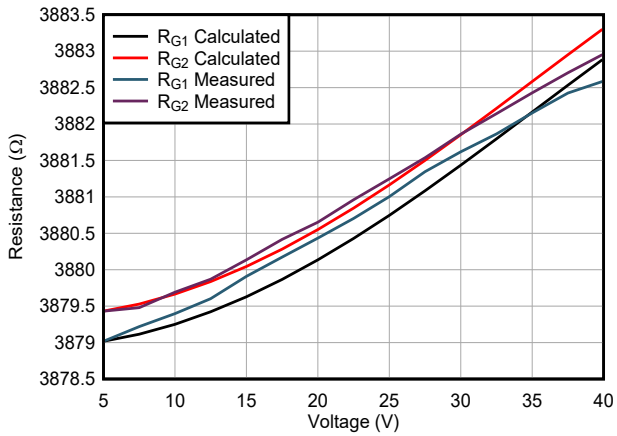


図 7-2. R_G Resistance vs Voltage

The difference of the expected value of *R* from the actual value of *R* describes the actual-to-expected mismatch error of *R*, due to non-temperature-related effects on the voltage coefficient. Similar to the logarithmic conformity error of a logarithmic amplifier or the integrated nonlinearity error of an ADC, this error describes the deviations of the actual device behavior from the predictable behavior. While the absolute magnitude of the shift varies, the slope or trend is predictable.

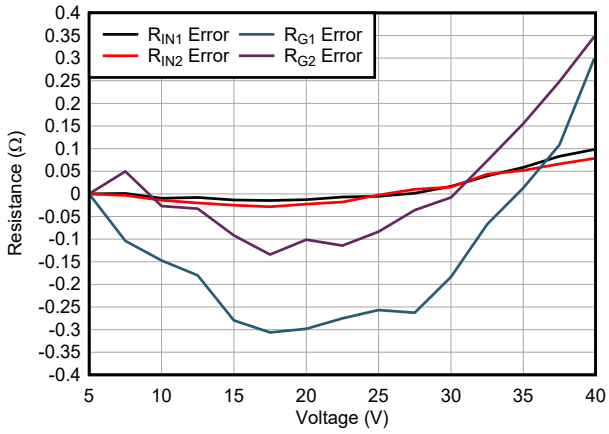


図 7-3. Resistor Actual-to-expected Mismatch vs Voltage

The measured value of *R* for low bias (measured by sourcing a very small current) is used with the actual value of *R* to calculate the effective voltage coefficient of resistance.

$$\text{Voltage coefficient } (\Omega/\text{V}) = \frac{R_{\text{biased}} - R_{\text{initial}}}{V_{\text{bias}}} \quad (10)$$

This exercise is repeated for each R_x, t_{D1}, t_{D2}, and t_M, to calculate the voltage coefficients associated with each parameter. For example, the RES11A40 has a typical absolute voltage coefficient of approximately 0.02 Ω/V for R_{IN} or R_G. When considered in ratiometric terms, the typical voltage coefficient of t_{D1} or t_{D2} is 2 ppm/V, and the voltage coefficient of t_M is 0.5 ppm/V.

7.3.4 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less than 100 Hz. Thermal noise typically dominates in the region greater than 1 kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES11A, the thermal noise as measured at the center tap of two resistors, R_{IN} and R_G, is equivalent to the thermal noise of a resistor with value $R_{IN} \parallel R_G$:

$$e_N = \sqrt{(4k_BTR)} \quad (11)$$

where:

- e_N is the thermal noise density in nV/√Hz
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, 1.381 × 10-23 J/K
- $R = R_{IN} \parallel R_G$

As an example, for the RES11A40 at 25°C:

$$e_N = \sqrt{(4k_BTR)} = \sqrt{4 \times 1.38E^{-23}\frac{J}{K} \times 278\ K \times (1\ k\Omega\ \parallel\ 4\ k\Omega)} = 3.5\ \text{nV}/\sqrt{\text{Hz}} \quad (12)$$

7.4 Device Functional Modes

The RES11A is typically used with the two independently biased resistor dividers. R_{IN1} and R_{G1} in series form a resistive divider, with R_{IN2} and R_{G2} in series forming another divider. However, the two dividers do not have to be used independently. The resistors can be connected in series or in parallel like any other resistor.

Use one of the two GND pins to bias the part substrate. Connect the substrate to signal ground or a similar low-impedance bias point or plane for best noise rejection. While two GND/SUB connection pins are available on the device, connect only *one* of these to the ground plane. The two GND pins are internally connected through the substrate, which is not intended to conduct significant currents. Connect only *one* GND pin at a time and leave the other pin floating to prevent current return paths from developing through the substrate.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Discrete Difference Amplifier

The RES11A is commonly used to implement a simple difference amplifier. The ratiometric matching between the two resistor dividers improves CMRR performance and gain drift for the circuit, when compared to a similar implementation using unmatched discrete resistors. The basic circuit is shown in 図 8-1.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_G}{R_{IN}}\right) + V_{REF} \tag{13}$$

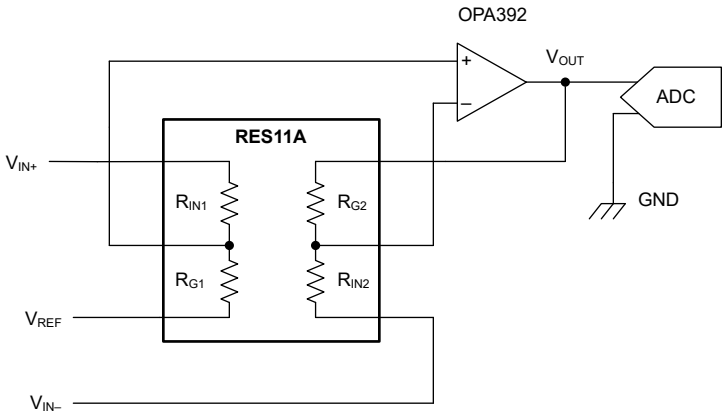

図 8-1. Discrete Difference Amplifier Using RES11A

8.1.1.1 Difference-Amplifier Common-Mode Rejection Analysis

In this simple difference amplifier configuration, the nominal CMRR is calculated as:

$$CMRR = 20 \times \log_{10}\left(\left|\frac{A_D}{A_{CM}}\right|\right) \tag{14}$$

The term A_D is the differential gain of the circuit, and the term A_{CM} is the common-mode gain of the circuit. These are defined as the following:

$$A_D \times = \frac{V_{OUT}}{V_D} = 0.5 \times \frac{\left(\frac{R_{G1}}{R_{G1}+R_{IN1}}\right) + \left(\frac{R_{G2}}{R_{G2}+R_{IN2}}\right)}{\left(\frac{R_{IN2}}{R_{G2}+R_{IN2}}\right)} \tag{15}$$

$$A_{CM} = \frac{V_{OUT}}{V_{CM}} = \frac{\left(\frac{R_{G1}}{R_{G1}+R_{IN1}}\right) - \left(\frac{R_{G2}}{R_{G2}+R_{IN2}}\right)}{\left(\frac{R_{IN2}}{R_{G2}+R_{IN2}}\right)} \tag{16}$$

Therefore,

$$\mathrm{CMRR} = 20 \times \log_{10}\left(\left| 2\times \frac{\mathrm{R_{G1}} \times (\mathrm{R_{IN2}} + \mathrm{R_{G2}}) - \mathrm{R_{G2}} \times (\mathrm{R_{IN1}} + \mathrm{R_{G1}})}{\mathrm{R_{G1}} \times (\mathrm{R_{IN2}} + \mathrm{R_{G2}}) + \mathrm{R_{G2}} \times (\mathrm{R_{IN1}} + \mathrm{R_{G1}})} \right|\right) \quad (17)$$

When this expression is evaluated with the definitions given in セクション 7.3.1, assuming the worst-case scenario of the most unbalanced divider matching possible,

$$\mathrm{CMRR} = 20 \times \log_{10}\left(\left| \frac{\mathrm{G_{nom}} + 1 + \mathrm{t_{Rx}}^2 (1 - \mathrm{G_{nom}})}{4 \times \mathrm{t_{Rx}}} \right|\right) \quad (18)$$

Because t_{Rx}^2 << 1, the worst-case CMRR is approximated as

$$\mathrm{CMRR} = 20 \times \log_{10}\left(\left| \frac{\mathrm{G_{nom}} + 1}{4 \times \mathrm{t_{Rx}}} \right|\right) \quad (19)$$

By definition, the parameter t_M describes the effective error that is otherwise equivalent to 4 × t_x for an unmatched divider network, and so the maximum value of t_M can be used to calculate the same worst-case result. Likewise, the typical value of t_M can be used to approximate the typical CMRR.

$$\mathrm{CMRR} = 20 \times \log_{10}\left(\left| \frac{\mathrm{G_{nom}} + 1}{\mathrm{t_M}} \right|\right) \quad (20)$$

For example, the worst-case CMRR for a RES11A40 device with G = 4 is approximately 74.0 dB, with a typical CMRR of approximately 95.4 dB. In comparison, implementation of a comparable G = 4 difference amplifier with unmatched 0.1%-tolerance resistors results in a worst-case CMRR of approximately 62 dB.

In a difference amplifier configuration, the CMRR of the op amp contributes error as well. The op-amp CMRR is considered in parallel with the CMRR of the resistor network, as per the following equation:

$$\frac{1}{\mathrm{CMRR_{TOTAL}}} = \frac{1}{\mathrm{CMRR_{AMP}}} + \frac{1}{\mathrm{CMRR_{RESISTORS}}} \quad (21)$$

Additional mismatches in the divider end-to-end resistances reduce the effective CMRR of a difference amplifier. While the low absolute tolerance span of the RES11A (235 ppm typical) helps reduce these concerns, parasitic trace resistances can lead to additional mismatches that impact the CMRR specs. Bench results from a difference amplifier implementation of the RES11A40 and the OPA210 are presented for various deliberate input-impedance mismatches.

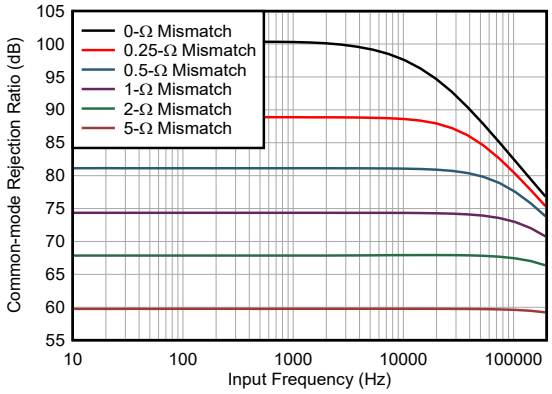

図 8-2. Effect of Input Impedance Mismatch on Common-mode Rejection Ratio

8.1.2 Discrete Instrumentation Amplifiers

The RES11A can be used to in conjunction with a dual-channel operational amplifier to implement a discrete instrumentation amplifier (INA). The ratiometric matching between the two resistor dividers improves CMRR

performance for the circuit when compared to a similar implementation using unmatched discrete resistors, and results in better overtemperature and overaging gain drift characteristics. INAs are often used instead of difference amplifiers when high input impedance and low bias currents are needed, such as when measuring bridge sensors.

Discrete INAs are often configured as a differential-input differential-output circuit as shown in 図 8-3. While not shown, if needed, use an additional discrete difference amplifier stage (requiring a second RES11A and another op-amp channel) to convert the differential output voltage to a single-ended voltage (for example, when driving a single-ended ADC). This extra stage can also add an additional offset and provide additional gain, effectively mimicking the common three-amplifier INA architecture.

$$V_{OUT+} - V_{OUT-} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{R_G}{R_{IN}} \right) \quad (22)$$

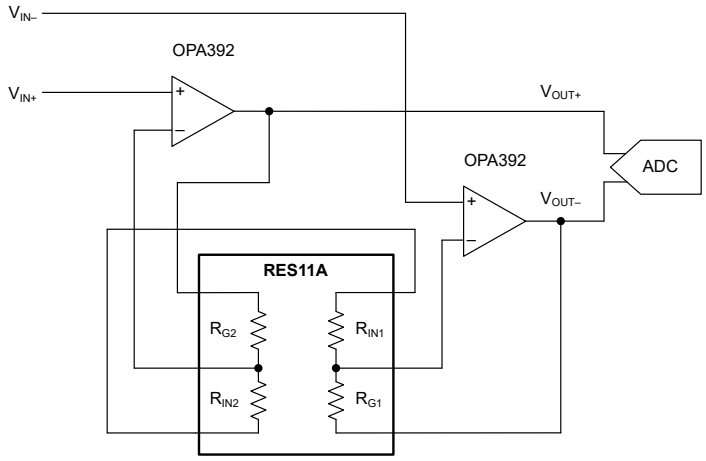

図 8-3. Differential-Input, Differential-Output Instrumentation Amplifier Using the RES11A

Less commonly, a discrete INA can be implemented as a differential-input, single-ended output circuit as shown in 図 8-4. This topology maintains high input impedances, allows an offset to be applied, and gives a single-ended output without requiring a third amplifier channel. The offset must be driven by a low-impedance source, such as a reference buffer. When designing a discrete INA, carefully consider the output swing and input common-mode range limitations of the amplifiers used in the circuit design process.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{R_G}{R_{IN}} \right) + V_{REF} \quad (23)$$

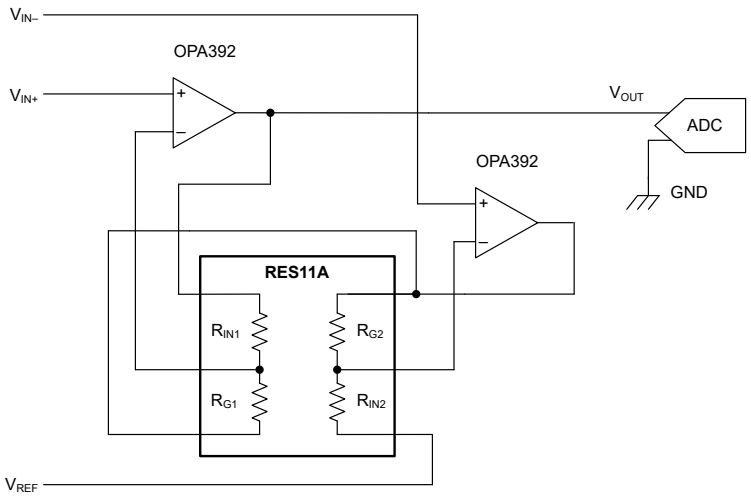

図 8-4. Differential-Input, Single-Ended Output Instrumentation Amplifier Using the RES11A

8.1.2.1 Instrumentation Amplifier Common-Mode Rejection Analysis

The differential-input, differential-output instrumentation amplifier shown in 図 8-3 has a common-mode gain of A_{CM} = 1 V/V. The differential gain is described by the following (assuming an ideal amplifier):

$$A_D = \frac{R_{G1} + R_{G2}}{R_{IN1} + R_{IN2}} + 1 = G_{nom} \times \frac{(1 \pm t_{RG1}) + (1 \pm t_{RG2})}{(1 \pm t_{RIN1}) + (1 \pm t_{RIN2})} + 1 \quad (24)$$

Because the worst-case-stage CMRR occurs when the differential gain is lowest, and the common-mode gain is unity, the minimum CMRR is evaluated as:

$$\frac{A_D}{A_{CM}} = G_{nom} \times \frac{(1 - t_{RG1}) + (1 - t_{RG2})}{(1 + t_{RIN1}) + (1 + t_{RIN2})} + 1 = G_{nom} \times \frac{1.9995}{2.0005} + 1 \quad (25)$$

For example, for an instrumentation amplifier with RES11A90, the worst-case CMRR is:

$$\frac{A_D}{A_{CM}} = G_{nom} \times \frac{(1 - t_{RG1}) + (1 - t_{RG2})}{(1 + t_{RIN1}) + (1 + t_{RIN2})} + 1 = 9\ V/V \times \frac{1.9995}{2.0005} + 1 = 9.9955\ V/V \quad (26)$$

8.1.3 Fully Differential Amplifier

The RES11A can be used to set the gain of a fully differential amplifier, such as the THP210. The ratiometric matching between the two resistor dividers leads to improved gain matching and CMRR performance for the circuit, when compared to a similar implementation using unmatched discrete resistors.

図 8-5 shows a generic schematic representation of a fully differential amplifier driving a differential ADC, with a RES11A used to set the amplifier gain.

$$V_{OUT+} - V_{OUT-} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_G}{R_{IN}}\right) \quad (27)$$

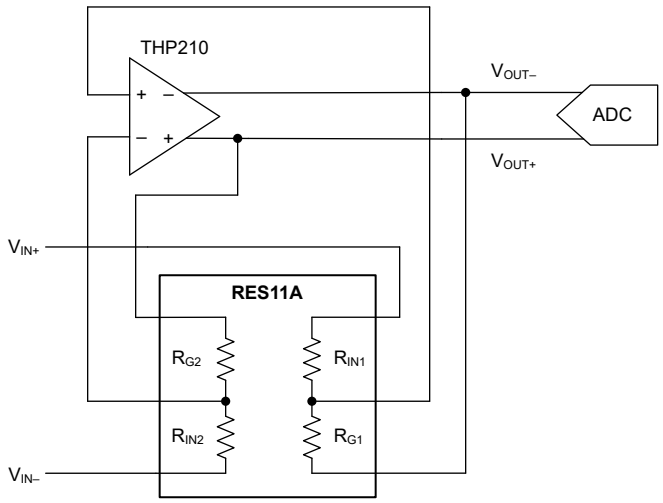

図 8-5. Fully-differential Amplifier Gain Setting Using RES11A

8.2 Typical Application

8.2.1 Common-Mode Shifting Input Stage

The RES11A can be used to implement a common-mode attenuator at the high-impedance inputs of an instrumentation amplifier (INA). This configuration extends the usable signal range, so long as the maximum differential voltage limitation of each resistor divider is respected.

図 8-6 shows an example of a high-side current-sense circuit where a differential voltage, V_{SHUNT}, develops across a sense resistor with an undesirably high common-mode voltage V_{CM}. V_{REF} is used to shift input common-mode voltages V_{MID1} and V_{MID2} to levels within the specified input common-mode range of the INA. The amplifier output, V_{OUT}, is a scaled function of V_{SHUNT}, such that nominally:

$$V_{OUT} = V_{SHUNT} \times \left(\frac{R_{IN}}{R_G + R_{IN} + R_{EQUIV}} \right) \quad (28)$$

V_{OUT} can be gained up further by the INA stage, to make maximal use of the effective resolution of a downstream ADC. In practice R_{EQUIV} is optional; however, if R_{EQUIV} = R_{SHUNT}, this resistance equalizes the nominal impedance between V_{CM} and each of the INA high-impedance inputs, thus improving CMRR performance. Select an INA with input bias currents I_{B1} and I_{B2} << $I_{STATIC1}$ and $I_{STATIC2}$, such as the INA333 or INA823. Select a RES11A device with a sufficiently high divider series resistance so that $I_{STATIC1}$ and $I_{STATIC2}$ << I_{LOAD}.

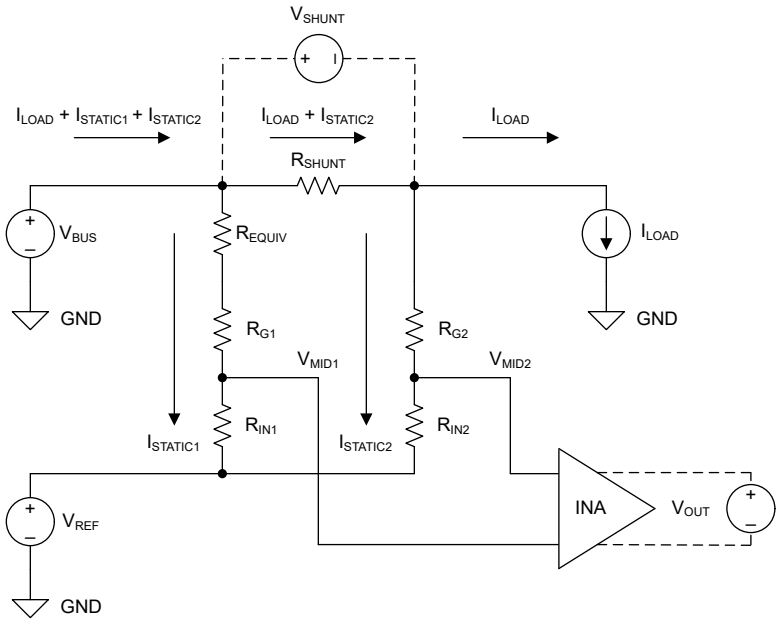

図 8-6. RES11A Common-Mode Shifting Circuit

To achieve a desired nominal input common-mode voltage, $V_{MID1TARGET}$, set V_{REF} as follows:

$$V_{REF} = V_{MID1TARGET} \times \left(\frac{R_G + R_{IN} + R_{EQUIV}}{R_G + R_{EQUIV}} \right) - V_{CM} \times \left(\frac{R_G + R_{IN} + R_{EQUIV}}{R_G + R_{EQUIV}} - 1 \right) \quad (29)$$

8.2.1.1 Design Requirements

Consider a level-shifting application where a high-side current shunt measurement from an 18-V supply rail must be measured by a 3.3-V amplifier and ADC.

PARAMETER	DESIGN GOAL
Input V_{BUS}	18 V
I_{LOAD}	300 mA (maximum)
R_{SHUNT}	1 Ω
ADC full-scale range (target V_{OUT})	3.3 V
Possible V_{REF} voltages	3.3 V, 0 V

8.2.1.2 Detailed Design Procedure

The design parameters are used with the aforementioned equations to select a nominal target G. When the possible V_{REF} voltages available in the system are considered, V_{REF} = 0 V with G = 9 is found to result in a V_{MID1} value of 1.8 V, well within the input common-mode range of a 3.3-V rail-to-rail amplifier such as the OPA392. When the corresponding RES11A90 is employed, the loss terms $I_{STATIC1}$ and $I_{STATIC2}$ are nominally 1.80 mA and 1.77 mA for I_{LOAD} = 300 mA, resulting in an effective floor of 1.77 mA for I_{LOAD}. For simplicity, the error contributions of the INA stage V_{OS} and I_B are ignored.

For the INA stage, an integrated TI instrumentation amplifier (IA) can be used. Alternatively, a discrete approach can be implemented using another RES11A device or devices, and one or more op amps. For this example, an IA stage is constructed with two channels of a OPA4392 and a second RES11A90 (R_{IN3}, R_{G3}, R_{IN4}, and R_{G4}). This stage is in turn cascaded with a difference amplifier stage, constructed with the third amplifier channel and a RES11A00 (R_{IN5}, R_{G5}, R_{IN6}, and R_{G6}). The level-shifting stage gain of 10^{-1}, multiplied by the instrumentation amplifier stage gain of 10, results in an effective unity-gain transfer function for V_{SHUNT}. Therefore, the differential output voltage for this stage is approximately 0.3 V, with amplifier outputs of 1.936 V and 1.634 V. After the final difference amplifier stage gain of G = 10, the common-mode voltage drops out and the maximum value of the resulting V_{OUT} is nominally 3.0 V, compatible with a single-ended 3.3-V ADC such as the ADS7046. If desired, the fourth channel of the OPA4392 can be used to buffer this output signal and serve as a dedicated ADC driver.

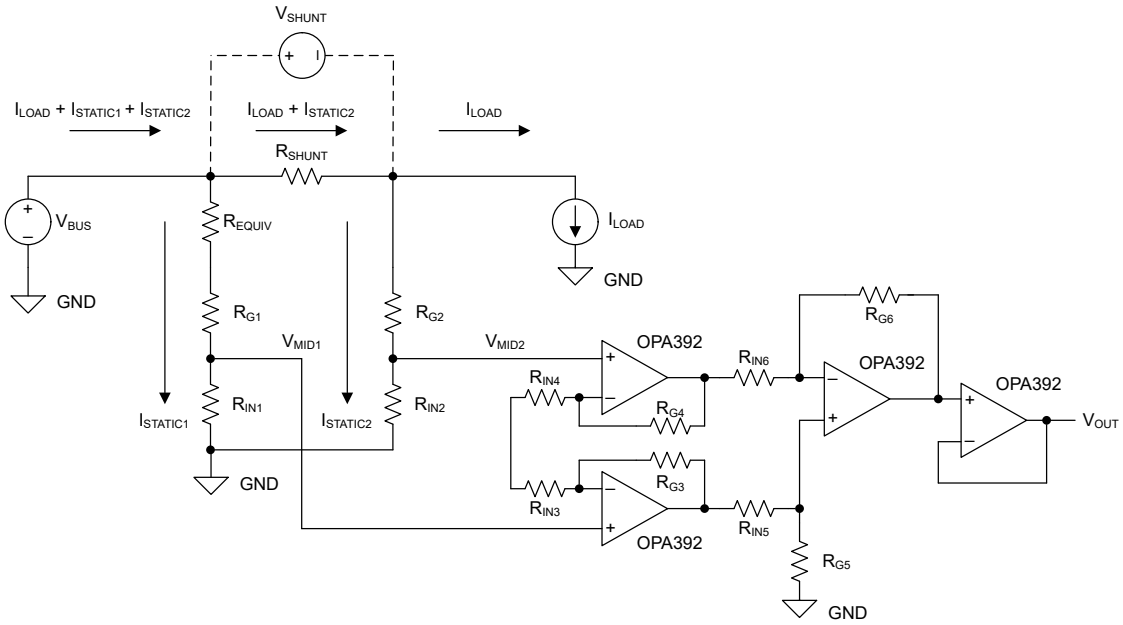

図 8-7. High-Side Current Shunt Common-Mode Shifting Circuit

8.2.1.3 Application Curves

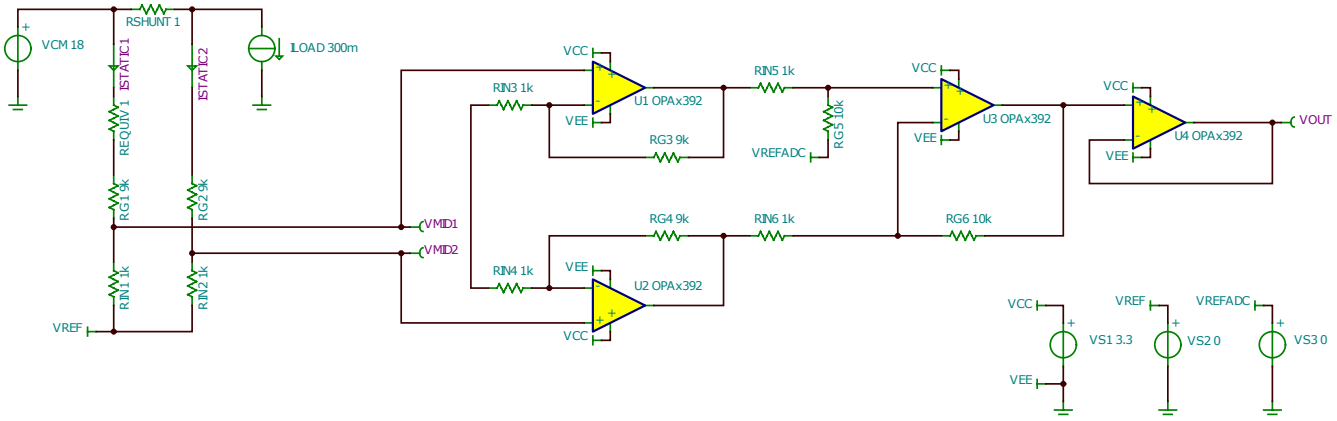

図 8-8. Circuit Model in TINA-TI

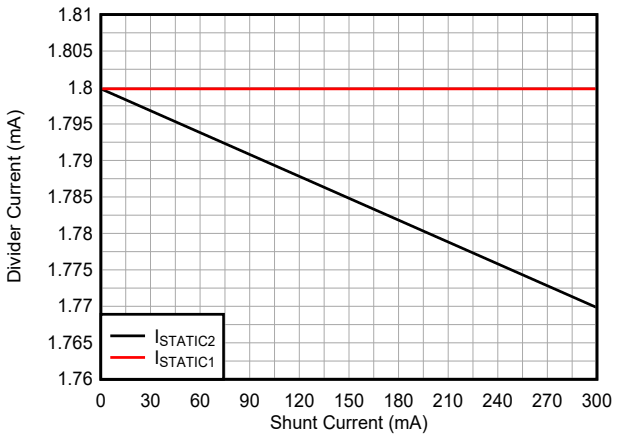

図 8-9. Simulation Result for I_{STATIC}

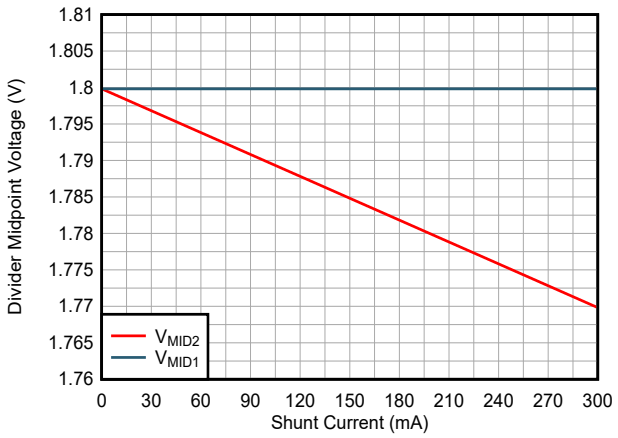

図 8-10. Simulation Result for VMID

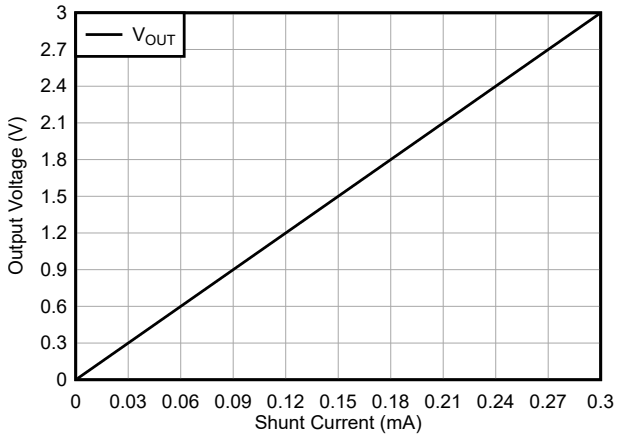

図 8-11. Simulation Result for VOUT

8.3 Power Supply Recommendations

The ratio of a given RES11A device dictates the maximum differential voltage rating for the resistor dividers of the device. See the *Absolute Maximum Ratings* and *Recommended Operating Conditions* for device-specific values under transient and sustained bias conditions, respectively. See 図 8-12 for approximate values, assuming $R_{\theta JA}$ = 156.2°C/W and that both dividers are biased to the same dc voltage at the same time. Keep T_J less than the absolute maximum rating of 150°C.

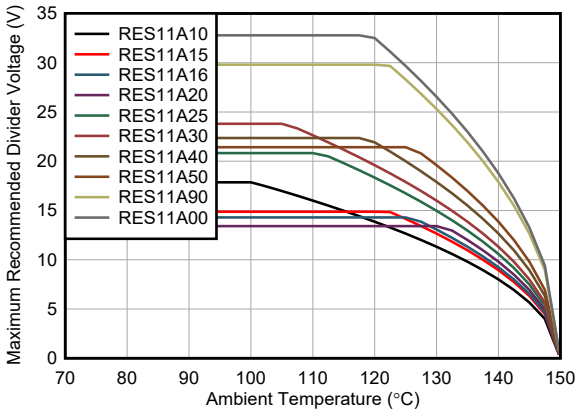

図 8-12. Maximum Recommended Divider Voltage vs Ambient Temperature

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running input traces as far away from supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit. For differential circuits, match the length of the input traces as best possible.
- Keep high impedance input signals away from noisy traces.
- Make sure system supply voltages are adequately filtered.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Only connect one of the two GND/SUB pins to the ground plane, to prevent the formation of current return paths through the device substrate. Float the other GND/SUB pin.

8.4.2 Layout Examples

In the following examples, the RES11A is shown with a VSSOP amplifier and 0402-size decoupling capacitors.

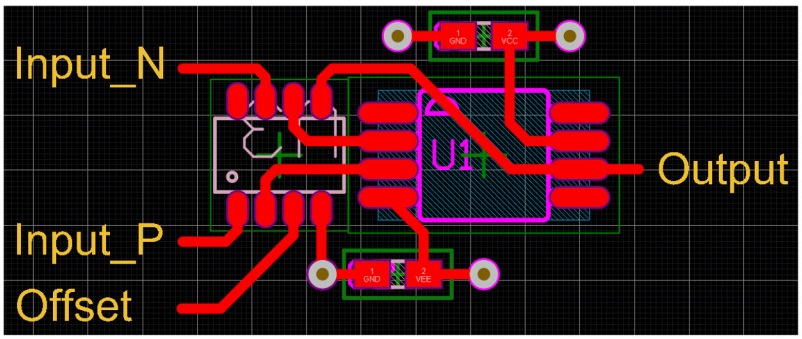

図 8-13. Single-Layer Difference Amplifier Implementation

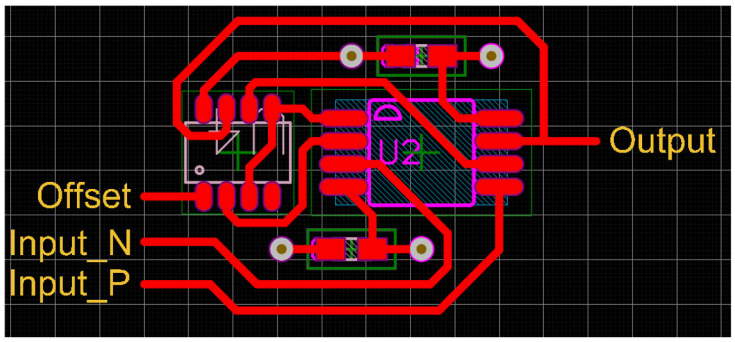

図 8-14. Single-Layer Instrumentation Amplifier Implementation

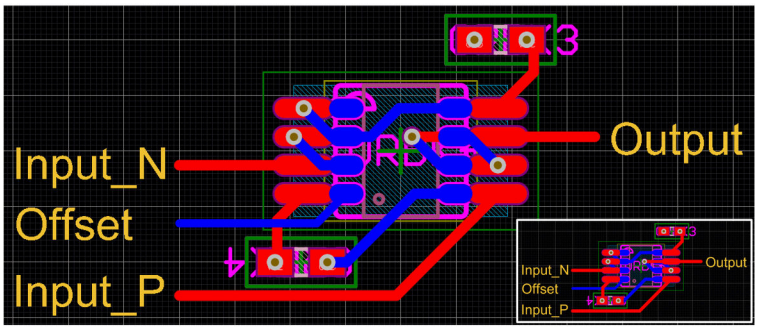

図 8-15. Front-and-Back Instrumentation Amplifier Implementation

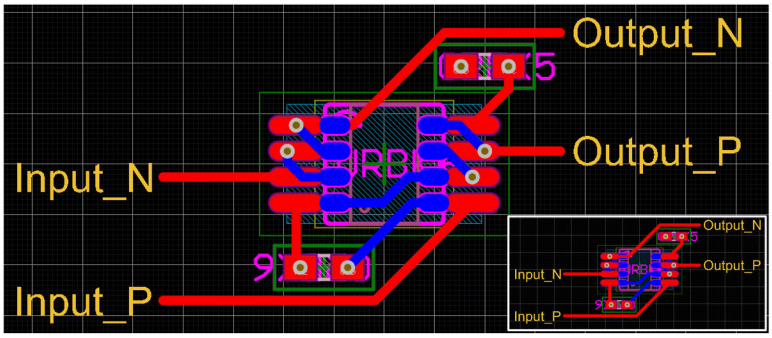

図 8-16. Front-and-Back, Differential-Output Instrumentation Amplifier Implementation

For 図 8-17, two RES11A devices (bottom side) and one dual-channel op-amp (top side) are used.

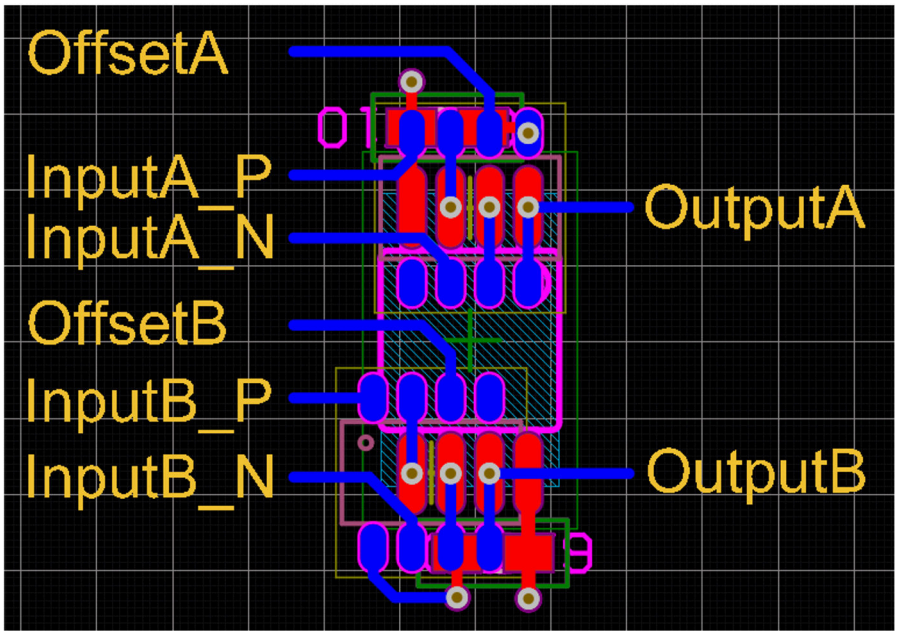

図 8-17. Front-and-Back Dual Difference Amplifiers Implementation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

9.1.1.2 TINA-TI™ シミュレーション・ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア・フォルダから、無償の TINA-TI シミュレーション・ソフトウェアをダウンロードしてください。

9.1.1.3 TI のリファレンス・デザイン

TI のリファレンス・デザインは、TI の高精度アナログ・アプリケーション専門家により作成されたアナログ・ソリューションです。TI のリファレンス・デザインは、動作原理、部品の選択、シミュレーション、完全な PCB 回路図およびレイアウト、部品表、測定済みの性能を提供します。TI のリファレンス・デザインは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

9.1.1.4 フィルタ設計ツール

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs* application note
- Texas Instruments, *THP210 Ultra-Low Offset, High-Voltage, Low-Noise, Precision, Fully-Differential Amplifier* data sheet
- Texas Instruments, *OPAx392 Precision, Low-Offset-Voltage, Low-Noise, Low-Input-Bias-Current, Rail-to-Rail I/O, e-trim™ Operational Amplifiers* data sheet

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

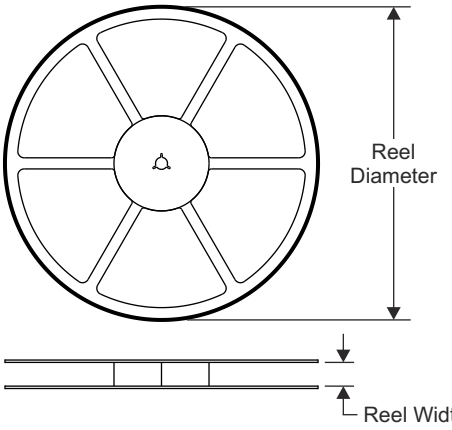
DATE	REVISION	NOTES
December 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

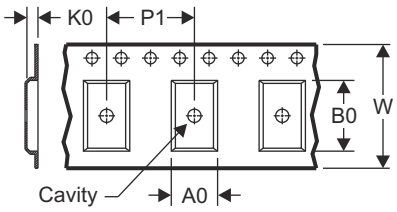
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

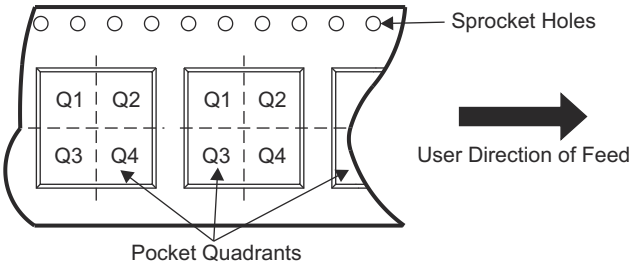


TAPE DIMENSIONS



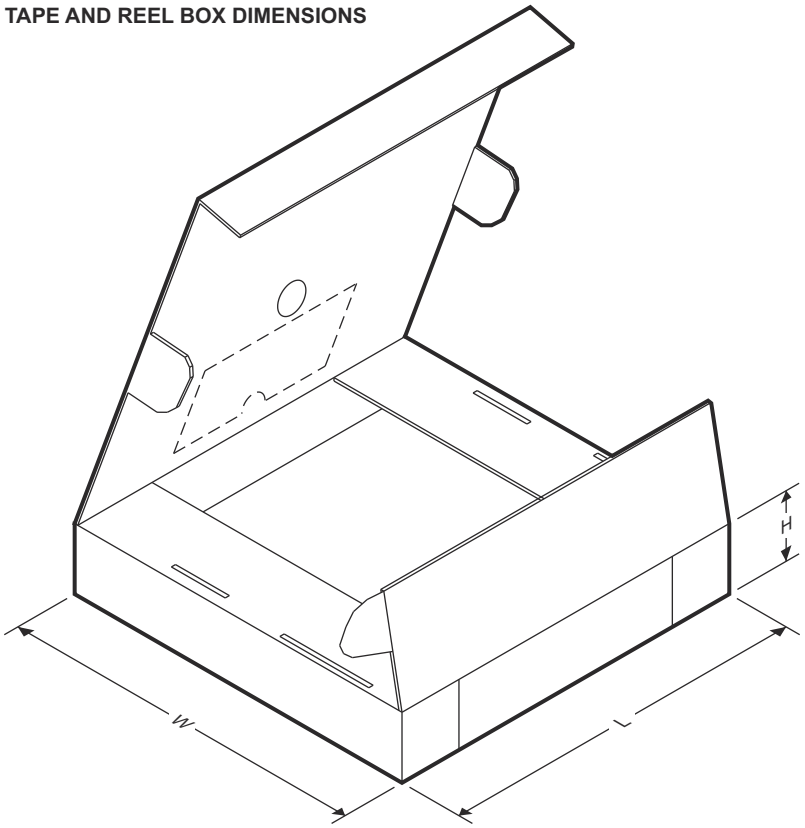
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PRES11A00QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A10QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A150QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A16QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A20QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A25QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A30QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A40QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A50QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PRES11A90QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



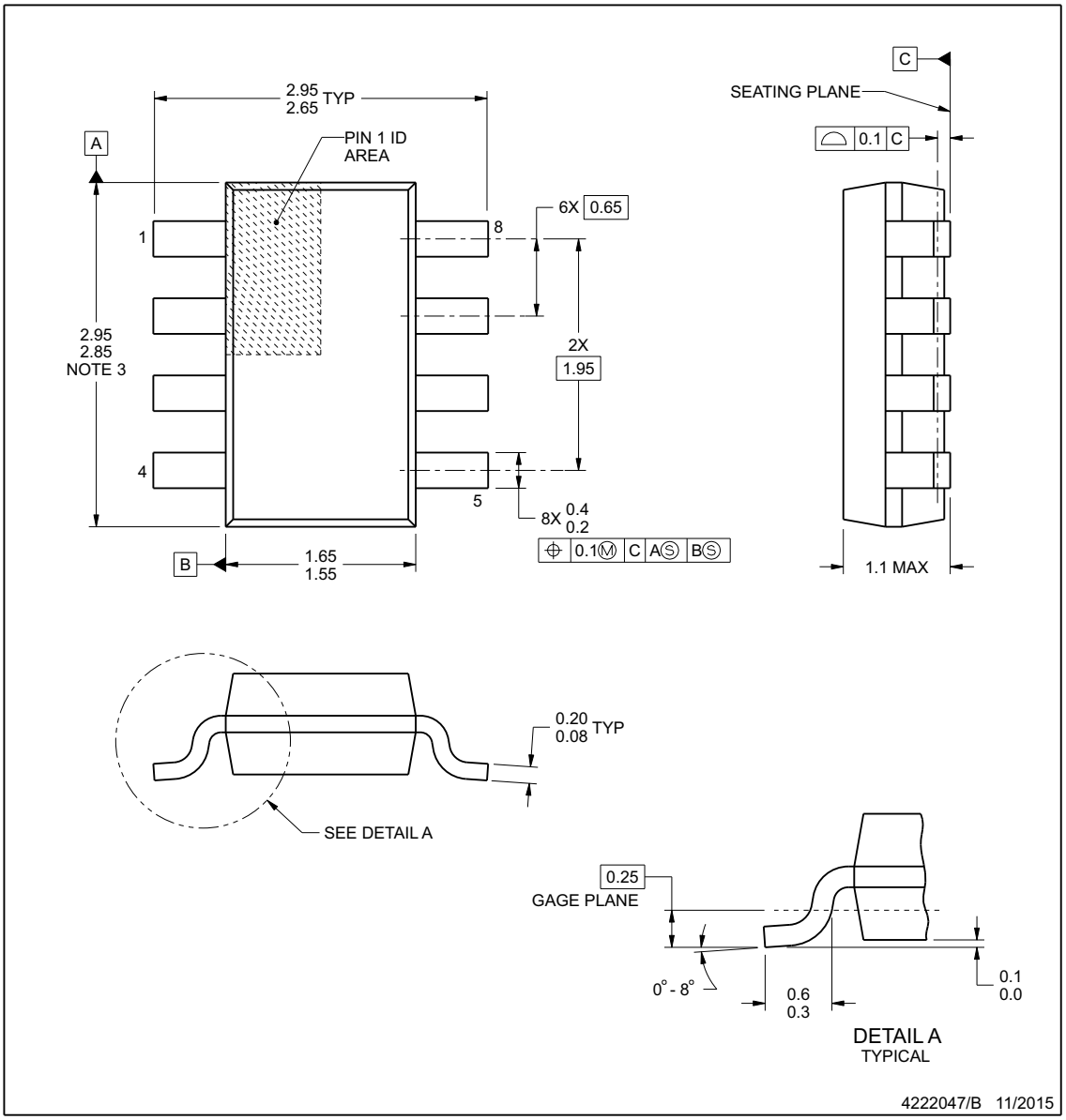
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PRES11A00QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A10QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A15QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A16QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A20QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A25QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A30QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A40QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A50QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0
PRES11A90QDDFRQ1	SOT-23-THIN	DFF	8	3000	201.0	185.0	35.0

11.2 Mechanical Data

PACKAGE OUTLINE

DDF0008A — **SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES:

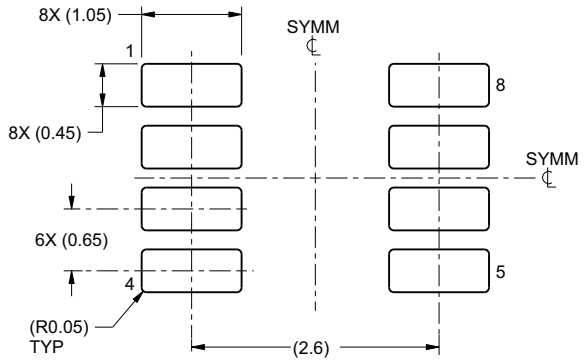
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

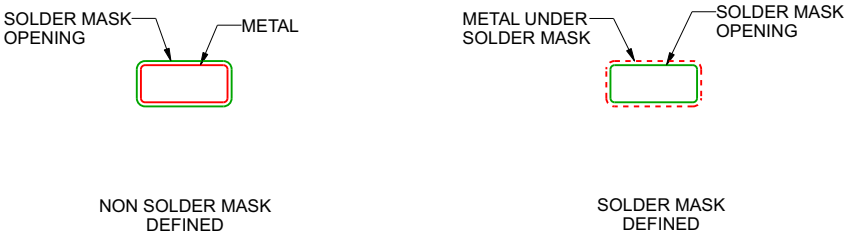
DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222047/B 11/2015

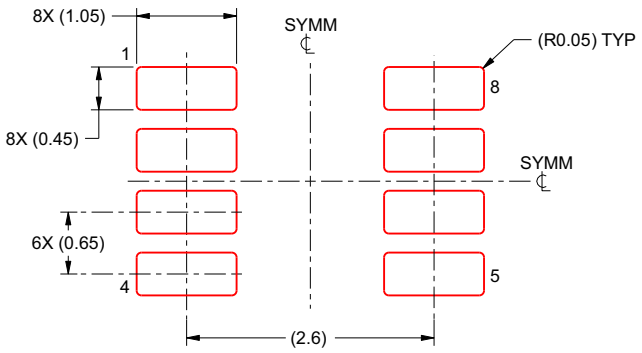
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A — **SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RES11A40DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R1140	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

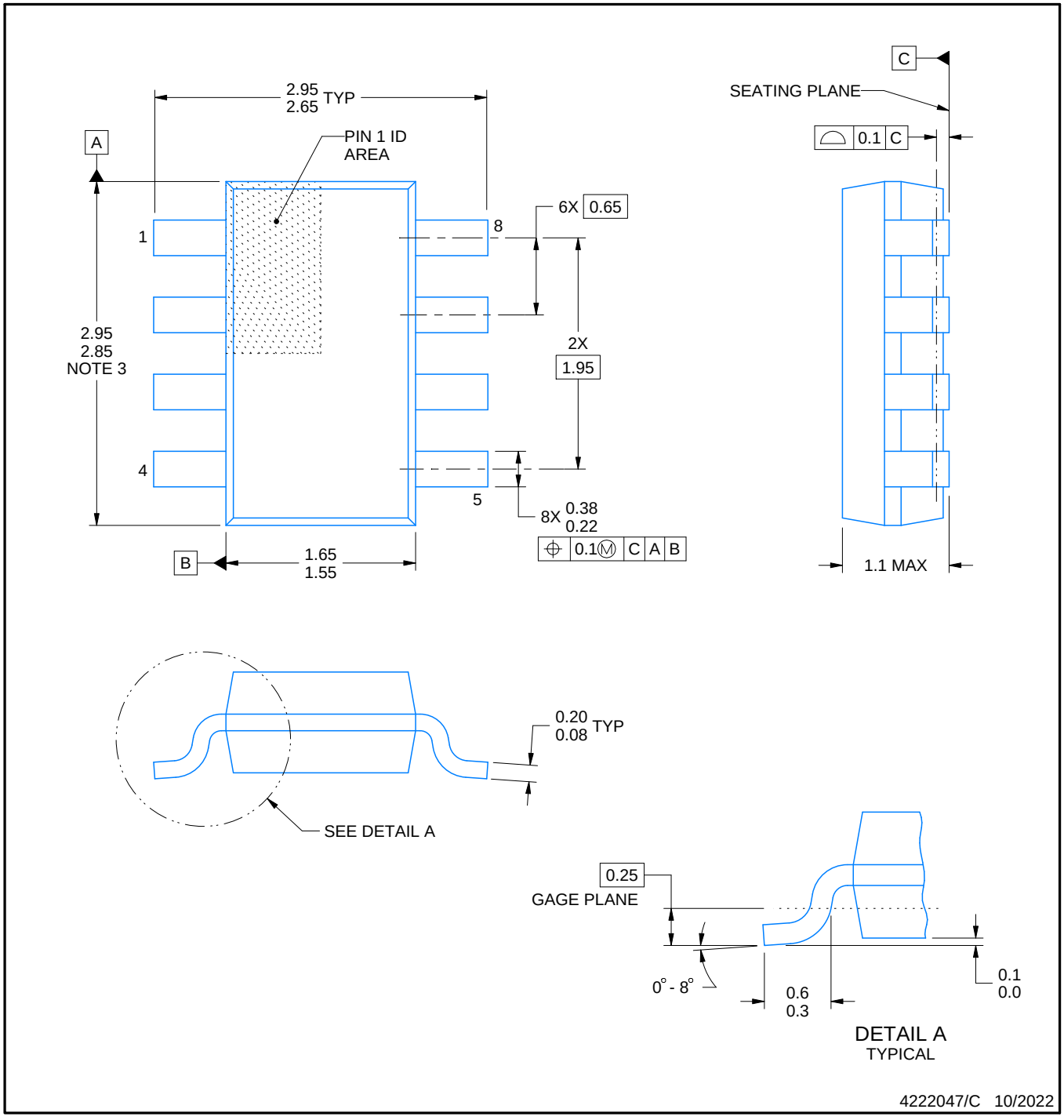
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDF0008A

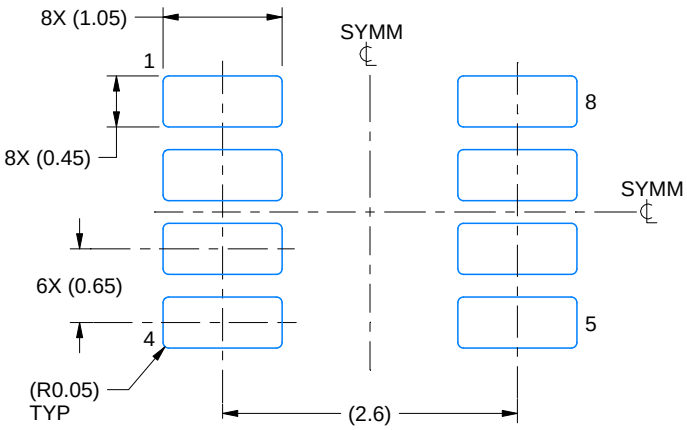
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

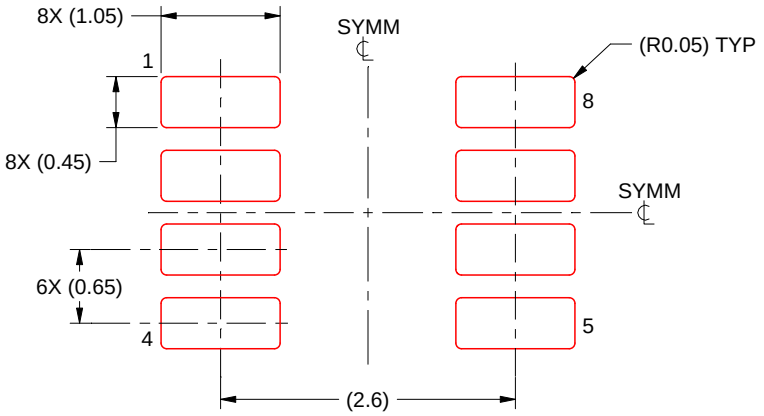
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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