

SNx4HCT74 デュアル D タイプ、ポジティブ・エッジ・トリガ・フリップ・フロップ、クリアおよびプリセット付き

1 特長

- 4.5V～5.5V の動作電源電圧範囲
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低消費電力、 I_{CC} : 40 μ A 以下
- $t_{pd} = 17$ ns (標準値)
- 5V で ± 4 mA の出力駆動能力
- 小さい入力電流: 最大 1 μ A
- 入力は TTL 電圧互換

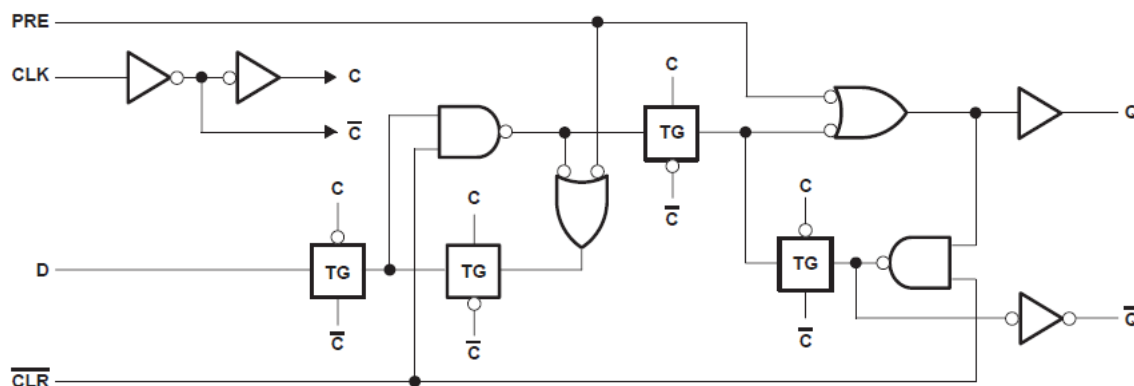
2 概要

'HCT74 には、2 つの独立した D タイプのポジティブ・エッジ・トリガ・フリップ・フロップが含まれています。その他の入力のレベルに関係なく、プリセット (PRE) 入力を Low レベルにすると出力は High になり、クリア (CLR) 入力を Low レベルにすると出力は Low になります。PRE と CLR が非アクティブ (High) の場合、セットアップ時間の要件を満たすデータ (D) 入力のデータは、クロック (CLK) パルスの正方向エッジで出力に転送されます。クロックのトリガは電圧レベルで発生し、CLK の立ち上がり時間とは直接関係しません。ホールド時間が経過した後、D 入力のデータは、出力のレベルに影響を及ぼさずに変化させることができます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SN74HCT74D	SOIC (14)	8.65mm × 3.90mm
SN74HCT74DB	SSOP (14)	6.20mm × 5.30mm
SN74HCT74N	PDIP (14)	19.31mm × 6.35mm
SN74HCT74NS	SO (14)	10.20mm × 5.30mm
SN74HCT74PW	TSSOP (14)	5.00mm × 4.40mm
SNJ54HCT74FK	LCCC (20)	8.89mm × 8.45mm
SNJ54HCT74W	CFP (14)	9.21mm × 6.29mm
SNJ54HCT74J	CDIP (14)	19.55mm × 6.71mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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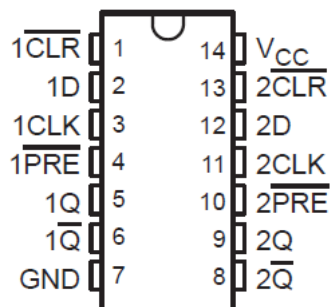
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3 Revision History

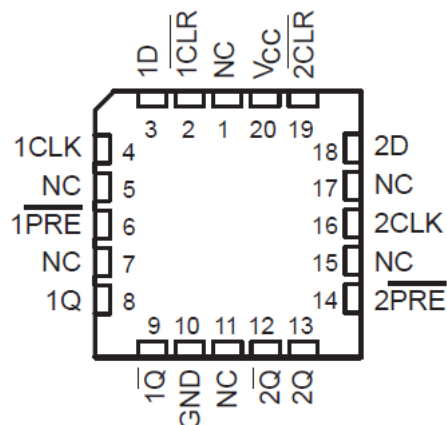
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (February 2022) to Revision G (October 2022)	Page
• Increased R _{θJA} for packages: D (86 to 138.7); N (80 to 103.8); NS (76 to 129.3); PW (113 to 157.6).....	4

4 Pin Configuration and Functions



J, W, D, DB, N, NS, or PW package
14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP
Top View



NC - No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HCT74 ⁽²⁾			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) SN54HCT74 is in product preview.

5.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
THERMAL METRIC		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	138.7	109.8	61.1	88.4	114.7	°C/W
$R_{\theta JC (top)}$	Junction-to-case (top) thermal resistance	93.8	54.7	48.9	46	44.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	58.6	40.9	48.9	57.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	49.1	15.5	28.5	13.8	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.3	58	40.6	48.4	57	°C/W
$R_{\theta JC (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT74 ⁽²⁾		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I _{OH} = -4 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA			0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			4		80		40	µA
ΔI _{CC} ⁽¹⁾	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4		3		2.9	mA
C _i			4.5 V to 5.5 V		3	10		10		10	pF

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

(2) SN54HCT74 is in product preview.

5.5 Timing Requirements

overrecommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 25°C		SN54HCT74 ⁽¹⁾		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		4.5 V	27		18		22		MHz
			5.5 V	30		20		24		
t _w	Pulse duration	PRE or CLR low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
		CLK high or low	4.5 V	18		27		23		
			5.5 V	16		24		21		
t _{su}	Setup time before CLK ↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
		PRE or CLR inactive	4.5 V	0		0		0		
			5.5 V	0		0		0		
t _h	Hold time, data after CLK ↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

(1) SN54HCT74 is in product preview.

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT74 ⁽¹⁾		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	PRE or CLR	Q or $\bar{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\bar{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\bar{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

(1) SN54HCT74 is in product preview.

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

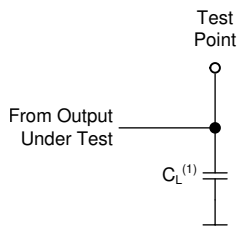
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

FIG 6-1. Load Circuit for Push-Pull Outputs

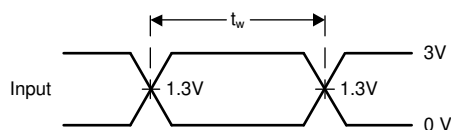


FIG 6-2. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

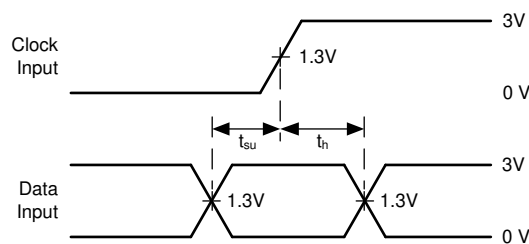
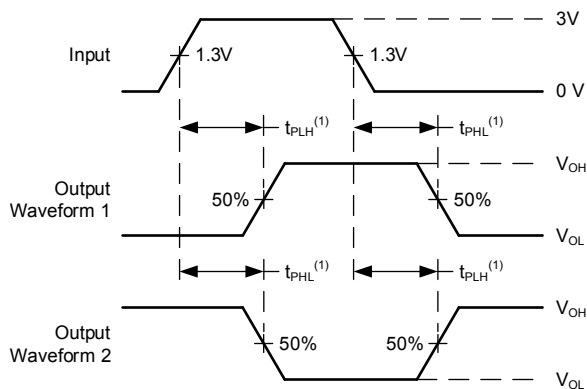


FIG 6-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

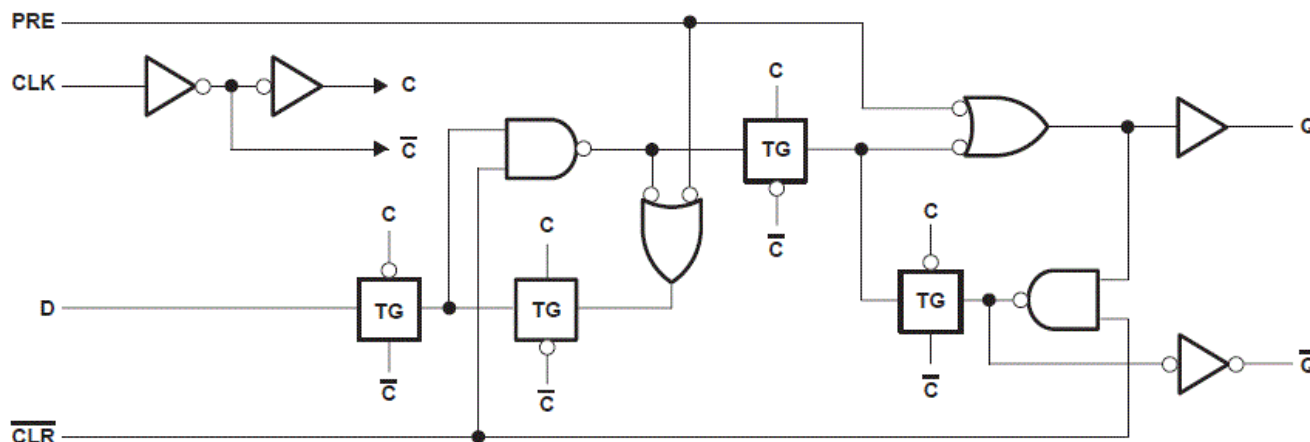
FIG 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table

INPUTS				OUTPUT	
PRE	CLR	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

- (1) This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/65352B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352B2A	Samples
JM38510/65352BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BCA	Samples
JM38510/65352BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BDA	Samples
M38510/65352B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352B2A	Samples
M38510/65352BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BCA	Samples
M38510/65352BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BDA	Samples
SN74HCT74DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74	Samples
SN74HCT74DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT74N	Samples
SN74HCT74NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT74N	Samples
SN74HCT74NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HT74	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCT74, SN74HCT74 :

- Catalog : [SN74HCT74](#)
- Military : [SN54HCT74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

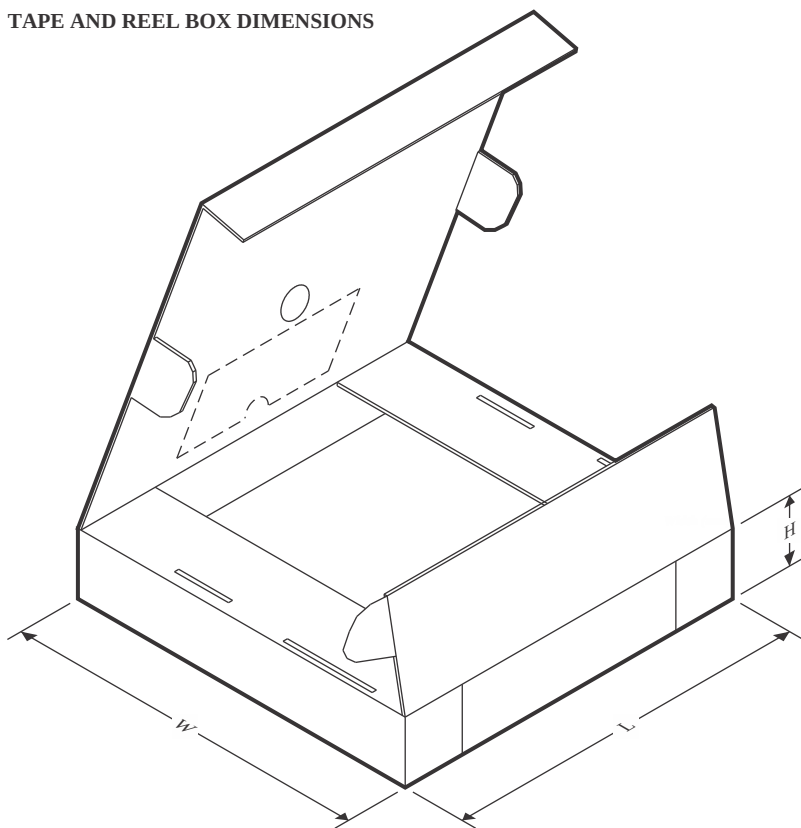
TAPE AND REEL INFORMATION



*All dimensions are nominal

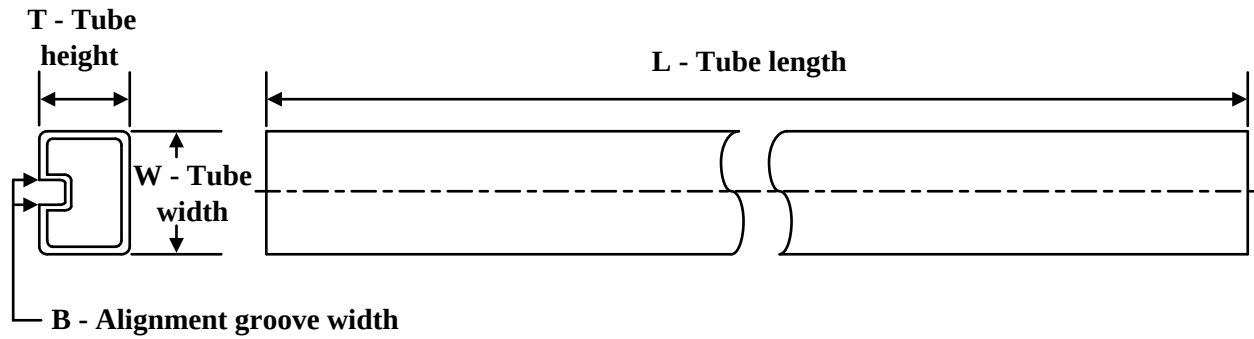
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT74DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCT74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HCT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT74DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74HCT74DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCT74DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT74DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT74NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74HCT74PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT74PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT74PWR	TSSOP	PW	14	2000	366.0	364.0	50.0

TUBE


*All dimensions are nominal

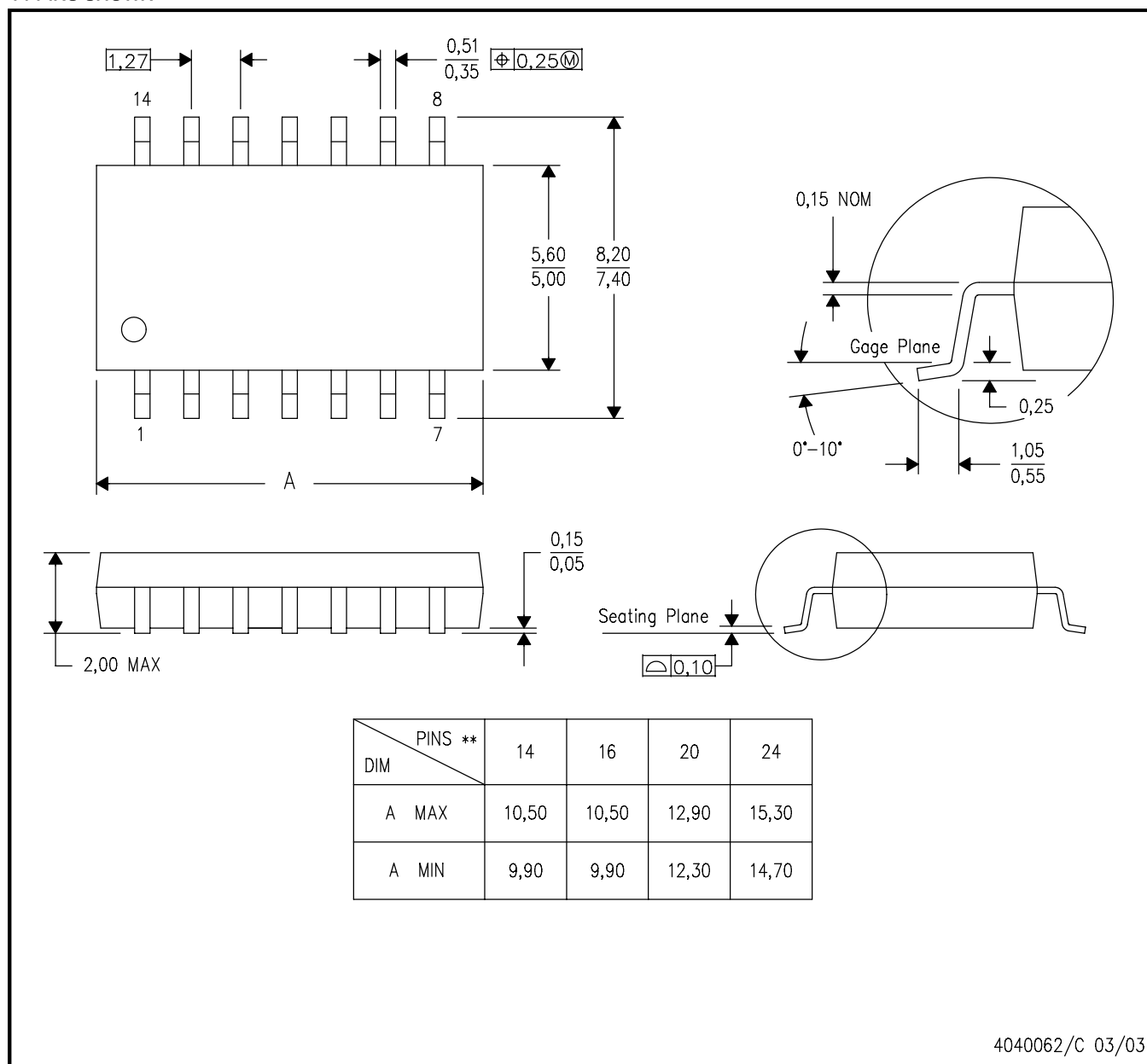
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/65352B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65352BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/65352B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65352BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

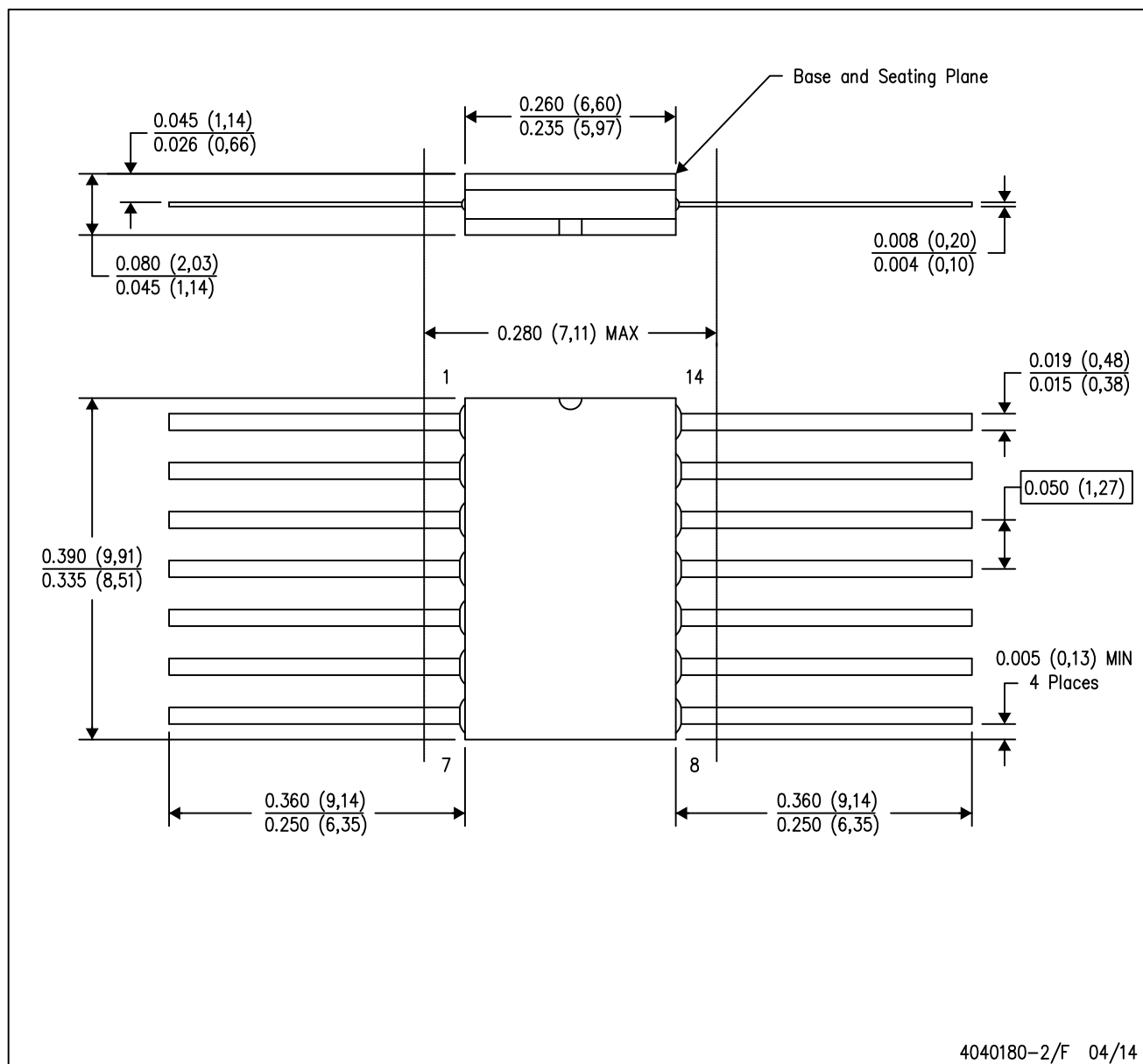
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



GENERIC PACKAGE VIEW

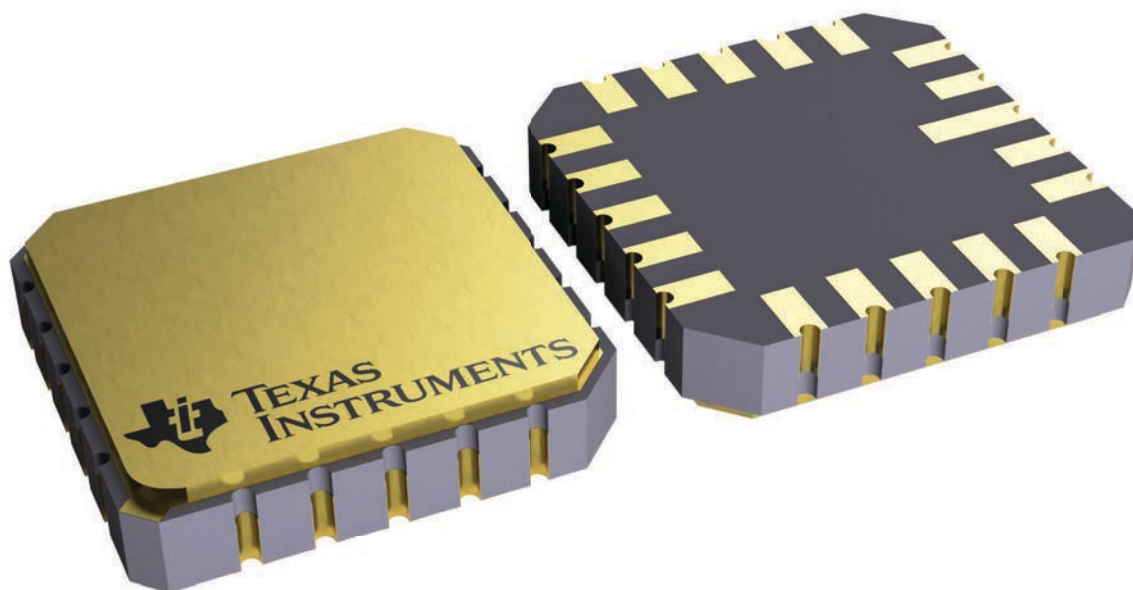
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



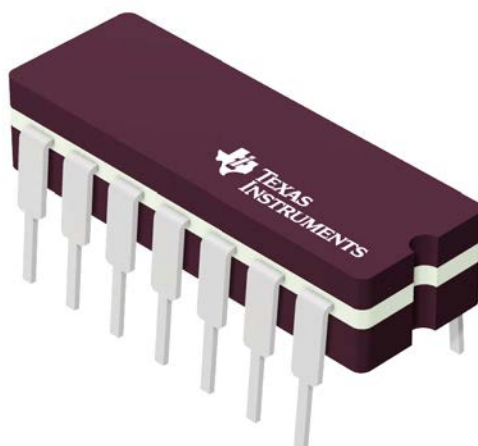
4229370VA\

J 14

GENERIC PACKAGE VIEW

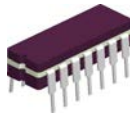
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

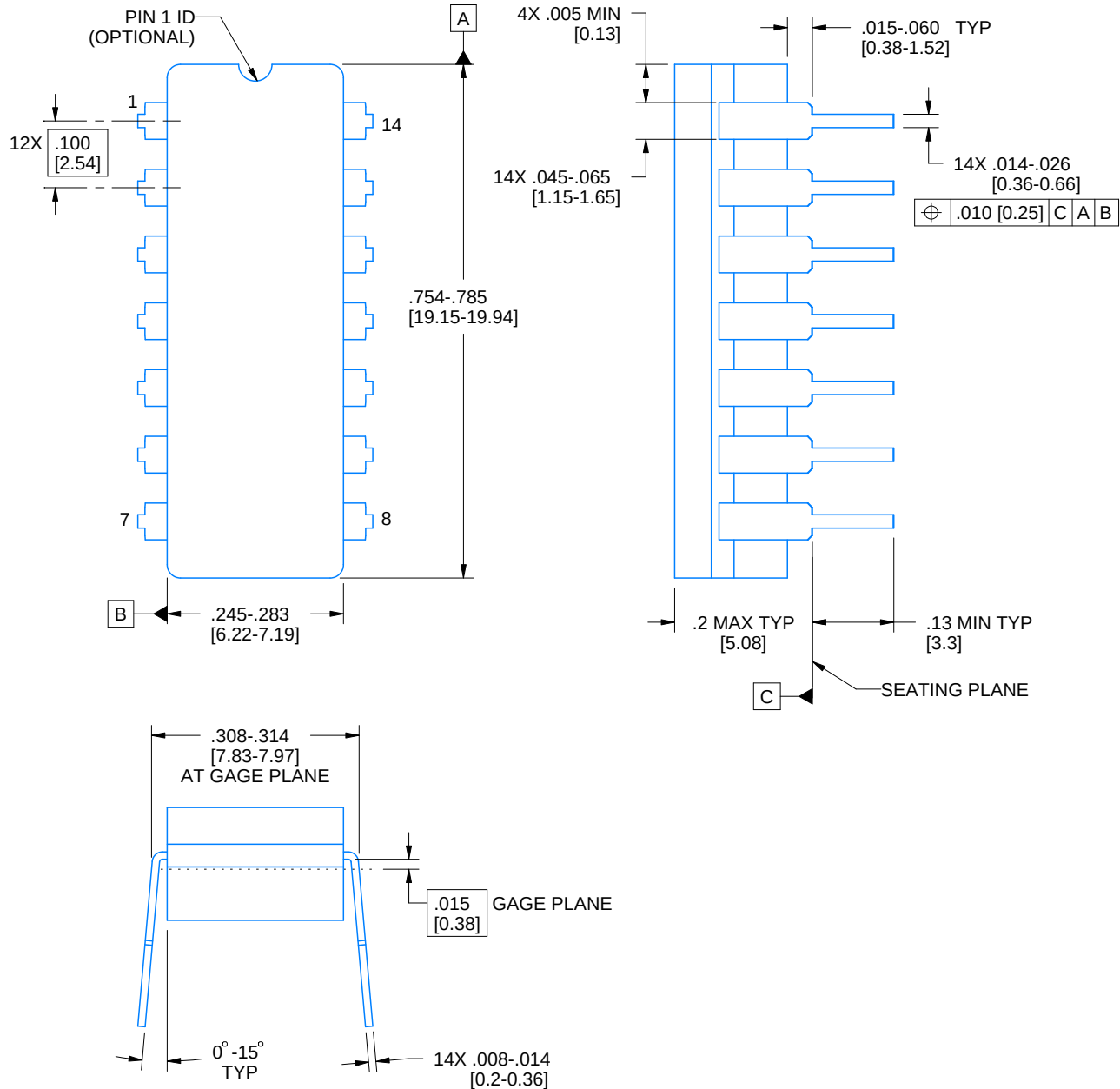


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



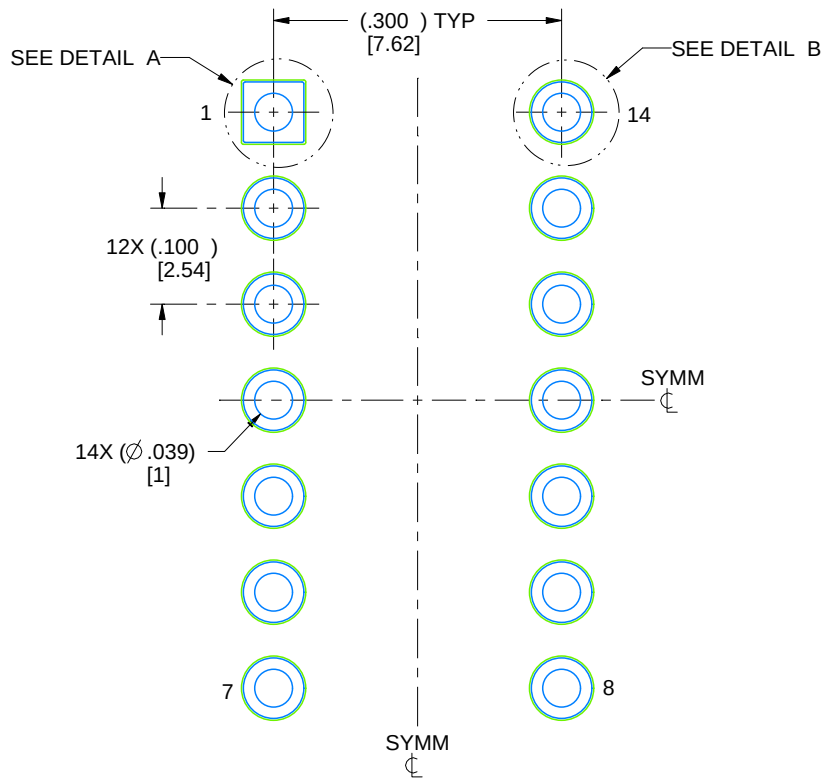
**TEXAS
INSTRUMENTS**
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EXAMPLE BOARD LAYOUT

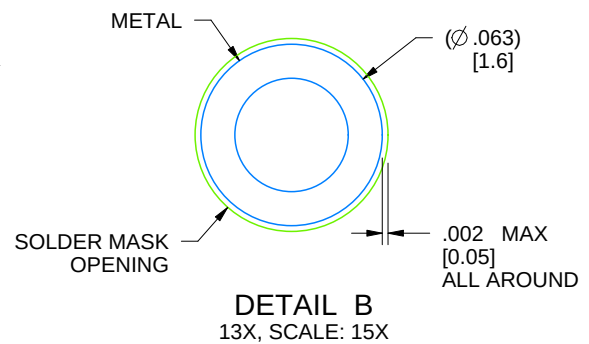
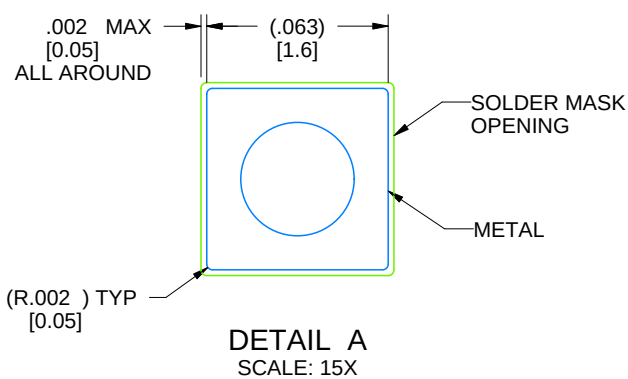
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



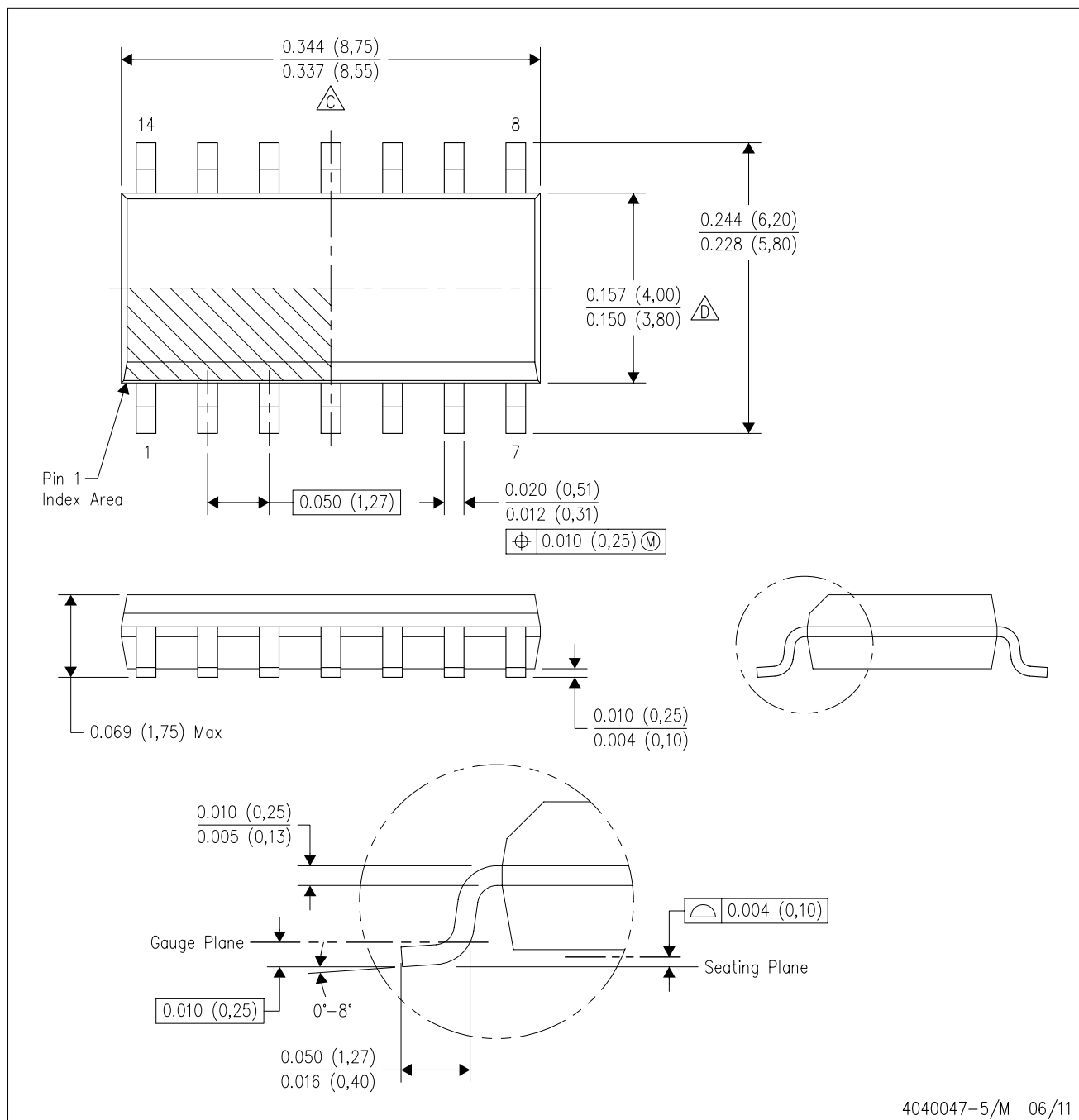
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



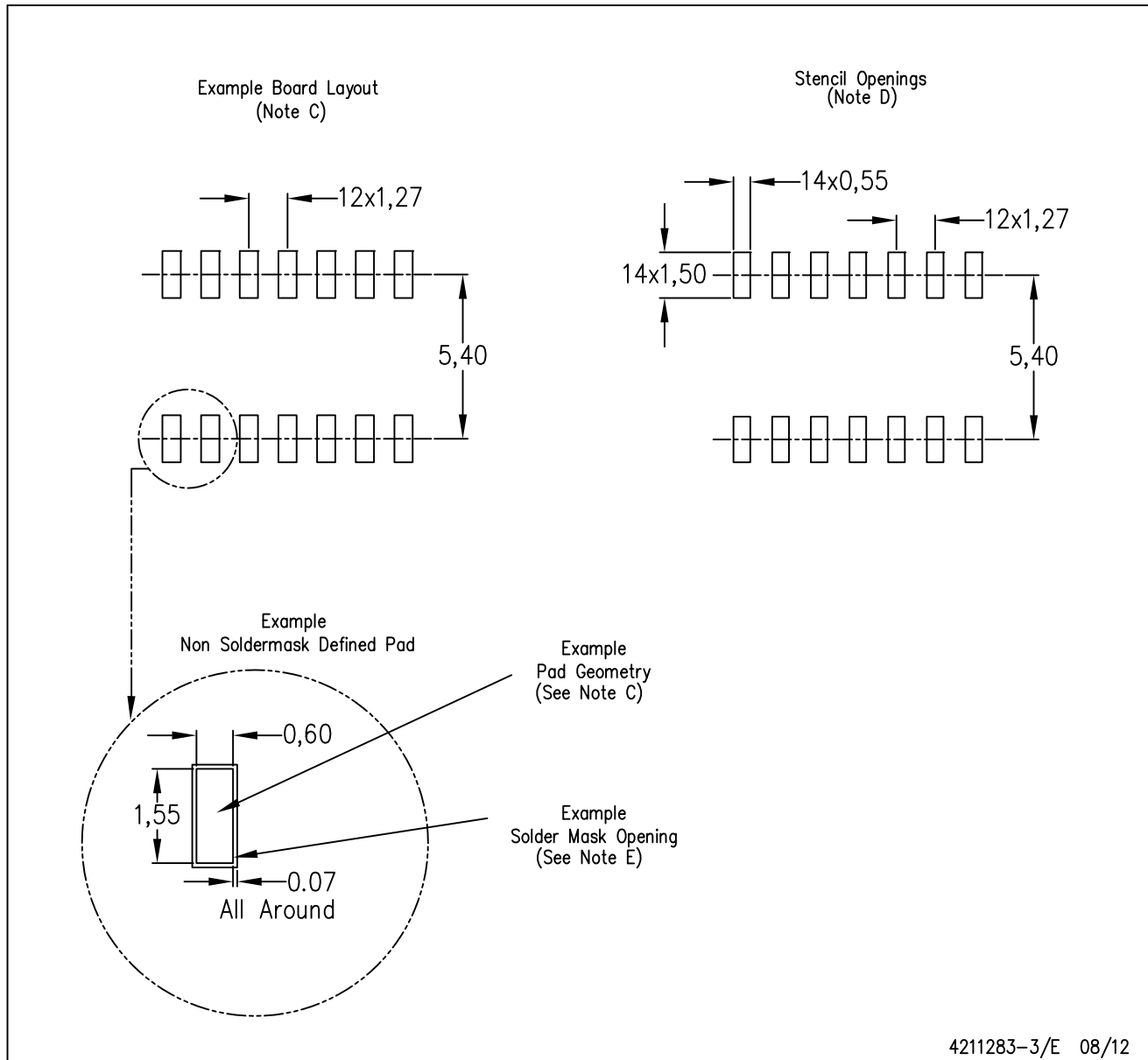
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

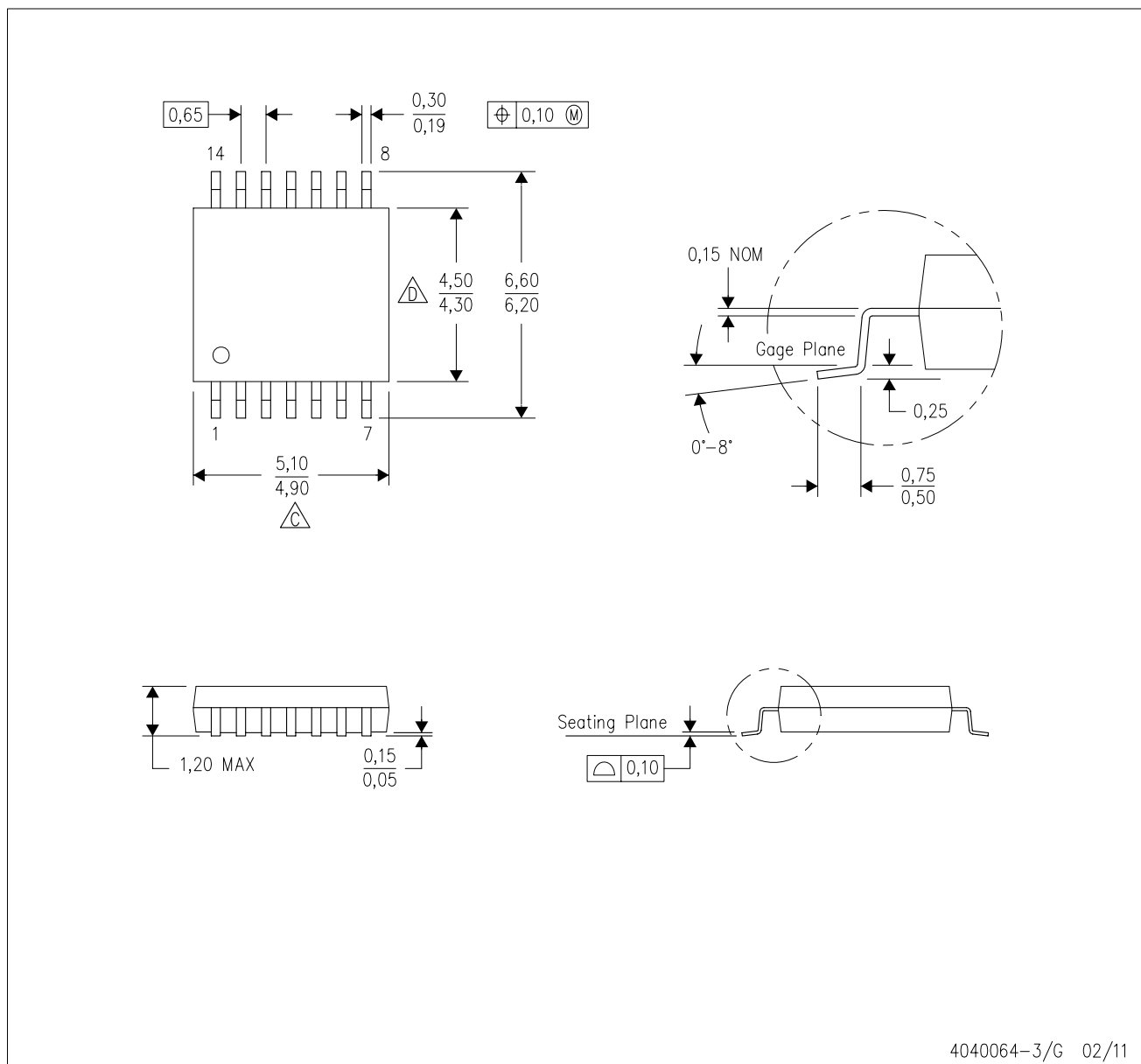
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

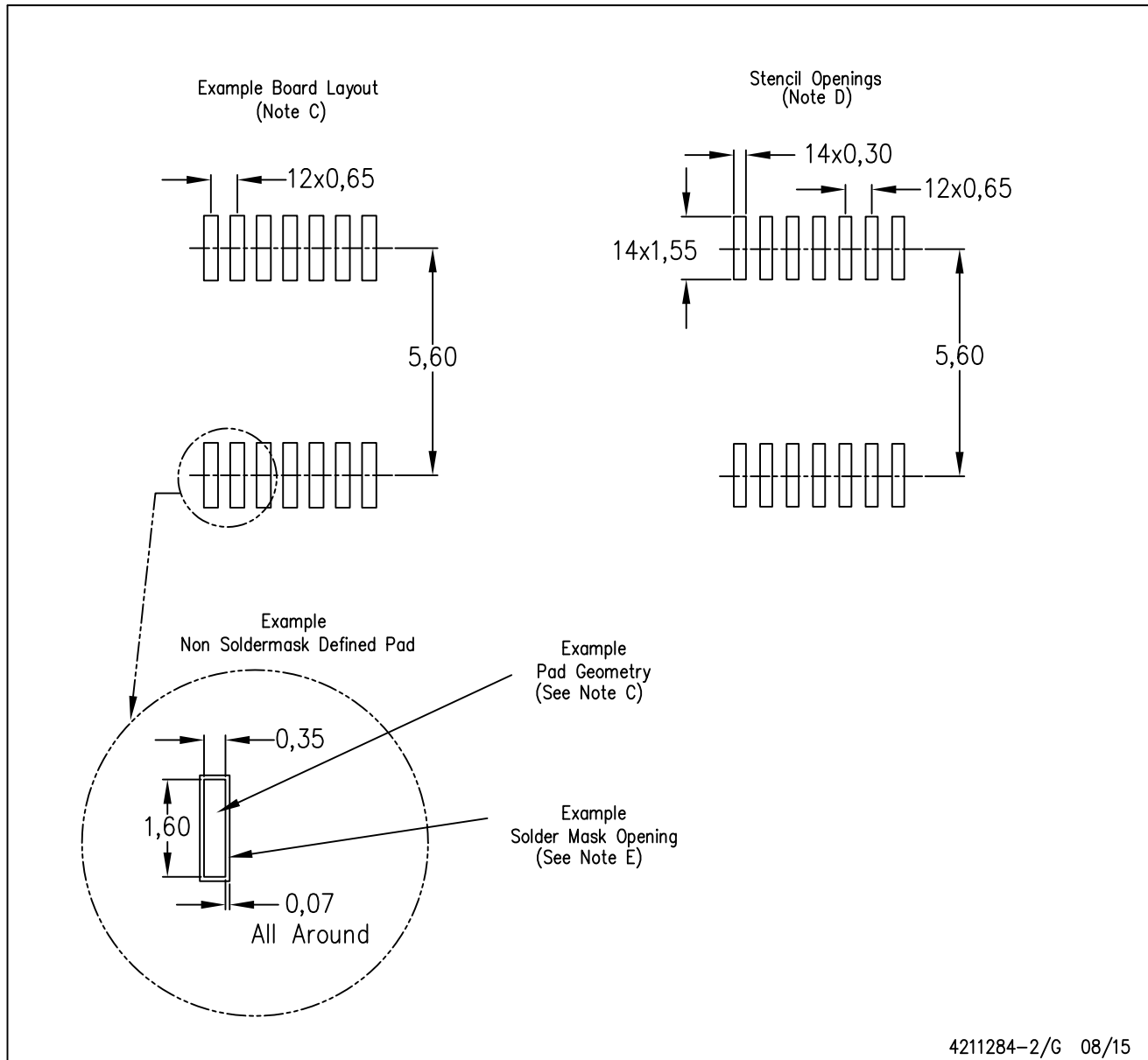


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

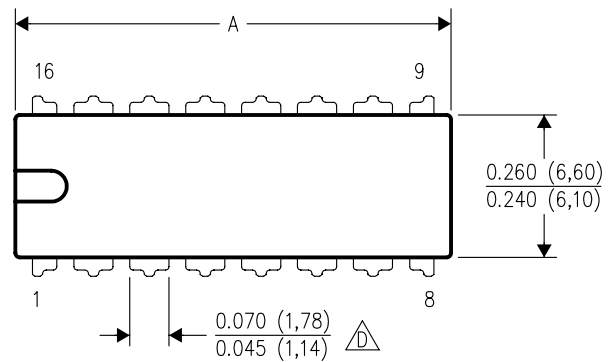


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

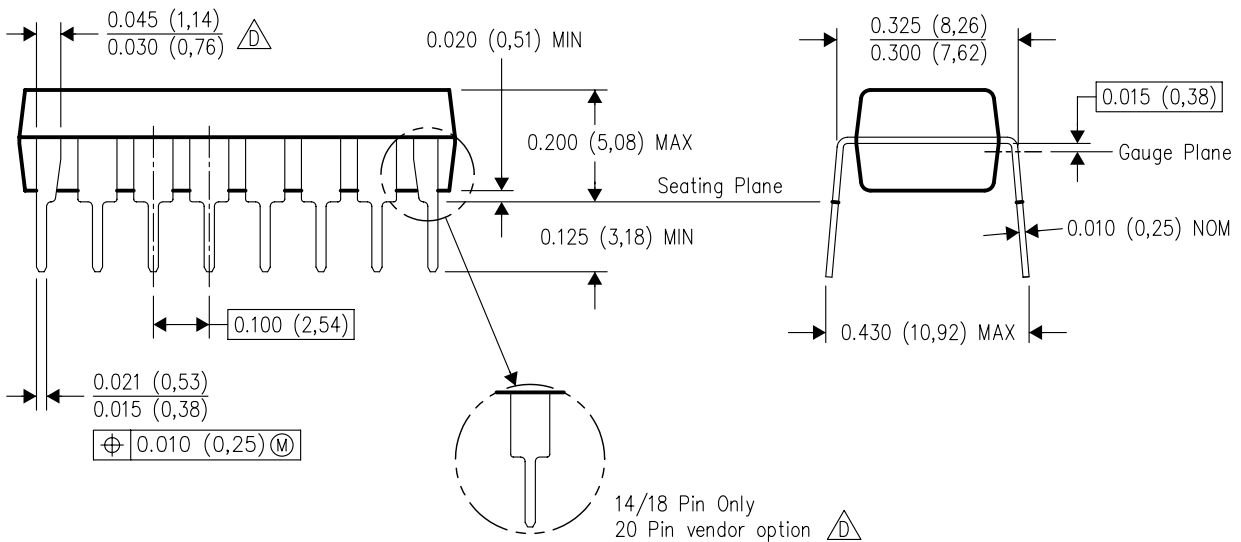
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

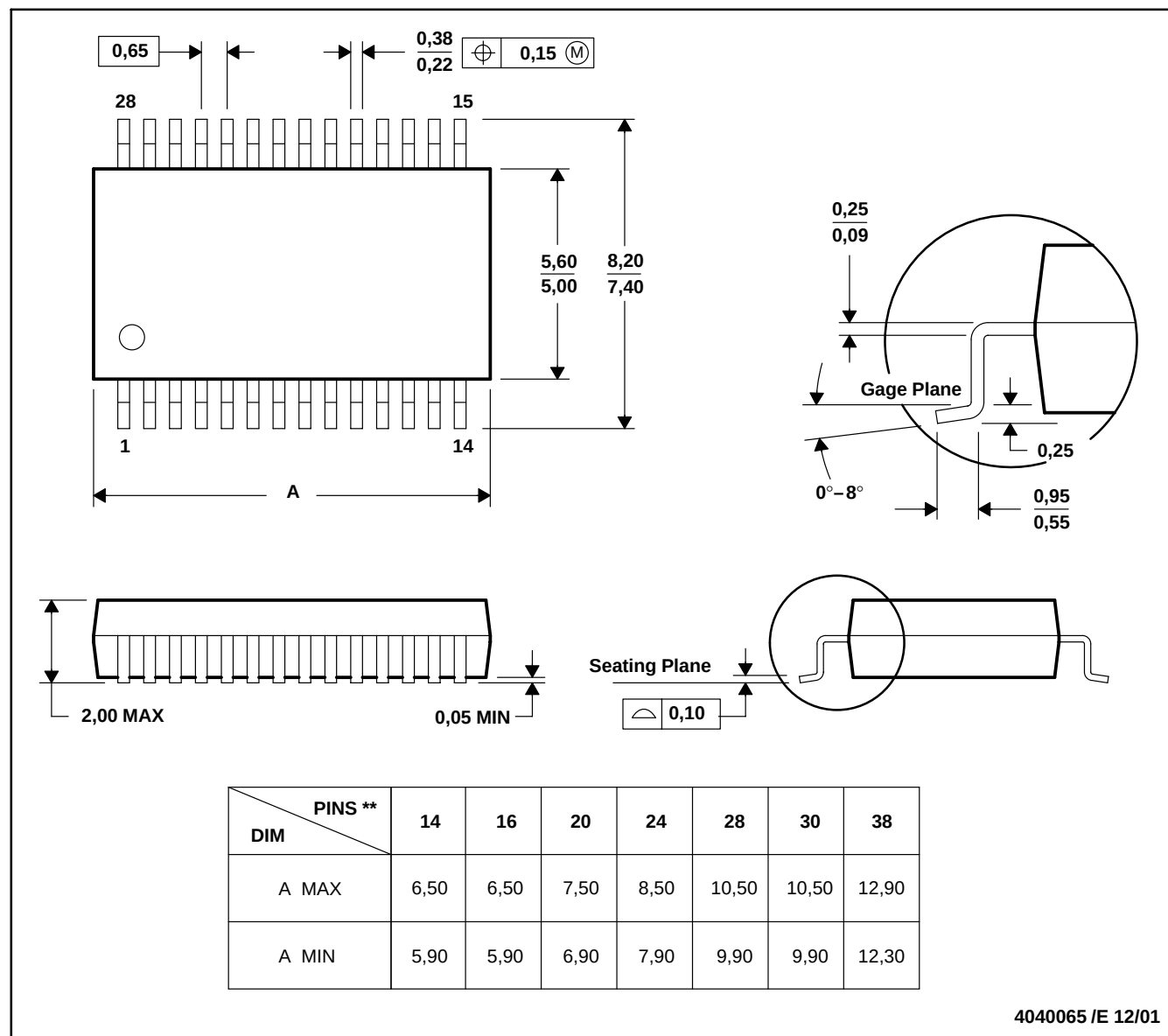
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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