TEXAS INSTRUMENTS
SN65HVD70, SN65HVD71, SN65HVD73
SN65HVD74, SN65HVD76, SN65HVD77
JAJSH84G – MAY 2014 – REVISED OCTOBER 2019

SN65HVD7x 3.3V 電源、全二重 RS-485 トランシーバ、±12kV IEC ESD 保護付き

1 特長

- 1/8 単位負荷のオプションを提供
  - バス上に最大 256 個のノード
- バス I/O 保護
  - ±30kV を超える HBM 保護
  - ±12kV を超える IEC 61000-4-2 接触放電
  - ±4kV を超える IEC 61000-4-4 高速過渡バースト
- 拡張産業用温度範囲：
  -40°C ～ 125°C
- レシーバの大きなヒステリシス (70mV) によるノイズ除去
- 低消費電力
  - 動作中の静止電流 1.1mA 未満
  - 低いスタンバイ時消費電流：標準値 10nA、最大値 5µA 未満
- 電源オンおよび電源オフ時のグリッチ・フリー保護によりホットプラグ・アプリケーションに対応
- 5V 許容のロジック入力、3.3V または 5V のコントローラと互換
- 信号速度オプション：
  400kbps (70、71)、20Mbps (73、74)、50Mbps (76、77) に対して最適化

2 アプリケーション

- e メーター
- 産業用オートメーション
- ビルディング・オートメーション
- セキュリティと監視
- エンコーダ / デコーダ

3 概要

これらのデバイスは、堅牢な 3.3V ドライバおよびレシーバと高レベルの ESD 保護を備えた全二重トランシーバ・ファミリとして、RS-485 ポートフォリオを拡張します。ESD 保護機能には、±30kV を超える HBM、±12kV を超える IEC61000-4-2 接触放電が含まれます。SN65HVD7x デバイスの大きなレシーバ・ヒステリシスは伝導差動ノイズに対する耐性を実現し、その広い温度範囲は過酷な動作環境での高い信頼性を可能にします。SN65HVD7x デバイスは、標準の SOIC パッケージに加えて、占有面積の小さい MSOP パッケージでも提供しています。

これらのデバイスはそれぞれ差動ドライバと差動レシーバを組み合わせたものであり、3.3V 単一電源で動作します。各ドライバおよびレシーバは、全二重バス通信設計用に、独立した入力および出力ピンを備えています。これらのデバイスはいずれも同相電圧範囲が広いため、長いケーブルを使用するマルチポイント・アプリケーションに適しています。

SN65HVD71、SN65HVD74、SN65HVD77 デバイスは、外部イネーブル・ピンなしで完全にイネーブルになります。

SN65HVD70、SN65HVD73、SN65HVD76 デバイスは、アクティブ HIGH のドライバ・イネーブルと、アクティブ LOW のレシーバ・イネーブルを備えています。ドライバとレシーバの両方をディセーブルにすると、5µA 未満の低いスタンバイ電流が得られます。

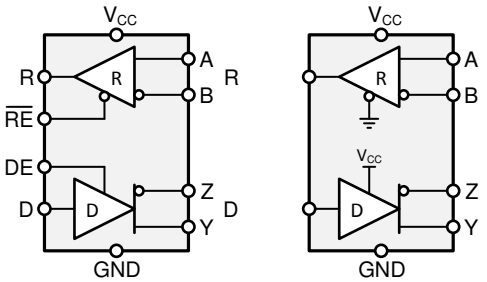
これらのデバイスは、–40°C～125°Cで動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
SN65HVD71	MSOP (8)	3.00mm×3.00mm
SN65HVD74 SN65HVD77	SOIC (8)	4.90mm×3.91mm
SN65HVD70	MSOP (10)	3.00mm×3.00mm
SN65HVD73 SN65HVD76	SOIC (14)	8.65mm×3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック図



SN65HVD70, SN65HVD73, and SN65HVD76　　SN65HVD71, SN65HVD74, and SN65HVD77

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (April 2019) から **Revision G** に変更 **Page**

- Changed device numbers to the 8-Pin DGK package image ... 4
- Changed device numbers to the 10-Pin DGS package image ... 5

Revision E (October 2014) から **Revision F** に変更 **Page**

- Changed the *Pin Configuration* images ... 4
- Changed the Supply Voltage MAX value From: 5.5 V To 5 V in the *Absolute Maximum Ratings* ... 7
- Moved Storage Temperature From the ESD table to the *Absolute Maximum Ratings* ... 7
- Changed the Hadleing Ratings table to *ESD Ratings* ... 7
- Added Note: to Supply voltage in the *Recommended Operating Conditions* ... 7

Revision D (August 2014) から **Revision E** に変更 **Page**

- Updated the MSOP–10 logic diagram ... 5

Revision C (July 2014) から **Revision D** に変更 **Page**

- Updated the *Device Comparison Table* ... 3

Revision B (July 2014) から **Revision C** に変更 **Page**

- Updated SN65HVD70 and SN65HVD71 specifications to production values ... 3

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Revision A (June 2014) から Revision B に変更 **Page**

- Updated the *Device Comparison Table*..... 3
- SN65HVD74 device status changed from *Product Preview* to *Production Data*..... 3

2014年5月発行のものから更新 **Page**

- *デバイスのステータスを「製品プレビュー」から混在ステータスの「量産データ」に* 変更 1

5 Device Comparison Table

PART NUMBER(1)	SIGNALING RATE	DUPLEX	ENABLES	PACKAGE	NODES
SN65HVD70	up to 400 kbps	Full	DE, $\overline{RE}$	SOIC-14 MSOP-10	256
SN65HVD71	up to 400 kbps	Full	None	SOIC-8 MSOP-8	256
SN65HVD73	up to 20 Mbps	Full	DE, $\overline{RE}$	SOIC-14 MSOP-10	256
SN65HVD74	up to 20 Mbps	Full	None	SOIC-8 MSOP-8	256
SN65HVD76	up to 50 Mbps	Full	DE, $\overline{RE}$	SOIC-14 MSOP-10	96
SN65HVD77	up to 50 Mbps	Full	None	SOIC-8 MSOP-8	96

(1) For device status, see the *メカニカル、パッケージ、および注文情報* section.

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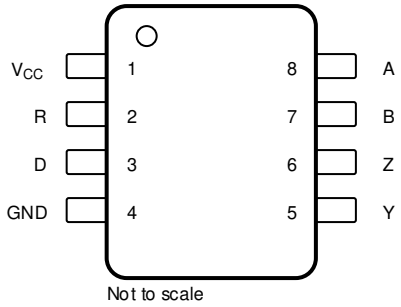
6 Pin Configuration and Functions

SN65HVD71, SN65HVD74, SN65HVD77
8-Pin SOIC, D Package, and 8-Pin MSOP, DGK Package
(Top View)



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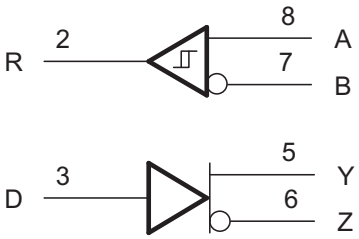

Pin Functions — SOIC-8 and MSOP-8

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{CC}	1	Supply	3-V to 3.6-V supply
R	2	Digital output	Receive data output
D	3	Digital input	Driver data input
GND	4	Reference potential	Local device ground
Y	5	Bus output	Digital bus output, Y (Complementary to Z)
Z	6	Bus output	Digital bus output, Z (Complementary to Y)
B	7	Bus input	Digital bus input, B (Complementary to A)
A	8	Bus input	Digital bus input, A (Complementary to B)

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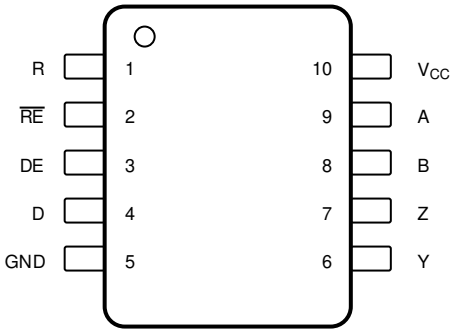
SN65HVD70, SN65HVD73, SN65HVD76
10-Pin MSOP, DGS Package
(Top View)



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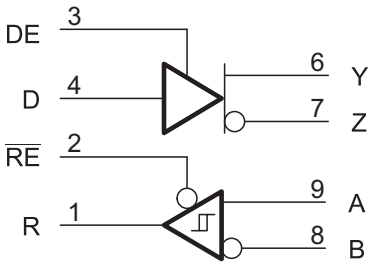

Pin Functions — MSOP–10

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receive enable *Low*
DE	3	Digital input	Driver enable *High*
D	4	Digital input	Driver data input
GND	5	Reference potential	Local device ground
Y	6	Bus output	Digital bus output, Y (Complementary to Z)
Z	7	Bus output	Digital bus output, Z (Complementary to Y)
B	8	Bus input	Digital bus input, B (Complementary to A)
A	9	Bus input	Digital bus input, A (Complementary to B)
V_{CC}	10	Supply	3-V to 3.6-V supply

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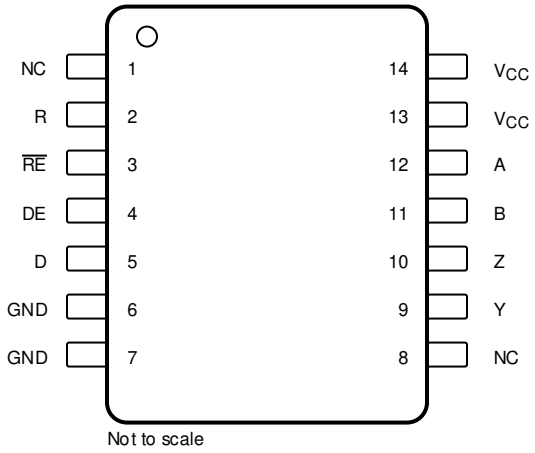
SN65HVD70, SN65HVD73, SN65HVD76
14-Pin SOIC, D Package
(Top View)



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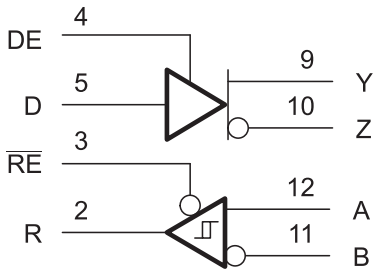

Pin Functions — SOIC-14

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1	No connect	Not connected
	8		
R	2	Digital output	Receive data output
$\overline{RE}$	3	Digital input	Receive enable *Low*
DE	4	Digital input	Driver enable *High*
D	5	Digital input	Driver data input
GND	6 (1)	Reference potential	Local device ground
	7 (1)		
Y	9	Bus output	Digital bus output, Y (Complementary to Z)
Z	10	Bus output	Digital bus output, Z (Complementary to Y)
B	11	Bus input	Digital bus input, B (Complementary to A)
A	12	Bus input	Digital bus input, A (Complementary to B)
V_{CC}	13 (2)	Supply	3-V to 3.6-V supply
	14 (2)		

(1) Pin 6 and pin 7 are connected internally.
(2) Pin 13 and pin 14 are connected internally.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	5	V
Voltage	Range at any bus pin (A, B, Y, or Z)	–13	16.5	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	–0.3	5.7	V
	Voltage input range, transient pulse, any bus pin (A, B, Y, or Z) through 100 Ω	–100	100	V
Output current	Receiver output	–24	24	mA
Junction temperature, T_J			170	°C
Storage temperature range, T_{stg}		–65	150	°C
Continuous total power dissipation		See the *Thermal Information* table		

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JEDEC specification JESD22-A114, all pins	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1500	V
		Machine model (MM), all pins	±300	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND(1)(2)	±12000	V
		IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND	±12000	V
		IEC 61000-4-4 EFT (Fast transient or burst), bus pins and GND	±4000	V
		IEC 60749-26 ESD (Human Body Model), bus pins and GND(2)	±30000	V

(1) By inference from contact-discharge results, see the *Application and Implementation* section
(2) Limited by tester capability.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (1)		3	3.3	3.6	V
V_I	Input voltage at any bus pin (separately or common mode) (2)		–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (Driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, Driver		–60		60	mA
I_O	Output current, Receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD70, HVD71			400	kbps
		HVD73, HVD74			20	Mbps
		HVD76, HVD77			50	
T_A (3)	Operating free-air temperature (See the *Application and Implementation* for thermal information)		–40		125	°C
T_J	Junction Temperature		–40		150	°C

(1) Exposure to conditions beyond the recommended operation maximum for extended periods may affect device reliability.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(3) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating because of internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

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7.4 Thermal Information — D Packages

THERMAL METRIC		D (8 PINS)	D (14 PINS)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	83.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	42.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	37.8	
ψ_{JT}	Junction-to-top characterization parameter	9.2	9.3	
ψ_{JB}	Junction-to-board characterization parameter	50.7	37.5	
$T_{J(TSD)}$	Thermal shut-down junction temperature	170		°C

7.5 Thermal Information — DGS and DGK Packages

THERMAL METRIC		DGS (10 PINS)	DGK (8 PINS)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.5	168.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.7	62.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	86.4	89.5	
ψ_{JT}	Junction-to-top characterization parameter	1.4	7.4	
ψ_{JB}	Junction-to-board characterization parameter	84.8	87.9	
$T_{J(TSD)}$	Thermal shut-down junction temperature	170		°C

7.6 Power Dissipation

PARAMETER			TEST CONDITIONS		VALUE	UNITS
PD	Power Dissipation driver and receiver enabled, V_{CC} = 3.6 V, T_J = 150°C 50% duty cycle square-wave signal at signaling rate: • HVD70 and HVD71 at 400 kbps • HVD73 and HVD74 at 20 Mbps • HVD76 and HVD77 at 50 Mbps	Unterminated	R_L = 300 Ω, C_L = 50 pF (driver)	HVD70, HVD71	150	mW
				HVD73, HVD74	180	
				HVD76, HVD77	220	
		RS-422 load	R_L = 100 Ω, C_L = 50 pF (driver)	HVD70, HVD71	190	mW
				HVD73, HVD74	220	
				HVD76, HVD77	250	
		RS-485 load	R_L = 54 Ω, C_L = 50 pF (driver)	HVD70, HVD71	230	mW
				HVD73, HVD74	255	
				HVD76, HVD77	285	

7.7 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V, See 図 15	1.5	2		V
		R_L = 54 Ω (RS-485), See 図 16	1.5	2		V
		R_L = 100 Ω (RS-422) T_J ≥ 0°C, V_{CC} ≥ 3.2 V, See 図 16	2			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF, See 図 16	–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors, See 図 16	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage		–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage			500		mV
C_{OD}	Differential output capacitance			15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold		See (1)	-70	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold		–200	-140	See (1)	mV
V_{hys}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT-}$)		40	70		mV

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{hys} higher than V_{IT-}.

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Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	Receiver high-level output voltage		I_{OH} = –8 mA			2.4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage		I_{OL} = 8 mA				0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current					–3		3	µA
I_{OZ}	Receiver output high-impedance current	HVD70, HVD73, HVD76	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current					–150		150	mA
I_I	Bus input current (disabled driver)		V_{CC} = 0 to ROC (max), DE = GND	HVD70, HVD73	V_I = 12 V		75	125	µA
					V_I = –7 V	–100	–40		
				HVD76	V_I = 12 V		240	333	
					V_I = –7 V	–267	–180		
I_{CC}	Supply current (quiescent)		Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = GND, No load			750	1100	µA
			Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC}, No load			350	650	µA
			Driver disabled, receiver enabled	DE = GND, $\overline{RE}$ = GND, No load			650	800	µA
			Driver and receiver disabled	$\overline{DE}$ = GND, D = open, $\overline{RE}$ = V_{CC}, No load			0.1	5	µA
	Supply current (dynamic)		See the *Typical Characteristics* section						
T_{sd}	Thermal Shut-down junction temperature							170	°C

7.8 Switching Characteristics — 400 kbps

400-kbps devices (SN65HVD70, SN65HVD71) bit time ≥ 2 µs (over recommended operating conditions)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER								
t_r, t_f	Driver differential output rise/fall time		R_L = 54 Ω, C_L = 50 pF	See 図 17	100	400	750	ns
t_{PHL}, t_{PLH}	Driver propagation delay					350	550	ns
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$						40	ns
t_{PHZ}, t_{PLZ}	Driver disable time	HVD70		See 図 18 and 図 19		50	200	ns
t_{PZH}, t_{PZL}	Driver enable time		Receiver enabled			300	750	ns
			Receiver disabled			3	8	µs
RECEIVER								
t_r, t_f	Receiver output rise/fall time		C_L = 15 pF	See 図 20		13	25	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					70	110	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$						7	ns
t_{PLZ}, t_{PHZ}	Receiver disable time	HVD70				45	60	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time		Driver enabled	See 図 21		20	115	ns
			Driver disabled	See 図 22		3	8	µs

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7.9 Switching Characteristics — 20 Mbps

20-Mbps devices (SN65HVD73, SN65HVD74) bit time ≥ 50 ns (over recommended operating conditions)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER								
t_r, t_f	Driver differential output rise/fall time		R_L = 54 Ω, C_L = 50 pF	See 図 17	4	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay				4	10	20	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0	4	ns
t_{PHZ}, t_{PLZ}	Driver disable time	HVD73		See 図 18 and 図 19		12	25	ns
t_{PZH}, t_{PZL}	Driver enable time		Receiver enabled			10	20	ns
			Receiver disabled			3	8	µs
RECEIVER								
t_r, t_f	Receiver output rise/fall time		C_L = 15 pF	See 図 20		5	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					60	90	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0	5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time	HVD73				17	25	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time		Driver enabled	See 図 21		12	90	ns
			Driver disabled	See 図 22		3	8	µs

7.10 Switching Characteristics — 50 Mbps

50-Mbps devices (SN65HVD76, SN65HVD77) bit time ≥ 20 ns (over recommended operating conditions)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER								
t_r, t_f	Driver differential output rise/fall time		R_L = 54 Ω, C_L = 50 pF	See 図 17	2	3	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay				3	10	16	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0	3.5	ns
t_{PHZ}, t_{PLZ}	Driver disable time	HVD76		See 図 18 and 図 19		10	20	ns
t_{PZH}, t_{PZL}	Driver enable time		Receiver enabled			10	20	ns
			Receiver disabled			3	8	µs
RECEIVER								
t_r, t_f	Receiver output rise/fall time		C_L = 15 pF	See 図 20	1	3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					25	40	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0	2	ns
t_{PLZ}, t_{PHZ}	Receiver disable time	HVD76				8	15	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time		Driver enabled	See 図 21		8	90	ns
			Driver disabled	See 図 22		3	8	µs

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7.11 Typical Characteristics

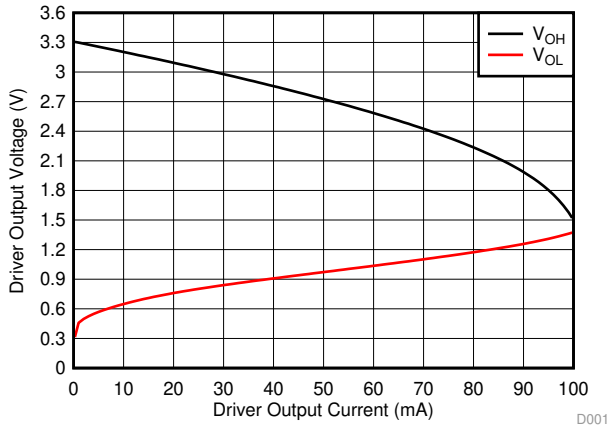

図 1. Driver Output Voltage vs Driver Output Current

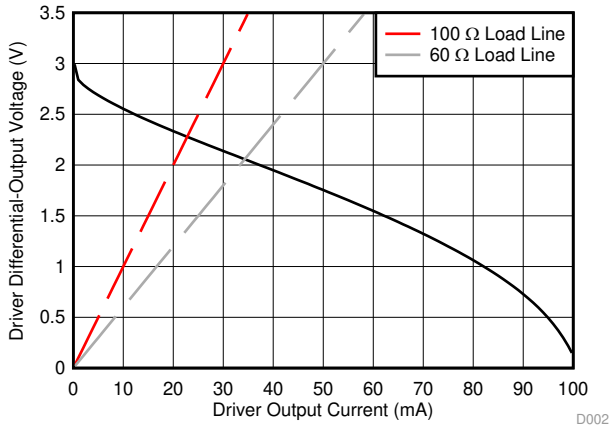

図 2. Driver Differential-Output Voltage vs Driver Output Current

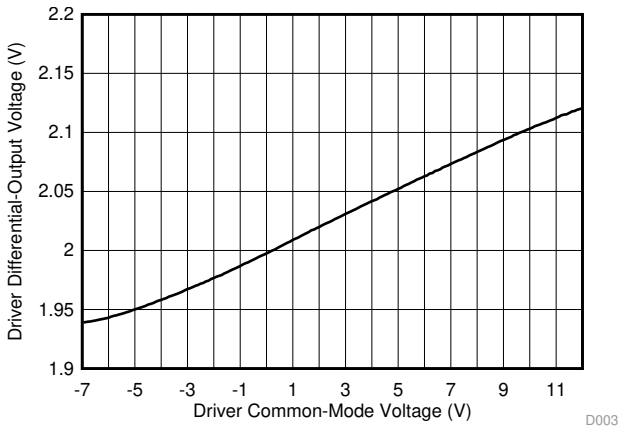

図 3. Driver Differential-Output Voltage vs Driver Common-Mode Voltage

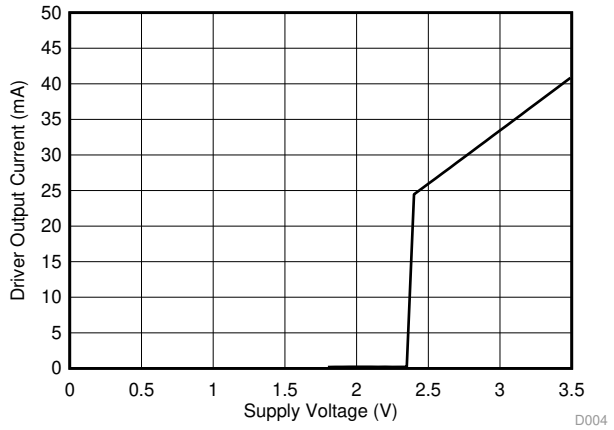

図 4. Driver Output Current vs Supply Voltage

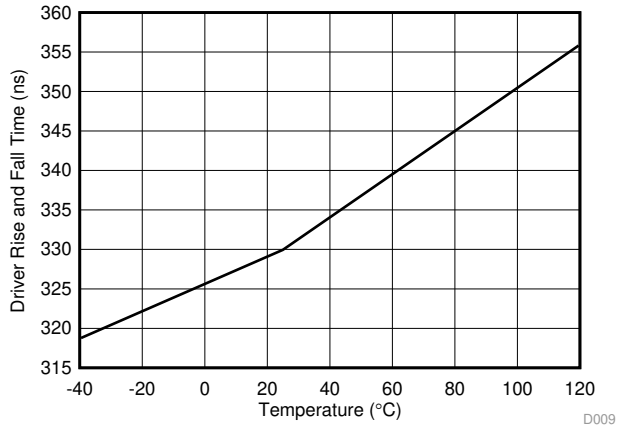

図 5. SN65HVD70, SN65HVD71 Driver Rise and Fall Time vs Temperature

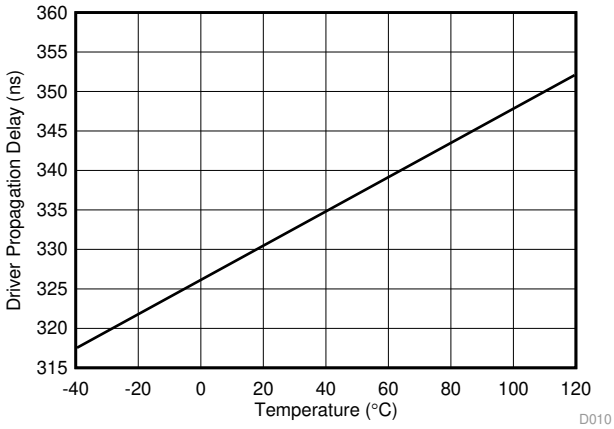

図 6. SN65HVD70, SN65HVD71 Driver Propagation Delay vs Temperature

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Typical Characteristics (continued)

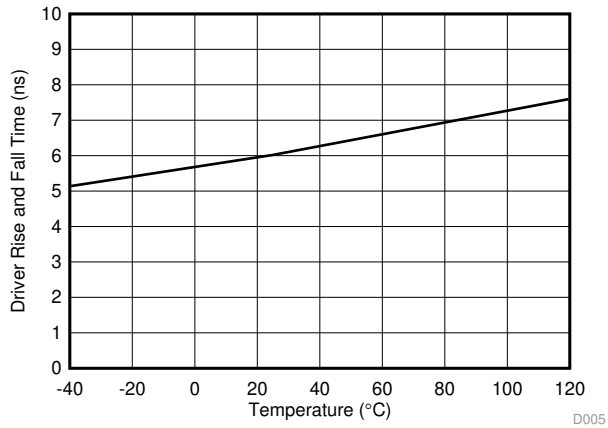

図 7. SN65HVD73, SN65HVD74 Driver Rise and Fall Time vs Temperature

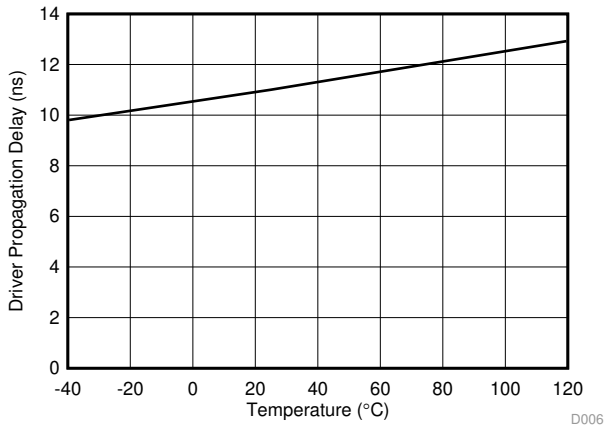

図 8. SN65HVD73, SN65HVD74 Driver Propagation Delay vs Temperature

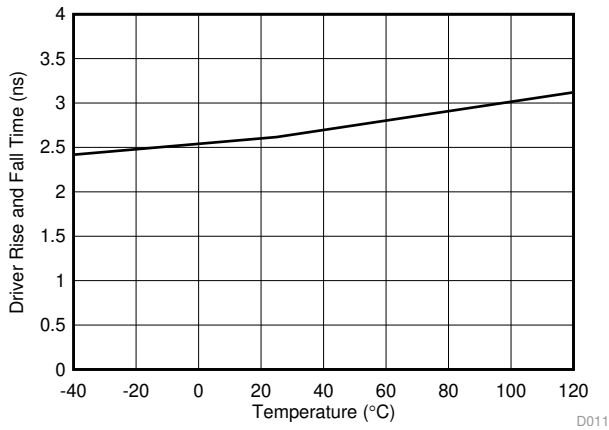

図 9. SN65HVD76, SN65HVD77 Driver Rise and Fall Time vs Temperature

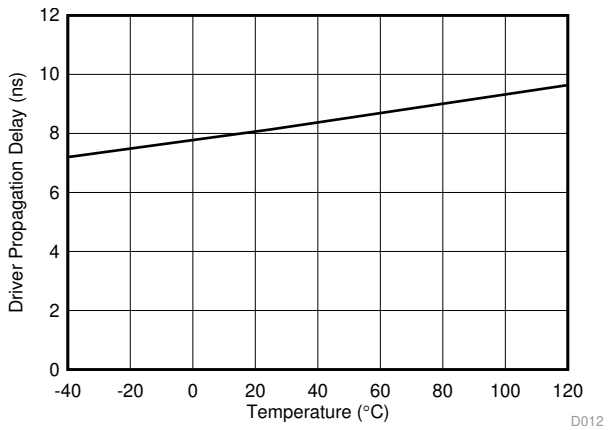

図 10. SN65HVD76, SN65HVD77 Driver Propagation Delay vs Temperature

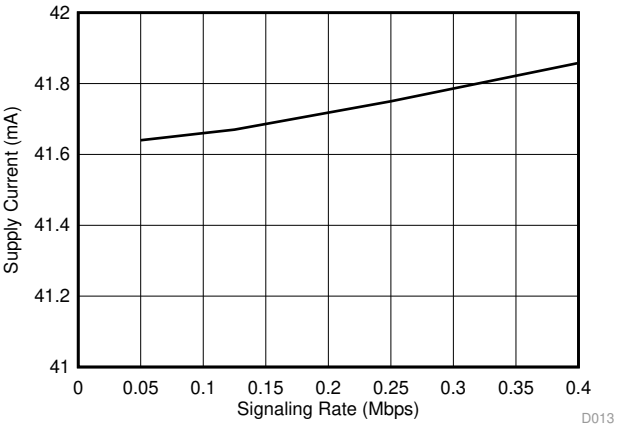

図 11. SN65HVD70, SN65HVD71 Supply Current vs Signal Rate

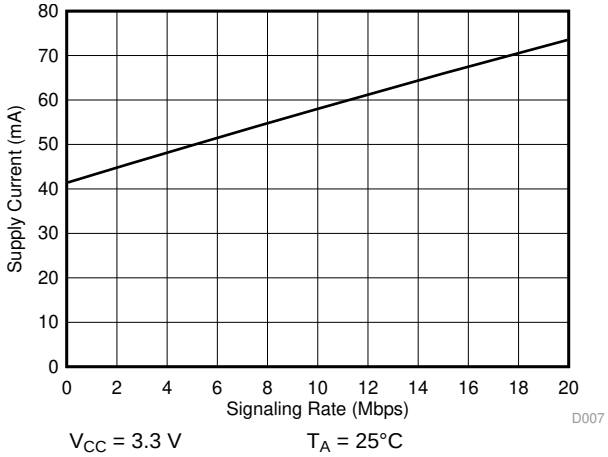

図 12. SN65HVD73, SN65HVD74 Supply Current vs Signal Rate

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Typical Characteristics (continued)

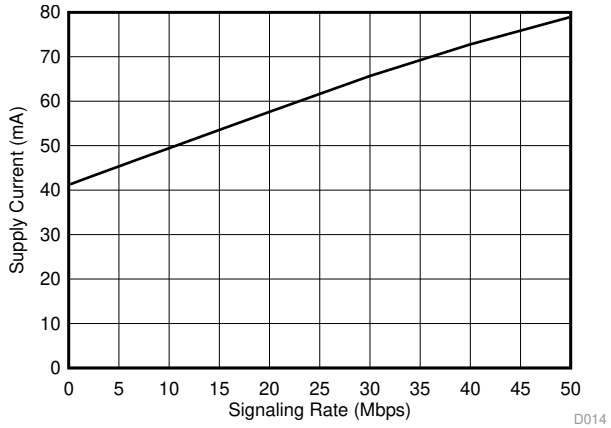


図 13. SN65HVD76, SN65HVD77 Supply Current vs Signal Rate

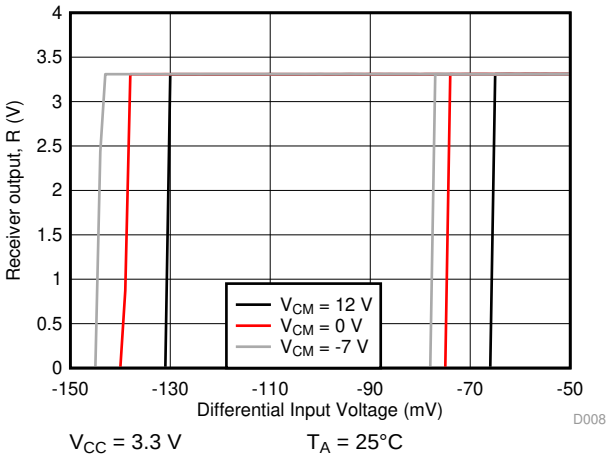


図 14. Receiver Output vs Input

8 Parameter Measurement Information

The input generator rate is 100 kbps with 50% duty cycle, than 6-ns rise and fall times, and 50-Ω output impedance.

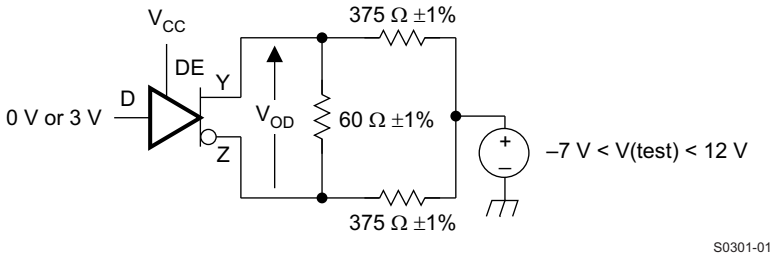


図 15. Measurement of Driver Differential Output Voltage With Common-Mode Load

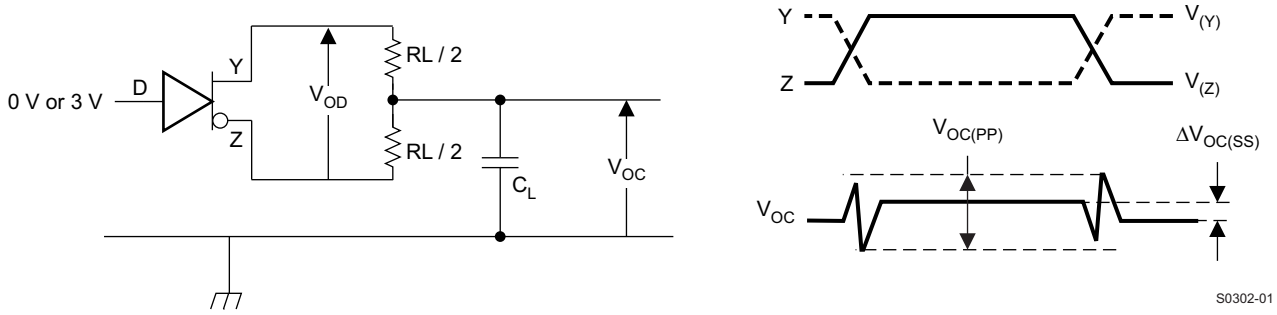


図 16. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

Parameter Measurement Information (continued)

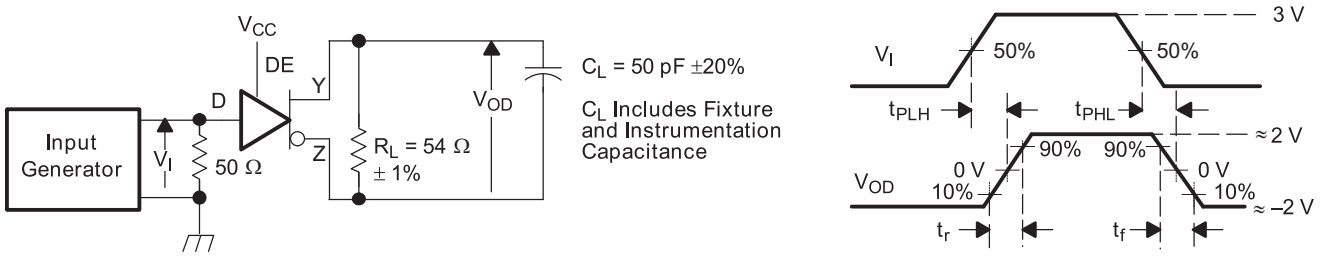
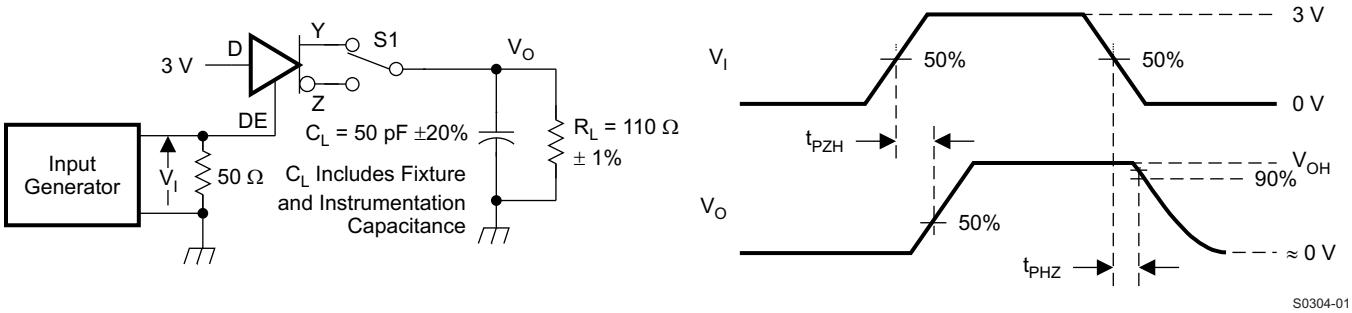
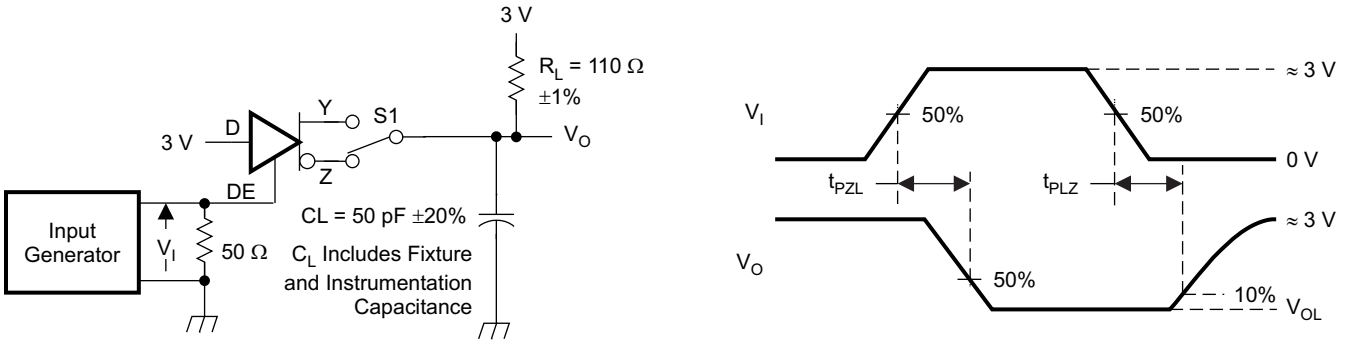


図 17. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

図 18. Measurement of Driver Enable and Disable Times with Active-High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

図 19. Measurement of Driver Enable and Disable Times with Active-Low Output and Pullup Load

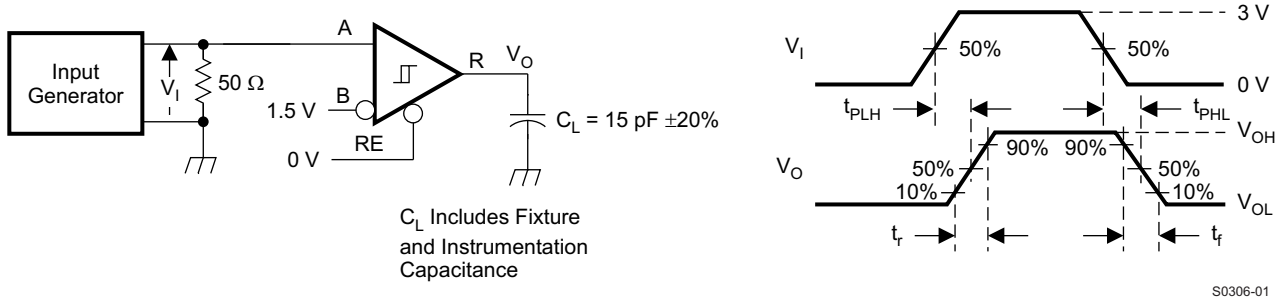


図 20. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

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Parameter Measurement Information (continued)

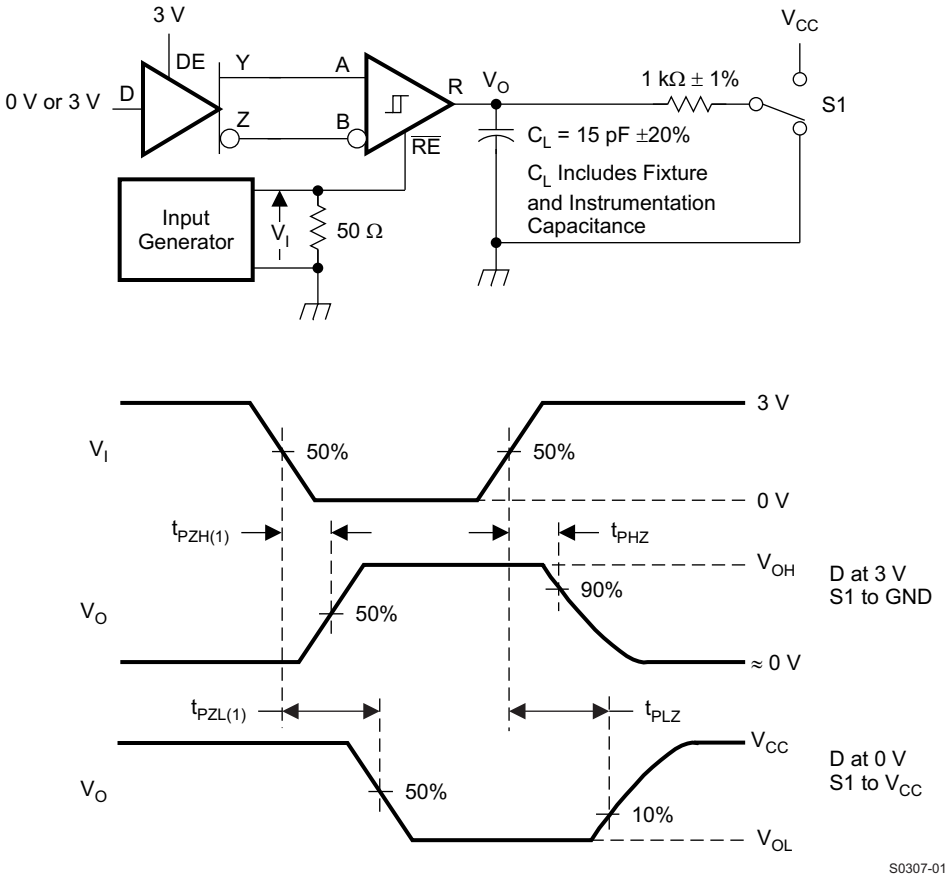

図 21. Measurement of Receiver Enable and Disable Times With Driver Enabled

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Parameter Measurement Information (continued)

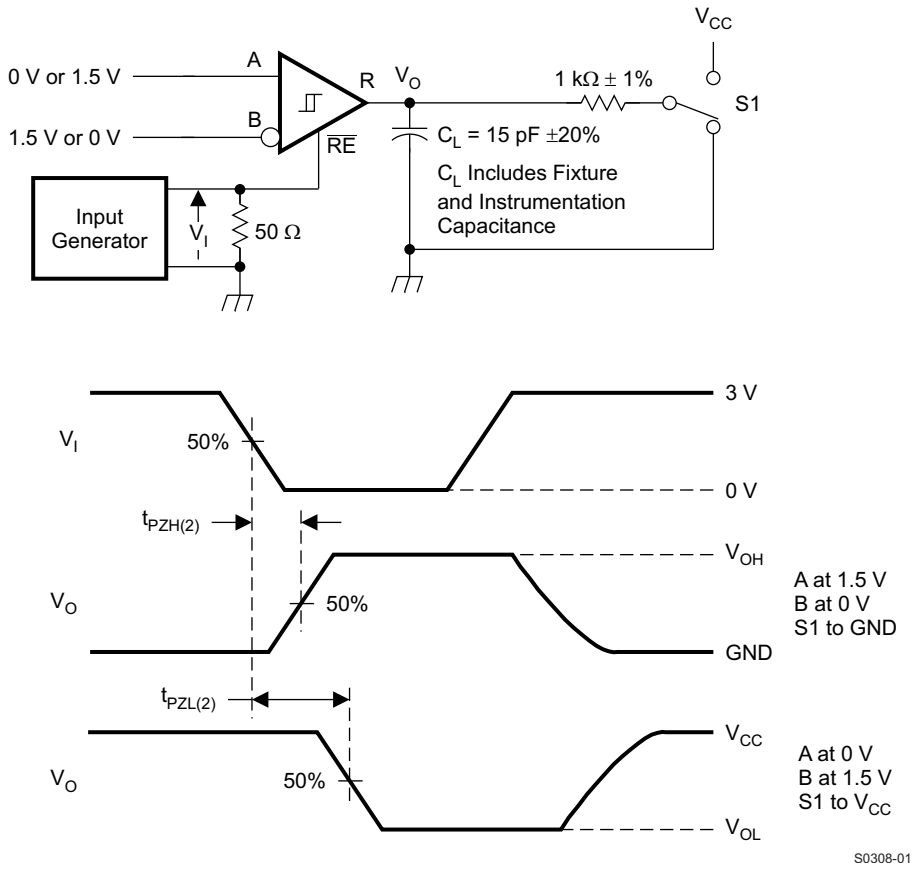

図 22. Measurement of Receiver Enable Times With Driver Disabled

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9 Detailed Description

9.1 Overview

The SN65HVD70, SN65HVD71, SN65HVD73, SN65HVD74, SN65HVD76, and SN65HVD77 devices are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 400 kbps, 20 Mbps, and 50 Mbps.

The SN65HVD71, SN65HVD74, and SN65HVD77 are fully enabled with no external enabling pins. The SN65HVD70, SN65HVD73, and SN65HVD76 have active-high driver enables and active-low receiver enables. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram

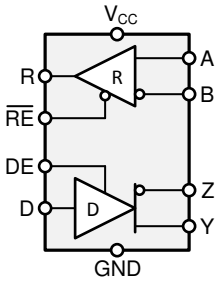

図 23. Block Diagram
SN65HVD70, SN65HVD73, and SN65HVD76

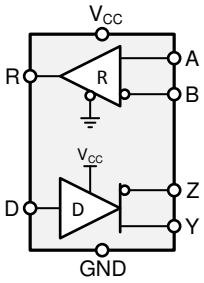

図 24. Block Diagram
SN65HVD71, SN65HVD74, and SN65HVD77

9.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC61000-4-2 of up to ±12 kV, and against electrical fast transients (EFT) according to IEC61000-4-4 of up to ±4 kV.

The SN65HVD7x full-duplex family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –20 mV and an input hysteresis of V_{hys} = 40 mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 120 mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide temperature range from –40°C to 125°C.

9.4 Device Functional Modes

For the SN65HVD70, SN65HVD73, and SN65HVD76, when the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 1. Driver Function Table SN65HVD70, SN65HVD73, SN65HVD76

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drives the bus high
L	H	L	H	Actively drives the bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives the bus high by default

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When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of VID are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table SN65HVD70, SN65HVD73, SN65HVD76

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_{(A)} – V_{(B)}$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receives valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receives valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

For the SN65HVD71, HVD74, and HVD77, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 3. Driver Function Table SN65HVD71, SN65HVD74, SN65HVD77

INPUT	OUTPUTS		FUNCTION
D	Y	Z	
H	H	L	Actively drives the bus High
L	L	H	Actively drives the bus Low
OPEN	H	L	Actively drives the bus High by default

When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 4. Receiver Function Table SN65HVD71, SN65HVD74, SN65HVD77

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_{(A)} – V_{(B)}$	R	
$V_{IT+} < V_{ID}$	H	Receives valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	Receives valid bus Low
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

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9.4.1 Equivalent Circuits

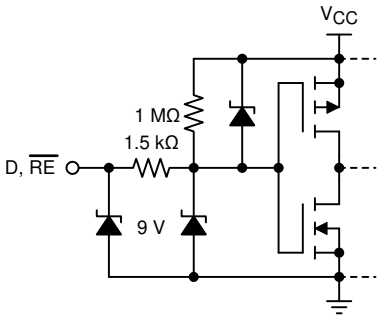

図 25. D and $\overline{RE}$ Inputs

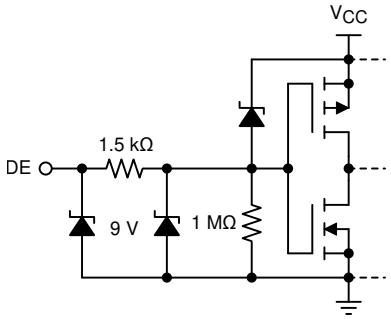

図 26. DE Input

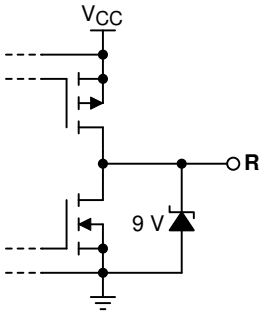

図 27. R Output

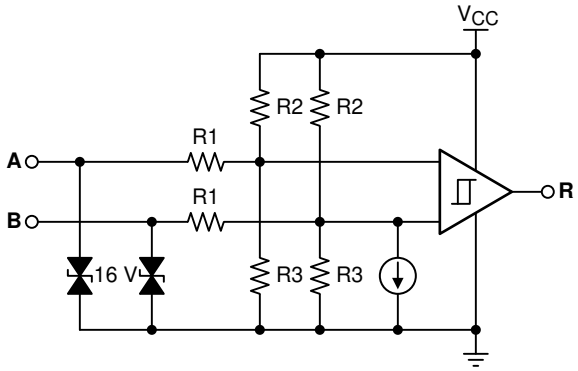

図 28. Receiver Inputs

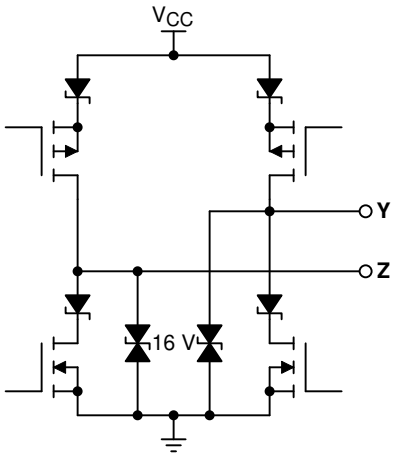

図 29. Driver Outputs

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD7x family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor, $R_{(T)}$, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

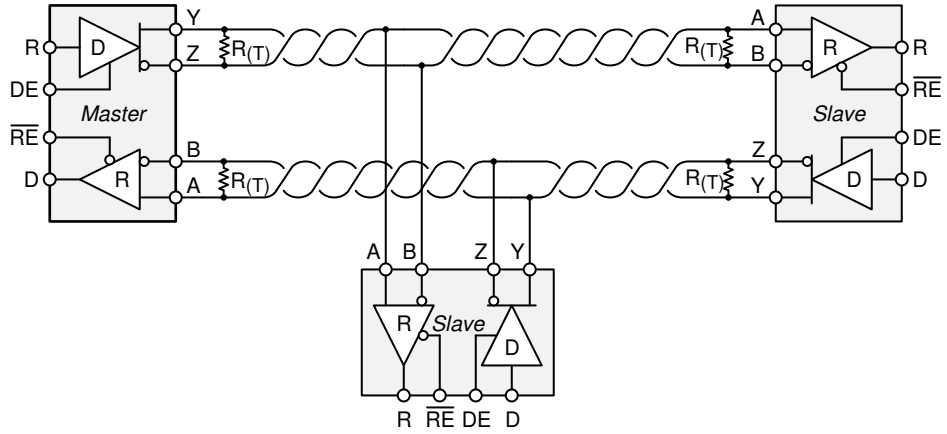

図 30. Typical RS-485 Network With SN65HVD7x Full-Duplex Transceivers

10.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a master driver transmits data to multiple slave receivers. The master driver and slave receivers may remain fully enabled at all times. On the other signal pair, multiple slave drivers transmit data to the master receiver. To avoid bus contention, the slave drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The master receiver may remain fully enabled at all times.

Because the driver may not be disabled, only one driver should be connected to the bus when using the SN65HVD71, SN65HVD74, or SN65HVD77 device.

図 31. Full-Duplex Transceiver Configurations

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Typical Application (continued)

10.2.1 Design Parameters

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

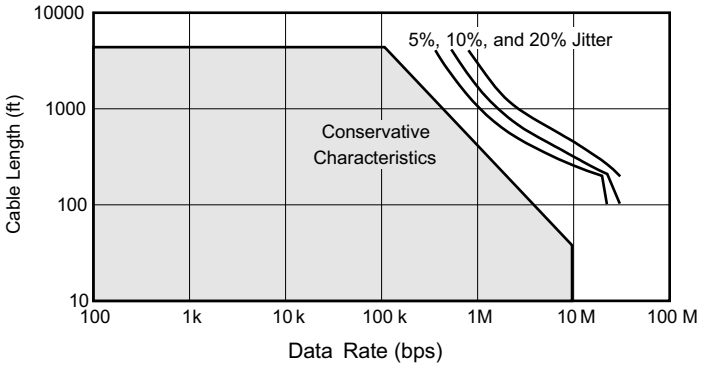

図 32. Cable Length vs Data Rate Characteristic

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

Per 式 1, 表 5 lists the maximum cable-stub lengths for the minimum-driver output rise-times of the SN65HVD7x full-duplex family of transceivers for a signal velocity of 78%.

表 5. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD70	100	2.34	7.7
SN65HVD71	100	2.34	7.7
SN65HVD73	4	0.1	0.3
SN65HVD74	4	0.1	0.3
SN65HVD76	2	0.05	0.15
SN65HVD77	2	0.05	0.15

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10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD7x family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

10.2.1.4 Receiver Failsafe

The differential receivers of the SN65HVD7x family are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{hys} (the separation between V_{IT+} and $V_{IT–}$). As shown in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more than V_{hys} below V_{IT+} will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{hys}, as well as the value of V_{IT+}.

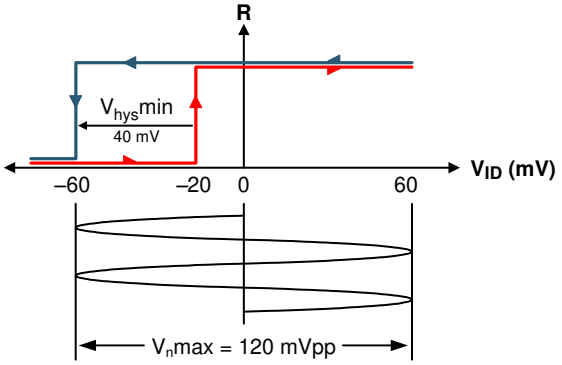

図 33. SN65HVD7x Noise Immunity Under Bus Fault Conditions

10.2.1.5 Transient Protection

The bus pins of the SN65HVD7x full-duplex transceiver family include on-chip ESD protection against ±30-kV HBM and ±12-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from contact discharge test results.

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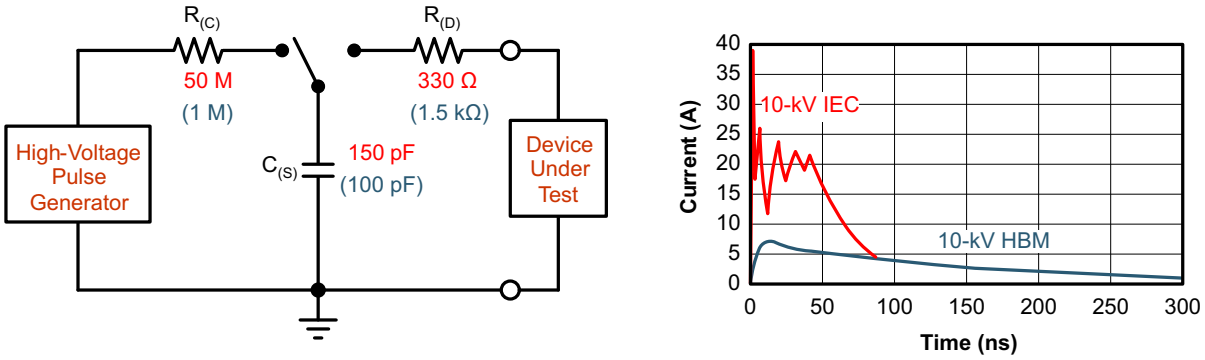

図 34. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 35 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automations.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

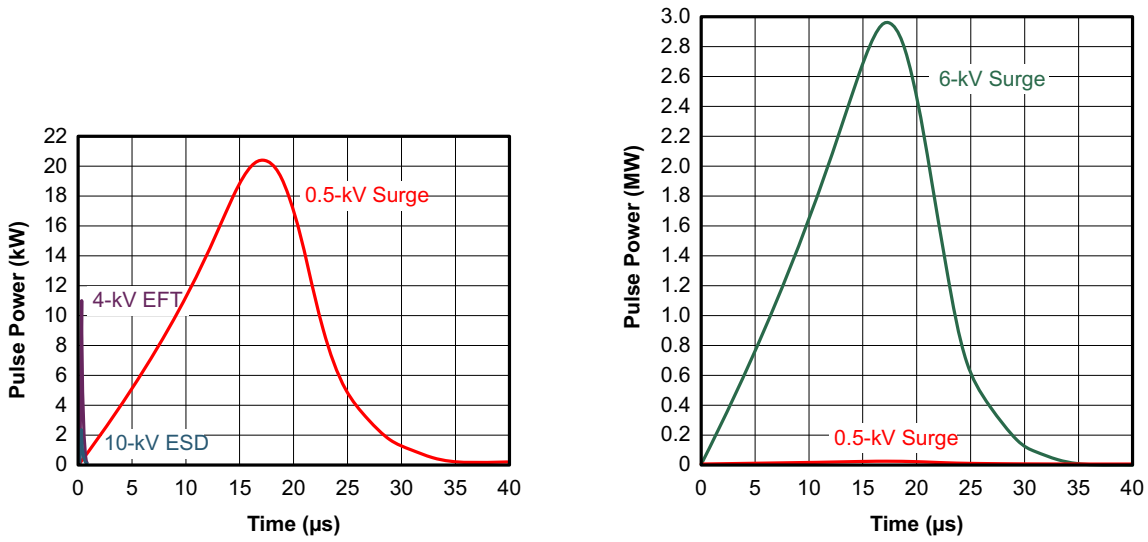

図 35. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 36 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

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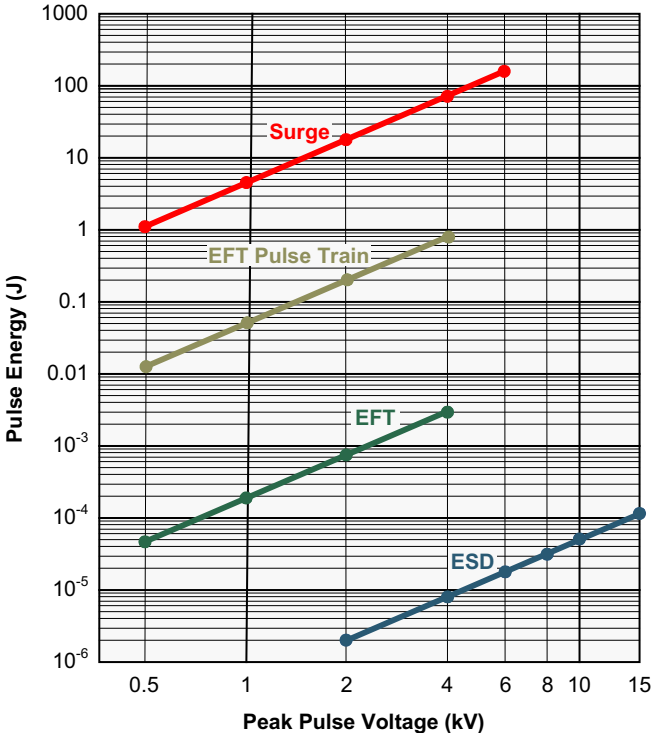

図 36. Comparison of Transient Energies

10.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. 図 37 shows a protection circuit against 16-kV ESD, 4-kV EFT, and 1-kV surge transients.

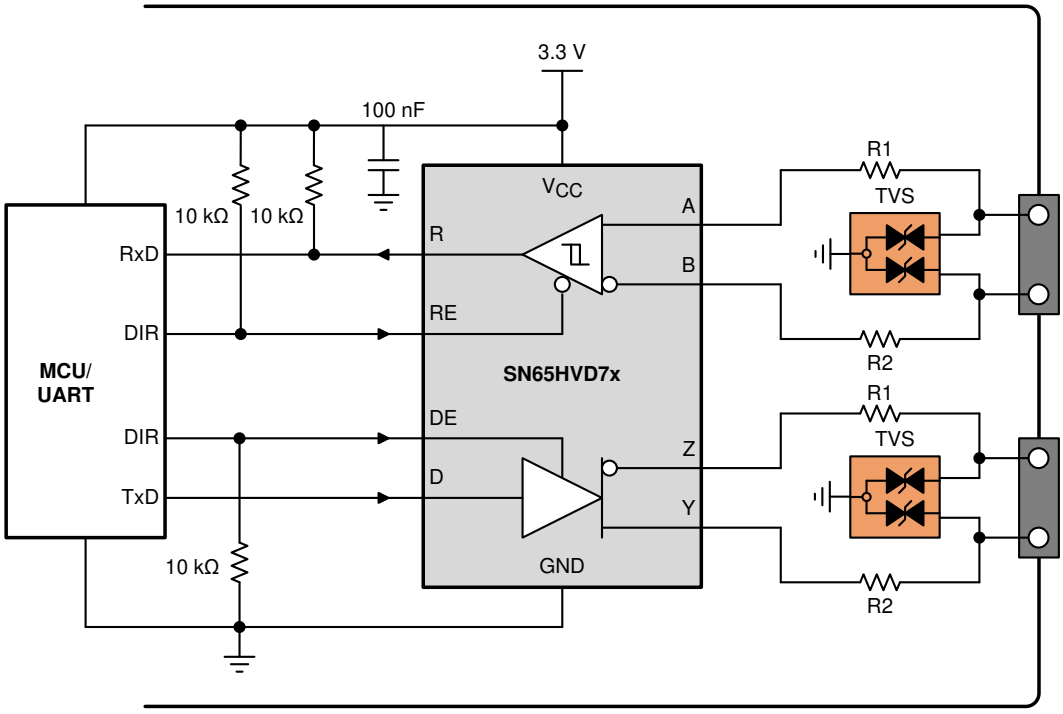

図 37. Transient Protection Against ESD, EFT, and Surge transients

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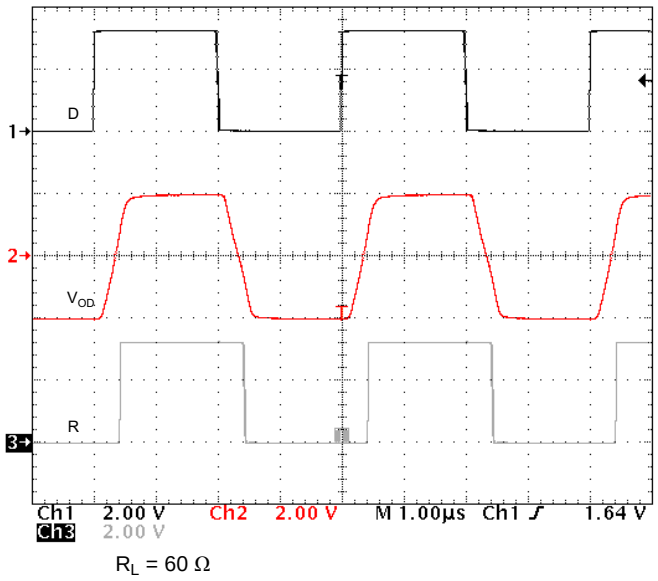
表 6. Bill of Materials

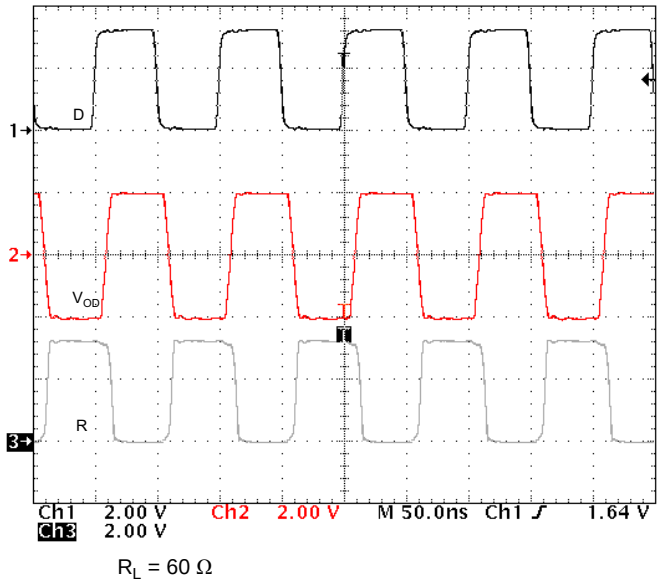
DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, full-duplex RS-485 transceiver	SN65HVD7xD	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

10.2.3 Application Curves



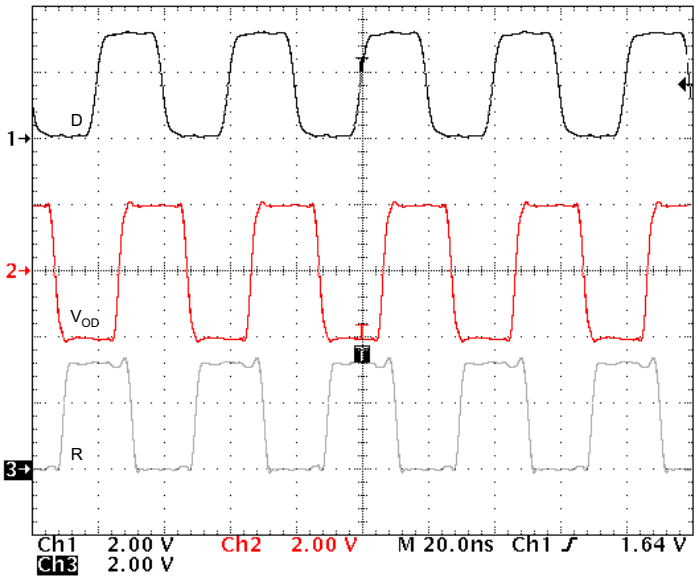
R_L = 60 Ω

図 38. SN65HVD70 and SN65HVD71, 500 kbps



R_L = 60 Ω

図 39. SN65HVD73 and SN65HVD74, 20 Mbps



R_L = 60 Ω

図 40. SN65HVD76 and SN65HVD77, 50 Mbps

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11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3-V supply.

12 Layout

12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design.

For successful PCB design, begin with the design of the protection circuit (see 図 41).

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, controller ICs on the board (see 図 41).
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see 図 41).
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events (see 図 41).
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see 図 41).
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

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12.2 Layout Example

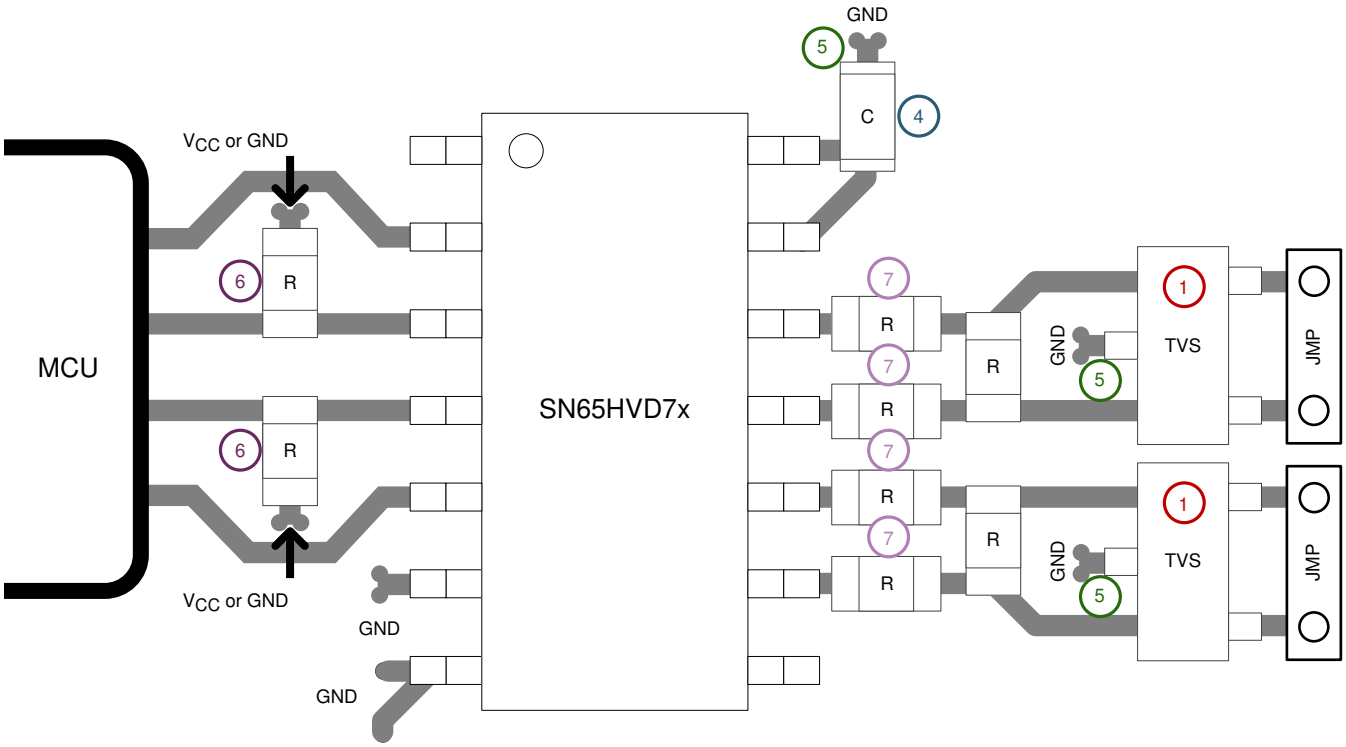

図 41. SN65HVD7x Layout Example

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 デベロッパー・ネットワークの製品に関する免責事項

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13.2 関連リンク

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表 7. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
SN65HVD70	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD71	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD73	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD74	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD76	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
SN65HVD77	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD70D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD70	Samples
SN65HVD70DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VD70	Samples
SN65HVD70DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD70	Samples
SN65HVD70DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD70	Samples
SN65HVD71D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD71	Samples
SN65HVD71DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD71	Samples
SN65HVD71DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD71	Samples
SN65HVD71DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD71	Samples
SN65HVD73D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD73	Samples
SN65HVD73DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD73	Samples
SN65HVD73DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD73	Samples
SN65HVD73DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD73	Samples
SN65HVD74D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD74	Samples
SN65HVD74DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD74	Samples
SN65HVD74DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VD74	Samples
SN65HVD74DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD74	Samples
SN65HVD76D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD76	Samples
SN65HVD76DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD76	Samples
SN65HVD76DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VD76	Samples
SN65HVD76DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD76	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD77D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD77	Samples
SN65HVD77DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD77	Samples
SN65HVD77DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VD77	Samples
SN65HVD77DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD77	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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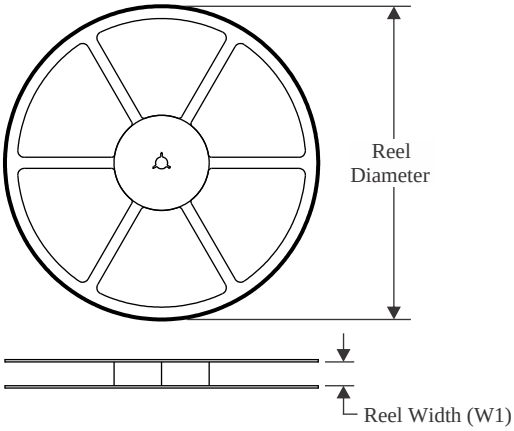
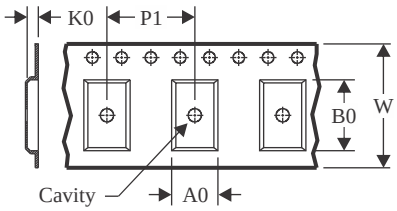
TAPE AND REEL INFORMATION

REEL DIMENSIONS

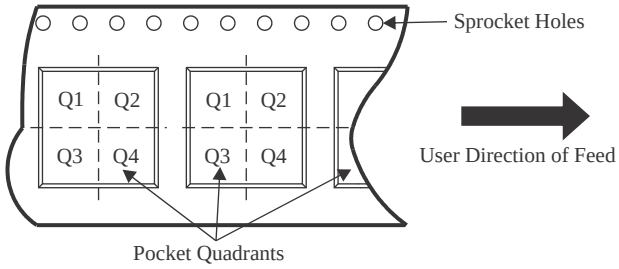


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

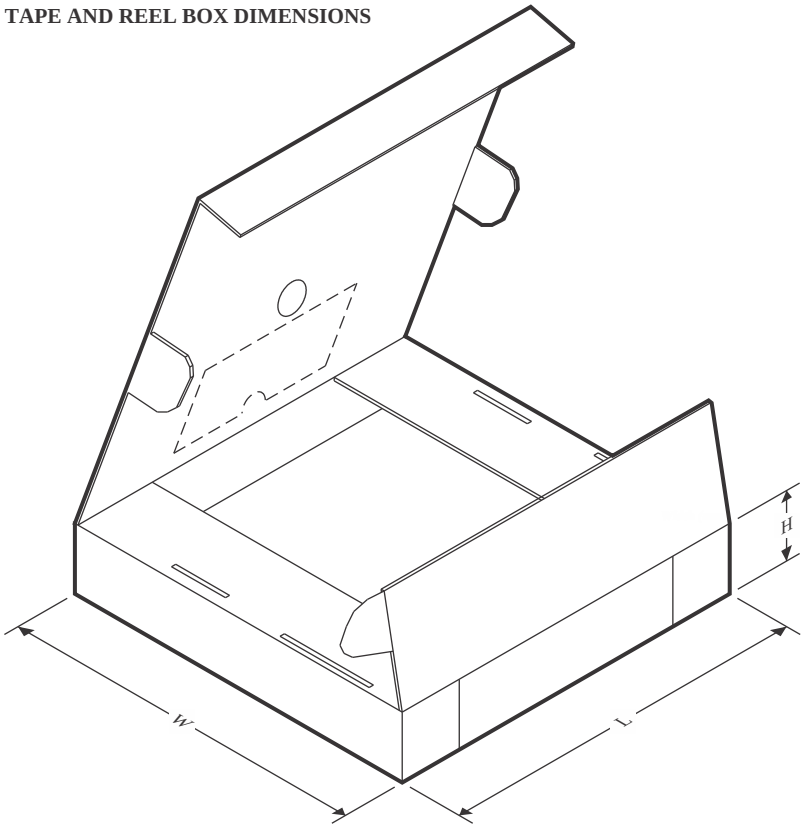
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD70DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD70DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD71DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD71DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD73DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD74DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD76DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD76DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD77DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD77DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

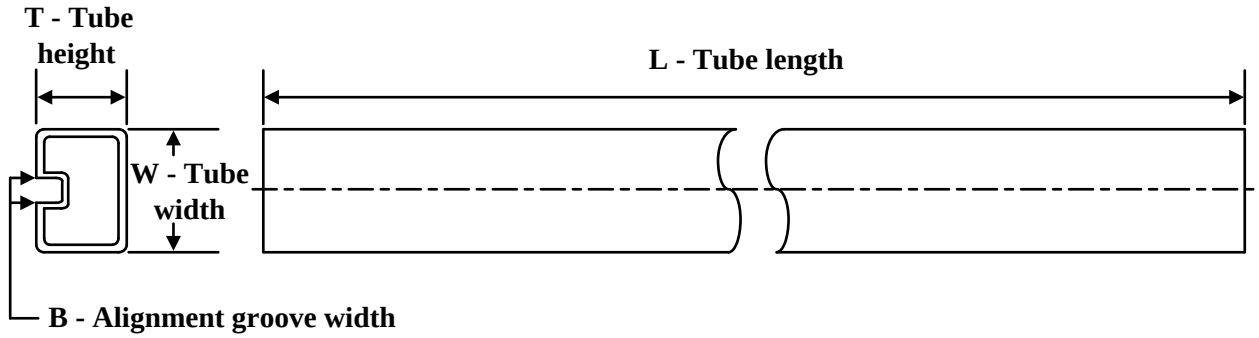
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD70DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
SN65HVD70DR	SOIC	D	14	2500	340.5	336.1	32.0
SN65HVD71DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD71DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD73DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
SN65HVD74DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD76DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD76DR	SOIC	D	14	2500	340.5	336.1	32.0
SN65HVD77DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD77DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

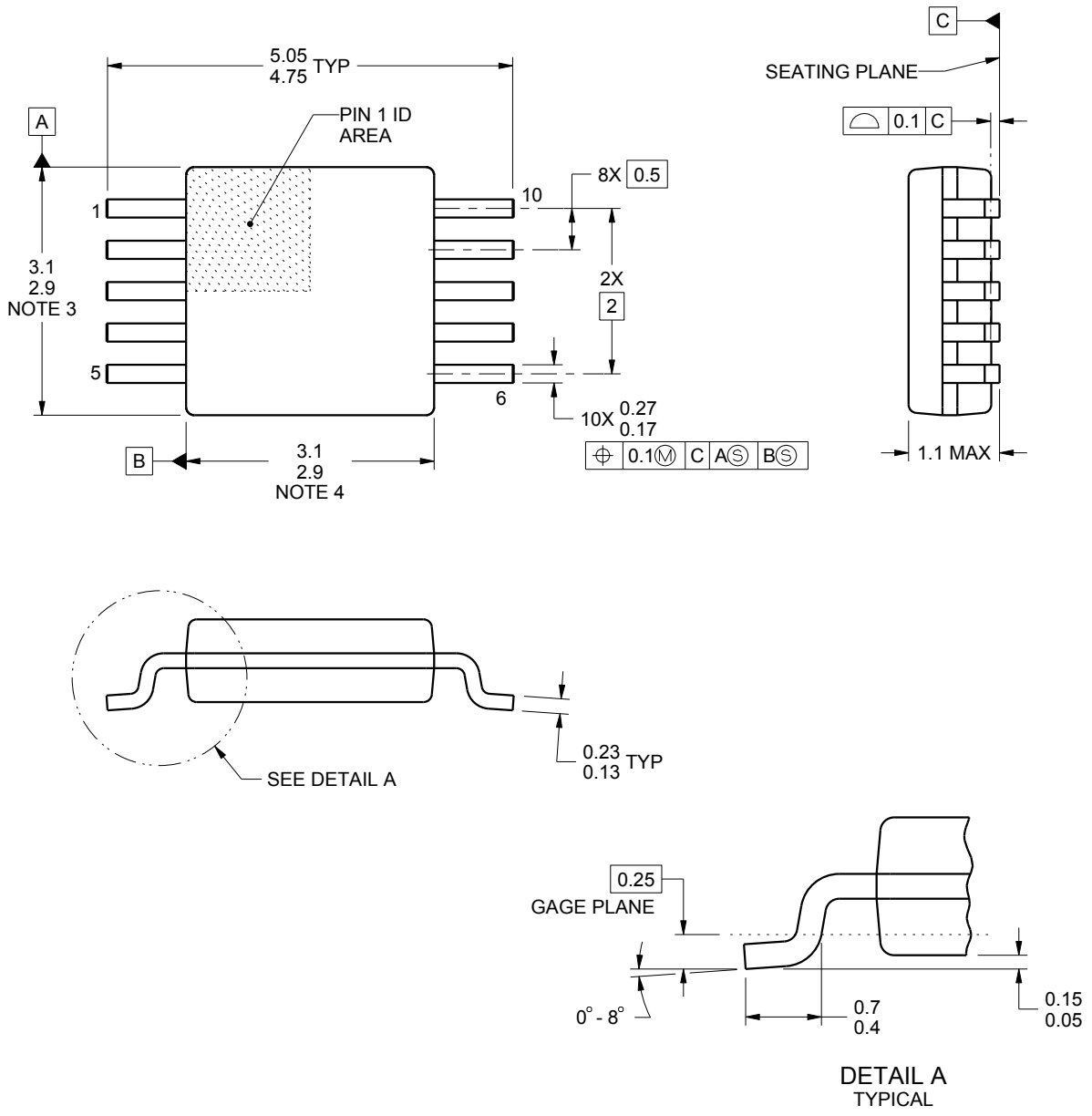
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD70D	D	SOIC	14	50	507	7.85	3750	2.24
SN65HVD70DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
SN65HVD71D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD71DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
SN65HVD73D	D	SOIC	14	50	507	7.85	3750	2.24
SN65HVD73DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
SN65HVD74D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD74DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
SN65HVD76D	D	SOIC	14	50	507	7.85	3750	2.24
SN65HVD76DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
SN65HVD77D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD77DGK	DGK	VSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

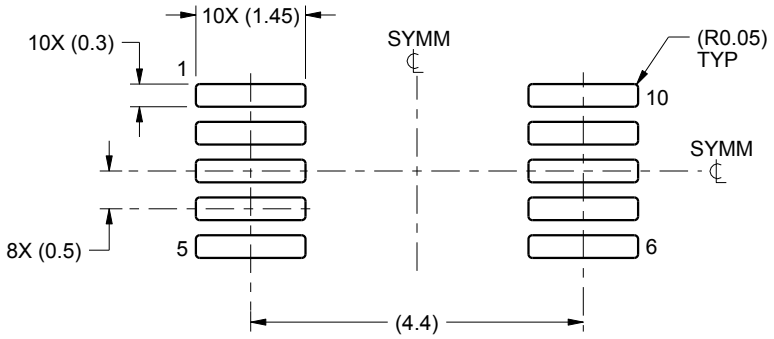
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

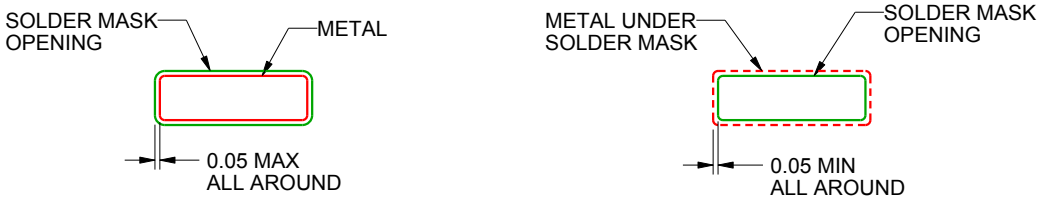


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

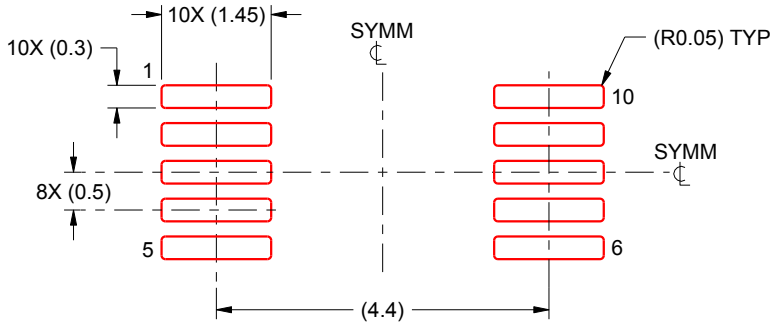


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



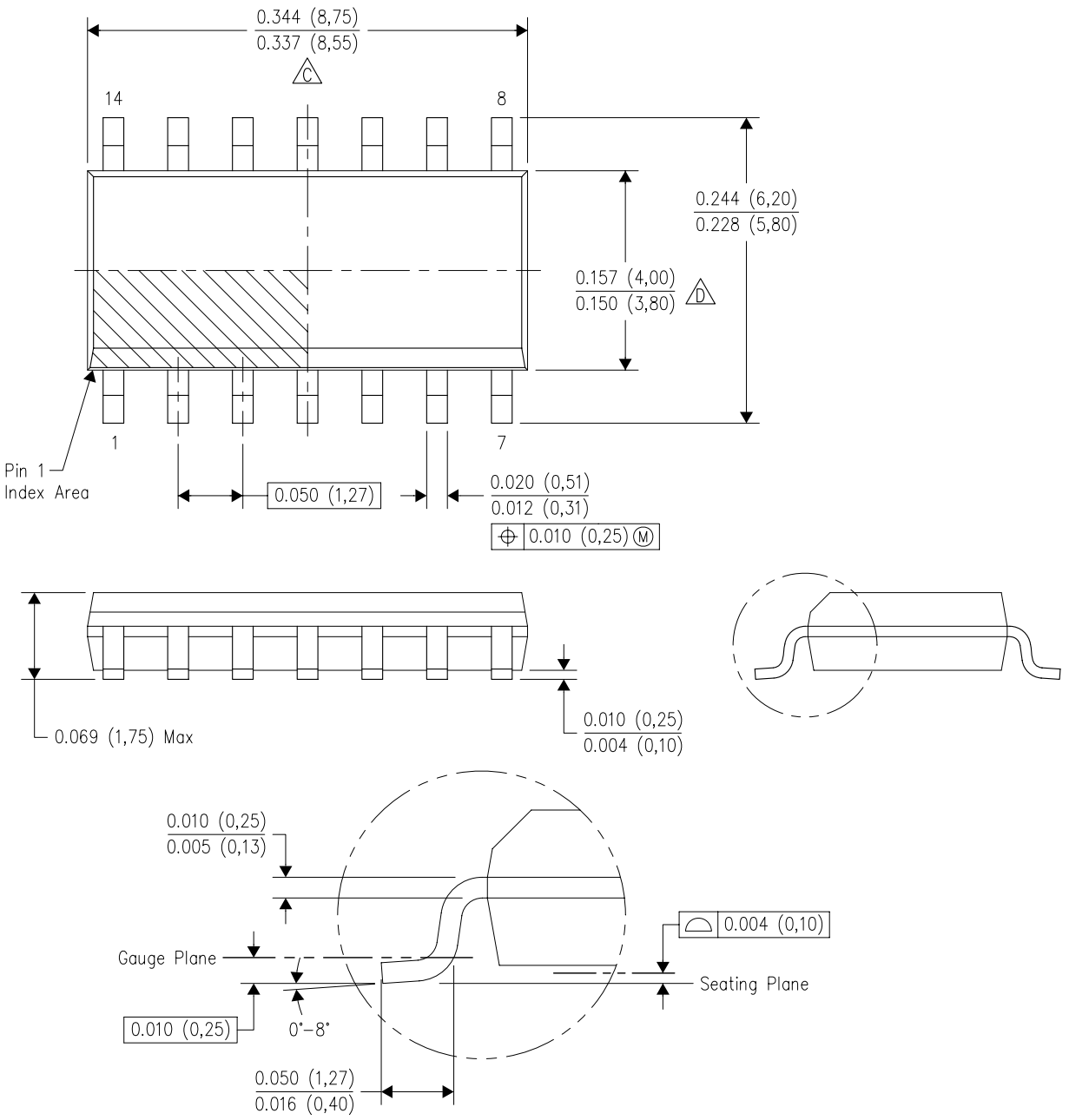
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

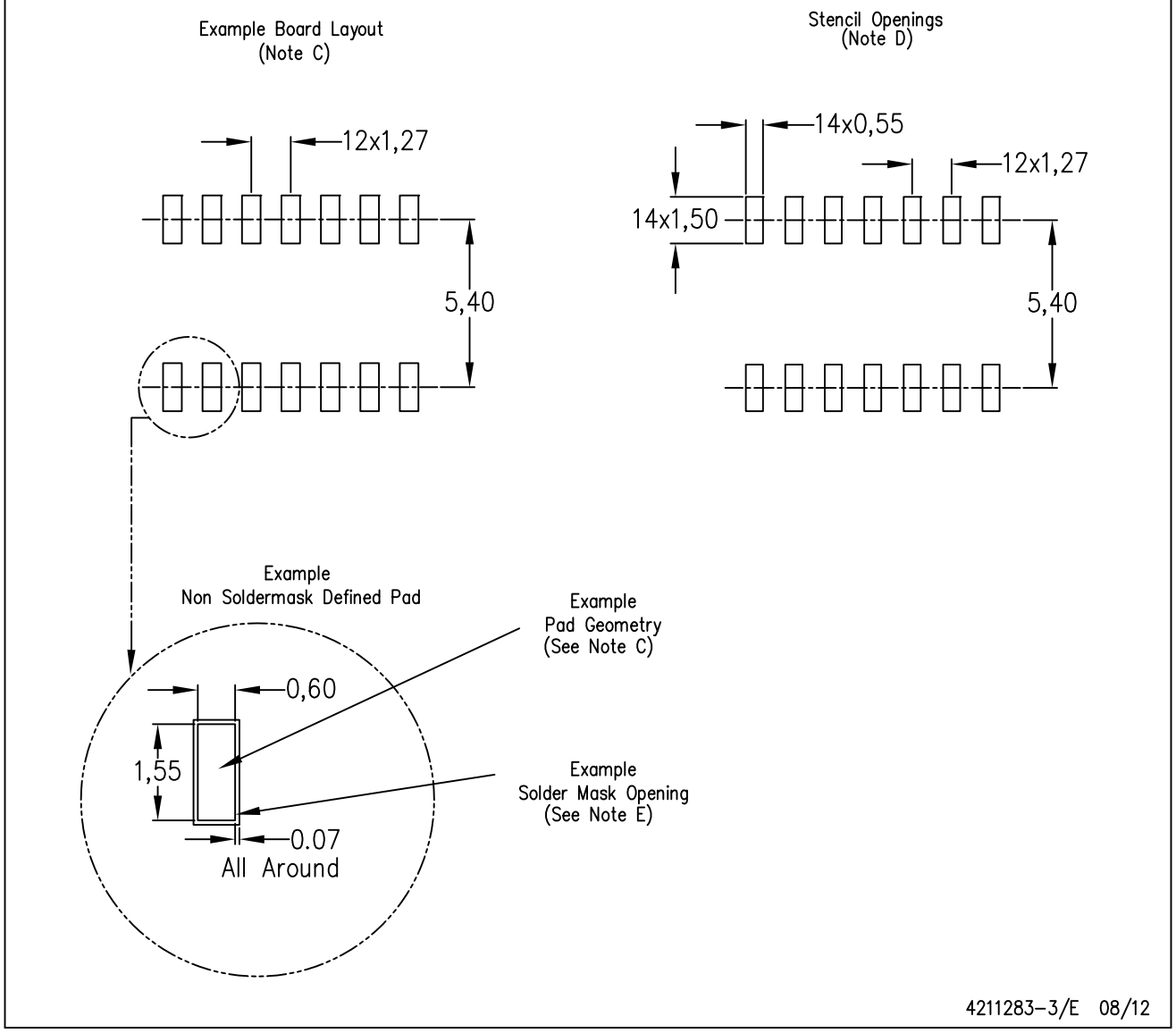
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

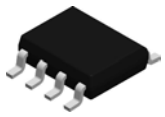


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

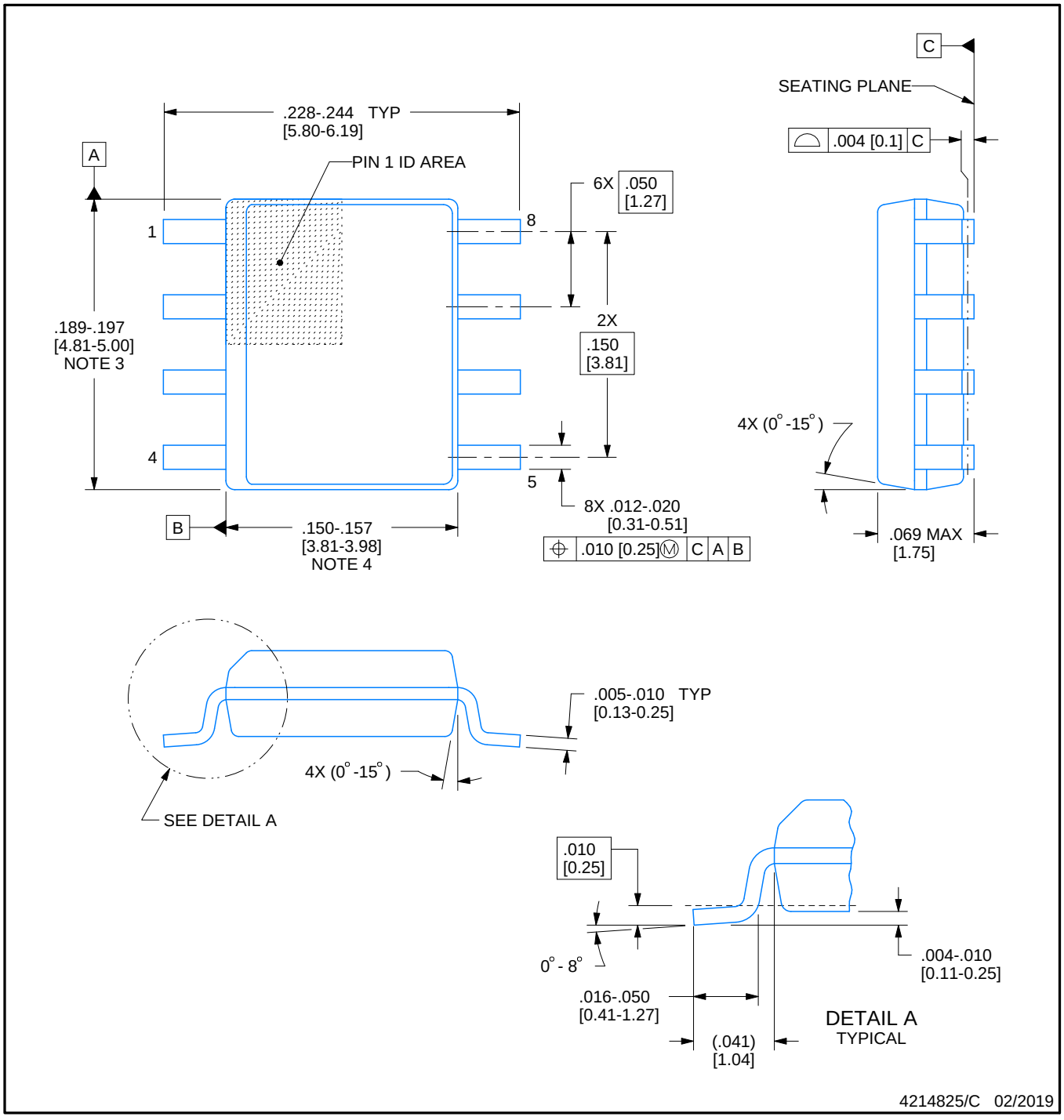


PACKAGE OUTLINE

D0008A

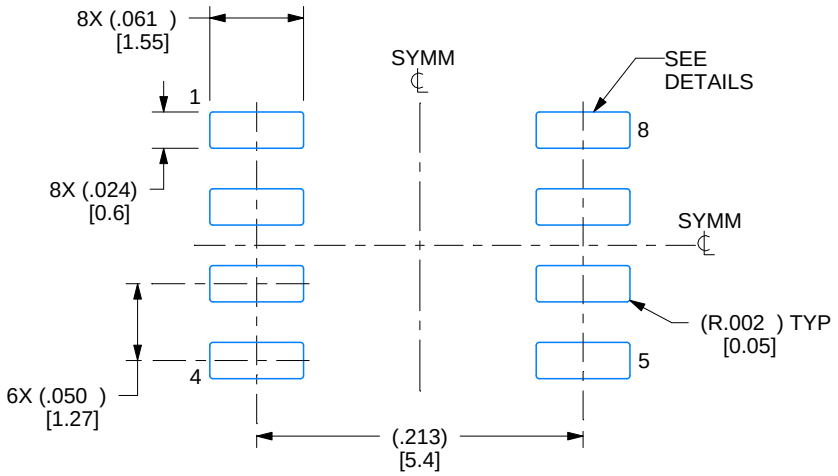
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

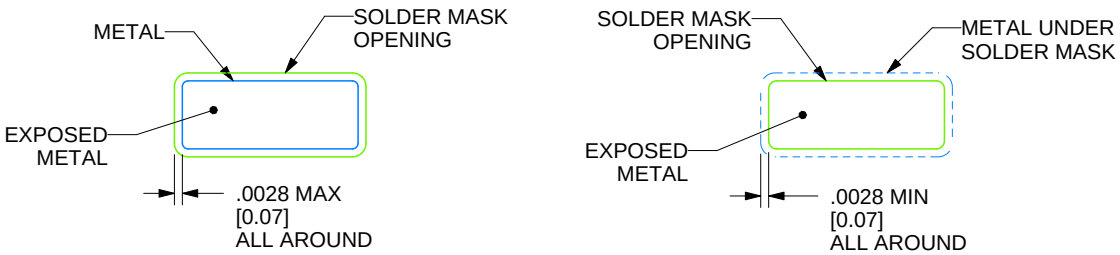


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

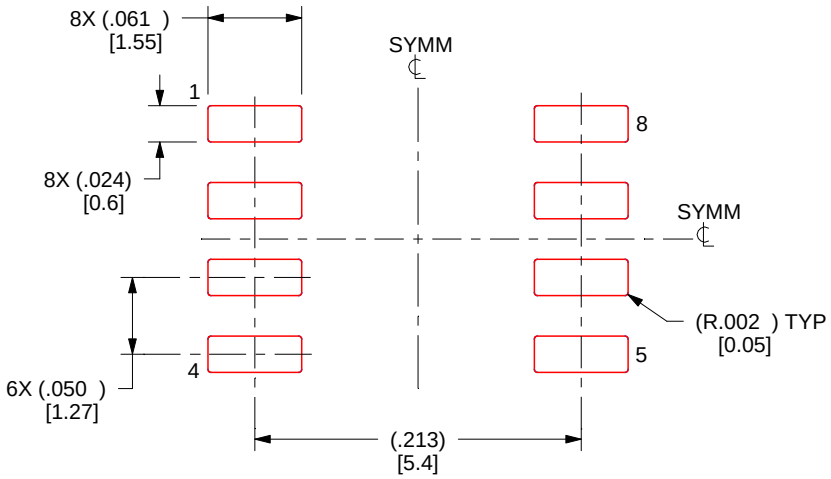
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



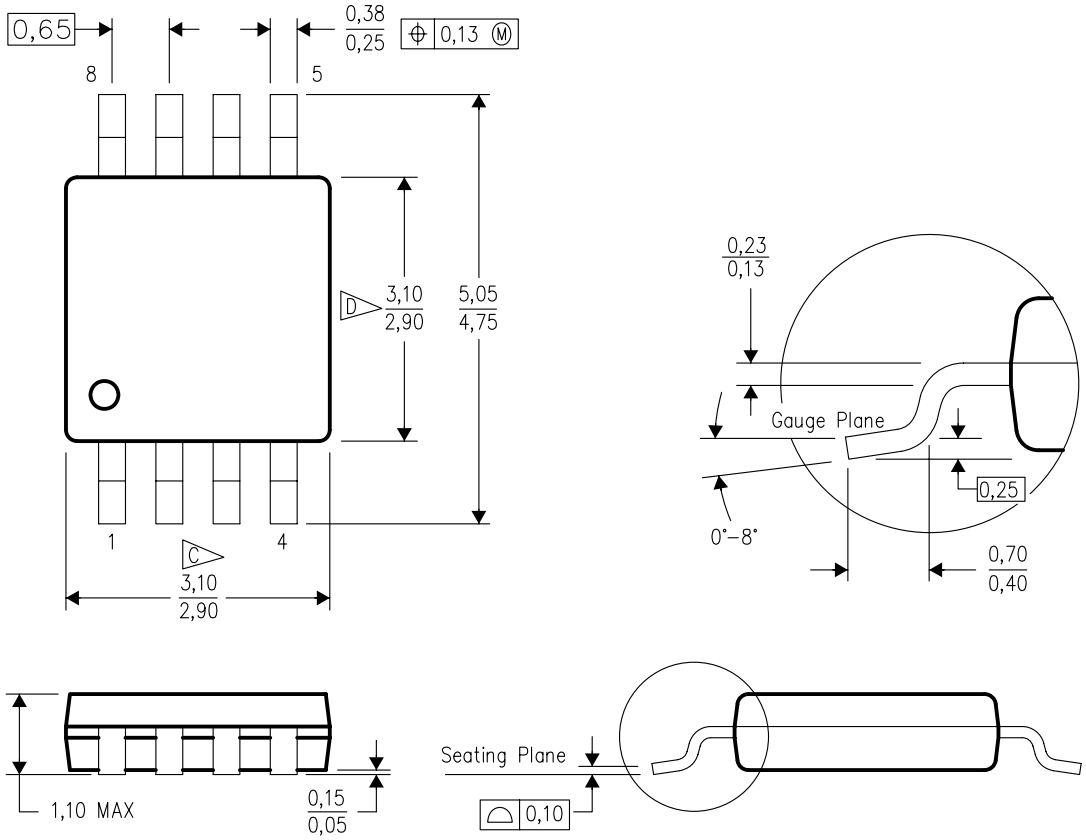
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

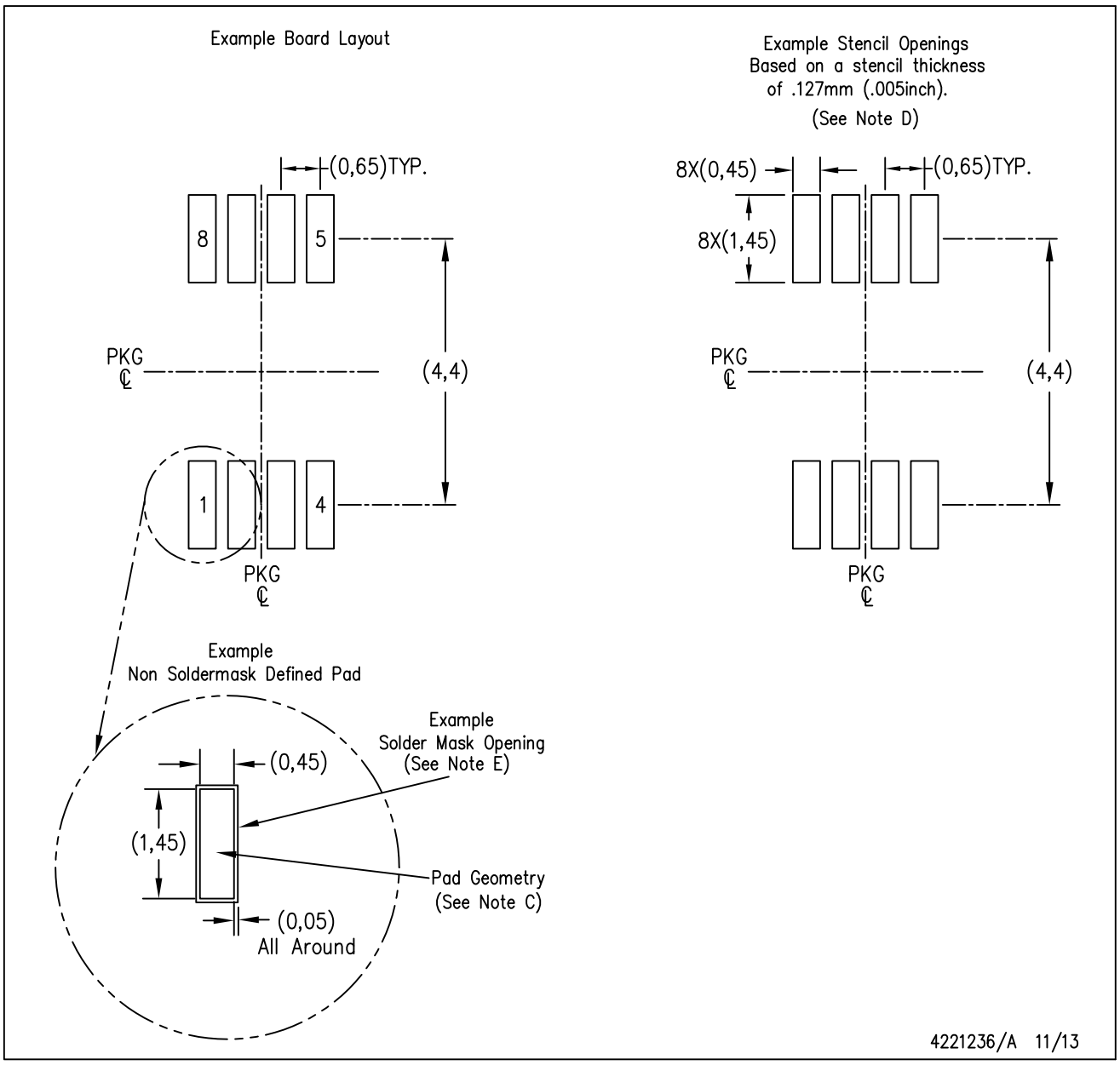
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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