

SN74AHC595 3 ステート出力レジスタ搭載 8 ビット シフトレジスタ

1 特長

- 動作範囲：2V ~ 5.5V V_{CC}
- 8 ビットのシリアル イン / パラレル アウト シフト
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
 - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- ネットワーク スイッチ
- 電源インフラストラクチャ
- LED ディスプレイ
- サーバー

3 概要

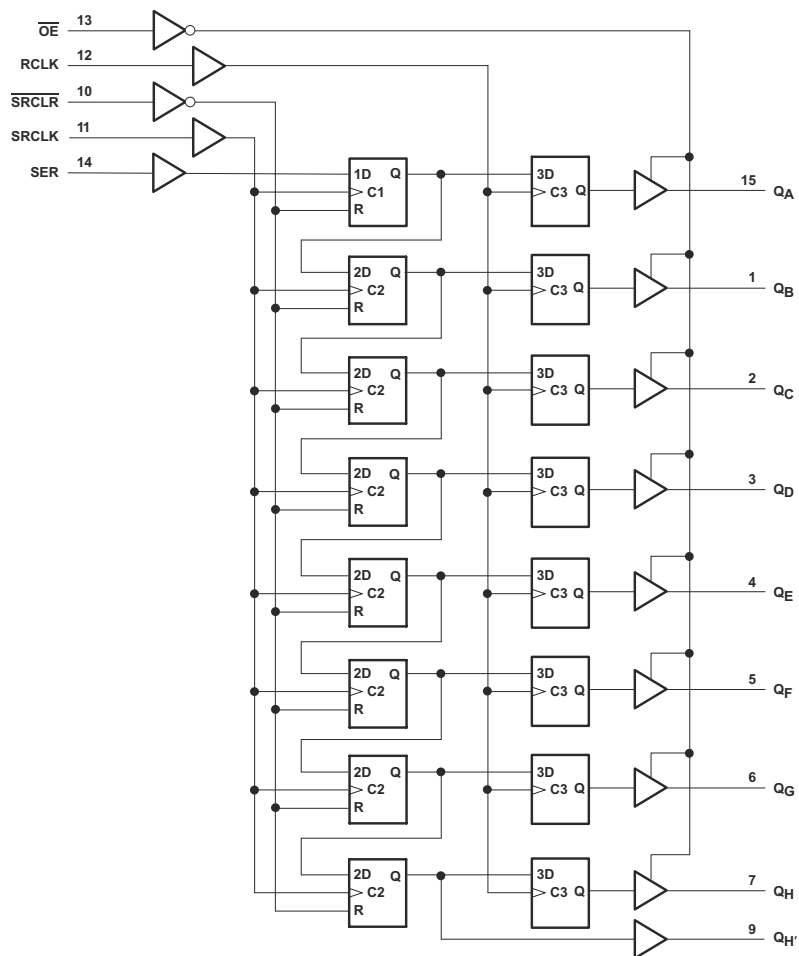
SN74AHC595 デバイスには 8 ビットのシリアル イン / パラレル アウトのシフト レジスタが搭載されており、8 ビットの D タイプ ストレージ レジスタヘデータを供給します。ストレージ レジスタはパラレル 3 ステート出力を備えています。シフト レジスタとストレージ レジスタの両方に、それぞれ独立したクロックが供給されます。シフト レジスタは、ダイレクト オーバーライディング クリア (SRCLR) 入力、シリアル (SER) 入力、カスケード接続用シリアル出力を備えています。出力イネーブル ($\overline{OE}$) 入力が High のとき、QH' を除くすべての出力が高インピーダンス状態になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (3)
SN74AHC595	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	N (PDIP, 16)	19.31mm × 9.4mm	19.31mm × 6.35mm
	D (SOIC, 16)	9.90 mm × 6mm	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00 mm × 4.40 mm

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。





論理図 (正論理)

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4 Pin Configuration and Functions

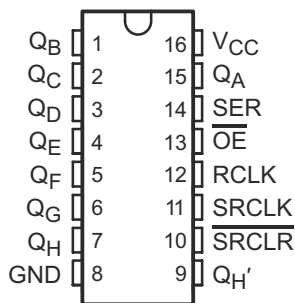


図 4-1. D, DB, N, PW Packages 16-Pin SOIC, SSOP, PDIP, TSSOP (Top View)

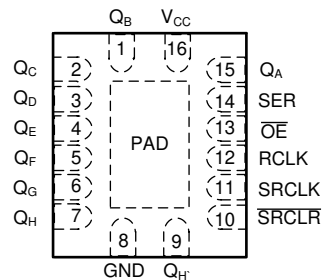


図 4-2. BQB Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	—	Ground Pin
$\overline{OE}$	13	I	Output Enable
Q _A	15	O	Q _A Output
Q _B	1	O	Q _B Output
Q _C	2	O	Q _C Output
Q _D	3	O	Q _D Output
Q _E	4	O	Q _E Output
Q _F	5	O	Q _F Output
Q _G	6	O	Q _G Output
Q _H	7	O	Q _H Output
Q _{H'}	9	O	Q _{H'} Output
RCLK	12	I	RCLK Input
SER	14	I	SER Input
SRCLK	11	I	SRCLK Input
SRCLR	10	I	SRCLR Input
V _{CC}	16	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	7	V
V _I	Input voltage ⁽²⁾		−0.5	7	V
V _O	Output voltage ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	−20		mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})	±20		mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25		mA
Continuous current through V _{CC} or GND			±75		mA
T _J	Junction temperature		150		°C

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
T _{stg} Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	2		5.5	V
V _{IH} High-level input voltage	V _{CC} = 2 V	1.5		V
	V _{CC} = 3 V	2.1		
	V _{CC} = 5.5 V	3.85		
V _{IL} Low-level input voltage	V _{CC} = 2 V		0.5	V
	V _{CC} = 3 V		0.9	
	V _{CC} = 5.5 V		1.65	
V _I Input voltage	0		5.5	V
V _O Output voltage	0		V _{CC}	V
I _{OH} High-level output current	V _{CC} = 2 V		–50	μA
	V _{CC} = 3.3 V ± 0.3 V		–4	mA
	V _{CC} = 5 V ± 0.5 V		–8	
I _{OL} Low-level output current	V _{CC} = 2 V		50	μA
	V _{CC} = 3.3 V ± 0.3 V		4	mA
	V _{CC} = 5 V ± 0.5 V		8	
Δt/Δv Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100	ns/V
	V _{CC} = 5 V ± 0.5 V		20	
T _A Operating free-air temperature	–40		125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC595					UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	91.8	73	97.8	47.8	135.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	87.7	—	48.1	35.1	70.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	61.6	—	48.5	27.8	81.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.9	—	10.0	20.1	22.5	°C/W

THERMAL METRIC ⁽¹⁾		SN74AHC595					UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	61.4	—	47.9	27.7	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	39.4	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = –50 µA	T _A = 25°C	2 V	1.9	2		V
		T _A = –40°C to 85°C		1.9			
		T _A = –40°C to 125°C Recommended		1.9			
	I _{OH} = –50 µA	T _A = 25°C	3 V	2.9	3		
		T _A = –40°C to 85°C		2.9			
		T _A = –40°C to 125°C Recommended		2.9			
	I _{OH} = –50 µA	T _A = 25°C	4.5 V	4.4	4.5		
		T _A = –40°C to 85°C		4.4			
		T _A = –40°C to 125°C Recommended		4.4			
	I _{OH} = –4 mA	T _A = 25°C	3 V	2.58			
		T _A = –40°C to 85°C		2.48			
		T _A = –40°C to 125°C Recommended		2.48			
	I _{OH} = –8 mA	T _A = 25°C	4.5 V	3.94			
		T _A = –40°C to 85°C		3.8			
		T _A = –40°C to 125°C Recommended		3.8			
V _{OL}	I _{OL} = 50 µA	T _A = 25°C	2 V			0.1	V
		T _A = –40°C to 85°C				0.1	
		T _A = –40°C to 125°C Recommended				0.1	
	I _{OL} = 50 µA	T _A = 25°C	3 V			0.1	
		T _A = –40°C to 85°C				0.1	
		T _A = –40°C to 125°C Recommended				0.1	
	I _{OL} = 50 µA	T _A = 25°C	4.5 V			0.1	
		T _A = –40°C to 85°C				0.1	
		T _A = –40°C to 125°C Recommended				0.1	
	I _{OL} = 4 mA	T _A = 25°C	3 V			0.36	
		T _A = –40°C to 85°C				0.44	
		T _A = –40°C to 125°C Recommended				0.44	
	I _{OL} = 8 mA	T _A = 25°C	4.5 V			0.36	
		T _A = –40°C to 85°C				0.44	
		T _A = –40°C to 125°C Recommended				0.44	
I _I	V _I = 5.5 V or GND	T _A = 25°C	0 V to 5.5 V			±0.1	µA
		T _A = –40°C to 85°C				±1	
		T _A = –40°C to 125°C Recommended				±1	
I _{OZ}	V _I = V _{CC} or GND, V _O = V _{CC} or GND, OE = V _{IH} or V _{IL}	Q _A – Q _H	5.5 V			±0.25	µA
						±2.5	
						±2.5	

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS			V _{CC}	MIN	TYP	MAX	UNIT
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	T _A = 25°C	5.5 V			4	μA
			T _A = −40°C to 85°C				40	
			T _A = −40°C to 125°C Recommended				40	
C _i	V _I = V _{CC} or GND	T _A = 25°C		5 V		3	10	pF
		T _A = −40°C TO 85°C					10	
C _O	V _O = V _{CC} or GND,	T _A = 25°C		5 V		5.5		pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t _w	SRCLK high or low	T _A = 25°C	5		ns
		T _A = –40°C to 85°C	5		
		T _A = –40°C to 125°C Recommended	6		
	RCLK high or low	T _A = 25°C	5		
		T _A = –40°C to 85°C	5		
		T _A = –40°C to 125°C Recommended	6		
	SRCLR low	T _A = 25°C	5		
		T _A = –40°C to 85°C	5		
		T _A = –40°C to 125°C Recommended	6.5		
t _{su}	SER before SRCLK↑	T _A = 25°C	3.5		ns
		T _A = –40°C to 85°C	3.5		
		T _A = –40°C to 125°C Recommended	4.5		
	SRCLK↑ before RCLK↑ ⁽¹⁾	T _A = 25°C	8		
		T _A = –40°C to 85°C	8.5		
		T _A = –40°C to 125°C Recommended	9.5		
	SRCLR low before RCLK↑	T _A = 25°C	8		
		T _A = –40°C to 85°C	9		
		T _A = –40°C to 125°C Recommended	10		
	SRCLR high (inactive) before SRCLK↑	T _A = 25°C	3		
		T _A = –40°C to 85°C	3		
		T _A = –40°C to 125°C Recommended	4		
t _h	SER after SRCLK↑	T _A = 25°C	1.5		ns
		T _A = –40°C to 85°C	1.5		
		T _A = –40°C to 125°C Recommended	2.5		

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

			MIN	NOM	MAX	UNIT
t_W	Pulse duration	SRCLK high or low	$T_A = 25^\circ\text{C}$	5		ns
			$T_A = -40^\circ\text{C}$ to 85°C	5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	6		
	RCLK high or low	RCLK high or low	$T_A = 25^\circ\text{C}$	5		
			$T_A = -40^\circ\text{C}$ to 85°C	5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	6		
	SRCLR low	SRCLR low	$T_A = 25^\circ\text{C}$	5		
			$T_A = -40^\circ\text{C}$ to 85°C	5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	6.2		
t_{su}	Set-up time	SER before SRCLK $\uparrow$	$T_A = 25^\circ\text{C}$	3		ns
			$T_A = -40^\circ\text{C}$ to 85°C	3		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	4		
	SRCLK $\uparrow$ before RCLK $\uparrow$ (1)	SRCLK $\uparrow$ before RCLK $\uparrow$ (1)	$T_A = 25^\circ\text{C}$	5		
			$T_A = -40^\circ\text{C}$ to 85°C	5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	6		
	SRCLR low before RCLK $\uparrow$	SRCLR low before RCLK $\uparrow$	$T_A = 25^\circ\text{C}$	5		
			$T_A = -40^\circ\text{C}$ to 85°C	5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	6		
	SRCLR high (inactive) before SRCLK $\uparrow$	SRCLR high (inactive) before SRCLK $\uparrow$	$T_A = 25^\circ\text{C}$	2.5		
			$T_A = -40^\circ\text{C}$ to 85°C	2.5		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	3.5		
t_h	Hold time	SER after SRCLK $\uparrow$	$T_A = 25^\circ\text{C}$	2		ns
			$T_A = -40^\circ\text{C}$ to 85°C	2		
			$T_A = -40^\circ\text{C}$ to 125°C Recommended	3		

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.8 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$	80 ⁽¹⁾	120 ⁽¹⁾		MHz
				$T_A = -40^\circ\text{C}$ to 85°C	70			
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	60			
			$C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$	55	105		
				$T_A = -40^\circ\text{C}$ to 85°C	50			
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	40			
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		6 ⁽¹⁾	11.9 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C	1		13.5	
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	1		14.9	
t_{PHL}	RCLK	$Q_A - Q_H$	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		6 ⁽¹⁾	11.9 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C	1		13.5	
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	1		14.9	
t_{PLH}	SRCLK	Q_H	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		6.6 ⁽¹⁾	13 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C	1		15	
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	1		16.4	
t_{PHL}	SRCLK	Q_H	$C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		6.6 ⁽¹⁾	13 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C}$ to 85°C	1		15	
				$T_A = -40^\circ\text{C}$ to 125°C Recommended	1		16.4	

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	$\overline{SRCLR}$	Q_H	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		6.2 ⁽¹⁾	12.8 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		13.7	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		15	
t_{PZH}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		6 ⁽¹⁾	11.5 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		13.5	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		14.9	
t_{PZL}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.8 ⁽¹⁾	11.5 ⁽¹⁾	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		13.5	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		14.9	
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.9	15.4	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		17	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		18.6	
t_{PHL}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.9	15.4	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		17	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		18.6	
t_{PLH}	SRCLK	Q_H	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9.2	16.5	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		18.5	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		20	
t_{PHL}	SRCLK	Q_H	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9.2	16.5	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		18.5	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		20	
t_{PHL}	$\overline{SRCLR}$	Q_H	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9	16.3	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		17.2	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		18.7	
t_{PZH}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		7.8	15	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		17	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		18.6	
t_{PZL}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9.6	15	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		17	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		18.6	
t_{PHZ}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		8.1	15.7	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		16.2	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		17.4	
t_{PLZ}	$\overline{OE}$	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		9.3	15.7	ns
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	1		16.2	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended}$	1		17.4	

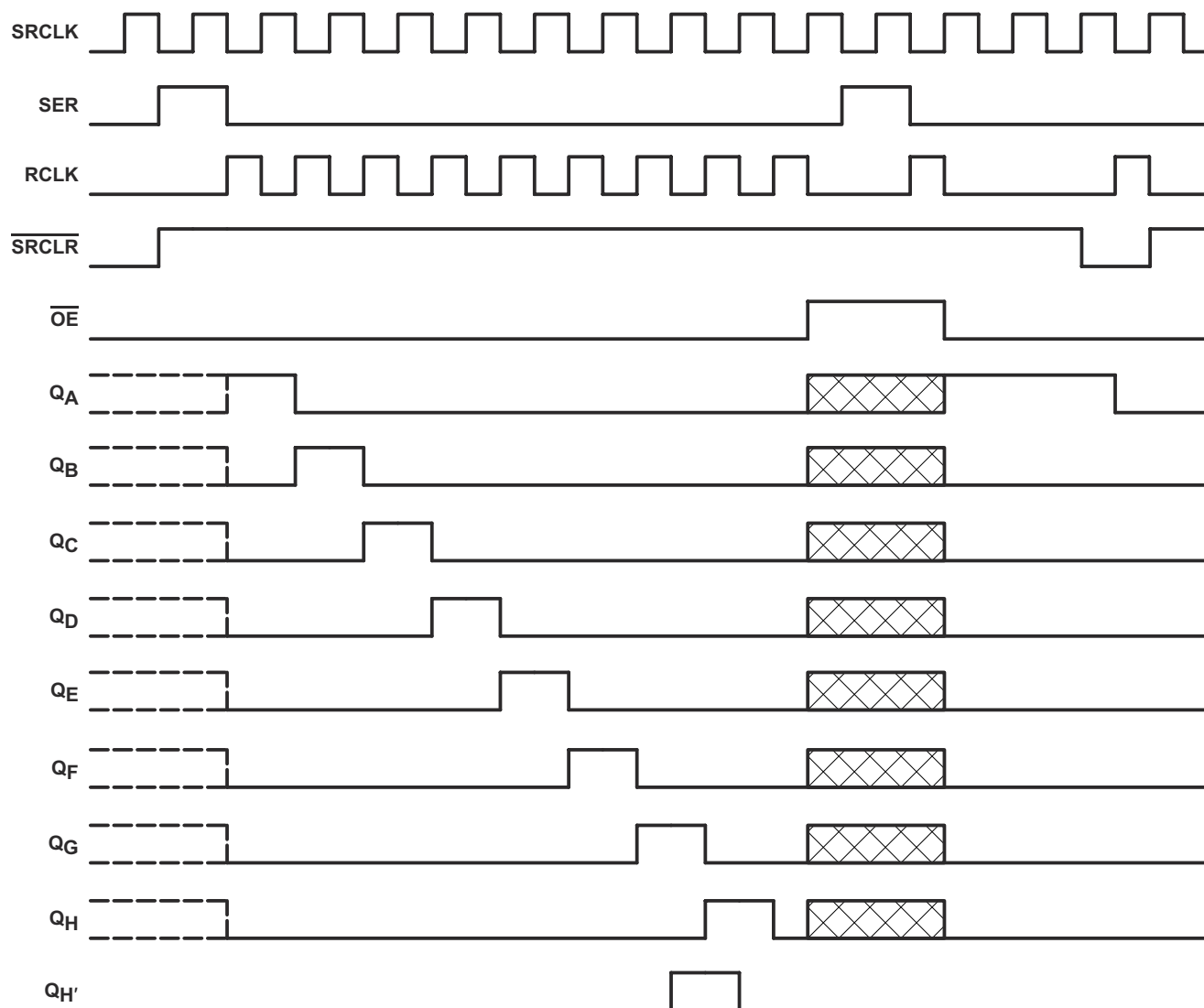
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.9 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF	T _A = 25°C	135 ⁽¹⁾	170 ⁽¹⁾	MHz	
				T _A = −40°C to 85°C	115			
			C _L = 50 pF	T _A = 25°C	95	140		
				T _A = −40°C to 85°C	85			
t _{PLH}	RCLK	Q _A − Q _H	C _L = 15 pF	T _A = 25°C		4.3 ⁽¹⁾	7.4 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		8.5	
t _{PHL}	RCLK	Q _A − Q _H	C _L = 15 pF	T _A = 25°C		4.3 ⁽¹⁾	7.4 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		8.5	
t _{PLH}	SRCLK	Q _{H'}	C _L = 15 pF	T _A = 25°C		4.5 ⁽¹⁾	8.2 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		9.4	
t _{PHL}	SRCLK	Q _{H'}	C _L = 15 pF	T _A = 25°C		4.5 ⁽¹⁾	8.2 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		9.4	
t _{PHL}	SRCLR	Q _{H'}	C _L = 15 pF	T _A = 25°C		4.5 ⁽¹⁾	8 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		9.1	
t _{PZH}	OE	Q _A − Q _H	C _L = 15 pF	T _A = 25°C		4.3 ⁽¹⁾	8.6 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		10	
t _{PZL}	OE	Q _A − Q _H	C _L = 15 pF	T _A = 25°C		5.4 ⁽¹⁾	8.6 ⁽¹⁾	ns
				T _A = −40°C to 85°C	1		10	
t _{PLH}	RCLK	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		5.6	9.4	ns
				T _A = −40°C to 85°C	1		10.5	
t _{PHL}	RCLK	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		5.6	9.4	ns
				T _A = −40°C to 85°C	1		10.5	
t _{PLH}	SRCLK	Q _{H'}	C _L = 50 pF	T _A = 25°C		6.4	10.2	ns
				T _A = −40°C to 85°C	1		11.4	
t _{PHL}	SRCLK	Q _{H'}	C _L = 50 pF	T _A = 25°C		6.4	10.2	ns
				T _A = −40°C to 85°C	1		11.4	
t _{PHL}	SRCLR	Q _{H'}	C _L = 50 pF	T _A = 25°C		6.4	10	ns
				T _A = −40°C to 85°C	1		11.1	
t _{PZH}	OE	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		5.7	10.6	ns
				T _A = −40°C to 85°C	1		12	
t _{PZL}	OE	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		6.8	10.6	ns
				T _A = −40°C to 85°C	1		12	
t _{PHZ}	OE	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		3.5	10.3	ns
				T _A = −40°C to 85°C	1		11	
t _{PLZ}	OE	Q _A − Q _H	C _L = 50 pF	T _A = 25°C		3.4	10.3	ns
				T _A = −40°C to 85°C	1		11	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



NOTE:  implies that the output is in 3-State mode.

図 5-1. Timing Diagram

5.10 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	25.2	pF

5.11 Typical Characteristics

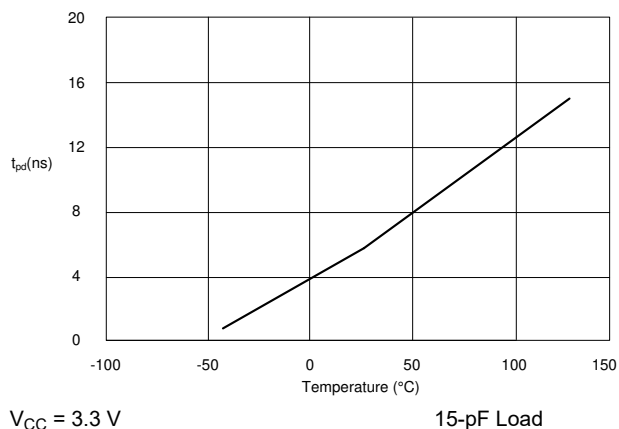
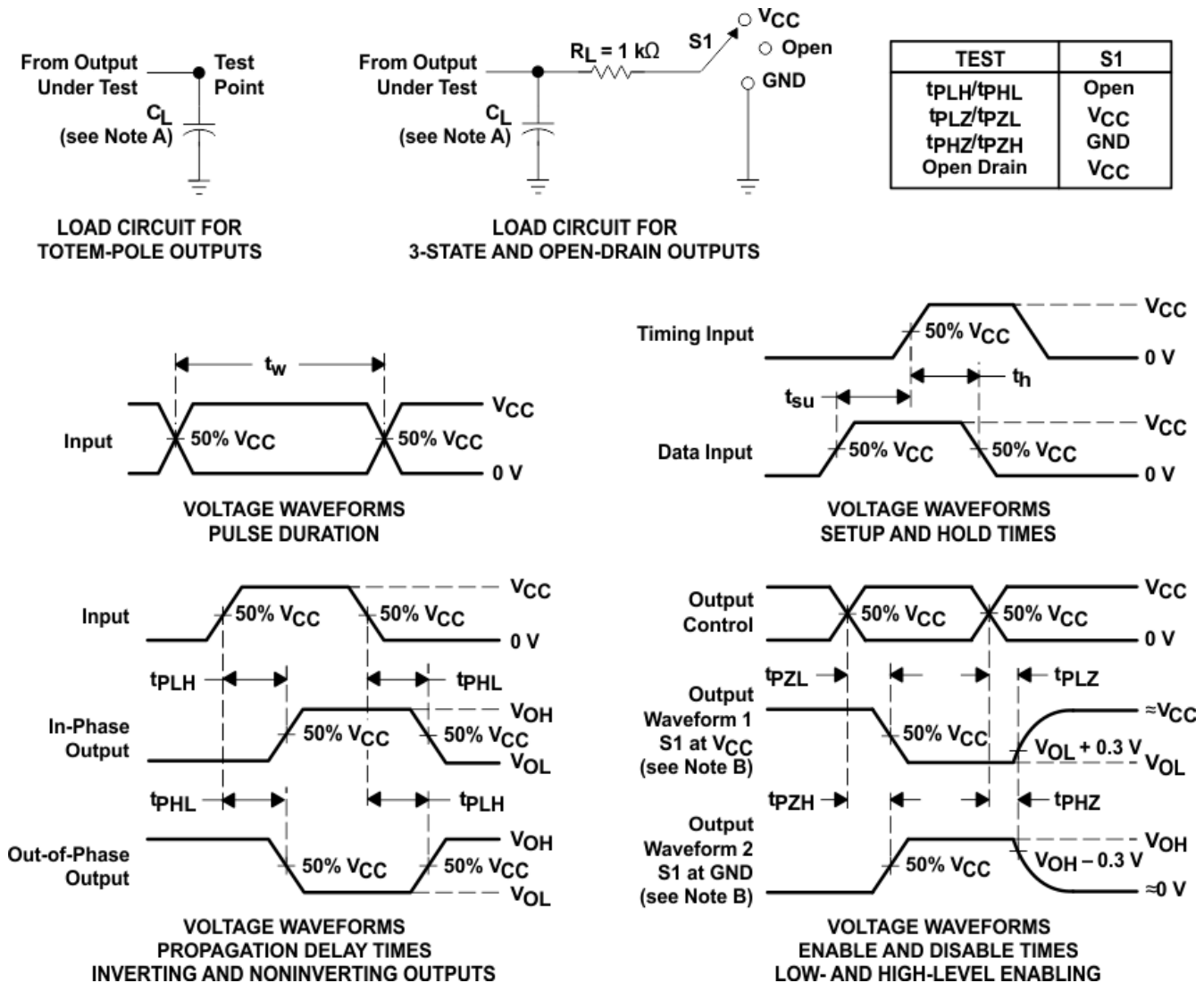


図 5-2. SN74AHC595 RCLK to Q TPD vs Temperature

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

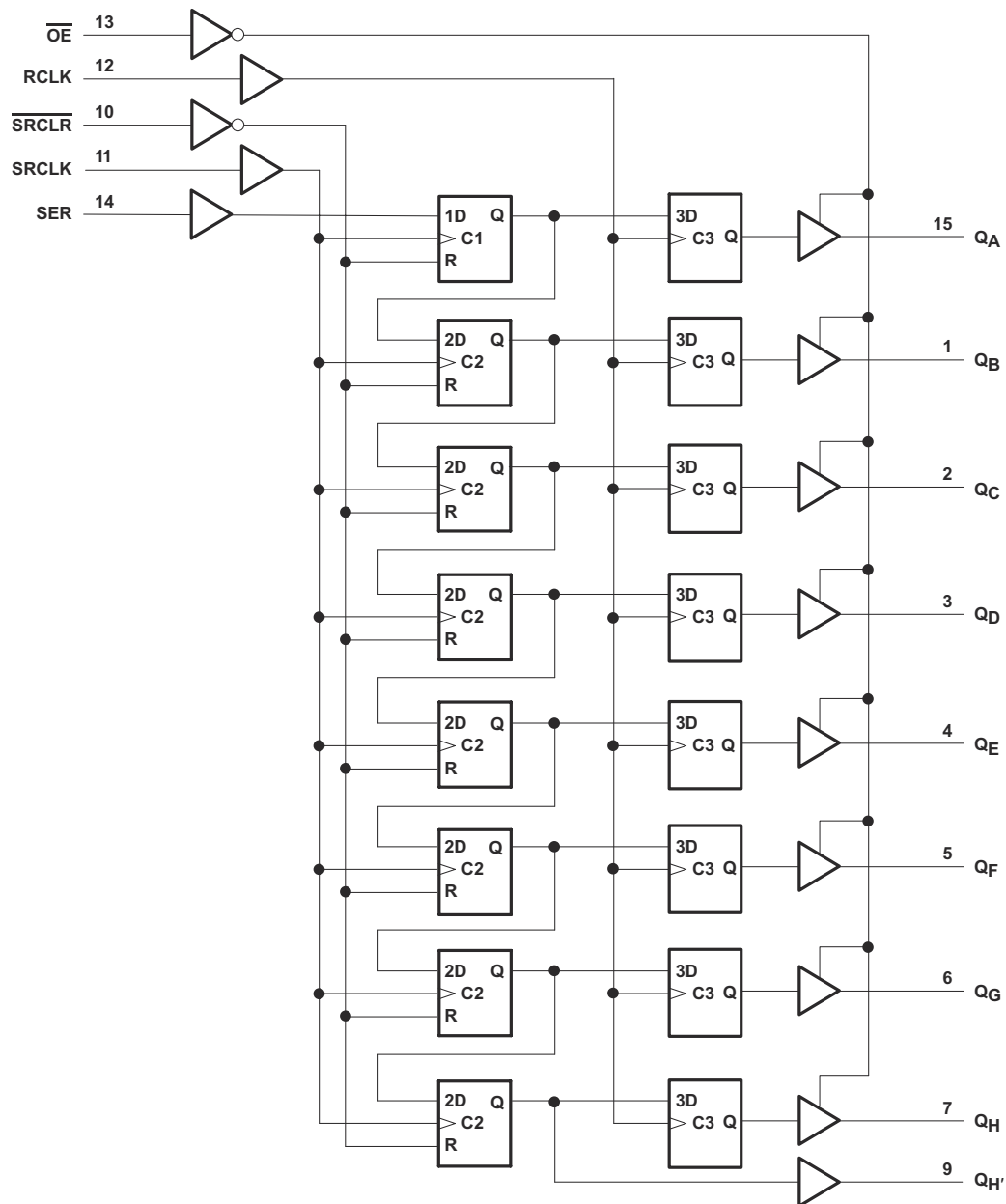
7 Detailed Description

7.1 Overview

The SN74AHC595 device is part of the AHC family of logic devices intended for CMOS applications. The SN74HC595 device is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74AHC595 device is an 8-bit serial-in, parallel-out shift registers that have a wide operating voltage range from 2 V to 5.5 V and a low current consumption of 40-μA (max) I_{CC} .

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

8 Application and Implementation

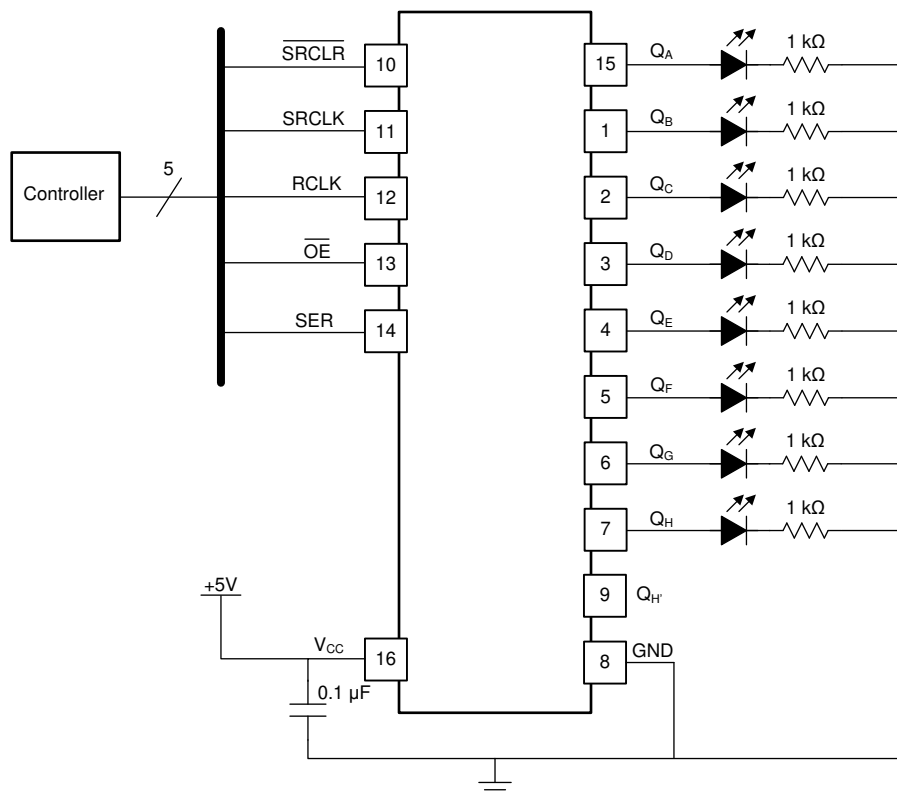
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN74AHC595 device is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. [図 8-1](#) shows an application where eight LEDs are used to visualize the data bits contained within the shift register.

8.2 Typical Application



✎ 8-1. Shift Register Display of 8 bits

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 6.0 V at any valid V_{CC}
- Recommend output conditions:
 - Load currents must not exceed 25 mA per output and 75 mA total for the part
 - Outputs must not be pulled above V_{CC}

8.2.3 Application Curve

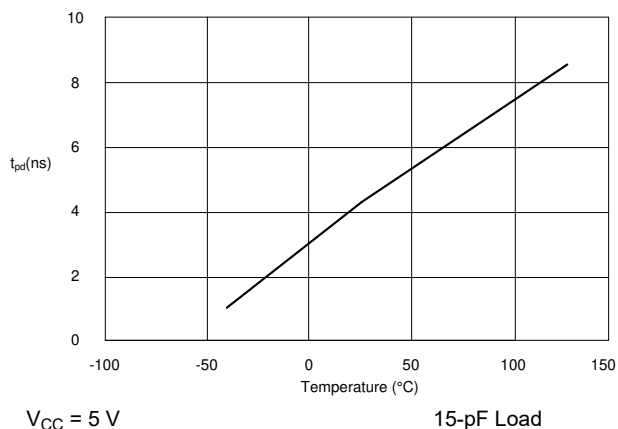


図 8-2. SN74AHC595 RCLK to Q TPD vs Temperature

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1- μF capacitor is recommended; if there are multiple V_{CC} pins, then a 0.01- μF or a 0.022- μF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μF and a 1- μF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must **not** be left unconnected because the undefined voltages at the outside connections results in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, these unused inputs will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output-enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8.4.2 Layout Example

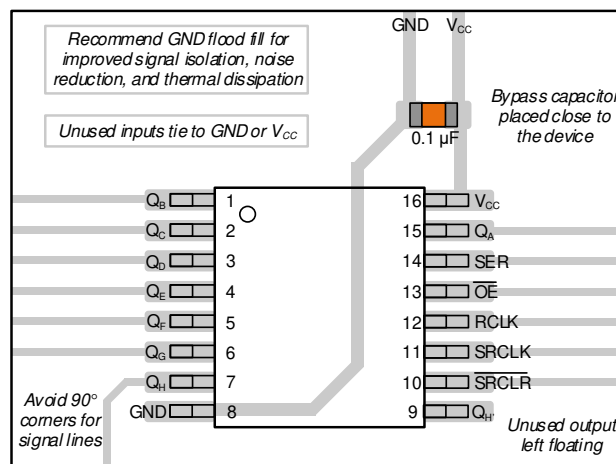


图 8-3. Example Layout for the SN74AHC595

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.4 Trademarks

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9.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (March 2024) to Revision M (April 2024)	Page
• Updated thermal values for PW package from RθJA = 106.1 to 135.9, RθJC(top) = 40.8 to 70.3, RθJB = 51.1 to 81.3, ΨJT = 3.8 to 22.5, ΨJB = 50.6 to 80.8, all values in °C/W.....	5
• Added <i>Typical Characteristics</i>	12
• Updated <i>Layout Example</i>	18

Changes from Revision K (September 2015) to Revision L (March 2024)	Page
• マシン モデルへの参照を削除、「製品情報」を「パッケージ情報」に変更、表にパッケージ サイズを追加.	1
• 「パッケージ情報」表、「ピン構成および機能」セクション、「熱に関する情報」の表に BQB パッケージを追加	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC595D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AHC595	
SN74AHC595DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595	Samples
SN74AHC595DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC595	Samples
SN74AHC595N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC595N	Samples
SN74AHC595PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125	HA595	
SN74AHC595PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HA595	Samples
SN74AHC595PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC595 :

- Automotive : [SN74AHC595-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595PWGR4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC595DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHC595DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC595PWGR4	TSSOP	PW	16	2000	367.0	367.0	35.0

TUBE



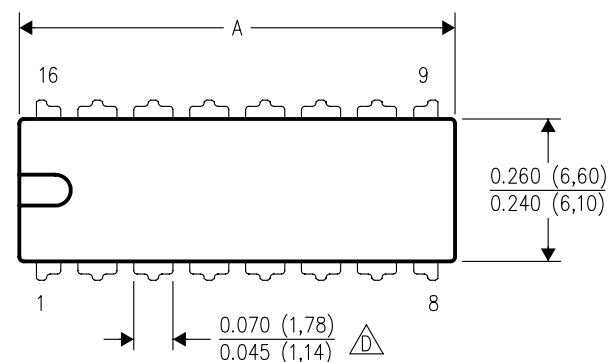
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC595N	N	PDIP	16	25	506	13.97	11230	4.32

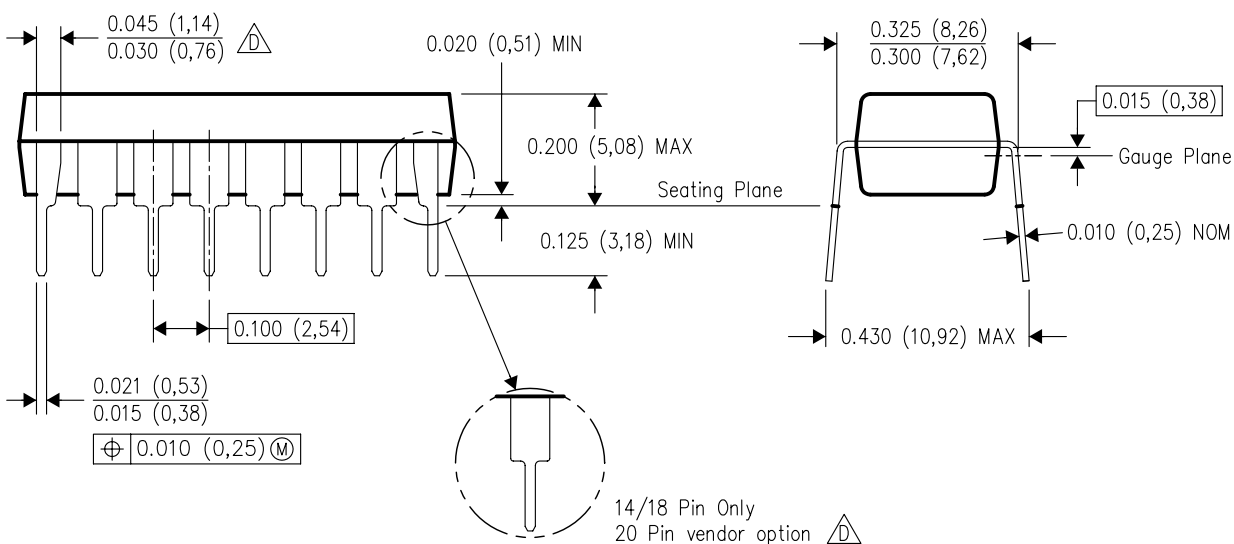
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

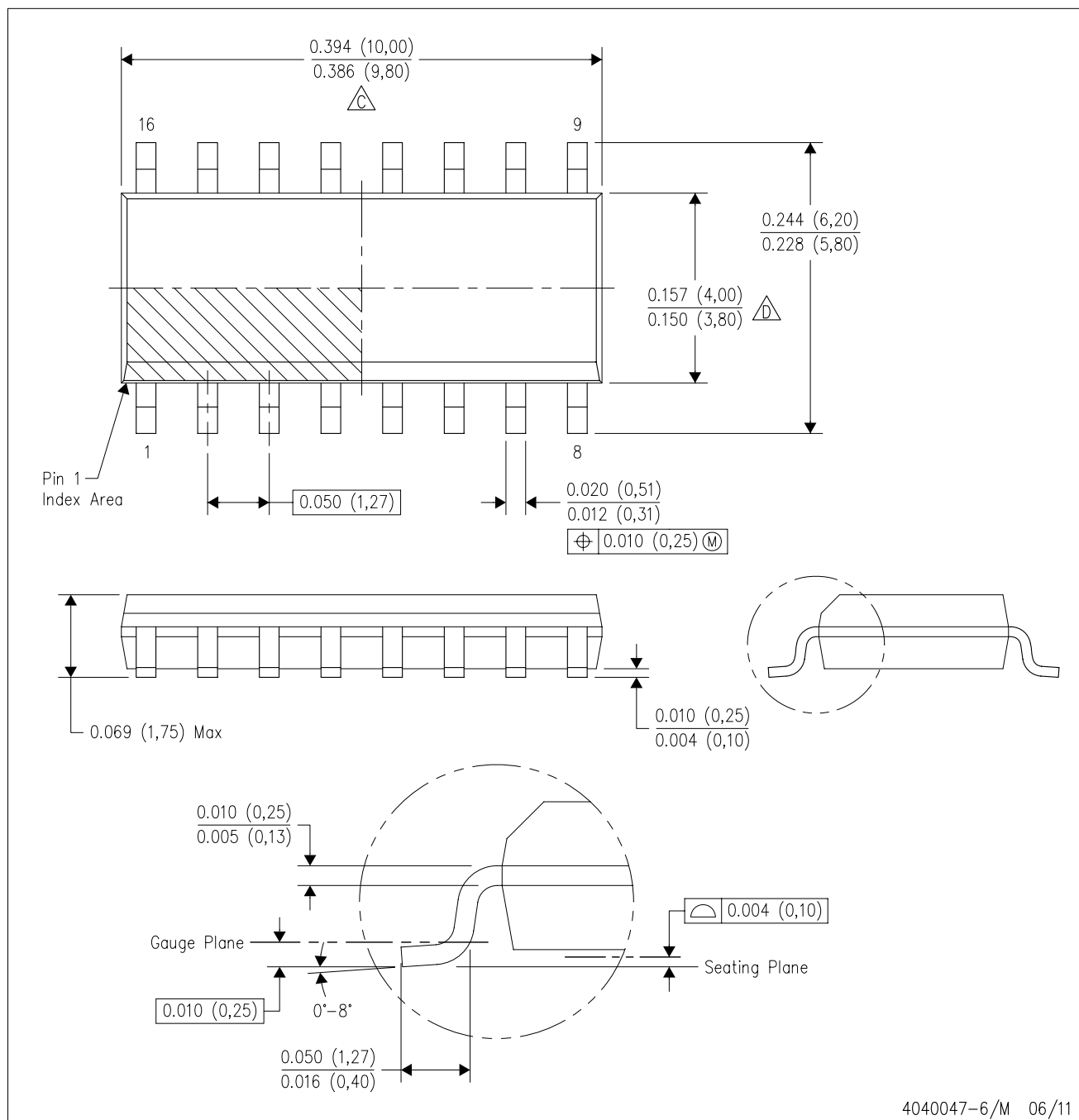


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

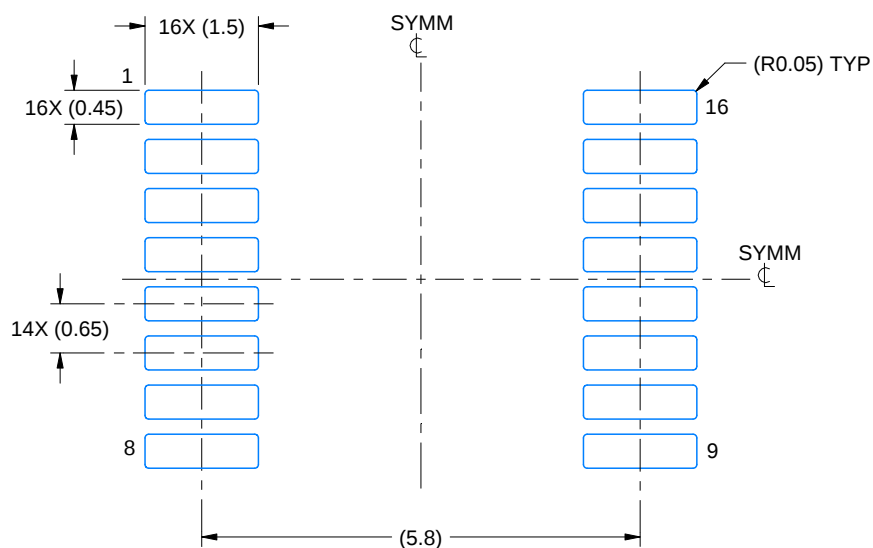
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

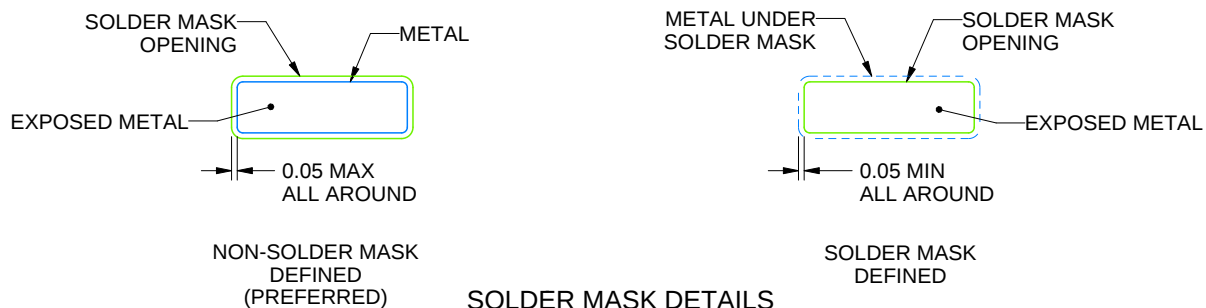
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

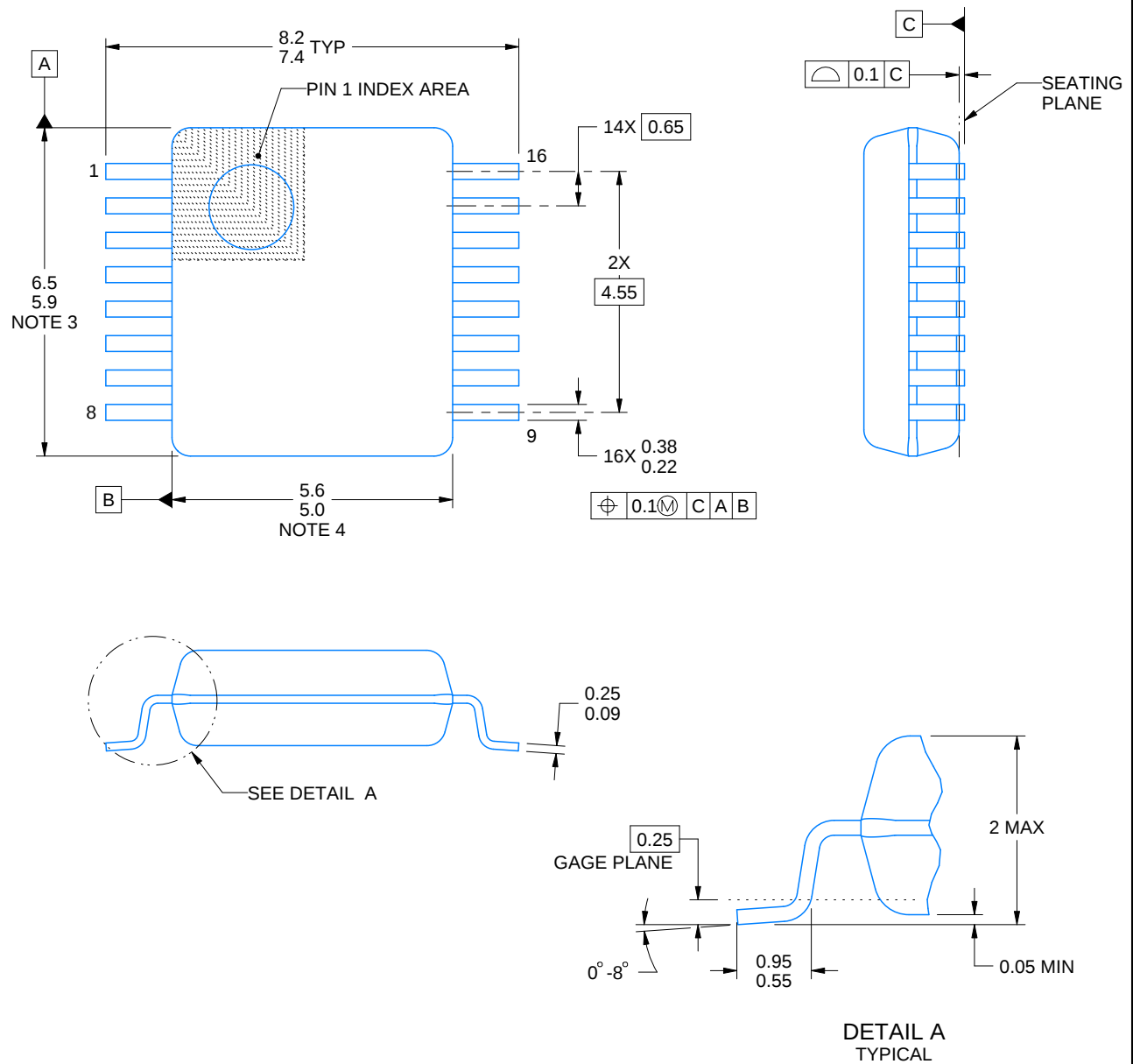


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

NOTES:

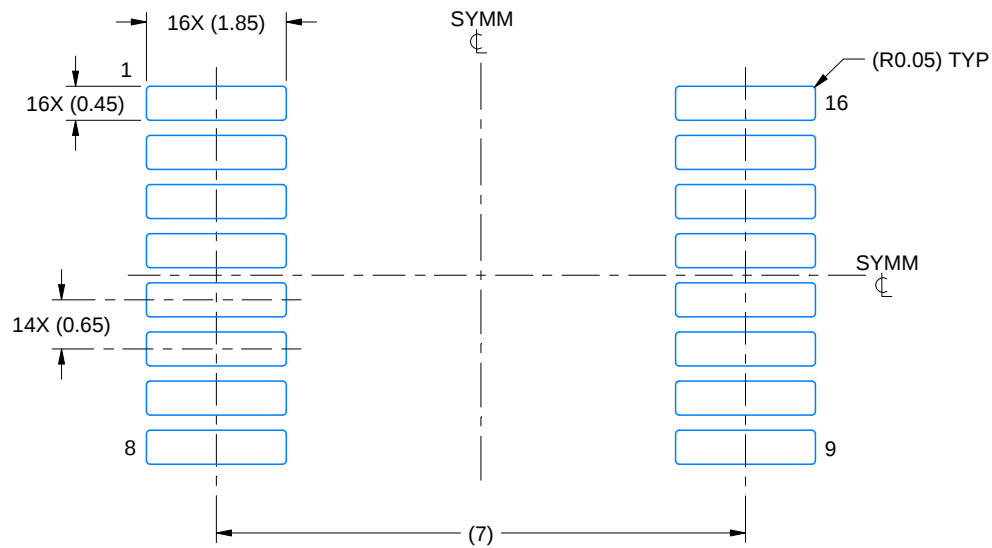
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

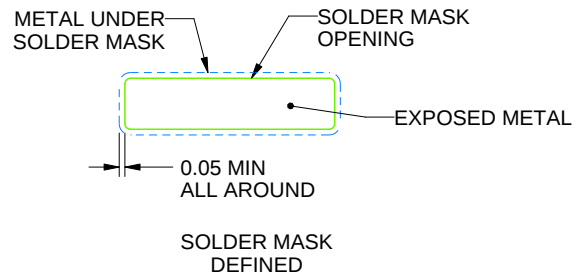
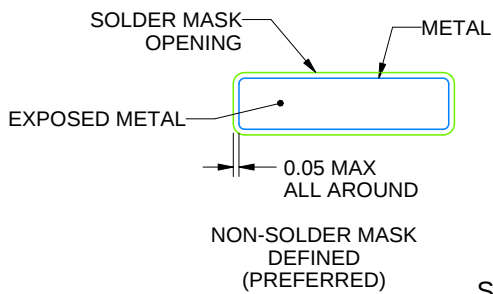
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

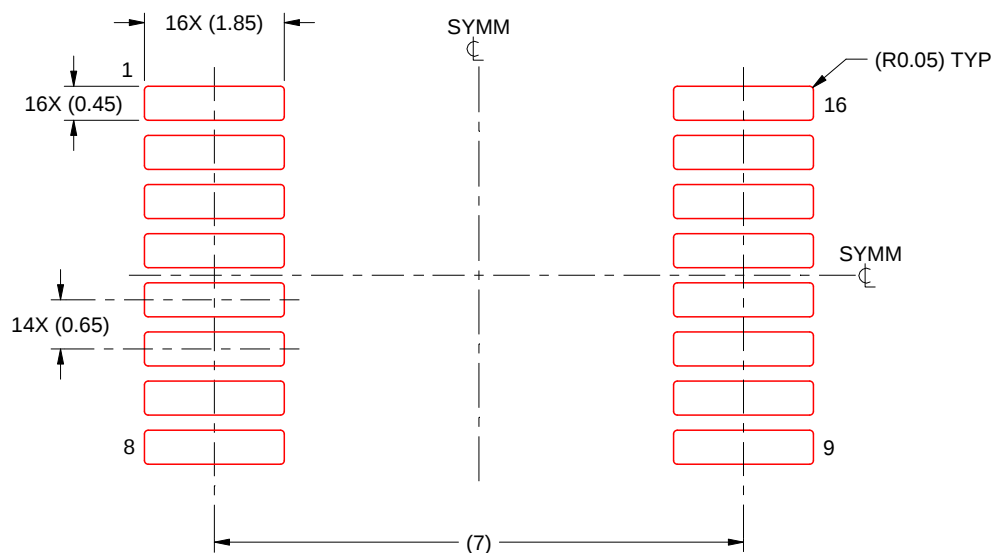
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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