

## SNx4HCT08 クワッド 2 入力正論理 AND ゲート

### 1 特長

- 4.5V～5.5V の動作電源電圧範囲
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低消費電力、最大  $I_{CC}$  20 $\mu$ A
- $t_{pd} = 13$ ns (標準値)
- 5V で  $\pm 4$ mA の出力駆動能力
- 小さい入力電流、最大 1 $\mu$ A
- 入力は TTL 電圧互換

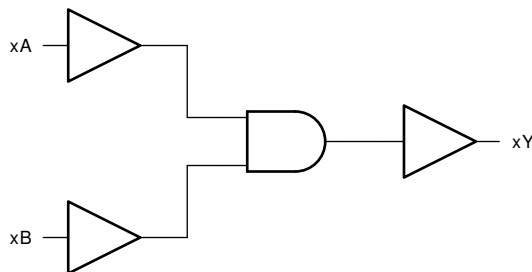
### 2 概要

これらのデバイスには、4 つの独立した 2 入力 AND ゲートが内蔵されています。これらはブール関数  $Y = A \cdot B$  を正論理で実行します。

#### 製品情報

| 部品番号        | パッケージ <sup>(1)</sup> | 本体サイズ (公称)       |
|-------------|----------------------|------------------|
| SN74HCT08D  | SOIC (14)            | 8.65mm × 3.90mm  |
| SN74HCT08DB | SSOP (14)            | 6.20mm × 5.30mm  |
| SN74HCT08N  | PDIP (14)            | 19.31mm × 6.35mm |
| SN74HCT08NS | SO (14)              | 10.20mm × 5.30mm |
| SN74HCT08PW | TSSOP (14)           | 5.00mm × 4.40mm  |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



## Table of Contents

|                                                           |          |                                                                  |          |
|-----------------------------------------------------------|----------|------------------------------------------------------------------|----------|
| <b>1 特長</b> .....                                         | <b>1</b> | 7.3 Device Functional Modes.....                                 | <b>7</b> |
| <b>2 概要</b> .....                                         | <b>1</b> | <b>8 Power Supply Recommendations</b> .....                      | <b>8</b> |
| <b>3 Revision History</b> .....                           | <b>2</b> | <b>9 Layout</b> .....                                            | <b>8</b> |
| <b>4 Pin Configuration and Functions</b> .....            | <b>3</b> | 9.1 Layout Guidelines.....                                       | <b>8</b> |
| <b>5 Specifications</b> .....                             | <b>4</b> | 9.2 Layout Example.....                                          | <b>8</b> |
| 5.1 Absolute Maximum Ratings.....                         | <b>4</b> | <b>10 Device and Documentation Support</b> .....                 | <b>9</b> |
| 5.2 Recommended Operating Conditions <sup>(1)</sup> ..... | <b>4</b> | 10.1 Documentation Support.....                                  | <b>9</b> |
| 5.3 Thermal Information.....                              | <b>4</b> | 10.2 Receiving Notification of Documentation Updates....         | <b>9</b> |
| 5.4 Electrical Characteristics.....                       | <b>5</b> | 10.3 サポート・リソース.....                                              | <b>9</b> |
| 5.5 Switching Characteristics.....                        | <b>5</b> | 10.4 Trademarks.....                                             | <b>9</b> |
| 5.6 Operating Characteristics.....                        | <b>5</b> | 10.5 Electrostatic Discharge Caution.....                        | <b>9</b> |
| <b>6 Parameter Measurement Information</b> .....          | <b>6</b> | 10.6 Glossary.....                                               | <b>9</b> |
| <b>7 Detailed Description</b> .....                       | <b>7</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>9</b> |
| 7.1 Overview.....                                         | <b>7</b> |                                                                  |          |
| 7.2 Functional Block Diagram.....                         | <b>7</b> |                                                                  |          |

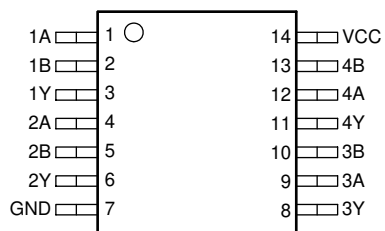
### 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

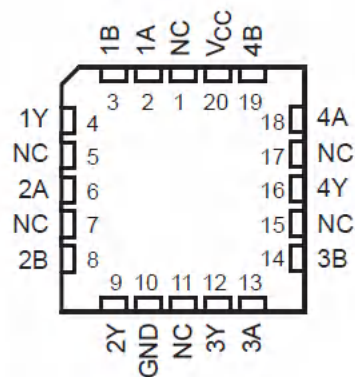
| <b>Changes from Revision E (February 2022) to Revision F (October 2022)</b>                                                         | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Increased R <sub>θJA</sub> for packages: D (86 to 138.7); DB (96 to 114.8); N (80 to 67); NS (76 to 93.3); PW (113 to 159.8)..... | <b>4</b>    |

| <b>Changes from Revision D (August 2003) to Revision E (February 2022)</b> | <b>Page</b> |
|----------------------------------------------------------------------------|-------------|
| • 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新.....                       | <b>1</b>    |

## 4 Pin Configuration and Functions



**D, DB, J, N, NS, PW or W Package**  
**14-Pin SOIC, SSOP, PDIP, SO or TSSOP**  
**Top View**



NC – No internal connection

**FK Package**  
**20-Pin LCCC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                        |                                     | MIN                                                       | MAX | UNIT       |
|------------------------|-------------------------------------|-----------------------------------------------------------|-----|------------|
| V <sub>CC</sub>        | Supply voltage range                | -0.5                                                      | 7   | V          |
| I <sub>IK</sub>        | Input clamp current <sup>(2)</sup>  | (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) |     | ±20 mA     |
| I <sub>OK</sub>        | Output clamp current <sup>(2)</sup> | (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) |     | ±20 mA     |
| I <sub>O</sub>         | Continuous output current           | (V <sub>O</sub> = 0 to V <sub>CC</sub> )                  |     | ±25 mA     |
| V <sub>CC</sub> or GND | Continuous current through          |                                                           |     | ±50 mA     |
| T <sub>J</sub>         | Junction temperature                |                                                           |     | 150 °C     |
| T <sub>stg</sub>       | Storage temperature                 |                                                           |     | -65 150 °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

|                 |                                 |                                  | SN54HCT08 <sup>(2)</sup> |     |                 | SN74HCT08 |     |                 | UNIT |
|-----------------|---------------------------------|----------------------------------|--------------------------|-----|-----------------|-----------|-----|-----------------|------|
|                 |                                 |                                  | MIN                      | NOM | MAX             | MIN       | NOM | MAX             |      |
| V <sub>CC</sub> | Supply voltage                  |                                  | 4.5                      | 5   | 5.5             | 4.5       | 5   | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 4.5 V to 5.5 V | 2                        |     |                 | 2         |     |                 | V    |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 4.5 V to 5.5 V |                          |     | 0.8             |           |     | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                   |                                  | 0                        |     | V <sub>CC</sub> | 0         |     | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                  |                                  | 0                        |     | V <sub>CC</sub> | 0         |     | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise/fall time |                                  |                          |     | 500             |           |     | 500             | ns   |
| T <sub>A</sub>  | Operating free-air temperature  |                                  | - 55                     |     | 125             | - 40      |     | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number [SCBA004](#).
- (2) SN54HCT08 is in product preview.

### 5.3 Thermal Information

|                        |                                                       | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|------------------------|-------------------------------------------------------|----------|-----------|----------|---------|------------|------|
| THERMAL METRIC         |                                                       | 14 PINS  | 14 PINS   | 14 PINS  | 14 PINS | 14 PINS    |      |
| R <sub>θJA</sub>       | Junction-to-ambient thermal resistance <sup>(1)</sup> | 138.7    | 114.8     | 67       | 93.3    | 159.8      | °C/W |
| R <sub>θJC (top)</sub> | Junction-to-case (top) thermal resistance             | 93.8     | 60        | 55       | 50.9    | 92.7       | °C/W |
| R <sub>θJB</sub>       | Junction-to-board thermal resistance                  | 94.7     | 63.8      | 46.7     | 53.8    | 102.1      | °C/W |
| Ψ <sub>JT</sub>        | Junction-to-top characterization parameter            | 49.1     | 19.7      | 35.1     | 17.8    | 40.4       | °C/W |
| Ψ <sub>JB</sub>        | Junction-to-board characterization parameter          | 94.3     | 63.1      | 46.5     | 53.3    | 101.7      | °C/W |
| R <sub>θJC (bot)</sub> | Junction-to-case (bottom) thermal resistance          | N/A      | N/A       | N/A      | N/A     | N/A        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

| PARAMETER                       |                           | TEST CONDITIONS <sup>(1)</sup>                                   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |       |      | SN54HCT08 <sup>(3)</sup> |       | SN74HCT08 |       | UNIT |
|---------------------------------|---------------------------|------------------------------------------------------------------|------------------------|-----------------------|-------|------|--------------------------|-------|-----------|-------|------|
|                                 |                           |                                                                  |                        | MIN                   | TYP   | MAX  | MIN                      | MAX   | MIN       | MAX   |      |
| V <sub>OH</sub>                 | High-level output voltage | I <sub>OH</sub> = –20 µA                                         | 4.5                    | 4.4                   | 4.499 |      | 4.4                      |       | 4.4       |       | V    |
|                                 |                           | I <sub>OH</sub> = –4 mA                                          |                        | 3.98                  | 4.3   |      | 3.7                      |       | 3.84      |       |      |
| V <sub>OL</sub>                 | Low-level output voltage  | I <sub>OL</sub> = 20 µA                                          | 4.5                    |                       | 0.001 | 0.1  |                          | 0.1   |           | 0.1   | V    |
|                                 |                           | I <sub>OL</sub> = 4 mA                                           |                        |                       | 0.17  | 0.26 |                          | 0.4   |           | 0.33  |      |
| I <sub>I</sub>                  | Input hold current        | V <sub>I</sub> = V <sub>CC</sub> or 0                            | 5.5                    |                       | ±0.1  | ±100 |                          | ±1000 |           | ±1000 | nA   |
| I <sub>CC</sub>                 | Supply current            | V <sub>I</sub> = V <sub>CC</sub> or 0. I <sub>O</sub> = 0        | 5.5                    |                       |       | 2    |                          | 40    |           | 20    | µA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | Supply-current change     | One input at 0.5V or 2.4 V, Other inputs at 0 or V <sub>CC</sub> | 5.5                    |                       | 1.4   | 2.4  |                          | 3     |           | 2.9   | mA   |
| C <sub>i</sub>                  | Input capacitance         |                                                                  | 4.5 to 5.5             |                       | 3     | 10   |                          | 10    |           | 10    | pF   |

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

(3) SN54HCT08 is in product preview.

## 5.5 Switching Characteristics

C<sub>L</sub> = 50 pF. See [Parameter Measurement Information](#)

| PARAMETER       |                   | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |     |     | SN54HCT08 <sup>(1)</sup> |     | SN74HCT08 |     |    |
|-----------------|-------------------|--------------|-------------|------------------------|-----------------------|-----|-----|--------------------------|-----|-----------|-----|----|
|                 |                   |              |             |                        | MIN                   | TYP | MAX | MIN                      | MAX | MIN       | MAX |    |
| t <sub>pd</sub> | Propagation delay | A or B       | Y           | 4.5                    |                       | 15  | 24  |                          | 35  |           | 30  | ns |
|                 |                   |              |             | 5.5                    |                       | 13  | 22  |                          | 32  |           | 27  |    |
| t <sub>t</sub>  | Transition time   |              | Y           | 4.5                    |                       | 9   | 15  |                          | 22  |           | 19  | ns |
|                 |                   |              |             | 5.5                    |                       | 8   | 14  |                          | 20  |           | 17  |    |

(1) SN54HCT08 is in product preview.

## 5.6 Operating Characteristics

T<sub>A</sub> = 25°C

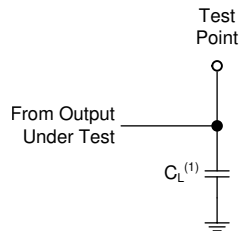
|                 |                                        | Test Conditions | TYP | UNIT |
|-----------------|----------------------------------------|-----------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance per gate | No load         | 20  | pF   |

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \, \Omega$ ,  $t_t < 6 \text{ ns}$ .

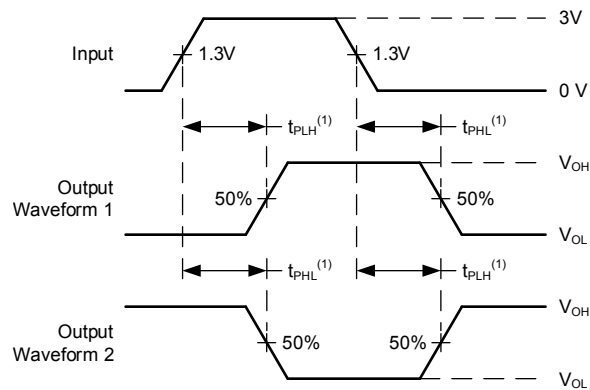
For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1)  $C_L$  includes probe and test-fixture capacitance.

**FIG 6-1. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

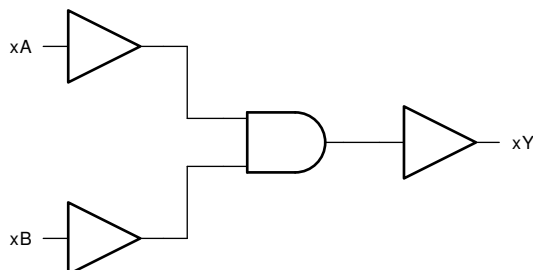
**FIG 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**

## 7 Detailed Description

### 7.1 Overview

This device contains four independent 2-input AND Gates. Each gate performs the Boolean function  $Y = A \bullet B$  in positive logic.

### 7.2 Functional Block Diagram



✎ 7-1. Functional Block Diagram

### 7.3 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCT08.

表 7-1. Function Table

| INPUTS <sup>(1)</sup> |   | OUTPUT |
|-----------------------|---|--------|
| A                     | B | Y      |
| H                     | H | H      |
| L                     | X | L      |
| X                     | L | L      |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## 8 Power Supply Recommendations

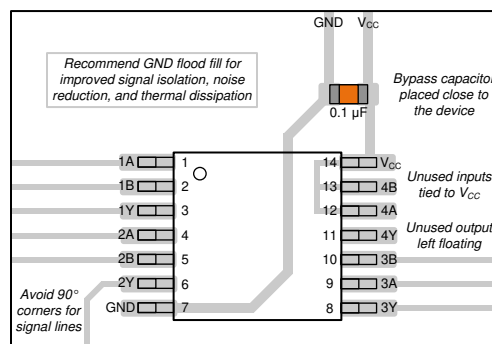
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.2 Layout Example



 **9-1. Example layout for the SN74HCT08**



## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74HCT08DBR     | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT08                    | <a href="#">Samples</a> |
| SN74HCT08DR      | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | HCT08                   | <a href="#">Samples</a> |
| SN74HCT08DRE4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT08                   | <a href="#">Samples</a> |
| SN74HCT08DRG4    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT08                   | <a href="#">Samples</a> |
| SN74HCT08N       | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HCT08N              | <a href="#">Samples</a> |
| SN74HCT08NE4     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HCT08N              | <a href="#">Samples</a> |
| SN74HCT08NSR     | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT08                   | <a href="#">Samples</a> |
| SN74HCT08PWR     | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | HT08                    | <a href="#">Samples</a> |
| SN74HCT08PWRG4   | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT08                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

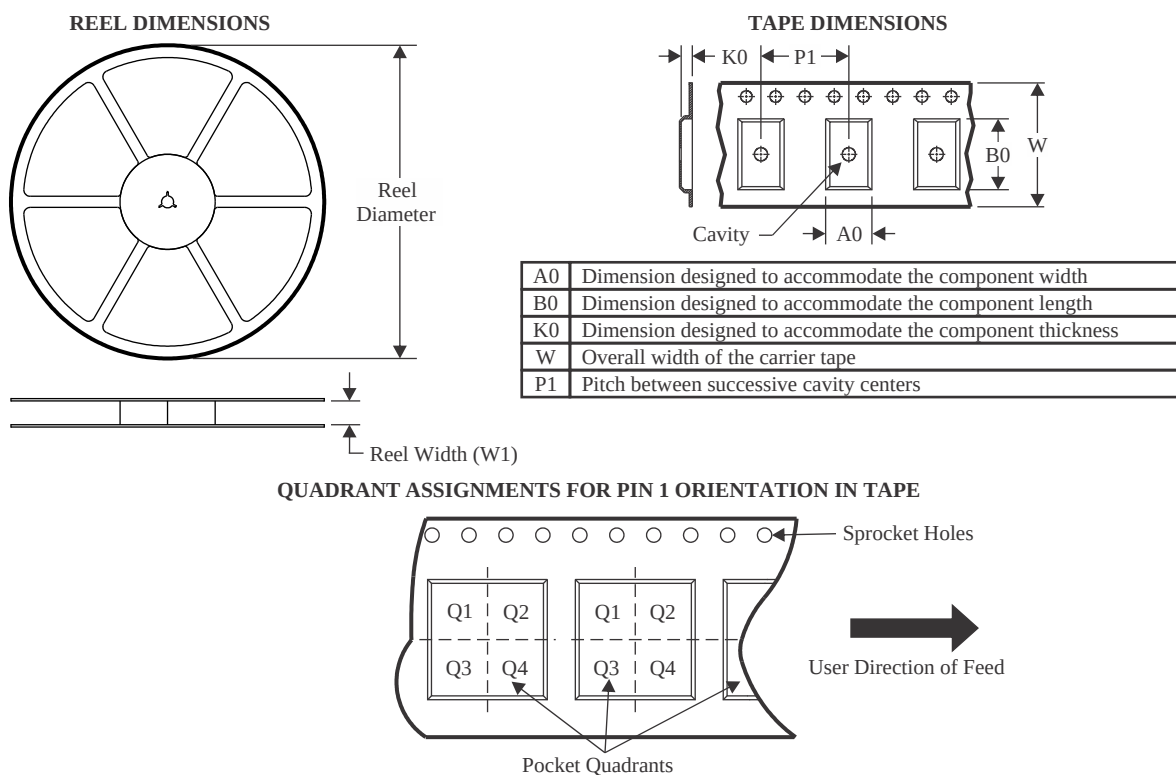
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

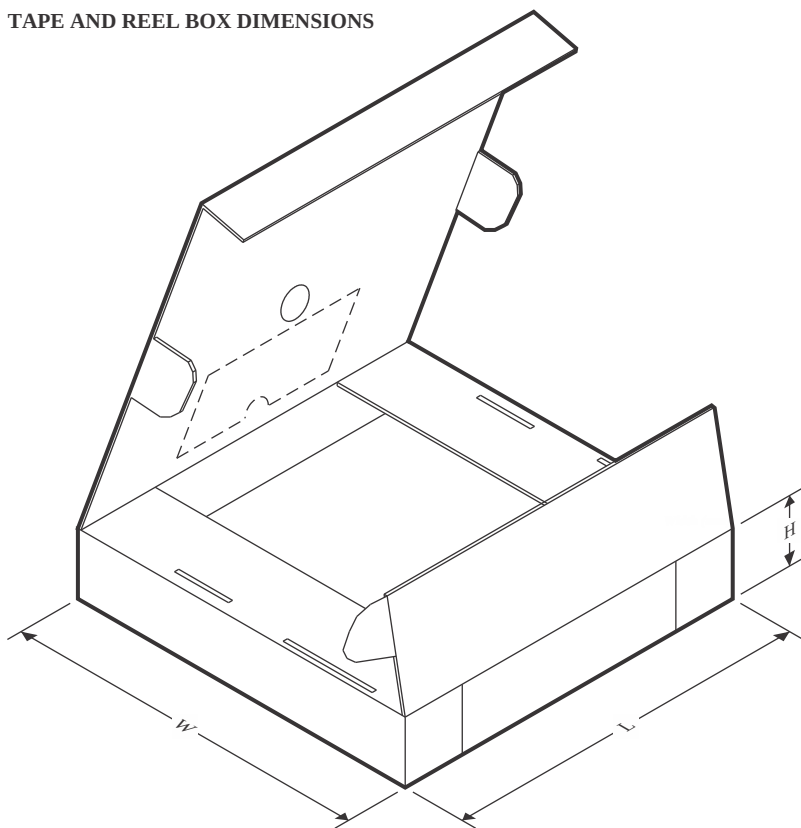
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT08DBR | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74HCT08DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.6     | 9.3     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HCT08NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.85    | 5.45    | 1.6     | 8.0     | 12.0   | Q1            |

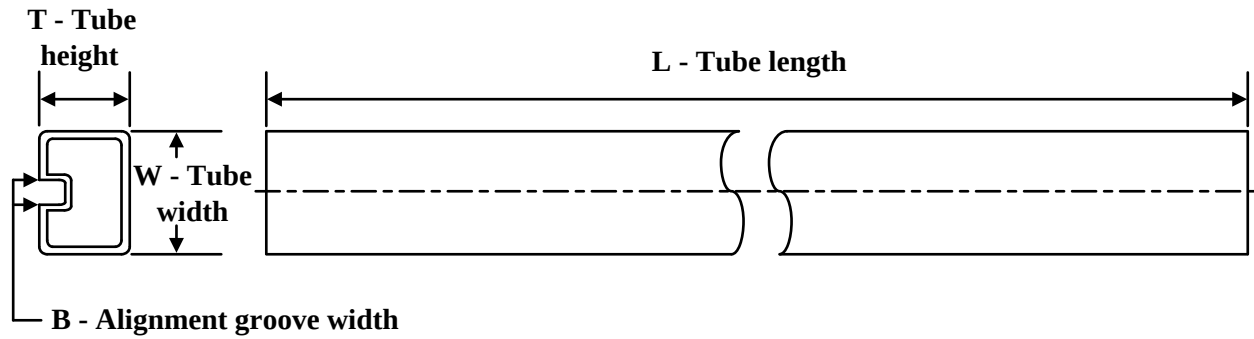
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT08DBR | SSOP         | DB              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HCT08DR  | SOIC         | D               | 14   | 2500 | 366.0       | 364.0      | 50.0        |
| SN74HCT08NSR | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HCT08PWR | TSSOP        | PW              | 14   | 2000 | 366.0       | 364.0      | 50.0        |

## TUBE



\*All dimensions are nominal

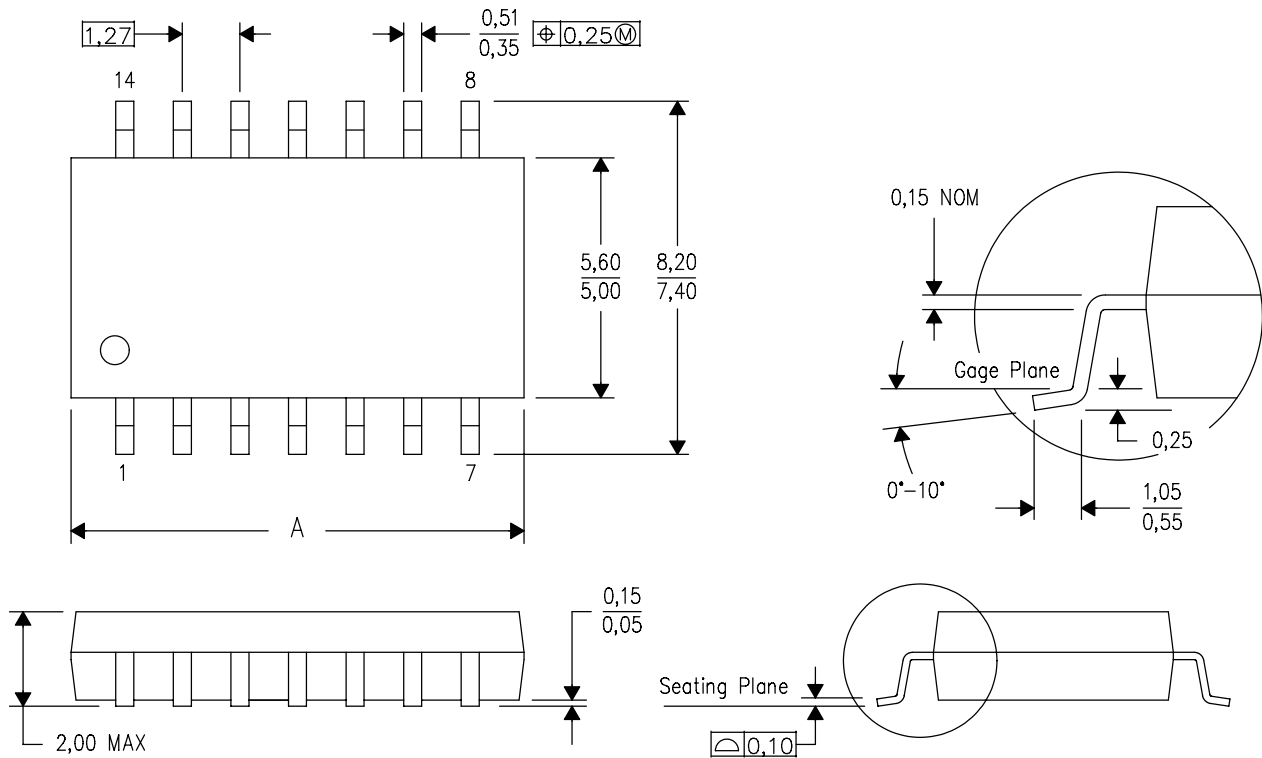
| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HCT08N   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HCT08N   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HCT08NE4 | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HCT08NE4 | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



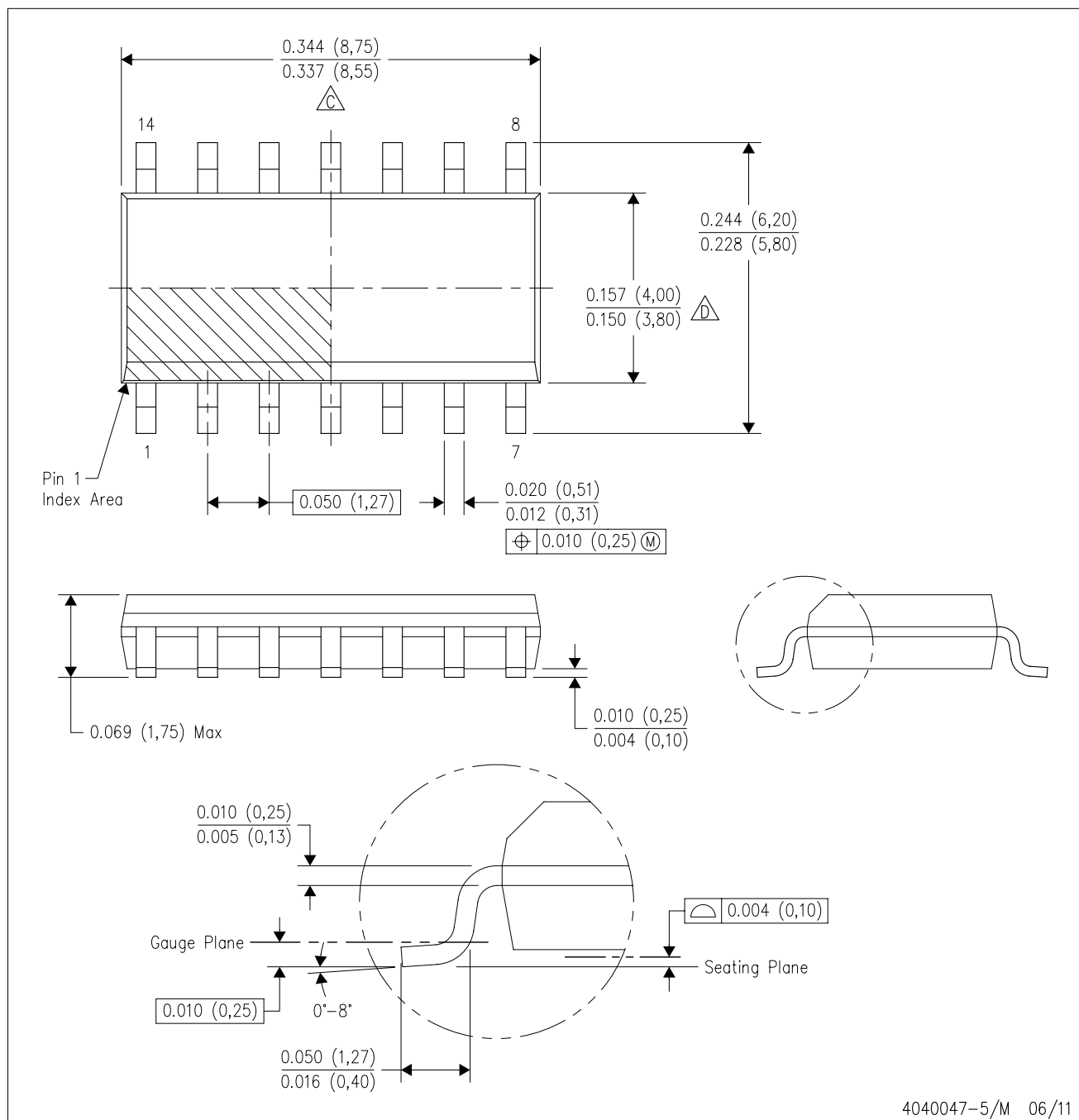
| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



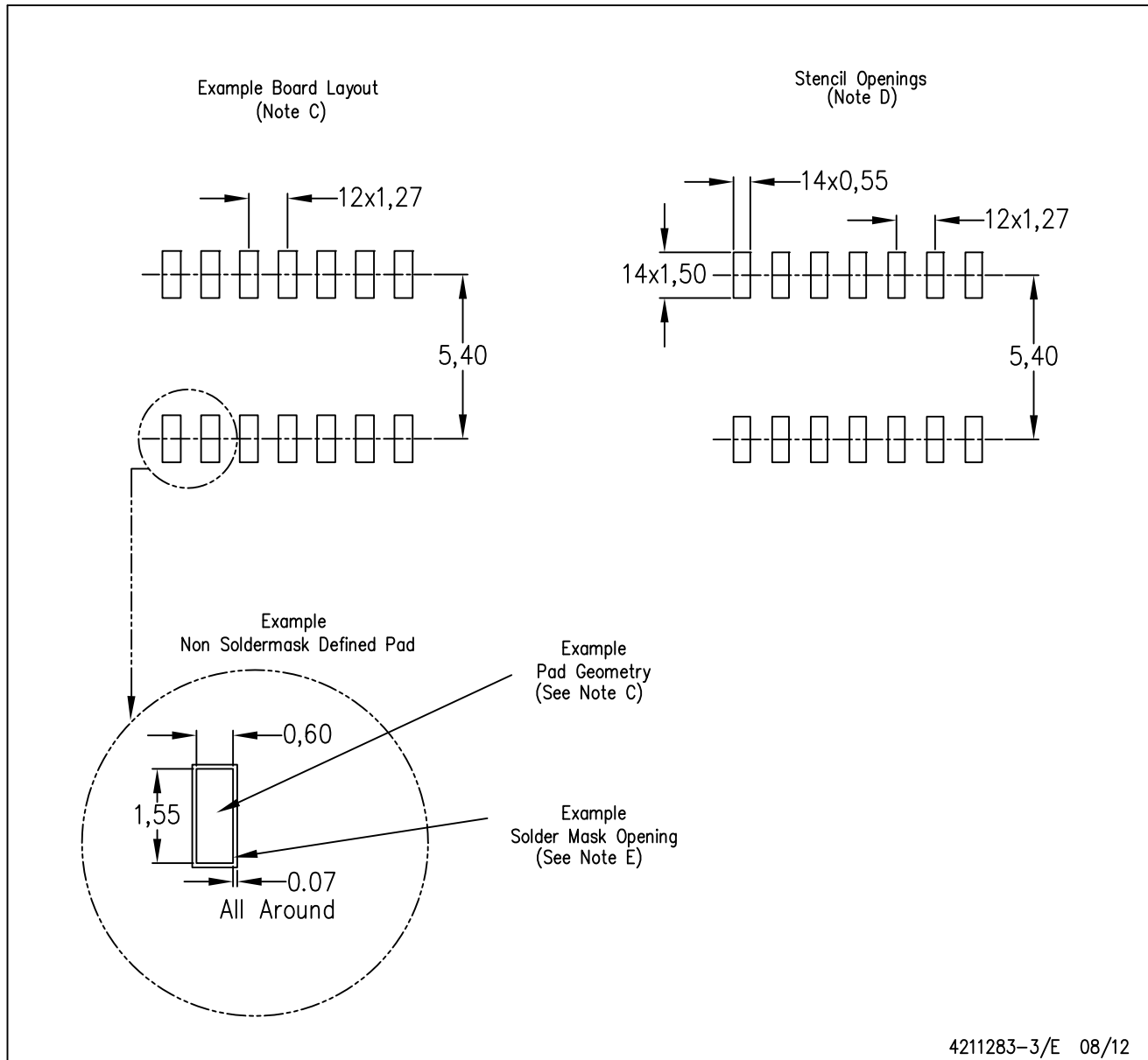
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

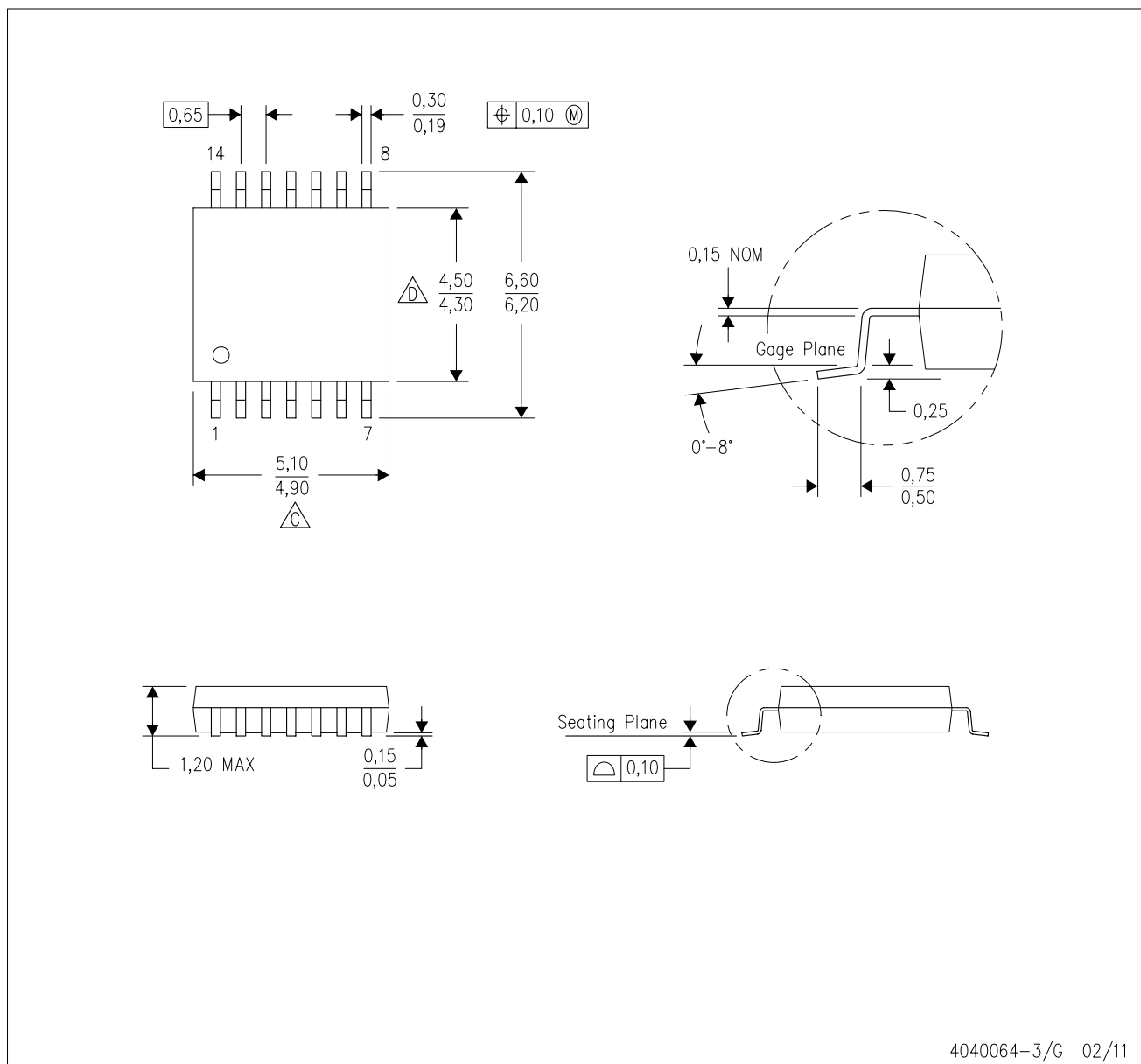
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

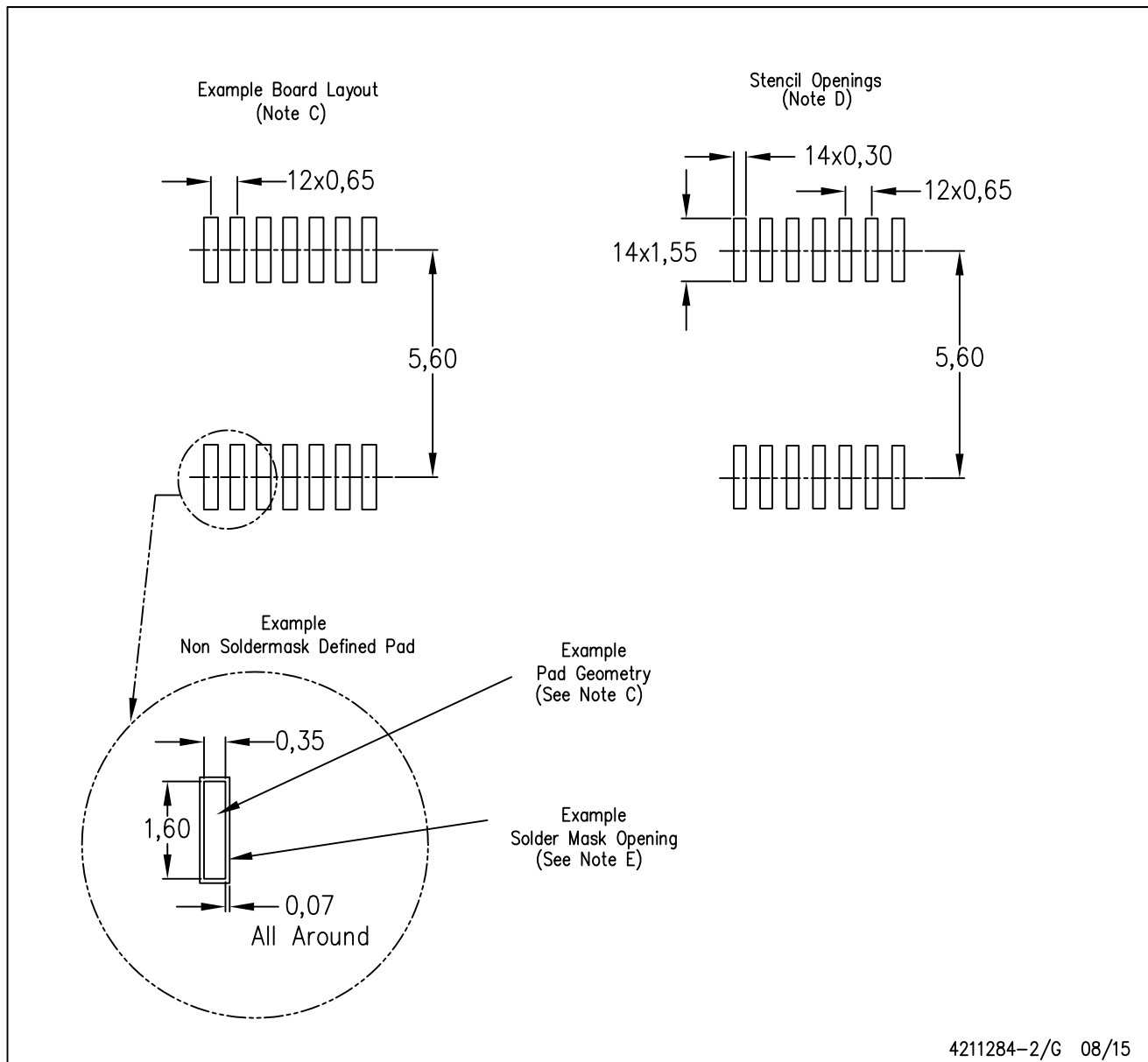
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



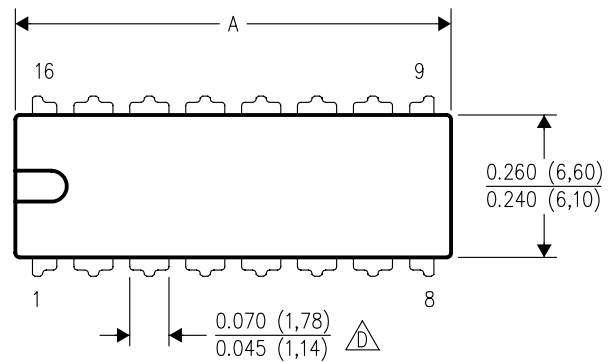
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

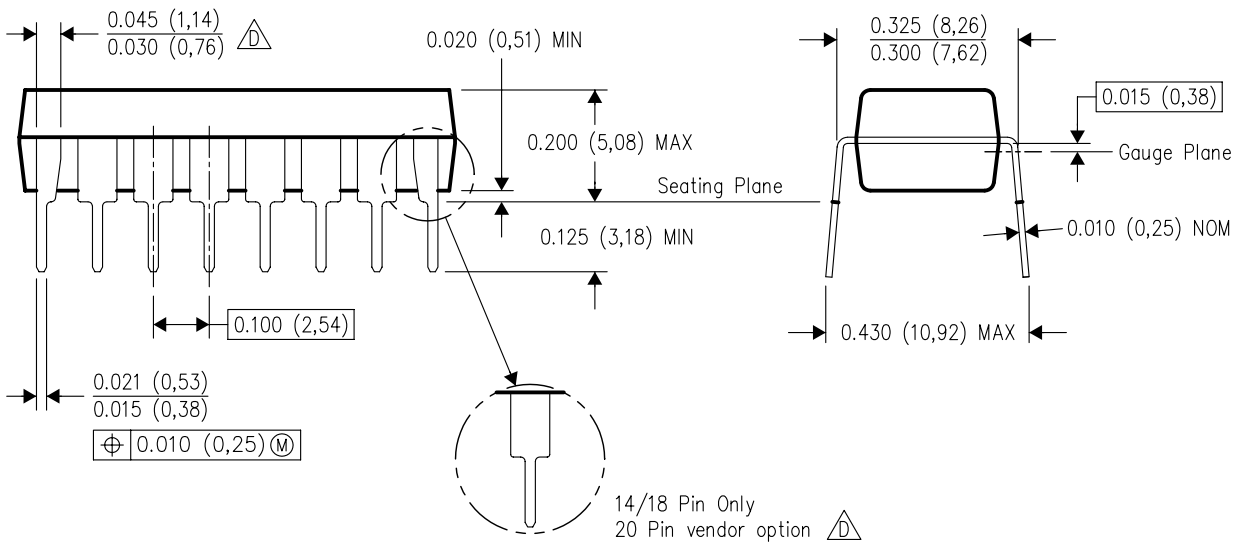
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

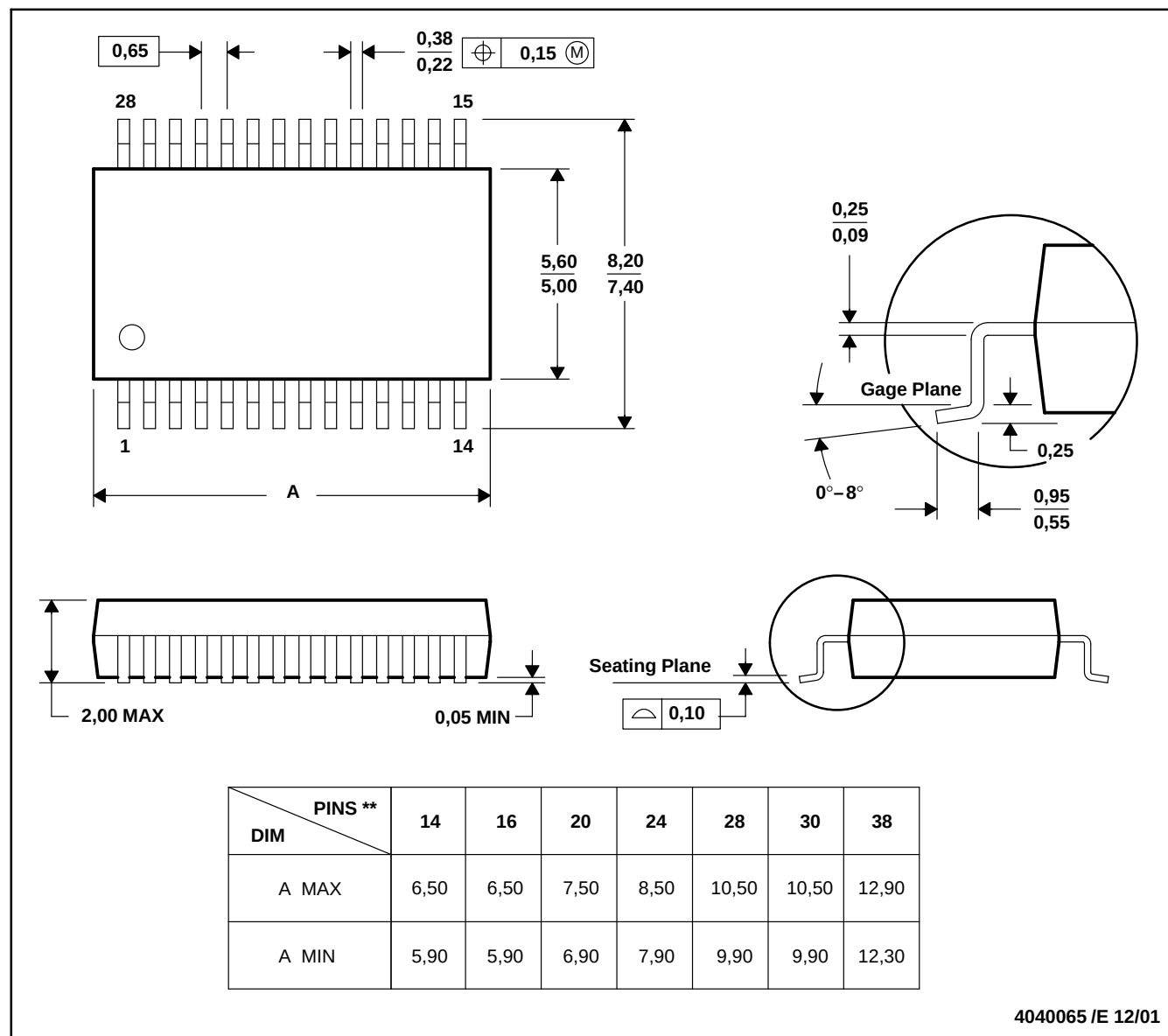
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとしします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated