

# TAS2505-Q1 2.6W デジタル/アナログ入力、オーディオ処理機能搭載、車載用 Class-D スピーカー・アンプ

## 1 特長

- 車載用アプリケーション向けに次の内容で AEC-Q100 認定済み:
  - デバイス温度グレード 2: -40°C ~ 105°C の動作時 周囲温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- モノラル D 級 BTL スピーカー・アンプ
  - 10% THD<sub>N</sub> で 2.6W (4Ω, 5.5V)
  - 10% THD+N で 1.7W (8Ω, 5.5V)
- デジタルとアナログ両方の入力に対応
- 単電源: 2.7V ~ 5.5V
- 負荷診断機能:
  - 出力から GND への短絡
  - 端子から端子への短絡
  - 出力から電源への短絡
  - 過熱
- 9kHz ~ 96kHz のサンプル・レートをサポート
- 2 つのシングル・エンド入力と、出力ミキシングおよびレベル制御
- パワーオン・リセットを内蔵
- プログラム可能なデジタル・オーディオ処理:
  - バス・ブースト
  - トレブル
  - EQ (最大 6 バイクワッドまで)
- I<sup>2</sup>S、左揃え、右揃え、DSP、TDM のオーディオ・インターフェイス
- I<sup>2</sup>C および SPI 制御、自動インクリメント付き
- 24 ピン、VQFN ウェットابل・フランク (車載用グレード) パッケージ

## 2 アプリケーション

- インストルメント・クラスタ
- 車載用緊急通報 (eCall)
- テレマティクス

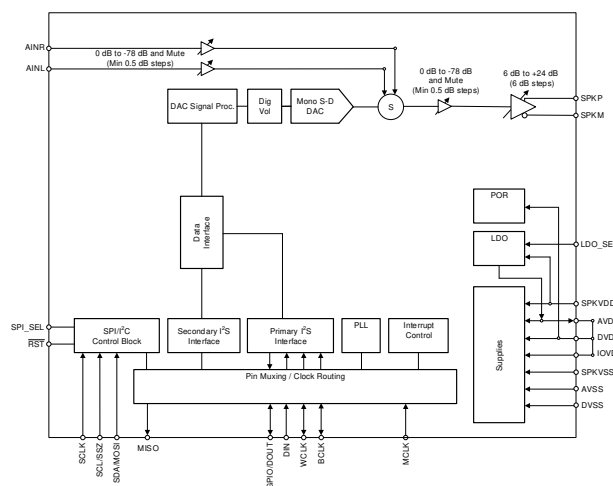
## 3 概要

TAS2505-Q1 は、モノラル D 級スピーカー・アンプで、デジタル入力とアナログ入力の両方に対応しています。このデバイスは、車載用インストルメント・クラスタ、緊急通報 (eCall)、テレマティクスなどのアプリケーション向けに設計されています。直接 I<sup>2</sup>S 入力により、オーディオ信号パスに外付け DAC が不要になり、内蔵の LDO によって単電源で動作します。このデバイスは、統合に加えて、プログラム可能なオーディオ処理を備えています。オンボードの DSP は、バス・ブースト、トレブル、EQ (最大 6 バイクワッドまで) をサポートします。オンチップの PLL が、DSP に必要な高速のクロックを供給します。ボリューム・レベルはレジスタで制御されています。

### 製品情報 (1)

| 部品番号        | パッケージ     | パッケージ・サイズ (2)   |
|-------------|-----------|-----------------|
| TAS2505-Q1  | VQFN (24) | 4.00mm × 4.00mm |
| TAS2505A-Q1 | VQFN (24) | 4.00mm × 4.00mm |

- 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図



## Table of Contents

|                                                         |           |                                                                  |           |
|---------------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                                       | <b>1</b>  | <b>8.1 Overview</b> .....                                        | <b>15</b> |
| <b>2 アプリケーション</b> .....                                 | <b>1</b>  | <b>8.2 Functional Block Diagram</b> .....                        | <b>15</b> |
| <b>3 概要</b> .....                                       | <b>1</b>  | <b>8.3 Feature Description</b> .....                             | <b>15</b> |
| <b>4 Revision History</b> .....                         | <b>2</b>  | <b>8.4 Device Functional Modes</b> .....                         | <b>17</b> |
| <b>5 Pin Configuration and Functions</b> .....          | <b>3</b>  | <b>8.5 Register Map</b> .....                                    | <b>21</b> |
| <b>6 Specifications</b> .....                           | <b>5</b>  | <b>9 Application and Implementation</b> .....                    | <b>24</b> |
| 6.1 Absolute Maximum Ratings.....                       | <b>5</b>  | 9.1 Application Information.....                                 | <b>24</b> |
| 6.2 ESD Ratings.....                                    | <b>5</b>  | 9.2 Typical Applications.....                                    | <b>24</b> |
| 6.3 Recommended Operating Conditions.....               | <b>5</b>  | <b>10 Power Supply Recommendations</b> .....                     | <b>27</b> |
| 6.4 Thermal Information.....                            | <b>5</b>  | <b>11 Layout</b> .....                                           | <b>28</b> |
| 6.5 Electrical Characteristics.....                     | <b>6</b>  | 11.1 Layout Guidelines.....                                      | <b>28</b> |
| 6.6 I <sup>2</sup> S/LJF/RJF Timing in Master Mode..... | <b>8</b>  | 11.2 Layout Example.....                                         | <b>28</b> |
| 6.7 I <sup>2</sup> S/LJF/RJF Timing in Slave Mode.....  | <b>8</b>  | 11.3 Thermal Pad.....                                            | <b>29</b> |
| 6.8 DSP Timing in Master Mode.....                      | <b>8</b>  | <b>12 Device and Documentation Support</b> .....                 | <b>30</b> |
| 6.9 DSP Timing in Slave Mode.....                       | <b>8</b>  | 12.1 Documentation Support.....                                  | <b>30</b> |
| 6.10 I <sup>2</sup> C Interface Timing.....             | <b>9</b>  | 12.2 Receiving Notification of Documentation Updates.....        | <b>30</b> |
| 6.11 SPI Interface Timing.....                          | <b>9</b>  | 12.3 Community Resources.....                                    | <b>30</b> |
| 6.12 Typical Characteristics.....                       | <b>12</b> | 12.4 Trademarks.....                                             | <b>30</b> |
| <b>7 Parameter Measurement Information</b> .....        | <b>14</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>30</b> |
| <b>8 Detailed Description</b> .....                     | <b>15</b> |                                                                  |           |

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

|                                                                                   |             |
|-----------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision D (June 2023) to Revision E (July 2023)</b> .....        | <b>Page</b> |
| • TAS2505A-Q1 をデータシートに追加.....                                                     | <b>1</b>    |
| <b>Changes from Revision C (February 2022) to Revision D (June 2023)</b> .....    | <b>Page</b> |
| • Errata in RevC datasheet with the LDO_SEL feature fixed.....                    | <b>3</b>    |
| <b>Changes from Revision B (October 2018) to Revision C (February 2022)</b> ..... | <b>Page</b> |
| • 「特長」セクションの温度定格を、推奨動作条件の温度定格と一致するよう整合.....                                       | <b>1</b>    |
| <b>Changes from Revision A (December 2017) to Revision B (October 2018)</b> ..... | <b>Page</b> |
| • Added the <i>Thermal Pad</i> section.....                                       | <b>29</b>   |
| <b>Changes from Revision * (July 2017) to Revision A (December 2017)</b> .....    | <b>Page</b> |
| • AEC 分類レベルを追加.....                                                               | <b>1</b>    |
| • パッケージの特長に「ウェットابل・フランク (車載用グレード)」の記述を追加.....                                    | <b>1</b>    |

## 5 Pin Configuration and Functions

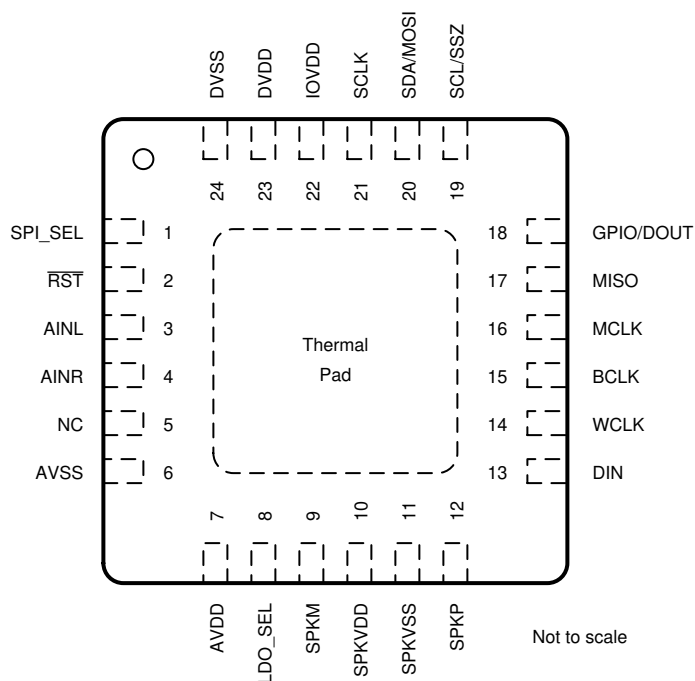


図 5-1. RGE Package 24-Pin VQFN Top View

表 5-1. Pin Functions

| PIN |           | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                  |
|-----|-----------|---------------------|--------------------------------------------------------------------------------------------------------------|
| NO. | NAME      |                     |                                                                                                              |
| 1   | SPI_SEL   | I                   | Selects between SPI and I <sup>2</sup> C digital interface modes; (1 = SPI mode) (0 = I <sup>2</sup> C mode) |
| 2   | RST       | I                   | Reset for logic, state machines, and digital filters; asserted LOW.                                          |
| 3   | AINL      | I                   | Analog single-ended line left input                                                                          |
| 4   | AINR      | I                   | Analog single-ended line right input                                                                         |
| 5   | NC        | O                   | No Connect (Leave unconnected)                                                                               |
| 6   | AVSS      | GND                 | Analog Ground, 0 V                                                                                           |
| 7   | AVDD      | PWR                 | Analog Core Supply Voltage, 1.5 V to 1.95 V, tied internally to the LDO output                               |
| 8   | LDO_SEL   | I                   | Select Pin for LDO; ties to either SPKVDD or SPKVSS                                                          |
| 9   | SPKM      | O                   | Class-D speaker driver inverting output                                                                      |
| 10  | SPKVDD    | PWR                 | Class-D speaker driver power supply                                                                          |
| 11  | SPKVSS    | PWR                 | Class-D speaker driver power supply ground supply                                                            |
| 12  | SPKP      | O                   | Class-D speaker driver noninverting output                                                                   |
| 13  | DIN       | I                   | Audio Serial Data Bus Input Data                                                                             |
| 14  | WCLK      | I/O                 | Audio Serial Data Bus Word Clock                                                                             |
| 15  | BCLK      | I/O                 | Audio Serial Data Bus Bit Clock                                                                              |
| 16  | MCLK      | I                   | Master CLK Input / Reference CLK for CLK Multiplier - PLL (On startup PLLCLK = CLKIN)                        |
| 17  | MISO      | O                   | SPI Serial Data Output                                                                                       |
| 18  | GPIO/DOUT | I/O/Z               | GPIO / Audio Serial Bus Output                                                                               |
| 19  | SCL/SSZ   | I                   | Either I <sup>2</sup> C Input Serial Clock or SPI Chip Select Signal depending on SPI_SEL state              |
| 20  | SDA/MOSI  | I                   | Either I <sup>2</sup> C Serial Data Input or SPI Serial Data Input depending on SPI_SEL state.               |
| 21  | SCLK      | I                   | Serial clock for SPI interface                                                                               |
| 22  | IOVDD     | PWR                 | I/O Power Supply, 1.1 V to 3.6 V                                                                             |
| 23  | DVDD      | PWR                 | Digital Power Supply, 1.65 V to 1.95 V                                                                       |

表 5-1. Pin Functions (continued)

| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION         |
|-----|------|---------------------|---------------------|
| NO. | NAME |                     |                     |
| 24  | DVSS | GND                 | Digital Ground, 0 V |

(1) I = Input, O = Output, GND = Ground, PWR = Power, Z = High Impedance

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                                                         | MIN                                     | MAX         | UNIT |
|-------------------------------------------------------------------------|-----------------------------------------|-------------|------|
| AVDD to AVSS                                                            | −0.3                                    | 2.2         | V    |
| DVDD to DVSS                                                            | −0.3                                    | 2.2         | V    |
| SPKVDD to SPKVSS                                                        | −0.3                                    | 6           | V    |
| IOVDD to IOVSS                                                          | −0.3                                    | 3.9         | V    |
| Digital input voltage                                                   | IOVSS − 0.3                             | IOVDD + 0.3 | V    |
| Analog input voltage                                                    | AVSS − 0.3                              | AVDD + 0.3  | V    |
| Operating temperature                                                   | −40                                     | 105         | °C   |
| Junction temperature, T <sub>J</sub> Max                                |                                         | 125         | °C   |
| Power dissipation for VQFN package (with thermal pad soldered to board) | $(T_J \text{ Max} - T_A) / \theta_{JA}$ |             | W    |
| Storage temperature, T <sub>stg</sub>                                   | −55                                     | 150         | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                            | VALUE                                                   | UNIT  |
|--------------------------------------------|---------------------------------------------------------|-------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000 |
|                                            | Charged-device model (CDM), per AEC Q100-011            | ±1500 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                                       |                                               | MIN  | NOM | MAX  | UNIT             |
|-----------------------|---------------------------------------|-----------------------------------------------|------|-----|------|------------------|
| AVDD <sup>(2)</sup>   | Power-supply voltage                  | Referenced to AVSS <sup>(1)</sup>             | 1.5  | 1.8 | 1.95 | V                |
| DVDD                  |                                       | Referenced to DVSS <sup>(1)</sup>             | 1.65 | 1.8 | 1.95 |                  |
| SPKVDD <sup>(2)</sup> |                                       | Referenced to SPKVSS <sup>(1)</sup>           | 2.7  |     | 5.5  |                  |
| IOVDD                 |                                       | Referenced to IOVSS <sup>(1)</sup>            | 1.1  | 1.8 | 3.6  |                  |
|                       | Speaker impedance                     | Load applied across class-D output pins (BTL) | 4    |     |      | Ω                |
| V <sub>I</sub>        | Analog audio full-scale input voltage | AVDD = 1.8 V, single-ended                    |      | 0.5 |      | V <sub>RMS</sub> |
| MCLK <sup>(3)</sup>   | Master clock frequency                | IOVDD = DVDD = 1.8 V                          |      |     | 50   | MHz              |
| SCL                   | SCL clock frequency                   |                                               |      |     | 400  | kHz              |
| T <sub>A</sub>        | Operating free-air temperature        |                                               | −40  |     | 105  | °C               |

- (1) All grounds on board are tied together, so they should not differ in voltage by more than 0.2 V maximum for any combination of ground signals. By use of a wide trace or ground plane, ensure a low-impedance connection between AVSS and DVSS.  
(2) To minimize battery-current leakage, the SPKVDD voltage level should not be below the AVDD voltage level.  
(3) The maximum input frequency should be 50 MHz for any digital pin used as a general-purpose clock.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                           | TAS2505-Q1 | UNIT |
|-------------------------------|-------------------------------------------|------------|------|
|                               |                                           | RGE (QFN)  |      |
|                               |                                           | 24 PINS    |      |
| θ <sub>JA</sub>               | Junction-to-ambient thermal resistance    | 32.2       | °C/W |
| θ <sub>JCTop</sub>            | Junction-to-case (top) thermal resistance | 30         | °C/W |

| THERMAL METRIC <sup>(1)</sup> |                                              | TAS2505-Q1 | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGE (QFN)  |      |
|                               |                                              | 24 PINS    |      |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 9.2        | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.3        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 9.2        | °C/W |
| $\theta_{JCbot}$              | Junction-to-case (bottom) thermal resistance | 2.2        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V,  $f_s$  (audio) = 48 kHz, CODEC\_CLKIN =  $256 \times f_s$ , PLL = Off

| PARAMETER                                                                                                       |                                   | TEST CONDITIONS                                                                                                | MIN | TYP   | MAX | UNIT |
|-----------------------------------------------------------------------------------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------|-----|-------|-----|------|
| INTERNAL OSCILLATOR—RC_CLK                                                                                      |                                   |                                                                                                                |     |       |     |      |
| Oscillator frequency                                                                                            |                                   |                                                                                                                |     | 8.48  |     | MHz  |
| DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS                                                                |                                   |                                                                                                                |     |       |     |      |
| See <a href="#">TAS2505 Application Reference Guide</a> (SLAU472) for DAC interpolation filter characteristics. |                                   |                                                                                                                |     |       |     |      |
| DAC OUTPUT TO CLASS-D SPEAKER OUTPUT; LOAD = 4 Ω (DIFFERENTIAL)                                                 |                                   |                                                                                                                |     |       |     |      |
| ICN                                                                                                             | Idle channel noise                | BTL measurement, class-D gain = 6 dB, Measured as idle-channel noise, A-weighted <sup>(2)</sup> <sup>(1)</sup> |     | 37    |     | μVms |
|                                                                                                                 | Output voltage                    | BTL measurement, class-D gain = 6 dB, −3-dBFS input                                                            |     | 1.4   |     | Vrms |
| THD+N                                                                                                           | Total harmonic distortion + noise | BTL measurement, DAC input = −6 dBFS, class-D gain = 6 dB                                                      |     | −73.9 |     | dB   |
| PSRR                                                                                                            | Power-supply rejection ratio      | BTL measurement, ripple on SPKVDD = 200 mV <sub>PP</sub> at 1 kHz                                              |     | 55    |     | dB   |
|                                                                                                                 | Mute attenuation                  | Mute                                                                                                           |     | 103   |     | dB   |
| P <sub>O</sub>                                                                                                  | Maximum output power              | SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 10%                                    |     | 1.1   |     | W    |
|                                                                                                                 |                                   | SPKVDD = 4.2 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 10%                                   |     | 1.4   |     |      |
|                                                                                                                 |                                   | SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%                                     |     | 0.8   |     |      |
|                                                                                                                 |                                   | SPKVDD = 4.2 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%                                     |     | 1.1   |     |      |
|                                                                                                                 |                                   | SPKVDD = 5.5 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB                                               |     |       | 2   |      |
| DAC OUTPUT TO CLASS-D SPEAKER OUTPUT; LOAD = 8 Ω (DIFFERENTIAL)                                                 |                                   |                                                                                                                |     |       |     |      |
| ICN                                                                                                             | Idle channel noise                | BTL measurement, class-D gain = 6 dB, measured as idle-channel noise, A-weighted <sup>(2)</sup> <sup>(1)</sup> |     | 35.2  |     | μVms |
|                                                                                                                 | Output voltage                    | BTL measurement, class-D gain = 6 dB, −3-dBFS input                                                            |     | 1.4   |     | Vrms |
| THD+N                                                                                                           | Total harmonic distortion + noise | BTL measurement, DAC input = −6 dBFS, class-D gain = 6 dB                                                      |     | −73.6 |     | dB   |

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V,  $f_S$  (audio) = 48 kHz, CODEC\_CLKIN = 256 ×  $f_S$ , PLL = Off

| PARAMETER                                  |                                   | TEST CONDITIONS                                                                                                            | MIN | TYP         | MAX         | UNIT |
|--------------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------|-----|-------------|-------------|------|
| P <sub>O</sub>                             | Maximum output power              | SPKVDD = 3.6 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 10%                                               |     | 0.7         |             | W    |
|                                            |                                   | SPKVDD = 4.2 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 10%                                               |     | 1           |             |      |
|                                            |                                   | SPKVDD = 5.5 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 10%                                               |     | 1.7         |             |      |
|                                            |                                   | SPKVDD = 3.6 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 1%                                                |     | 0.5         |             |      |
|                                            |                                   | SPKVDD = 4.2 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 1%                                                |     | 0.8         |             |      |
|                                            |                                   | SPKVDD = 5.5 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 1%                                                |     | 1.3         |             |      |
| ANALOG BYPASS TO CLASS-D SPEAKER AMPLIFIER |                                   |                                                                                                                            |     |             |             |      |
| Device setup                               |                                   | BTL measurement, driver gain = 6 dB, load = 4 Ω (differential), 50 pF, input signal frequency fi = 1 KHz                   |     |             |             |      |
| Voltage gain                               |                                   | Input common-mode = 0.9 V                                                                                                  |     | 4           |             | V/V  |
| Gain error                                 |                                   | −1 dBFS (446 mVrms), 1-kHz input signal                                                                                    |     | ±0.7        |             | dB   |
| ICN                                        | Idle channel noise                | Idle channel, IN1L and IN1R ac-shortcd to ground, measured as idle-channel noise, A-weighted <sup>(2)</sup> <sup>(1)</sup> |     | 32.6        |             | μVms |
| THD+N                                      | Total harmonic distortion + noise | −1 dBFS (446 mVrms), 1-kHz input signal                                                                                    |     | −73.7       |             | dB   |
| SHUTDOWN POWER CONSUMPTION                 |                                   |                                                                                                                            |     |             |             |      |
| Device setup                               |                                   | Power down POR, /RST held low, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 4.2 V, DVDD = 1.8 V                                    |     |             |             |      |
| I(AVDD)                                    |                                   |                                                                                                                            |     | 1.32        |             | μA   |
| I(DVDD)                                    |                                   |                                                                                                                            |     | 0.04        |             | μA   |
| I(IOVDD)                                   |                                   |                                                                                                                            |     | 0.68        |             | μA   |
| I(SPKVDD)                                  |                                   |                                                                                                                            |     | 2.24        |             | μA   |
| DIGITAL INPUT/OUTPUT                       |                                   |                                                                                                                            |     |             |             |      |
| Logic family                               |                                   |                                                                                                                            |     | CMOS        |             |      |
| V <sub>IH</sub>                            | Logic level                       | I <sub>IH</sub> = 5 μA, IOVDD ≥ 1.6 V                                                                                      |     | 0.7 × IOVDD |             | V    |
|                                            |                                   | I <sub>IH</sub> = 5 μA, IOVDD < 1.6 V                                                                                      |     | IOVDD       |             |      |
| V <sub>IL</sub>                            |                                   | I <sub>IL</sub> = 5 μA, IOVDD ≥ 1.6 V                                                                                      |     | −0.3        | 0.3 × IOVDD | V    |
|                                            |                                   | I <sub>IL</sub> = 5 μA, IOVDD < 1.6 V                                                                                      |     | 0           |             |      |
| V <sub>OH</sub>                            |                                   | I <sub>OH</sub> = 2 TTL loads                                                                                              |     | 0.8 × IOVDD |             | V    |
| V <sub>OL</sub>                            |                                   | I <sub>OL</sub> = 2 TTL loads                                                                                              |     | 0.25        |             | V    |
| Capacitive load                            |                                   |                                                                                                                            |     | 10          |             | pF   |

- (1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
- (2) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

## 6.6 I<sup>2</sup>S/LJF/RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER           |            | IOVDD = 1.8 V |     | IOVDD = 3.3 V |     | UNIT |
|---------------------|------------|---------------|-----|---------------|-----|------|
|                     |            | MIN           | MAX | MIN           | MAX |      |
| t <sub>d</sub> (WS) | WCLK delay |               | 45  |               | 45  | ns   |
| t <sub>s</sub> (DI) | DIN setup  | 8             |     | 6             |     | ns   |
| t <sub>h</sub> (DI) | DIN hold   | 8             |     | 6             |     | ns   |
| t <sub>r</sub>      | Rise time  |               | 25  |               | 10  | ns   |
| t <sub>f</sub>      | Fall time  |               | 25  |               | 10  | ns   |

(1) All timing specifications are measured at characterization but not tested at final test.

## 6.7 I<sup>2</sup>S/LJF/RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER             |                  | IOVDD = 1.8 V |     | IOVDD = 3.3 V |     | UNIT |
|-----------------------|------------------|---------------|-----|---------------|-----|------|
|                       |                  | MIN           | MAX | MIN           | MAX |      |
| t <sub>H</sub> (BCLK) | BCLK high period | 35            |     | 35            |     | ns   |
| t <sub>L</sub> (BCLK) | BCLK low period  | 35            |     | 35            |     | ns   |
| t <sub>s</sub> (WS)   | WCLK setup       | 8             |     | 6             |     | ns   |
| t <sub>h</sub> (WS)   | WCLK hold        | 8             |     | 6             |     | ns   |
| t <sub>s</sub> (DI)   | DIN setup        | 8             |     | 6             |     | ns   |
| t <sub>h</sub> (DI)   | DIN hold         | 8             |     | 6             |     | ns   |
| t <sub>r</sub>        | Rise time        |               | 4   |               | 4   | ns   |
| t <sub>f</sub>        | Fall time        |               | 4   |               | 4   | ns   |

(1) All timing specifications are measured at characterization but not tested at final test.

## 6.8 DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER           |            | IOVDD = 1.8 V |     | IOVDD = 3.3 V |     | UNIT |
|---------------------|------------|---------------|-----|---------------|-----|------|
|                     |            | MIN           | MAX | MIN           | MAX |      |
| t <sub>d</sub> (WS) | WCLK delay |               | 45  |               | 45  | ns   |
| t <sub>s</sub> (DI) | DIN setup  | 8             |     | 6             |     | ns   |
| t <sub>h</sub> (DI) | DIN hold   | 8             |     | 6             |     | ns   |
| t <sub>r</sub>      | Rise time  |               | 25  |               | 10  | ns   |
| t <sub>f</sub>      | Fall time  |               | 25  |               | 10  | ns   |

(1) All timing specifications are measured at characterization but not tested at final test.

## 6.9 DSP Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER             |                  | IOVDD = 1.8V |     | IOVDD = 3.3 V |     | UNIT |
|-----------------------|------------------|--------------|-----|---------------|-----|------|
|                       |                  | MIN          | MAX | MIN           | MAX |      |
| t <sub>H</sub> (BCLK) | BCLK high period | 35           |     | 35            |     | ns   |
| t <sub>L</sub> (BCLK) | BCLK low period  | 35           |     | 35            |     | ns   |
| t <sub>s</sub> (WS)   | WCLK setup       | 8            |     | 8             |     | ns   |
| t <sub>h</sub> (WS)   | WCLK hold        | 8            |     | 8             |     | ns   |
| t <sub>s</sub> (DI)   | DIN setup        | 8            |     | 8             |     | ns   |
| t <sub>h</sub> (DI)   | DIN hold         | 8            |     | 8             |     | ns   |
| t <sub>r</sub>        | Rise time        |              | 4   |               | 4   | ns   |

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER                | IOVDD = 1.8V |     | IOVDD = 3.3 V |     | UNIT |
|--------------------------|--------------|-----|---------------|-----|------|
|                          | MIN          | MAX | MIN           | MAX |      |
| t <sub>f</sub> Fall time |              | 4   |               | 4   | ns   |

(1) All timing specifications are measured at characterization but not tested at final test.

## 6.10 I<sup>2</sup>C Interface Timing

All specifications at 25°C, DVDD = 1.8 V<sup>(1)</sup>

| PARAMETER                                                                                                        | STANDARD MODE |     |      | FAST MODE               |     |     | UNIT |
|------------------------------------------------------------------------------------------------------------------|---------------|-----|------|-------------------------|-----|-----|------|
|                                                                                                                  | MIN           | TYP | MAX  | MIN                     | TYP | MAX |      |
| f <sub>SCL</sub> SCL clock frequency                                                                             | 0             |     | 100  | 0                       |     | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4             |     |      | 0.8                     |     |     | μs   |
| t <sub>LOW</sub> LOW period of the SCL clock                                                                     | 4.7           |     |      | 1.3                     |     |     | μs   |
| t <sub>HIGH</sub> HIGH period of the SCL clock                                                                   | 4             |     |      | 0.6                     |     |     | μs   |
| t <sub>SU,STA</sub> Setup time for a repeated START condition                                                    | 4.7           |     |      | 0.8                     |     |     | μs   |
| t <sub>HD,DAT</sub> Data hold time for I <sup>2</sup> C bus devices                                              | 0             |     | 3.45 | 0                       |     | 0.9 | μs   |
| t <sub>SU,DAT</sub> Data setup time                                                                              | 250           |     |      | 100                     |     |     | ns   |
| t <sub>r</sub> SDA and SCL rise time                                                                             |               |     | 1000 | 20 + 0.1 C <sub>b</sub> |     | 300 | ns   |
| t <sub>f</sub> SDA and SCL fall time                                                                             |               |     | 300  | 20 + 0.1 C <sub>b</sub> |     | 300 | ns   |
| t <sub>SU,STO</sub> Set-up time for STOP condition                                                               | 4             |     |      | 0.8                     |     |     | μs   |
| t <sub>BUF</sub> Bus free time between a STOP and START condition                                                | 4.7           |     |      | 1.3                     |     |     | μs   |
| C <sub>b</sub> Capacitive load for each bus line                                                                 |               |     | 400  |                         |     | 400 | pF   |

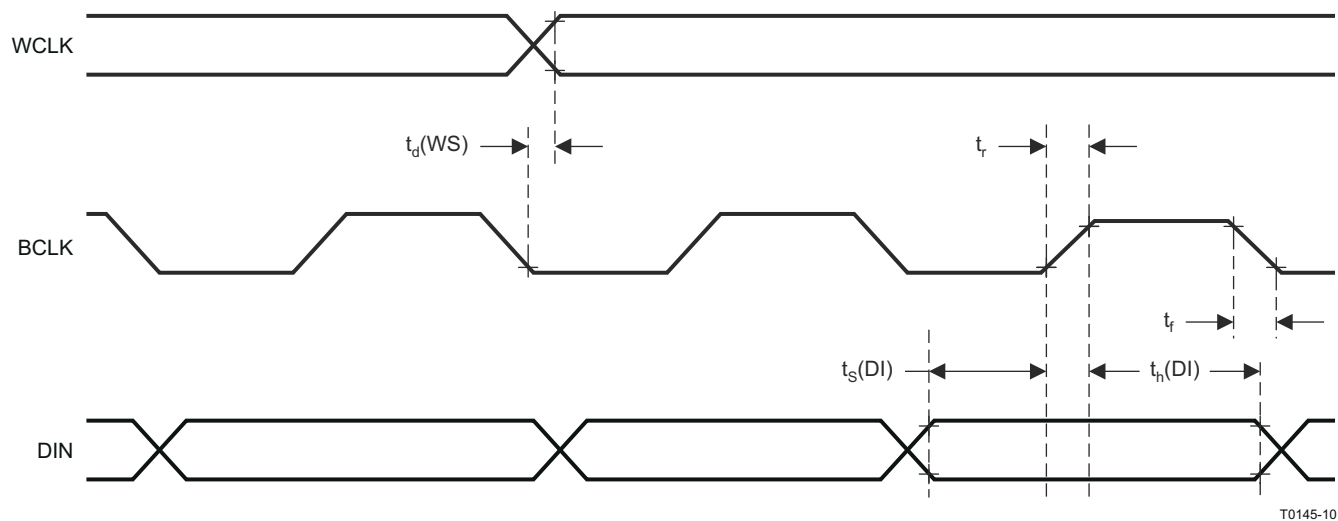
(1) All timing specifications are measured at characterization but not tested at final test.

## 6.11 SPI Interface Timing

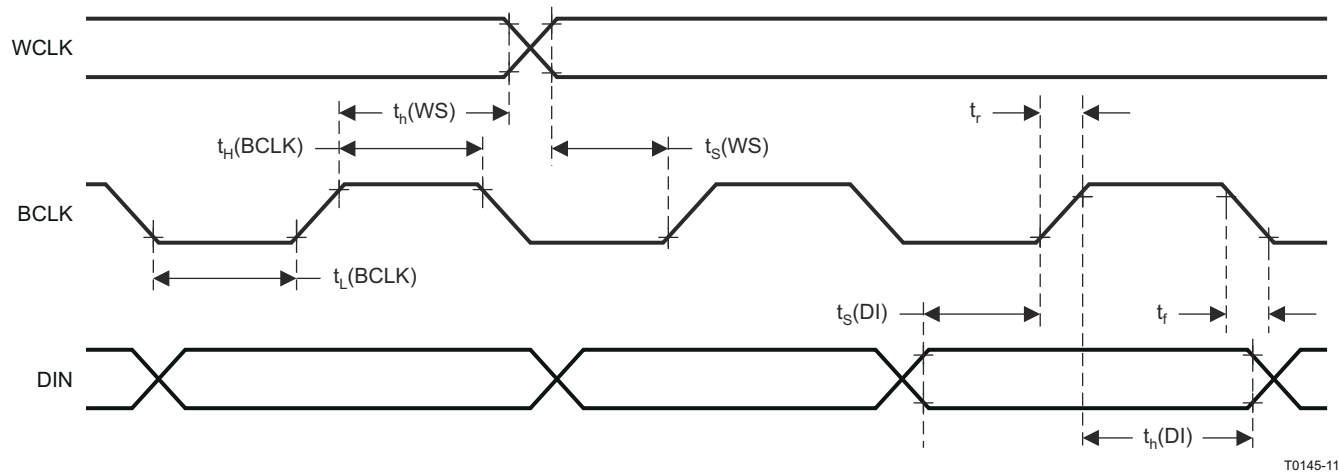
At 25°C, DVDD = 1.8V

| PARAMETER                                   | TEST CONDITION | IOVDD=1.8V |     |     | IOVDD=3.3V |     |     | UNIT |
|---------------------------------------------|----------------|------------|-----|-----|------------|-----|-----|------|
|                                             |                | MIN        | TYP | MAX | MIN        | TYP | MAX |      |
| t <sub>sck</sub> SCLK period <sup>(1)</sup> |                | 100        |     |     | 50         |     |     | ns   |
| t <sub>sckh</sub> SCLK pulse width High     |                | 50         |     |     | 25         |     |     | ns   |
| t <sub>sckl</sub> SCLK pulse width Low      |                | 50         |     |     | 25         |     |     | ns   |
| t <sub>lead</sub> Enable lead time          |                | 30         |     |     | 20         |     |     | ns   |
| t <sub>lag</sub> Enable lag time            |                | 30         |     |     | 20         |     |     | ns   |
| t <sub>d</sub> Sequential transfer delay    |                | 40         |     |     | 20         |     |     | ns   |
| t <sub>a</sub> Slave DOUT access time       |                |            |     | 40  |            |     | 40  | ns   |
| t <sub>dis</sub> Slave DOUT disable time    |                |            |     | 40  |            |     | 40  | ns   |
| t <sub>su</sub> DIN data setup time         |                | 15         |     |     | 15         |     |     | ns   |
| t <sub>hi</sub> DIN data hold time          |                | 15         |     |     | 10         |     |     | ns   |
| t <sub>v,DOUT</sub> DOUT data valid time    |                |            |     | 25  |            |     | 18  | ns   |
| t <sub>r</sub> SCLK rise time               |                |            |     | 4   |            |     | 4   | ns   |
| t <sub>f</sub> SCLK fall time               |                |            |     | 4   |            |     | 4   | ns   |

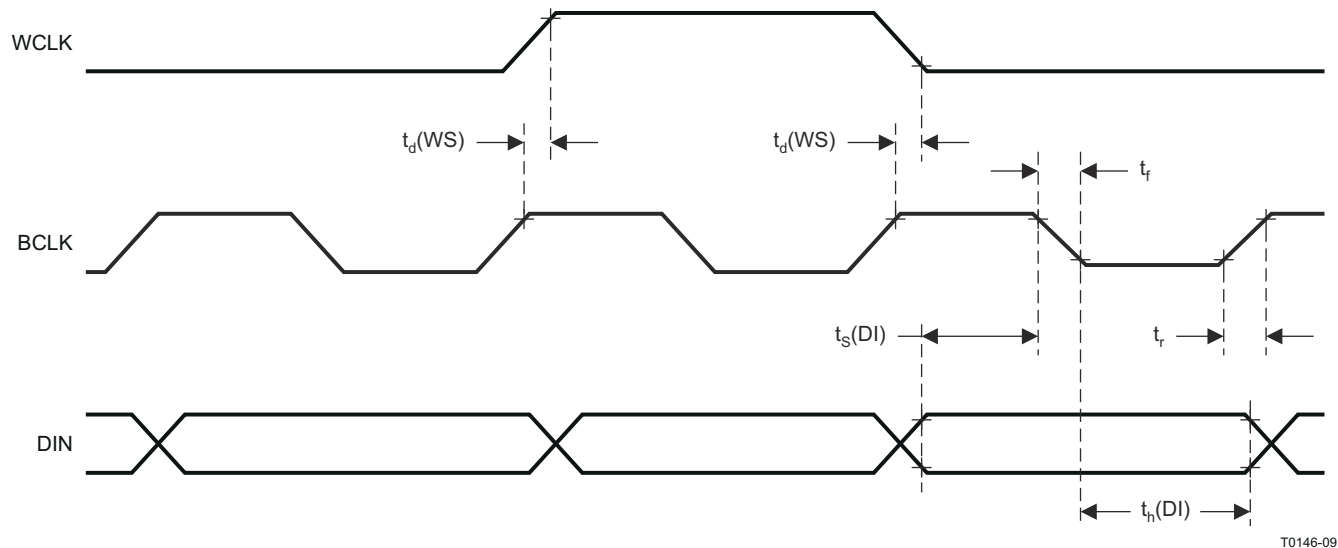
(1) These parameters are based on characterization and are not tested in production.



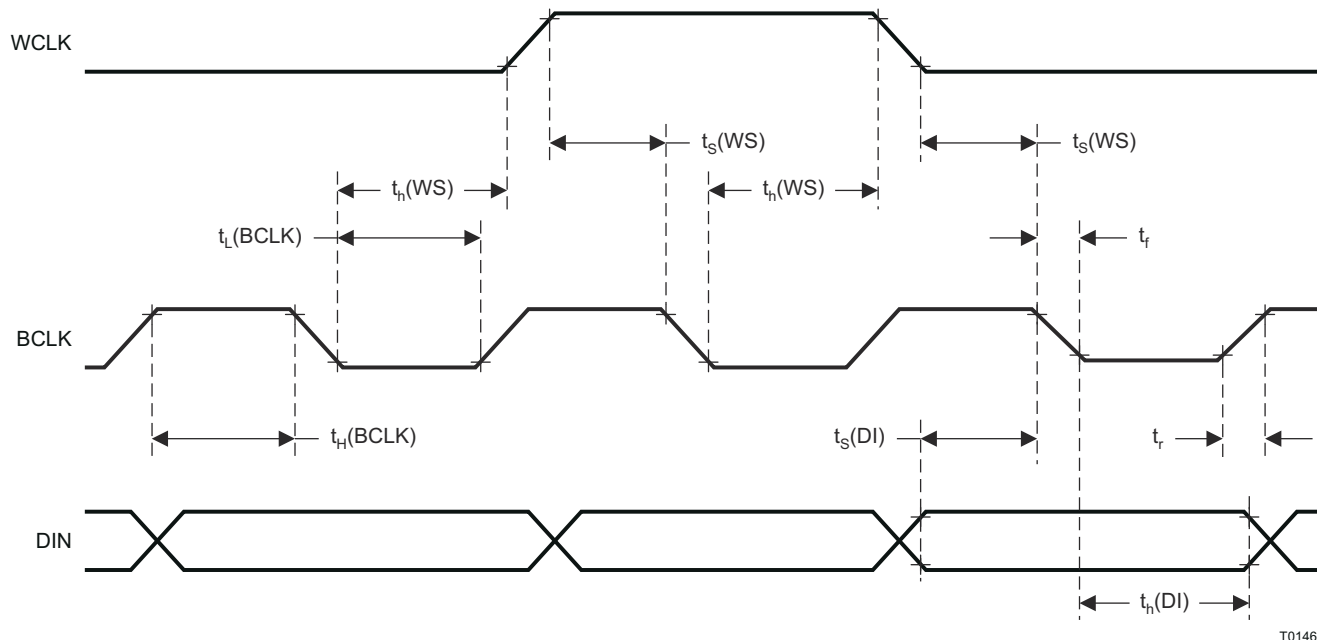
**图 6-1. I<sup>2</sup>S/LJF/RJF Timing in Master Mode**



**图 6-2. I<sup>2</sup>S/LJF/RJF Timing in Slave Mode**

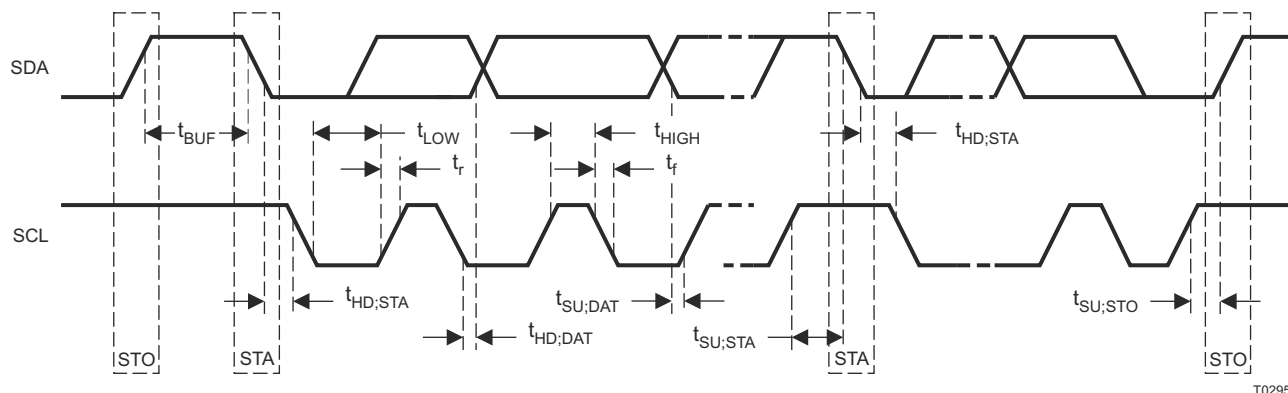


**图 6-3. DSP Timing in Master Mode**



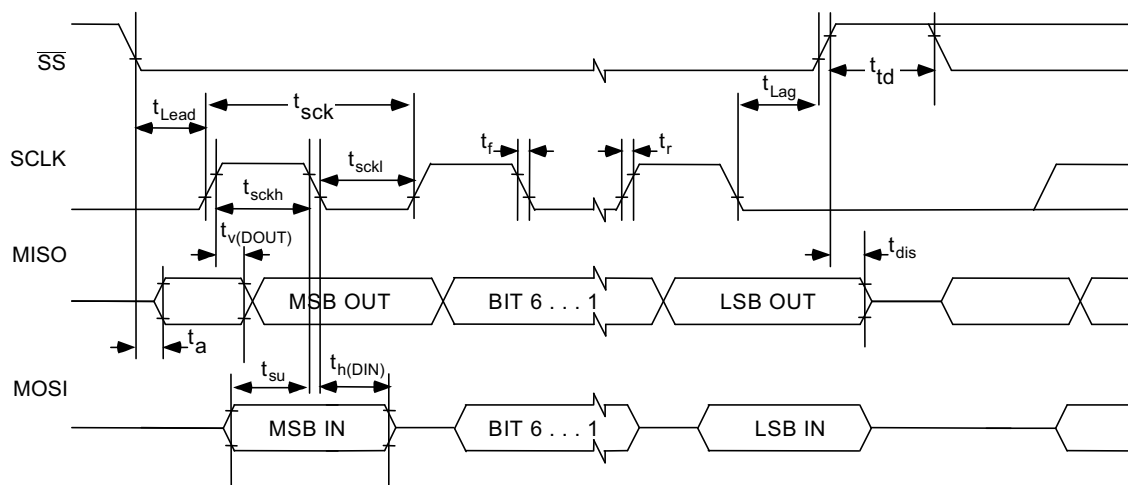
T0146-10

**6-4. DSP Timing in Slave Mode**



T0295-02

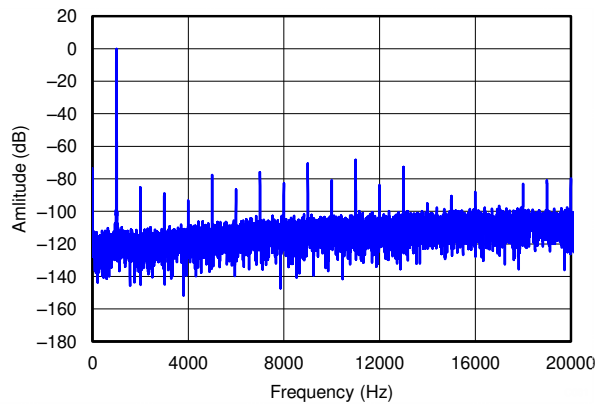
**6-5. I<sup>2</sup>C Interface Timing**



**6-6. SPI Interface Timing Diagram**

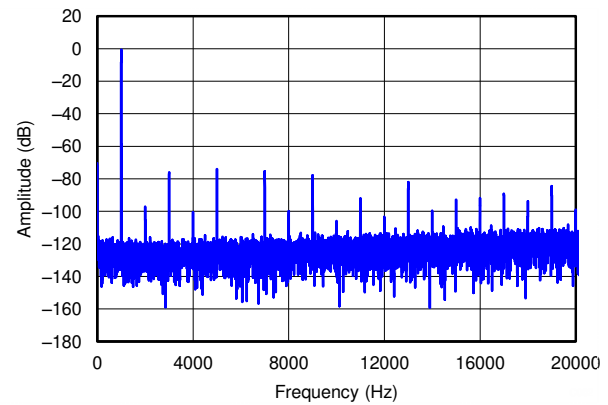
## 6.12 Typical Characteristics

### 6.12.1 Class D Speaker Driver Performance



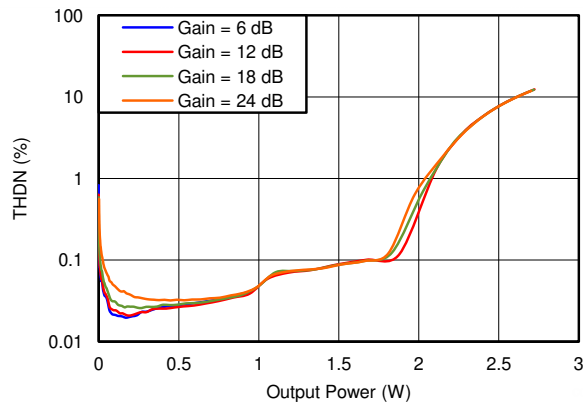
(4-Ω Load)

**FIG 6-7. DAC To Speaker Amplitude at 0 dBFS vs Frequency**



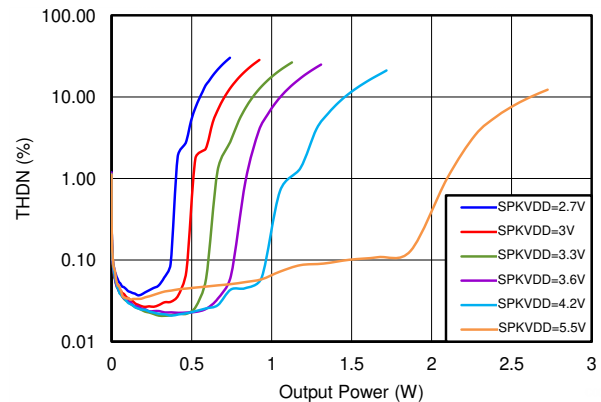
(4-Ω Load)

**FIG 6-8. AINL To Speaker FFT Amplitude at 0 dBFS vs Frequency**



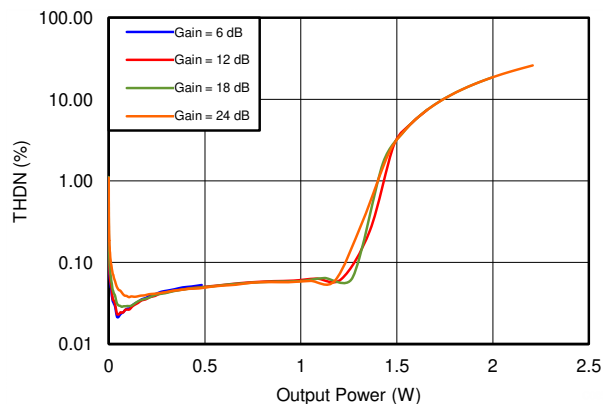
(SPKVDD = 5.5 V)

**FIG 6-9. Total Harmonic Distortion + Noise vs 4-Ω Speaker Power**



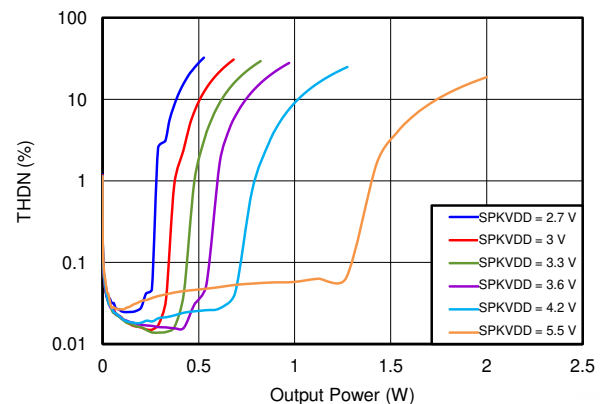
(Gain = 18 dB)

**FIG 6-10. Total Harmonic Distortion + Noise + NOISE vs 4-Ω Speaker Power**



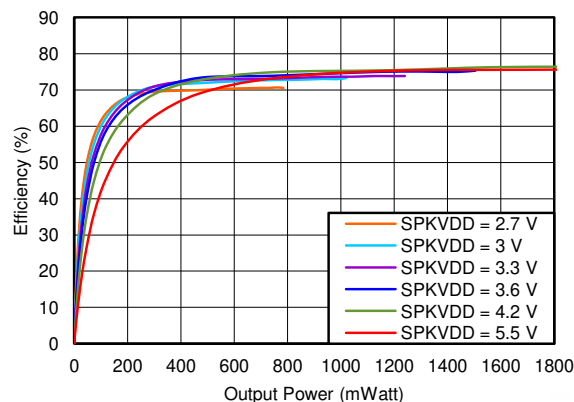
(SPKVDD = 5.5 V)

**FIG 6-11. Total Harmonic Distortion + Noise + NOISE vs 8-Ω Speaker Power**



(Gain = 18 dB)

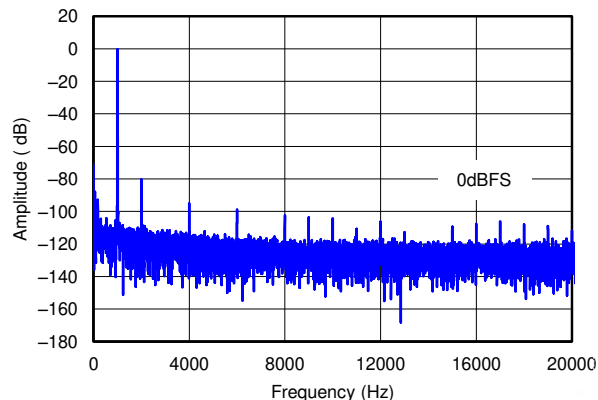
**FIG 6-12. Total Harmonic Distortion + Noise + NOISE vs 8-Ω Speaker Power**



(Gain = 18 dB, Load = 4  $\Omega$ )

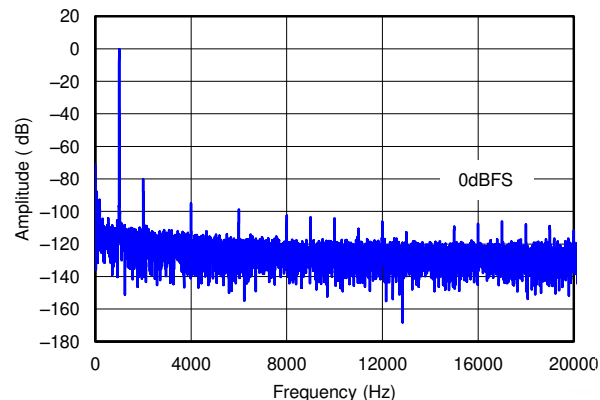
**6-13. Total Power Consumption vs Output Power Consumption**

## 6.12.2 HP Driver Performance



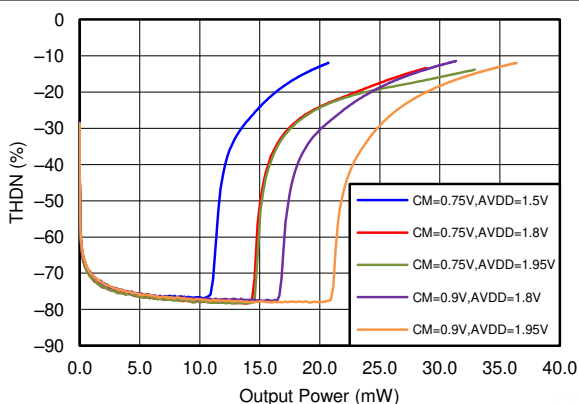
(16- $\Omega$  Load)

**6-14. DAC TO HP FFT Amplitude at 0 dBFS vs Frequency**



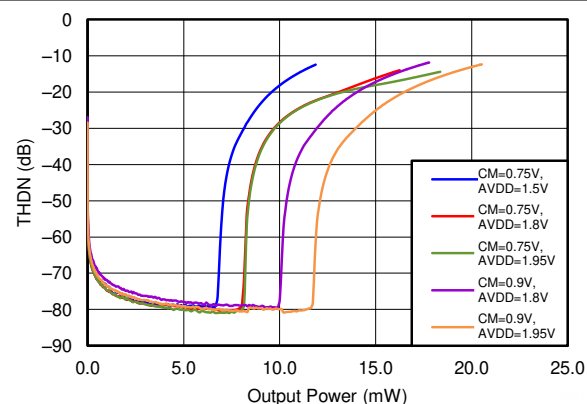
(16- $\Omega$  Load)

**6-15. AINL TO HP FFT Amplitude at 0 dBFS vs Frequency**



(Gain = 9 dB)

**6-16. Total Harmonic Distortion + Noise vs HP Power**



(Gain = 32 dB)

**6-17. Total Harmonic Distortion + Noise vs HP Power**

## 7 Parameter Measurement Information

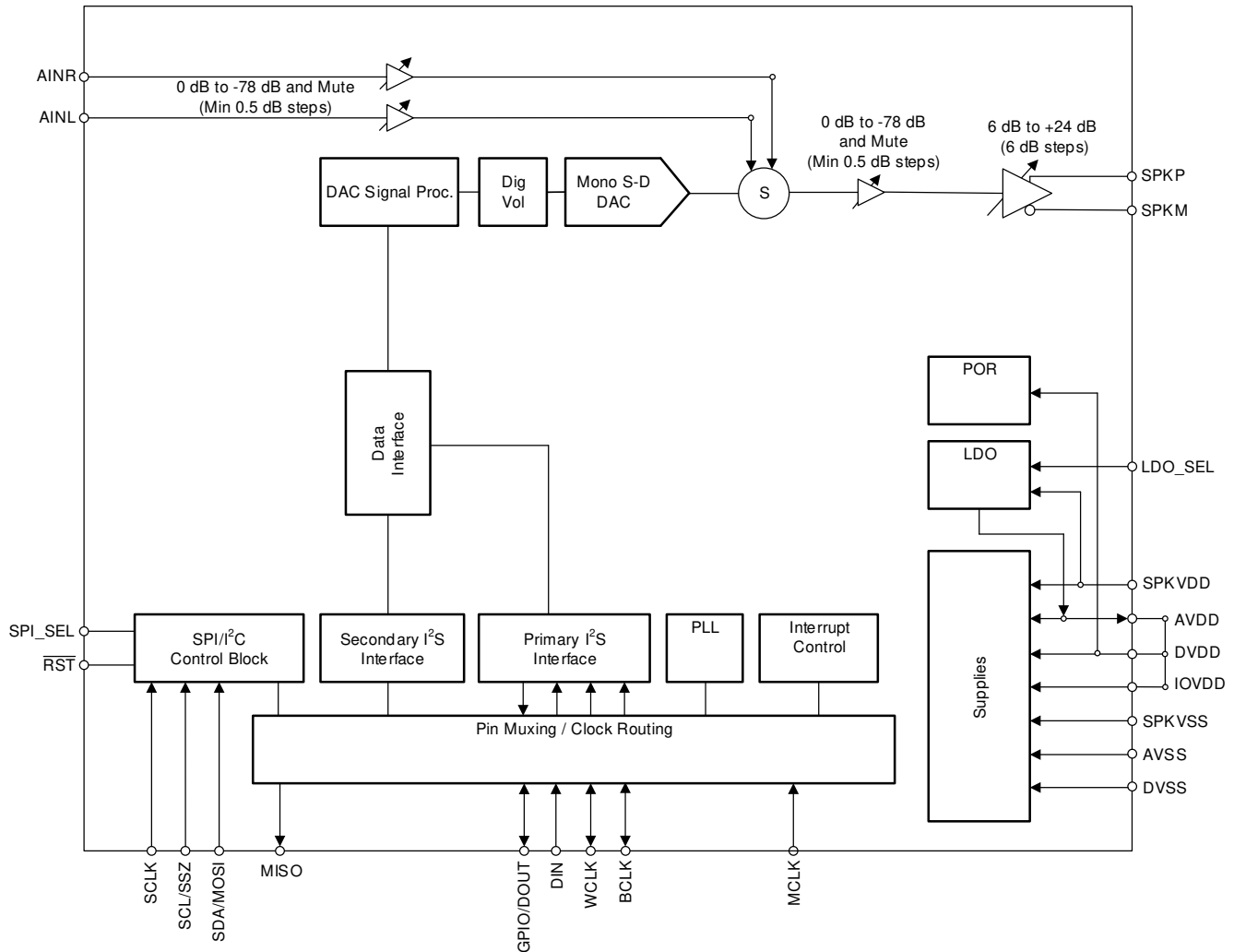
All parameters are measured according to the conditions described in the [セクション 6](#) section.

## 8 Detailed Description

### 8.1 Overview

TAS2505-Q1 is a low power analog and digital input class-D speaker amplifier. It supports 24-bit digital I2S data for mono playback. This device is able to drive a speaker up to 4  $\Omega$  and programmable digital-signal processing block. The programmable digital-signal processing block can support Bass boost, treble or EQ functions. The volume level can be controlled by register control. The device can be controlled through I<sup>2</sup>C or SPI bus. TAS2505-Q1 also includes an on-board LDO that runs off the speaker power supply to handle all internal device analog and digital power needs. The device also includes two analog inputs for mixing in speaker path.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Audio Analog I/O

The TAS2505-Q1 features a mono audio DAC. The TAS2505 can drive a speaker up to 4- $\Omega$  impedance.

#### 8.3.2 Audio DAC and Audio Analog Outputs

The mono audio DAC consists of a digital audio processing block, a digital interpolation filter, a digital delta-sigma modulator, and an analog reconstruction filter. The high oversampling ratio (normally DOSR is between 32 and 128) exhibits good dynamic range by ensuring that the quantization noise generated within the delta-sigma modulator stays outside of the audio frequency band. Audio analog outputs include mono class-D speaker

outputs. Because the TAS2505-Q1 contains a mono DAC, it inputs the mono data from the left channel, the right channel, or a mix of the left and right channels as  $[(L + R) \div 2]$ , selected by page 0, register 63, bits D5–D4.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

### 8.3.3 DAC

The TAS2505-Q1 mono audio DAC supports data rates from 8 kHz to 192 kHz. The audio channel of the mono DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multibit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and observed in the signal images strongly suppressed within the audio band to beyond 20 kHz. To handle multiple input rates and optimize power dissipation and performance, the TAS2505-Q1 allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring page 0, register 13 and page 0 / register 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TAS2505-Q1 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the delta-sigma modulator. The interpolation filter can be chosen from three different types, depending on required frequency response, group delay, and sampling rate.

The DAC path of the TAS2505-Q1 features many options for signal conditioning and signal routing:

- Digital volume control with a range of –63.5 to +24 dB
- Mute function

In addition to the standard set of DAC features the TAS2505-Q1 also offers the following special features:

- Digital auto mute
- Adaptive filter mode

### 8.3.4 POR

TAS2505-Q1 has a POR (Power-On-Reset) function. This function insures that all registers are automatically set to defaults when a proper power up sequence is executed.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

### 8.3.5 CLOCK Generation and PLL

The TAS2505-Q1 supports a wide range of options for generating clocks for the DAC sections as well as interface and other control blocks. The clocks for the DAC require a source reference clock. This clock can be provided on a variety of device pins, such as the MCLK, BCLK, or GPIO pins. The source reference clock for the codec can be chosen by programming the CODEC\_CLKIN value on page 0, register 4, bits D1–D0. The CODEC\_CLKIN can then be routed through highly-flexible clock dividers shown in Figure 2 through 7 in the [TAS2505 Application Reference Guide](#) to generate the various clocks required for the DAC and the Digital Effects section also found in the [TAS2505 Application Reference Guide](#) (SLAU472). In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO, the TAS2505-Q1 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC\_CLKIN, the TAS2505-Q1 provides several programmable clock dividers to help achieve a variety of sampling rates for the DAC and clocks for the Digital Effects sections.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

### 8.3.6 Speaker Driver

The TAS2505-Q1 has an integrated class-D mono speaker driver (SPKP/SPKM) capable of driving an 8-Ω or 4-Ω differential load. The speaker driver can be powered directly from the battery supply (2.7 V to 5.5 V) on the SPKVDD pins; however, the voltage (including spike voltage) must be limited below the absolute maximum voltage of 6 V. The speaker driver is capable of supplying 800 mW per channel with a 3.6-V power supply. Through the use of digital mixing, the device can connect one or both digital audio playback data channels to either speaker driver; this also allows digital channel swapping if needed. The class-D speaker driver can be

powered on by writing to page 1, register 45, bit D1. The class-D output-driver gain can be controlled by writing to page 1, register 48, bits D6–D4, and it can be muted by writing to page 1, register 48, bit D6 - D4 = 000.

### 8.3.7 Automotive Diagnostics

The TAS2505-Q1 has **SHORT-CIRCUIT PROTECTION /OVER CURRENT PROTECTION (OCP)** feature for the speaker drivers that is always enabled to provide protection. This protects outputs against **short to ground**, **short to supply** and **short between output terminals**. The output stage shuts down on the over current condition. (Current limiting is not an available option for the higher-current speaker driver output stage.) In case of a short circuit, the output is disabled. **A status flag for OC condition occurrence is provided as a read-only bit on page 1, register 45, bit D1.** The D1 bit is cleared when any of the above short circuit condition happens. If shutdown occurs due to an over current condition, then the device requires a reset to re-enable the output stage. Resetting can be done in two ways. First, the device master reset can be used, which requires either toggling the RST pin or using the software reset. If master reset is used, it resets all of the registers. Second, a dedicated speaker power-stage reset can be used that keeps all of the other device settings. The speaker power-stage reset is done by setting page 1, register 45, bit D1 for SPKP and SPKM. If the fault condition has been removed, then the device returns to normal operation. If the fault is still present, then another shutdown occurs. Repeated resetting (more than three times) is not recommended, as this could lead to overheating. To minimize battery current leakage, the SPKVDD voltage level should not be less than the AVDD voltage level.

The TAS2505 has a **OVER TEMPERATURE PROTECTION (OTP)** feature for the speaker driver which is always enabled to provide protection. If the device is overheated, then the output stops switching. When the device cools down, the output resumes switching. **An over temperature status flag is provided as a read-only bit on page 0, register 45, bit D7.** The OTP feature is for self-protection of the device. If die temperature can be controlled at the system/board level, then over temperature does not occur.

## 8.4 Device Functional Modes

### 8.4.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are  $\overline{\text{RST}}$  LDO\_SEL and the SPI\_SEL pin, which are HW control pins. Depending on the state of SPI\_SEL, the two control-bus pins SCL/SSZ and SDA/MOSI are configured for either I<sup>2</sup>C or SPI protocol.

Other digital IO pins can be configured for various functions through register control. An overview of available functionality is given in [セクション 8.4.3](#).

### 8.4.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

### 8.4.3 Multifunction Pins

[表 8-1](#) shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

**表 8-1. Multifunction Pin Assignments**

|          |                              | 1                                  | 2                   | 3    | 4   | 5          | 6                | 7    |
|----------|------------------------------|------------------------------------|---------------------|------|-----|------------|------------------|------|
|          | PIN FUNCTION                 | MCLK                               | BCLK                | WCLK | DIN | GPIO /DOUT | SCLK             | MISO |
| <b>A</b> | PLL Input                    | S <sup>(2)</sup>                   | S <sup>(3)</sup>    |      | E   |            | S <sup>(4)</sup> |      |
| <b>B</b> | Codec Clock Input            | S <sup>(2)</sup> ,D <sup>(5)</sup> | S <sup>(3)</sup>    |      |     |            | S <sup>(4)</sup> |      |
| <b>C</b> | I <sup>2</sup> S BCLK input  |                                    | S <sup>(3)</sup> ,D |      |     |            |                  |      |
| <b>D</b> | I <sup>2</sup> S BCLK output |                                    | E <sup>(1)</sup>    |      |     |            |                  |      |

**表 8-1. Multifunction Pin Assignments (continued)**

|   |                                       | 1    | 2    | 3    | 4    | 5          | 6    | 7    |
|---|---------------------------------------|------|------|------|------|------------|------|------|
|   | PIN FUNCTION                          | MCLK | BCLK | WCLK | DIN  | GPIO /DOUT | SCLK | MISO |
| E | I <sup>2</sup> S WCLK input           |      |      | E, D |      |            |      |      |
| F | I <sup>2</sup> S WCLK output          |      |      | E    |      |            |      |      |
| G | I <sup>2</sup> S DIN                  |      |      |      | E, D |            |      |      |
| I | General-Purpose Output I              |      |      |      |      | E          |      |      |
| I | General-Purpose Output II             |      |      |      |      |            |      | E    |
| J | General-Purpose Input I               |      |      |      | E    |            |      |      |
| J | General-Purpose Input II              |      |      |      |      | E          |      |      |
| J | General-Purpose Input III             |      |      |      |      |            | E    |      |
| K | INT1 output                           |      |      |      |      | E          |      | E    |
| L | INT2 output                           |      |      |      |      | E          |      | E    |
| M | Secondary I <sup>2</sup> S BCLK input |      |      |      |      | E          | E    |      |
| N | Secondary I <sup>2</sup> S WCLK input |      |      |      |      | E          | E    |      |
| O | Secondary I <sup>2</sup> S DIN        |      |      |      |      | E          | E    |      |
| P | Secondary I <sup>2</sup> S BCLK OUT   |      |      |      |      | E          |      | E    |
| Q | Secondary I <sup>2</sup> S WCLK OUT   |      |      |      |      | E          |      | E    |
| R | Secondary I <sup>2</sup> S DOUT       |      |      |      |      |            |      | E    |
| S | Aux Clock Output                      |      |      |      |      | E          |      | E    |

- (1) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/DOUT has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)
- (2) S<sup>(1)</sup>: The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.
- (3) S<sup>(2)</sup>: The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.
- (4) S<sup>(3)</sup>: The GPIO/DOUT pin can drive the PLL and Codec Clock inputs **simultaneously**.
- (5) D: Default Function

#### 8.4.4 Analog Signals

The TAS2505-Q1 analog signals consist of:

- Analog inputs AINR and AINL, which can be used to pass-through or mix analog signals to output stages
- Analog outputs class-D speaker driver providing output capability for the DAC, AINR, AINL, or a mix of the three

##### 8.4.4.1 Analog Inputs AINL and AINR

AINL (pin 3 or C2) and AINR (pin 4 or B2) are inputs to Mixer P and Mixer M along with the DAC output. Also AINL and AINR can be configured inputs to HP driver. Page1 / register 12 provides control signals for determining the signals routed through Mixer P, Mixer M and HP driver. Input of Mixer P can be attenuated by Page1 / register 24, input of Mixer M can be attenuated by Page1 / register 25 and input of HP driver can be attenuated by Page1 / register 22. Also AINL and AINR can be configured to a monaural differential input with use Mixer P and Mixer M by Page1 / register 12 setting.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

#### 8.4.5 DAC Processing Blocks — Overview

The TAS2505-Q1 implements signal-processing capabilities and interpolation filtering through processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choices among these processing blocks allows the system designer to balance power conservation and signal-processing flexibility. 表 8-2 gives an overview of all available processing blocks of the DAC channel and their properties. The resource-class column gives an approximate indication of power consumption for the digital

(DVDD) supply; however, based on the out-of-band noise spectrum, the analog power consumption of the drivers (AVDD) may differ.

The signal-processing blocks available are:

- First-order IIR
- Scalable number of biquad filters

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal-processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

**表 8-2. Overview – DAC Predefined Processing Blocks**

| PROCESSING BLOCK NO. | INTERPOLATION FILTER | CHANNEL | FIRST-ORDER IIR AVAILABLE | NUMBER OF BIQUADS | RESOURCE CLASS |
|----------------------|----------------------|---------|---------------------------|-------------------|----------------|
| PRB_P1               | A                    | Mono    | Yes                       | 6                 | 6              |
| PRB_P2               | A                    | Mono    | No                        | 3                 | 4              |
| PRB_P3               | B                    | Mono    | Yes                       | 6                 | 4              |

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

#### 8.4.6 Digital Mixing and Routing

The TAS2505-Q1 has four digital mixing blocks. Each mixer can provide either mixing or multiplexing of the digital audio data. The first mixer or multiplexer can be used to select input data for the mono DAC from left channel, right channel, or (left channel + right channel) / 2 mixing. This digital routing can be configured by writing to page 0, register 63, bits D5–D4.

#### 8.4.7 Analog Audio Routing

The TAS2505-Q1 has the capability to route the DAC output to the speaker output. If desirable, both output drivers can be operated at the same time while playing at different volume levels. The TAS2505-Q1 provides various digital routing capabilities, allowing digital mixing or even channel swapping in the digital domain. All analog outputs other than the selected ones can be powered down for optimal power consumption.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

#### 8.4.8 5V LDO

The TAS2505-Q1 has a built-in LDO which can generate the analog supply (AVDD) also the digital supply (DVDD) from input voltage range of 2.7 V to 5.5 V with high PSRR. If combined power supply current is 50 mA or less, then this LDO can deliver power to both analog and digital power supplies. If the only speaker power supply is present and LDO Select pin is enabled, the LDO can power up without requiring other supplies. This LDO requires a minimum dropout voltage of 300 mV and can support load currents up to 50 mA. For stability reasons the LDO requires a minimum decoupling capacitor of 1  $\mu$ F ( $\pm 50\%$ ) on the analog supply (AVDD) pin and the digital supply (DVDD) pin. If use this LDO output voltage for the digital supply (DVDD) pin, the analog supply (AVDD) pin connected to the digital supply (DVDD) externally is required.

The LDO is by default powered down for low sleep mode currents and can be enabled driving the LDO\_SELECT pin to SPKVDD (speaker power supply). When the LDO is disabled the AVDD pin is tri-stated and the device AVDD needs to be powered using external supply. In that case the DVDD pin is also tri-stated and the device DVDD needs to be powered using external supply. The output voltage of this LDO can be adjusted to a few different values as given in the [表 8-3](#).

**表 8-3. AVDD LDO Settings**

| Page-1, Register 2, D(5:4) | LDO Output |
|----------------------------|------------|
| 00                         | 1.8 V      |
| 01                         | 1.6 V      |
| 10                         | 1.7 V      |

**表 8-3. AVDD LDO Settings (continued)**

| Page-1, Register 2, D(5:4) | LDO Output |
|----------------------------|------------|
| 00                         | 1.5 V      |

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

## 8.4.9 Digital Audio and Control Interface

### 8.4.9.1 Digital Audio Interface

Audio data is transferred between the host processor and the TAS2505-Q1 via the digital audio data serial interface, or audio bus. The audio bus on this device is flexible, including left- or right-justified data options, support for I<sup>2</sup>S or PCM protocols, programmable data-length options, a TDM mode for multichannel operation, flexible master or slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TAS2505-Q1 can be configured for left- or right-justified, I<sup>2</sup>S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring page 0, register 27, bits D5–D4. In addition, the word clock and bit clock can be independently configured in either master or slave mode for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected DAC sampling frequencies.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

### 8.4.9.2 Control Interface

The TAS2505-Q1 control interface supports SPI or I<sup>2</sup>C communication protocols, with the protocol selectable using the SPI\_SEL pin. For SPI, SPI\_SEL should be tied high; for I<sup>2</sup>C, SPI\_SEL should be tied low. TI does not recommend changing the state of SPI\_SEL during device operation.

#### 8.4.9.2.1 I<sup>2</sup>C Control Mode

The TAS2505-Q1 supports the I<sup>2</sup>C control protocol, and will respond to the I<sup>2</sup>C address of 0011 000. I<sup>2</sup>C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I<sup>2</sup>C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

#### 8.4.9.2.2 SPI Digital Interface

In the SPI control mode, the TAS2505-Q1 uses the pins SCL/SSZ=SSZ, SCLK=SCLK, MISO=MISO, SDA/MOSI=MOSI as a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TAS2505-Q1) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

### 8.4.9.3 Device Special Functions

- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

## 8.5 Register Map

**表 8-4. Summary of Register Map**

| Decimal  |          | Hex      |             | DESCRIPTION                                                   |
|----------|----------|----------|-------------|---------------------------------------------------------------|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO.    |                                                               |
| 0        | 0        | 0x00     | 0x00        | Page Select Register                                          |
| 0        | 1        | 0x00     | 0x01        | Software Reset Register                                       |
| 0        | 2 - 3    | 0x00     | 0x02 - 0x03 | Reserved Registers                                            |
| 0        | 4        | 0x00     | 0x04        | Clock Setting Register 1, Multiplexers                        |
| 0        | 5        | 0x00     | 0x05        | Clock Setting Register 2, PLL P and R Values                  |
| 0        | 6        | 0x00     | 0x06        | Clock Setting Register 3, PLL J Values                        |
| 0        | 7        | 0x00     | 0x07        | Clock Setting Register 4, PLL D Values (MSB)                  |
| 0        | 8        | 0x00     | 0x08        | Clock Setting Register 5, PLL D Values (LSB)                  |
| 0        | 9 - 10   | 0x00     | 0x09 - 0x0A | Reserved Registers                                            |
| 0        | 11       | 0x00     | 0x0B        | Clock Setting Register 6, NDAC Values                         |
| 0        | 12       | 0x00     | 0x0C        | Clock Setting Register 7, MDAC Values                         |
| 0        | 13       | 0x00     | 0x0D        | DAC OSR Setting Register 1, MSB Value                         |
| 0        | 14       | 0x00     | 0x0E        | DAC OSR Setting Register 2, LSB Value                         |
| 0        | 15 - 24  | 0x00     | 0x0F - 0x18 | Reserved Registers                                            |
| 0        | 25       | 0x00     | 0x19        | Clock Setting Register 10, Multiplexers                       |
| 0        | 26       | 0x00     | 0x1A        | Clock Setting Register 11, CLKOUT M divider value             |
| 0        | 27       | 0x00     | 0x1B        | Audio Interface Setting Register 1                            |
| 0        | 28       | 0x00     | 0x1C        | Audio Interface Setting Register 2, Data offset setting       |
| 0        | 29       | 0x00     | 0x1D        | Audio Interface Setting Register 3                            |
| 0        | 30       | 0x00     | 0x1E        | Clock Setting Register 12, BCLK N Divider                     |
| 0        | 31       | 0x00     | 0x1F        | Audio Interface Setting Register 4, Secondary Audio Interface |
| 0        | 32       | 0x00     | 0x20        | Audio Interface Setting Register 5                            |
| 0        | 33       | 0x00     | 0x21        | Audio Interface Setting Register 6                            |
| 0        | 34       | 0x00     | 0x22        | Reserved Register                                             |
| 0        | 35 - 36  | 0x00     | 0x23 - 0x24 | Reserved Registers                                            |
| 0        | 37       | 0x00     | 0x25        | DAC Flag Register 1                                           |
| 0        | 38       | 0x00     | 0x26        | DAC Flag Register 2                                           |
| 0        | 39-41    | 0x00     | 0x27-0x29   | Reserved Registers                                            |
| 0        | 42       | 0x00     | 0x2A        | Sticky Flag Register 1                                        |
| 0        | 43       | 0x00     | 0x2B        | Interrupt Flag Register 1                                     |
| 0        | 44       | 0x00     | 0x2C        | Sticky Flag Register 2                                        |
| 0        | 45       | 0x00     | 0x2D        | Reserved Register                                             |
| 0        | 46       | 0x00     | 0x2E        | Interrupt Flag Register 2                                     |
| 0        | 47       | 0x00     | 0x2F        | Reserved Register                                             |
| 0        | 48       | 0x00     | 0x30        | INT1 Interrupt Control Register                               |
| 0        | 49       | 0x00     | 0x31        | INT2 Interrupt Control Register                               |
| 0        | 50-51    | 0x00     | 0x32-0x33   | Reserved Registers                                            |
| 0        | 52       | 0x00     | 0x34        | GPIO/DOUT Control Register                                    |
| 0        | 53       | 0x00     | 0x35        | DOUT Function Control Register                                |
| 0        | 54       | 0x00     | 0x36        | DIN Function Control Register                                 |
| 0        | 55       | 0x00     | 0x37        | MISO Function Control Register                                |
| 0        | 56       | 0x00     | 0x38        | SCLK/DMDIN2 Function Control Register                         |

表 8-4. Summary of Register Map (continued)

| Decimal  |           | Hex         |             | DESCRIPTION                                                         |
|----------|-----------|-------------|-------------|---------------------------------------------------------------------|
| PAGE NO. | REG. NO.  | PAGE NO.    | REG. NO.    |                                                                     |
| 0        | 57-59     | 0x00        | 0x39-0x3B   | Reserved Registers                                                  |
| 0        | 60        | 0x00        | 0x3C        | DAC Instruction Set                                                 |
| 0        | 61 - 62   | 0x00        | 0x3D -0x3E  | Reserved Registers                                                  |
| 0        | 63        | 0x00        | 0x3F        | DAC Channel Setup Register 1                                        |
| 0        | 64        | 0x00        | 0x40        | DAC Channel Setup Register 2                                        |
| 0        | 65        | 0x00        | 0x41        | DAC Channel Digital Volume Control Register                         |
| 0        | 66 - 80   | 0x00        | 0x42 - 0x50 | Reserved Registers                                                  |
| 0        | 81        | 0x00        | 0x51        | Dig_Mic Control Register                                            |
| 0        | 82 - 127  | 0x00        | 0x52 - 0x7F | Reserved Registers                                                  |
| 1        | 0         | 0x01        | 0x00        | Page Select Register                                                |
| 1        | 1         | 0x01        | 0x01        | REF, POR and LDO BGAP Control Register                              |
| 1        | 2         | 0x01        | 0x02        | LDO Control Register                                                |
| 1        | 3         | 0x01        | 0x03        | Playback Configuration Register 1                                   |
| 1        | 4 - 7     | 0x01        | 0x04 - 0x07 | Reserved Registers                                                  |
| 1        | 8         | 0x01        | 0x08        | DAC PGA Control Register                                            |
| 1        | 9         | 0x01        | 0x09        | Output Drivers, AINL, AINR, Control Register                        |
| 1        | 10        | 0x01        | 0x0A        | Common Mode Control Register                                        |
| 1        | 11        | 0x01        | 0x0B        | HP Over Current Protection Configuration Register                   |
| 1        | 12        | 0x01        | 0x0C        | HP Routing Selection Register                                       |
| 1        | 13 - 15   | 0x01        | 0x0D - 0x0F | Reserved Registers                                                  |
| 1        | 16        | 0x01        | 0x10        | Reserved Registers                                                  |
| 1        | 17 - 19   | 0x01        | 0x11 - 0x13 | Reserved Registers                                                  |
| 1        | 20        | 0x01        | 0x14        | Reserved Registers                                                  |
| 1        | 21        | 0x01        | 0x15        | Reserved Register                                                   |
| 1        | 22        | 0x01        | 0x16        | Reserved Registers                                                  |
| 1        | 23        | 0x01        | 0x17        | Reserved Register                                                   |
| 1        | 24        | 0x01        | 0x18        | AINL Volume Control Register                                        |
| 1        | 25        | 0x01        | 0x19        | AINR Volume Control Register                                        |
| 1        | 26 - 44   | 0x01        | 0x1A - 0x2C | Reserved Registers                                                  |
| 1        | 45        | 0x01        | 0x2D        | Speaker Amplifier Control 1                                         |
| 1        | 46        | 0x01        | 0x2E        | Speaker Volume Control Register                                     |
| 1        | 47        | 0x01        | 0x2F        | Reserved Register                                                   |
| 1        | 48        | 0x01        | 0x30        | Speaker Amplifier Volume Control 2                                  |
| 1        | 49 - 62   | 0x01        | 0x31 - 0x3E | Right MICPGA Positive Terminal Input Routing Configuration Register |
| 1        | 64 - 121  | 0x01        | 0x40 - 0x79 | Reserved Registers                                                  |
| 1        | 122       | 0x01        | 0x7A        | Reference Power Up Delay                                            |
| 1        | 123 - 127 | 0x01        | 0x7B - 0x7F | Reserved Registers                                                  |
| 2 - 43   | 0 - 127   | 0x02 - 0x2B | 0x00 - 0x7F | Reserved Registers                                                  |
| 44       | 0         | 0x2C        | 0x00        | Page Select Register                                                |
| 44       | 1         | 0x2C        | 0x01        | DAC Adaptive Filter Configuration Register                          |
| 44       | 2 - 7     | 0x2C        | 0x02 - 0x07 | Reserved                                                            |
| 44       | 8 - 127   | 0x2C        | 0x08 - 0x7F | DAC Coefficients Buffer-A C(0:29)                                   |
| 45 - 52  | 0         | 0x2D-0x34   | 0x00        | Page Select Register                                                |
| 45 - 52  | 1 - 7     | 0x2D-0x34   | 0x01 - 0x07 | Reserved.                                                           |

**表 8-4. Summary of Register Map (continued)**

| Decimal  |          | Hex         |             | DESCRIPTION                         |
|----------|----------|-------------|-------------|-------------------------------------|
| PAGE NO. | REG. NO. | PAGE NO.    | REG. NO.    |                                     |
| 45 - 52  | 8 - 127  | 0x2D-0x34   | 0x08 - 0x7F | DAC Coefficients Buffer-A C(30:255) |
| 53 - 61  | 0 - 127  | 0x35 - 0x3D | 0x00 - 0x7F | Reserved Registers                  |
| 62 - 70  | 0        | 0x3E-0x46   | 0x00        | Page Select Register                |
| 62 - 70  | 1 - 7    | 0x3E-0x46   | 0x01 - 0x07 | Reserved Registers                  |
| 62 - 70  | 8 - 127  | 0x3E-0x46   | 0x08 - 0x7F | DAC Coefficients Buffer-B C(0:255)  |
| 71 - 255 | 0 - 127  | 0x47 - 0x7F | 0x00 - 0x7F | Reserved Registers                  |

## 9 Application and Implementation

### 注

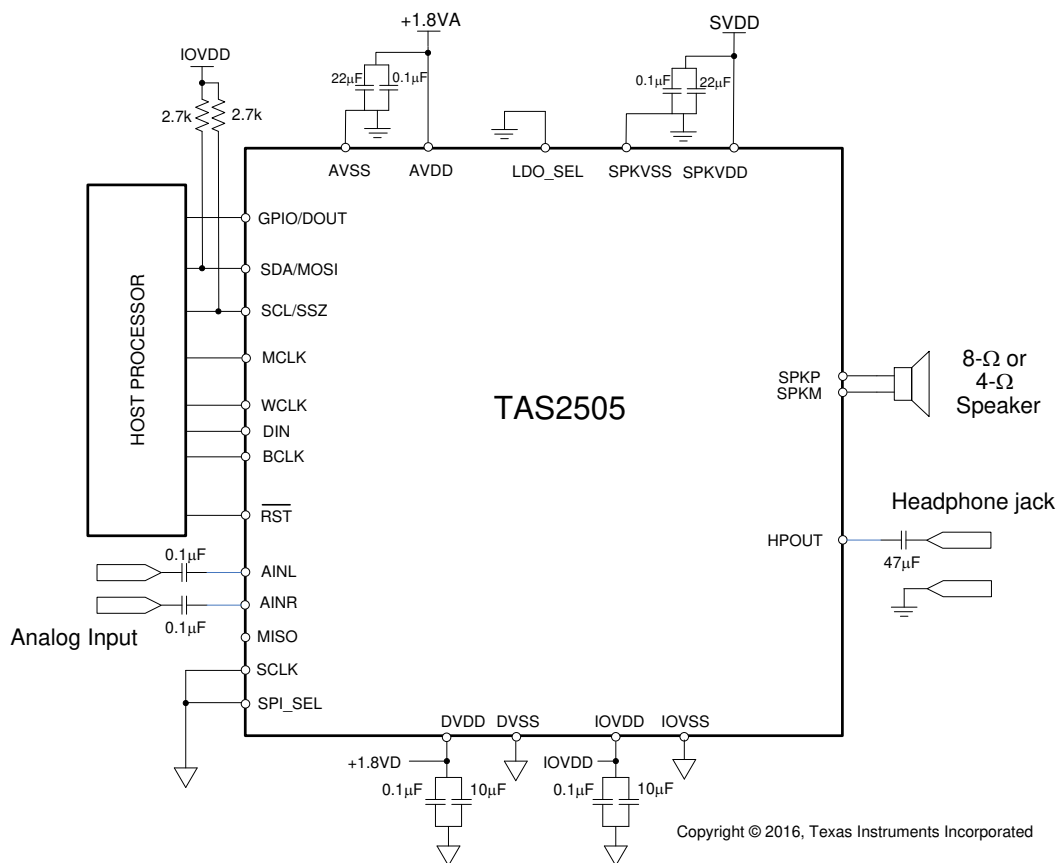
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TAS2505-Q1 is a digital or analog input Class-D audio power amplifier. This device include an internal LDO that can be used to supply the analog and digital internal supply rails. Below are shown different setups that show the features of the TAS2505-Q1.

### 9.2 Typical Applications

#### 9.2.1 Typical Configuration



9-1. Typical Circuit Configuration

### 9.2.1.1 Design Requirements

表 9-1 shows the design parameters.

**表 9-1. Design Parameters**

| PARAMETER    | EXAMPLE VALUE                                       |
|--------------|-----------------------------------------------------|
| Audio input  | Digital Audio (I <sup>2</sup> S), Analog Audio AINx |
| Internal LDO | Not used                                            |
| Speaker      | 8-Ω or 4-Ω                                          |

### 9.2.1.2 Detailed Design Procedure

In this application, the device is able to use both digital and analog inputs, working in mono output by summing left and right analog inputs and output from DAC and routing this signal into the speaker output.

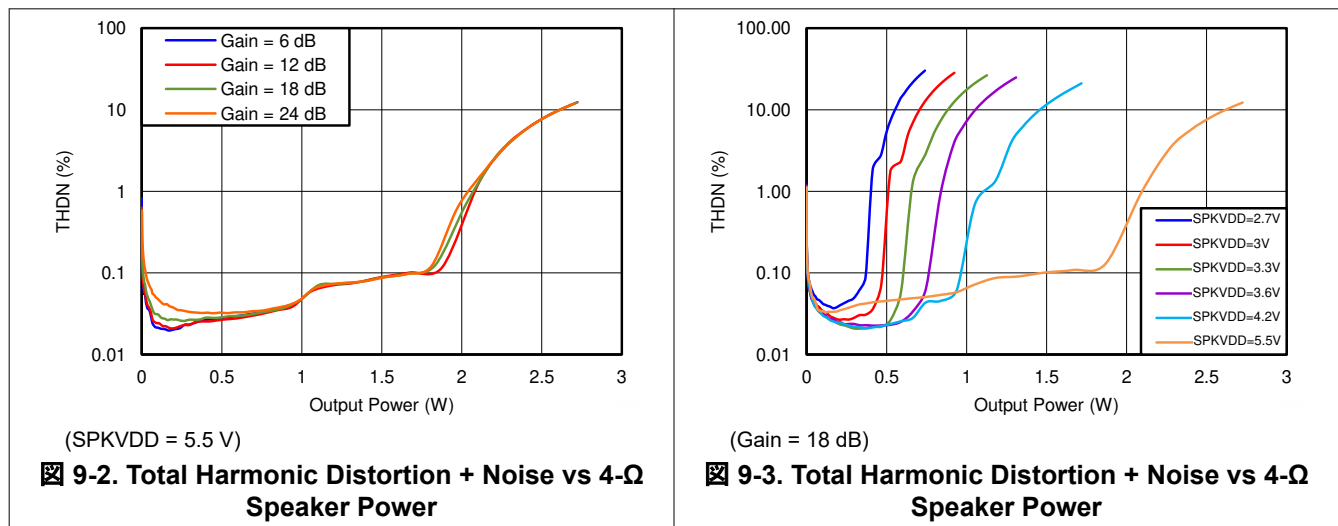
The internal LDO is not used in this application because the LDO\_SEL pin is tied to GND. External 1.8-V supply is used to power AVDD and DVDD. IOVDD can be supplied by voltages between 1.1 V and 3.6 V which lets the system to use conventional 1.8-V or 3.3-V supplies. The SPKVDD can be connected to voltages between 2.7 V and 5.5 V, although it is usually supplied by a 5-V voltage.

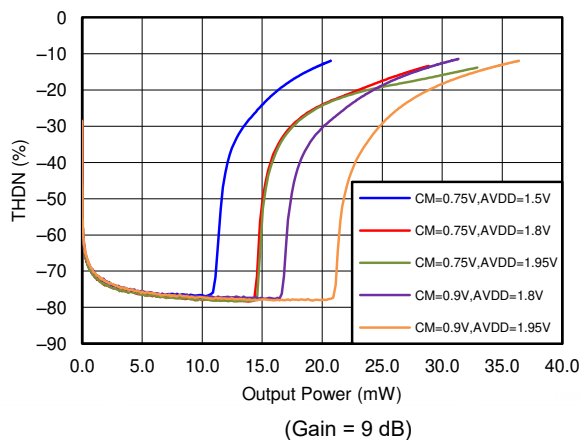
Decoupling capacitors should be used at all the supply lines. TI recommends using 0.1-μF, 10-μF, and 22-μF capacitors for a better system performance.

Decoupling series capacitors must be used at the analog input.

All grounds are tied together; route analog and digital paths are separated to avoid interference.

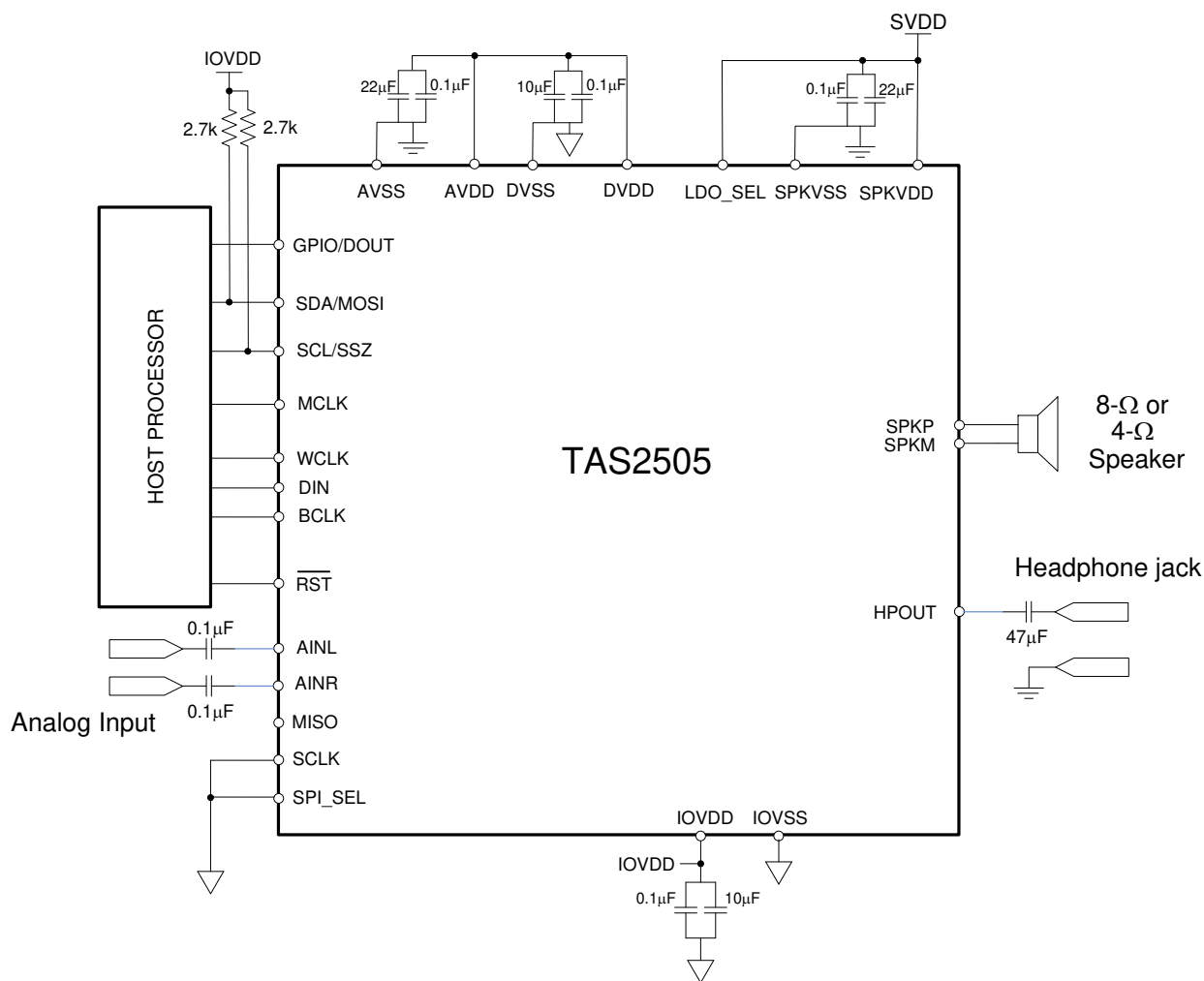
### 9.2.1.3 Application Curves





**图 9-4. Total Harmonic Distortion + Noise vs HP Power**

## 9.2.2 Circuit Configuration With Internal LDO



Copyright © 2016, Texas Instruments Incorporated

**图 9-5. Application Schematics for LDO**

### 9.2.2.1 Design Requirements

表 9-2 shows the design parameters.

**表 9-2. Design Parameters**

| PARAMETER    | EXAMPLE VALUE                                       |
|--------------|-----------------------------------------------------|
| Audio input  | Digital Audio (I <sup>2</sup> S), Analog Audio AINx |
| Internal LDO | Used                                                |
| Speaker      | 8-Ω or 4-Ω                                          |

## 10 Power Supply Recommendations

The TAS2505-Q1 integrates a large amount of digital and analog functionality, and each of these blocks can be powered separately to enable the system to select appropriate power supplies for desired performance and power consumption. The device has separate power domains for digital IO, digital core, analog core, analog input and speaker drivers. If desired, all of the supplies (except for the supplies for speaker drivers, which can directly connect to the battery) can be connected together and be supplied from one source in the range of 1.65 V to 1.95 V. Individually, the IOVDD voltage can be supplied in the range of 1.1 V to 3.6 V. For improved power efficiency, the digital core power supply can range from 1.26 V to 1.95 V. The analog core supply can either be derived from the internal LDO accepting an SPKVDD voltage in the range of 2.7V to 5.5V or the AVDD pin can directly be driven with a voltage in the range of 1.5 V to 1.95 V. The speaker driver voltages (SPKVDD) can range from 2.7 V to 5.5 V.

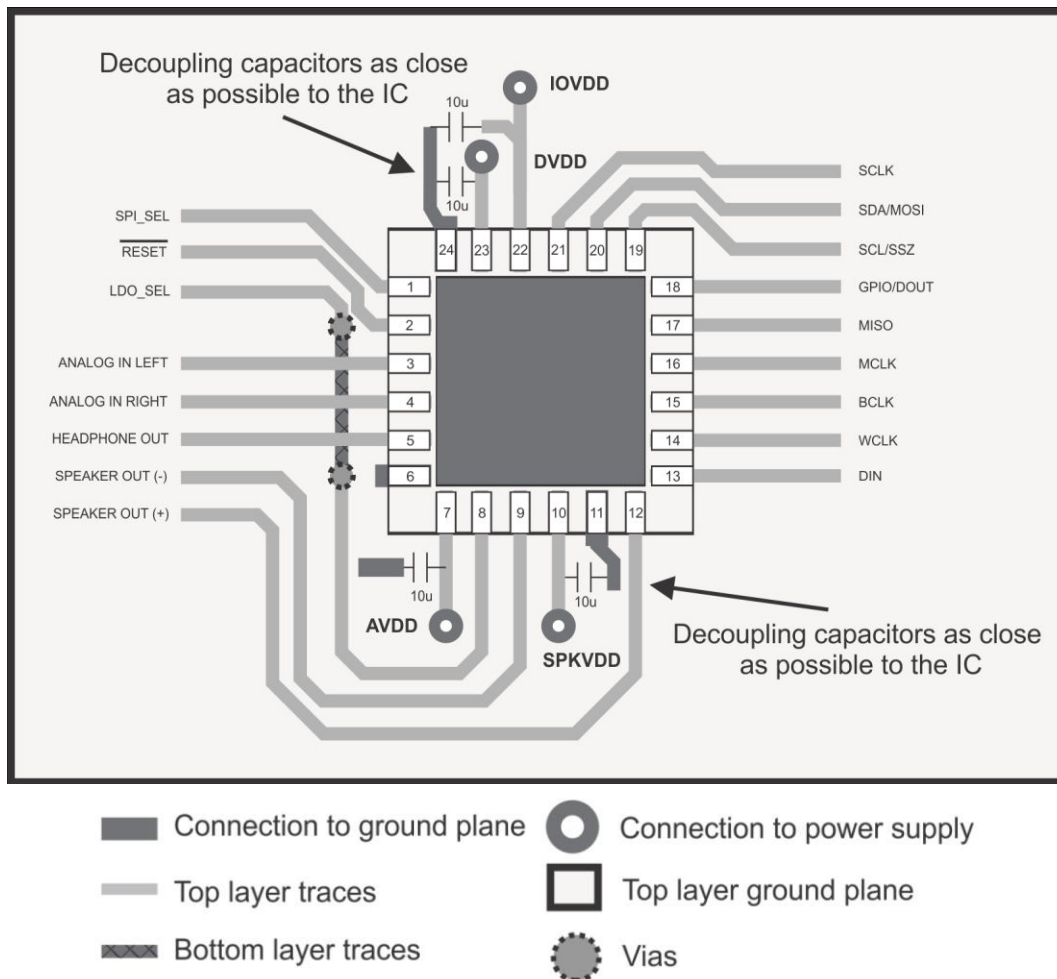
For more detailed information see the [TAS2505 Application Reference Guide](#) (SLAU472).

## 11 Layout

### 11.1 Layout Guidelines

- If the analog input, AINR and AINL, are:
  - Used, analog input traces must be routed symmetrically for true differential performance.
  - Used, do not run analog input traces parallel to digital lines.
  - Used, they must be AC-coupled.
  - Not used, they must be shorted together.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors.

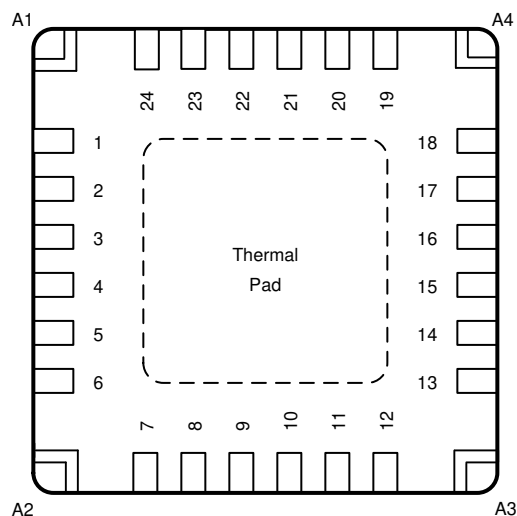
### 11.2 Layout Example



11-1. Layout Diagram

## 11.3 Thermal Pad

Solder the Thermal PAD to GND plane. The plane will work as heat sink. For details about the corner pads size and location, refer to the [セクション 13](#) at the end of this document.



**図 11-2. Thermal Pad Corner Locations**

**表 11-1. Thermal Pad Corner**

| CORNER | DESCRIPTION                                                                                      |
|--------|--------------------------------------------------------------------------------------------------|
| A1     | Internally connected to thermal pad. Leave floating or connect to the same plane as thermal pad. |
| A2     |                                                                                                  |
| A3     |                                                                                                  |
| A4     |                                                                                                  |

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[TAS2505 Application Reference Guide](#) (SLAU472)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

### 12.4 Trademarks

すべての商標は、それぞれの所有者に帰属します。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

The TAS2505TRGERQ1 orderable part number uses package outline RGE0024K, and the TAS2505ATRGERQ1 orderable part number uses package outline RGE0024Y.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS2505ATRGERQ1  | ACTIVE        | VQFN         | RGE                | 24   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 105   | TAS<br>2505AQ           | <a href="#">Samples</a> |
| TAS2505TRGERQ1   | ACTIVE        | VQFN         | RGE                | 24   | 3000           | RoHS & Green    | SN                                   | Level-3-260C-168 HR  | -40 to 105   | TAS<br>2505Q            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TAS2505-Q1 :**

- Catalog : [TAS2505](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS2505ATRGERQ1 | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TAS2505TRGERQ1  | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.3     | 4.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

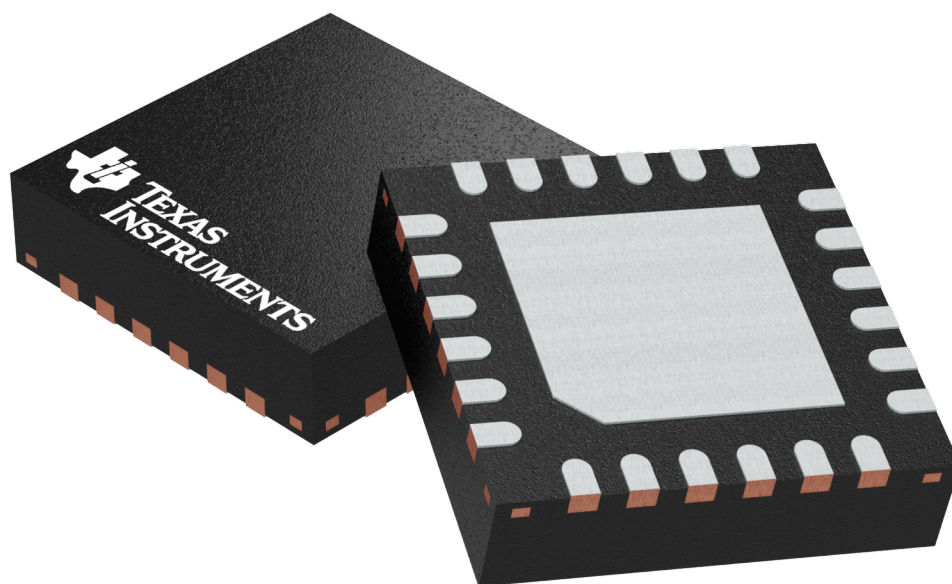
| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS2505ATRGERQ1 | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |
| TAS2505TRGERQ1  | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 38.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



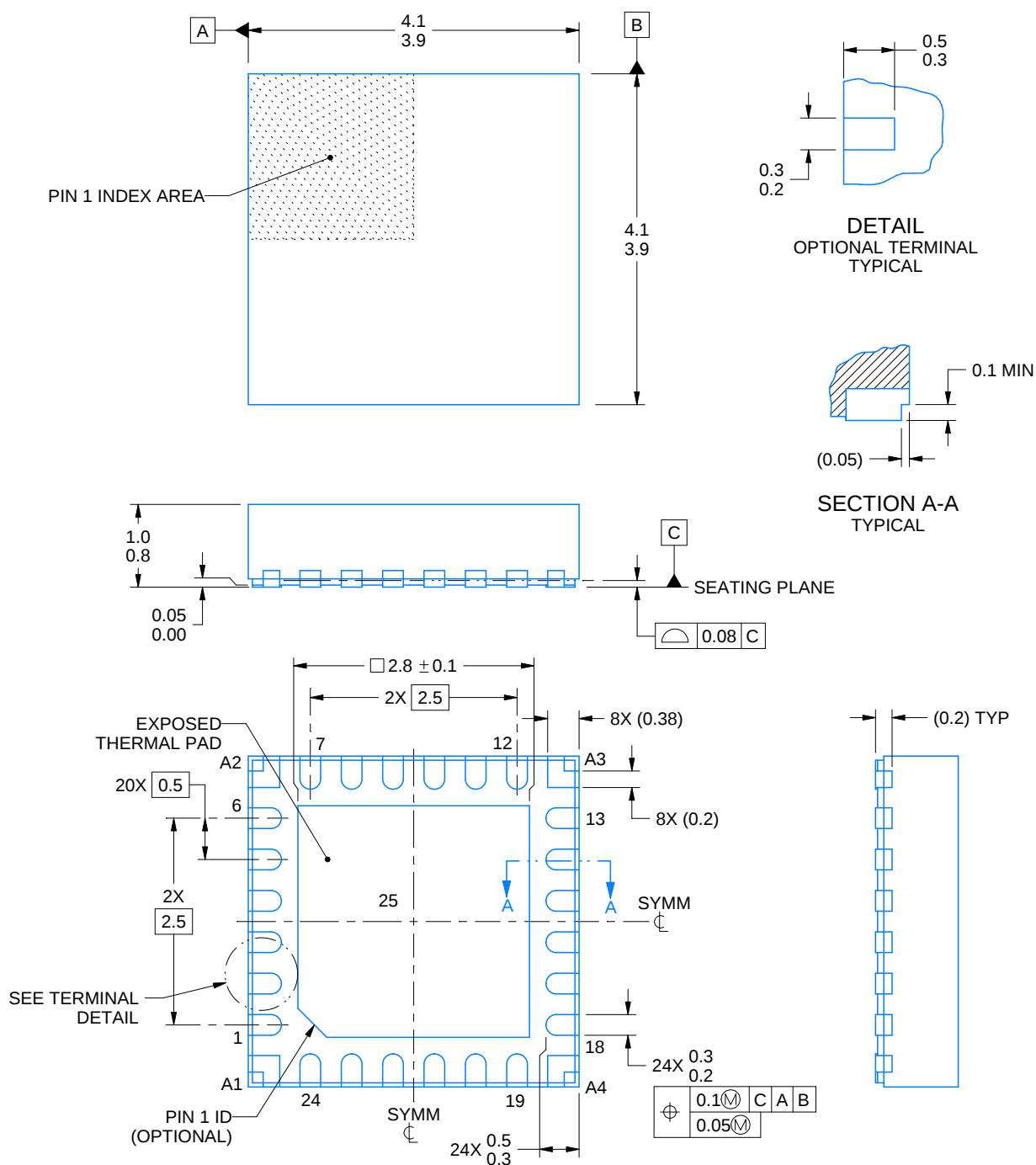
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223589/B 05/2018

NOTES:

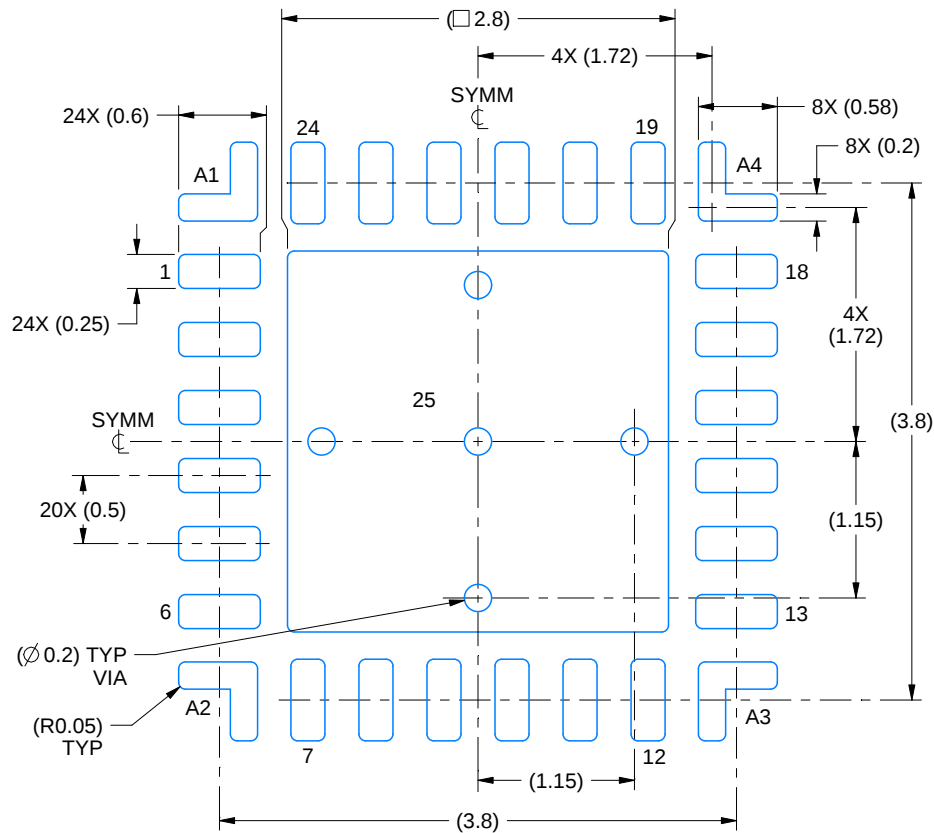
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

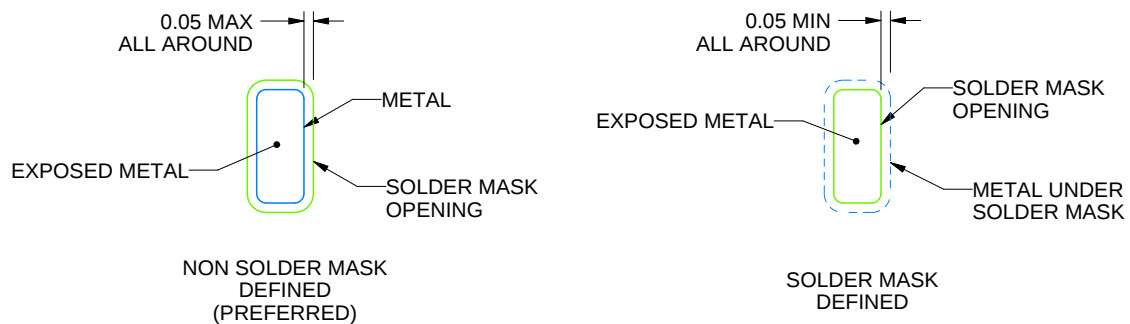
RGE0024K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4223589/B 05/2018

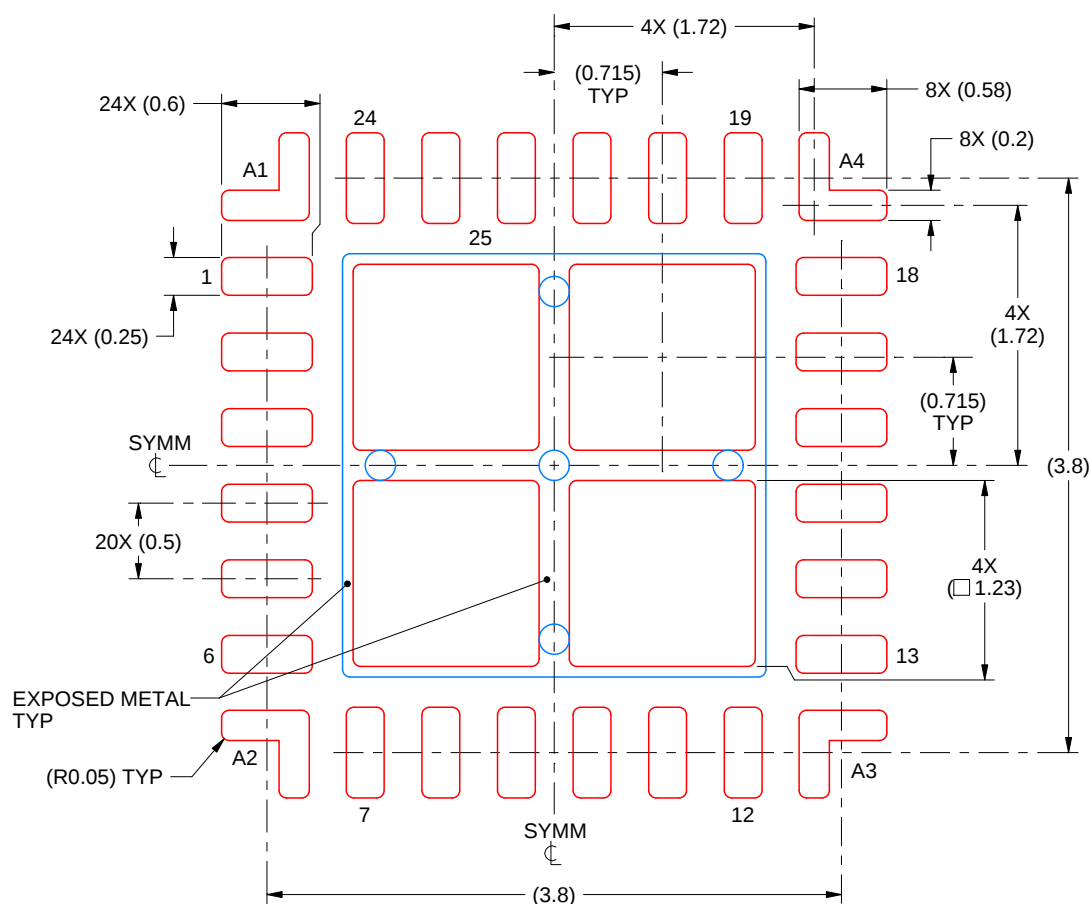
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**RGE0024K**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4223589/B 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

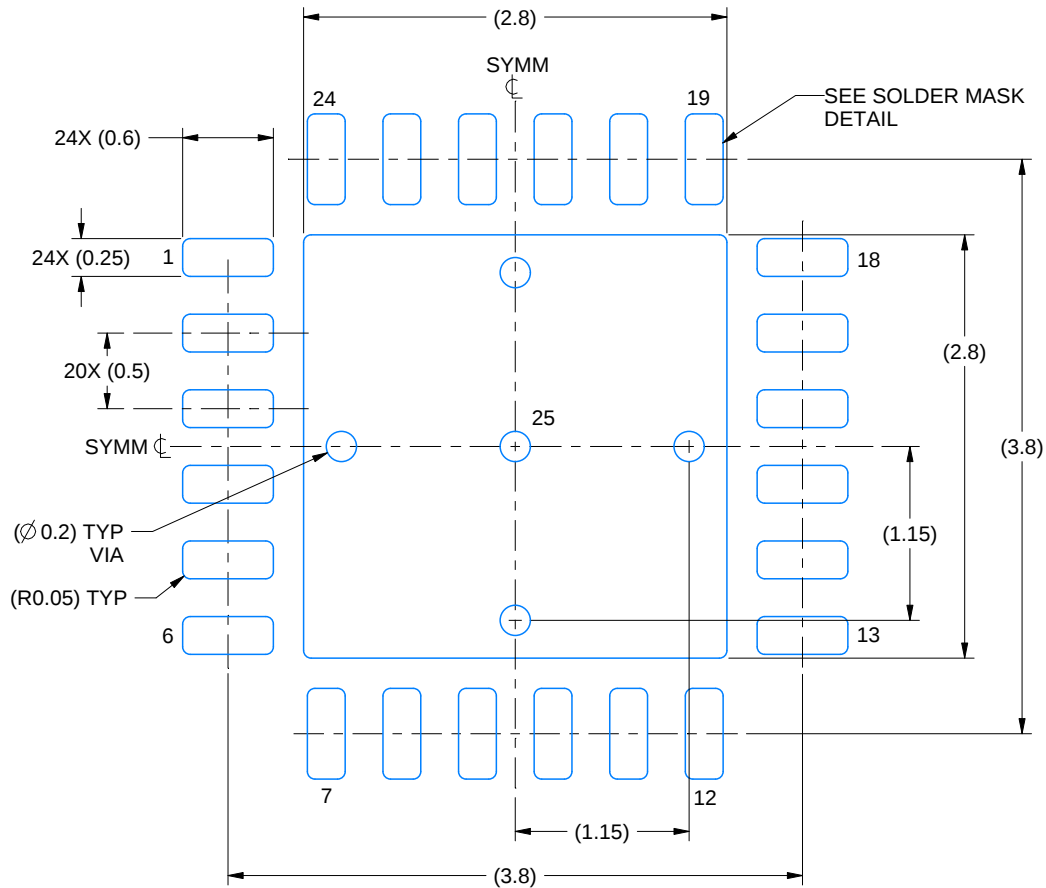
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

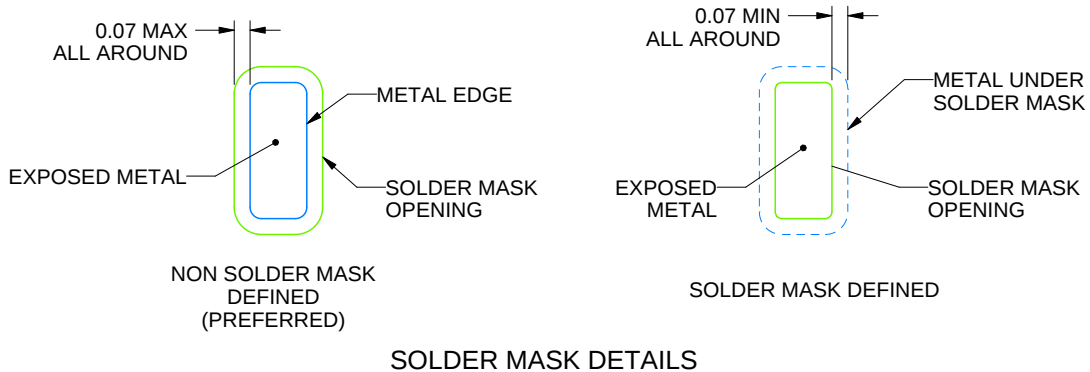
RGE0024Y

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4229066/A 09/2022

NOTES: (continued)

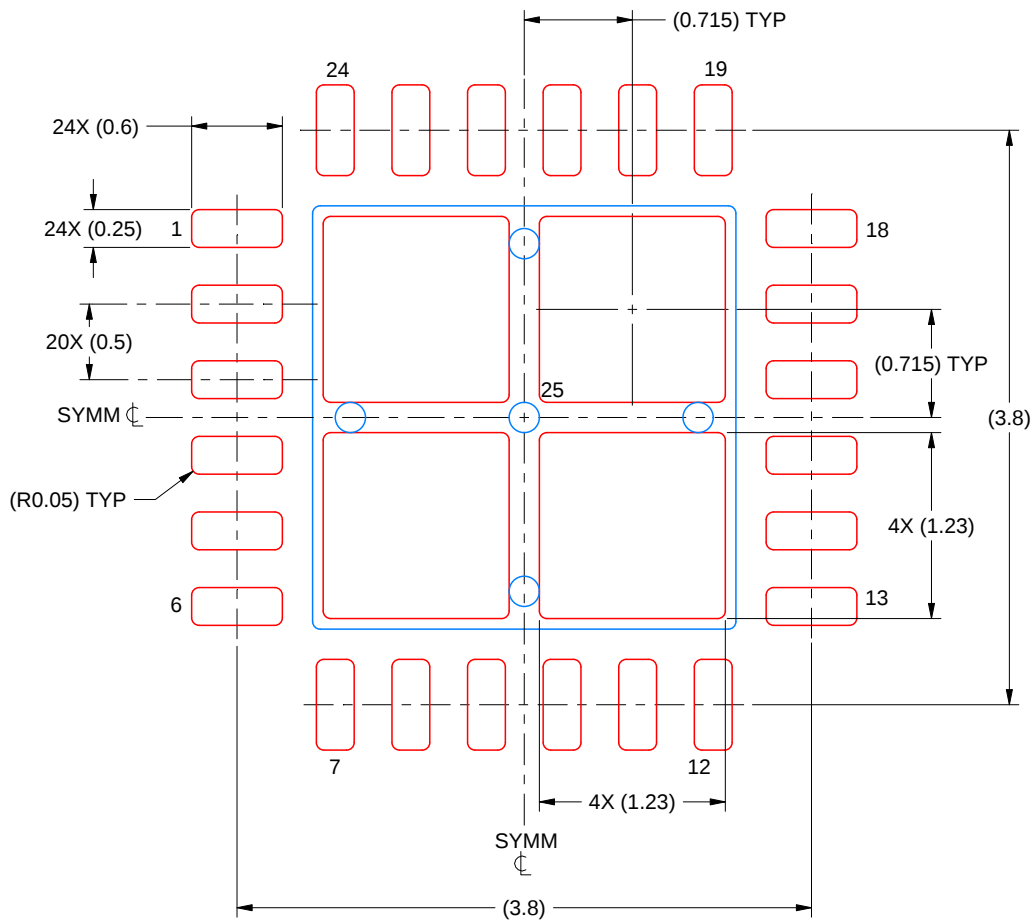
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024Y

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 25  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229066/A 09/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated