

# TAS5722L 15Wデジタル入力、モノラルClass-Dオーディオ・アンプ

## 1 特長

- モノラルClass-Dアンプ
  - 4Ω、17V、0.02% THDで連続的に15W
- 90%を超える効率のClass-D動作によりヒートシンクが不要
- オーディオ性能(PVDD = 16.5V、RSPK = 4Ω)
  - アイドル・チャンネル・ノイズ = 45μVRMS (A-Wtd)
  - THD+N = 0.04% (1W、1kHzのとき)
  - SNR=106dB A-Wtd (THD+N = 1%を基準)
- I<sup>2</sup>S入力: 32kHz~96kHz
- TDMオーディオ入力
  - 最大8チャンネル(32ビット、96kHz)
- I<sup>2</sup>C制御、8個のI<sup>2</sup>Cアドレスを選択可能
- 電源
  - パワー・アンプ: 4.5V~17V
  - デジタルI/O: 1.8V
- 堅牢性機能
  - クロック誤差検出器、DCオフセットおよび短絡保護
  - 過電圧、低電圧、過熱保護

## 2 アプリケーション

- サブウーファー、ブーム・ボックス、サウンドバー、ビルディング・オートメーション
- 電源内蔵スピーカ、パーソナル・コンピュータ
- サラウンド・サウンド・システム、1チャンネル・オーディオ・システム

## 3 概要

TAS5722Lデバイスは高効率のモノラルClass-Dオーディオ・パワー・アンプで、デジタル出力クリップ、複数のゲイン・オプション、広い動作電源範囲が特長です。4.5V~17VDCの公称電源電圧で動作します。

TAS5722Lは、高い過渡電力耐性を持ち、小型スピーカーの動的な電力ヘッドルームを活用するよう最適化されています。4Ωスピーカーへ連続的に15W以上を供給できます。

デジタル時分割多重化(TDM)インターフェイスにより、最大8個のデバイスが同じバスを共有できます。

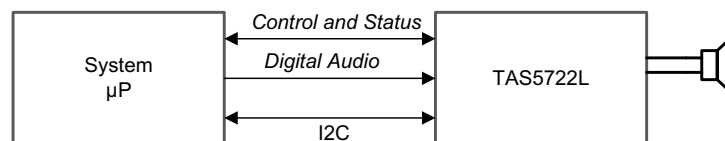
TAS5722Lデバイスは、4mm×4mm、32ピンのQFNパッケージで供給されます。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ
TAS5722L	QFN (32)	4mm×4mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 概略回路図



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## 4 改訂履歴

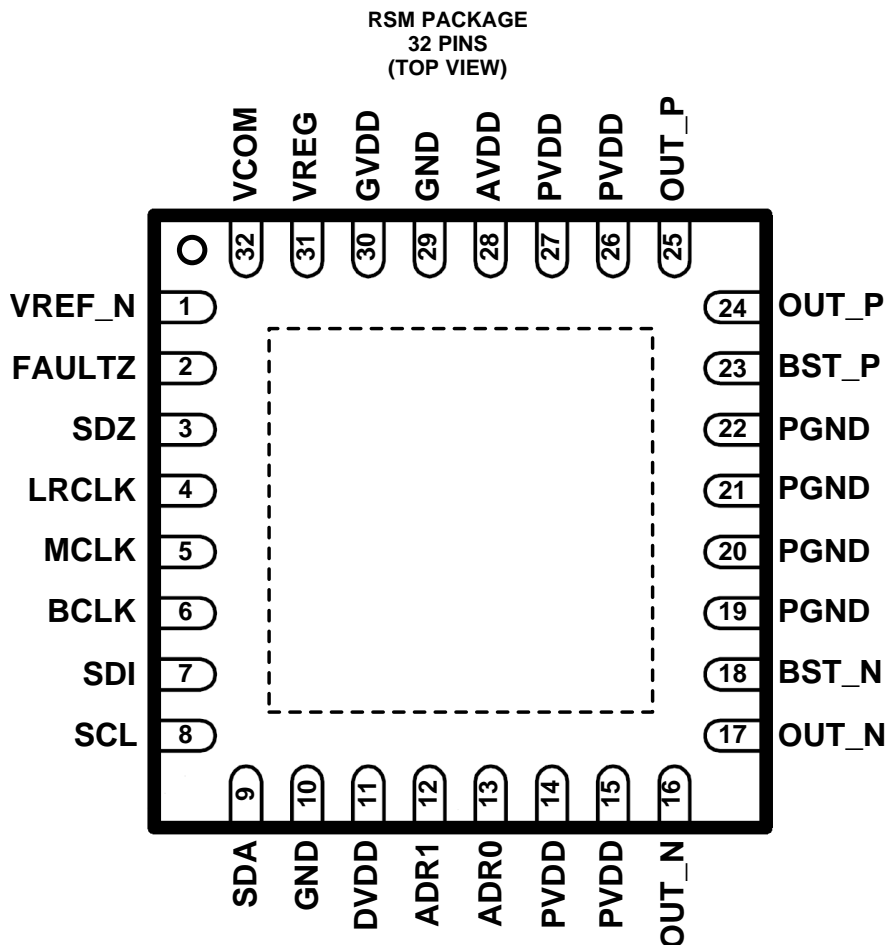
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### 2016年5月発行のものから更新

**Page**

•	製品を量産データへ変更 .....	<b>1</b>
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## 5 Pin Configuration and Functions



**Pin Functions<sup>(1)</sup>**

PIN		I/O/P <sup>(2)</sup>	DESCRIPTION
NAME	NO.		
ADR1	12	I	I <sup>2</sup> C address inputs. Each pin can detect a short to DVDD, a short to GND, a 22-kΩ connection to GND and a 22-kΩ connection to DVDD.
ADR0	13	I	
AVDD	28	P	Analog power supply input. Connect directly to PVDD.
BCLK	6	I	TDM Interface serial bit clock.
BST_N	18	P	Class-D Amplifier negative bootstrap. Connect a capacitor between BST_N and OUT_N.
BST_P	23	P	Class-D Amplifier positive bootstrap. Connect a capacitor between BST_P and OUT_P.
DVDD	11	P	Digital power supply. Connect to 1.8-V supply with external decoupling capacitor.
FAULTZ	2	O	Open drain active low fault flag. Pull up on PCB with resistor to DVDD.
GND	10 29	P	Ground. Connect to PCB ground plane.
GVDD	30	O	Class-D amplifier gate drive regulator output. Connect decoupling cap to PCB ground plane.
LRCLK	4	I	TDM interface left/right clock.
MCLK	5	I	Device master clock.

(1) Connect exposed thermal pad to PCB ground plane

(2) I = input, O = output, P = power, I/O = bi-directional

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[www.ti.com](http://www.ti.com)
**Pin Functions<sup>(1)</sup> (continued)**

PIN		I/O/P <sup>(2)</sup>	DESCRIPTION
NAME	NO.		
PGND	19	P	Power ground. Connect to PCB ground plane.
	20		
	21		
	22		
PVDD	14	P	Class-D amplifier power supply input. Connect to PVDD supply and decouple externally.
	15		
	26		
	27		
OUT_N	16	O	Class-D amplifier negative output.
	17		
OUT_P	24	O	Class-D amplifier positive output.
	25		
SCL	8	I	I <sup>2</sup> C clock Input. Pull up on PCB with a 2.4-kΩ resistor.
SDA	9	I/O	I <sup>2</sup> C bi-directional data. Pull up on PCB with a 2.4-kΩ resistor.
SDI	7	I	TDM interface data input.
SDZ	3	I	Active low shutdown signal. Assert low to hold device inactive.
VCOM	32	O	Common mode reference output. Connect decoupling capacitor to the VREF_N pin.
VREF_N	1	P	Negative reference for analog. Connect to VCOM and VREG capacitor negative pins.
VREG	31	O	Analog regulator output. Connect decoupling capacitor to the VREF_N pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	PVDD, AVDD	−0.3	20	V
		DVDD	−0.3	2.25	
	Digital input voltage	Digital inputs referenced to DVDD supply	−0.5	V <sub>DVDD</sub> + 0.5	V
T <sub>A</sub>	Ambient operating temperature		−25	85	°C
T <sub>stg</sub>	Storage temperature range		−40	125	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground pin.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
PVDD AVDD	Power supply voltage	4.5		17	V
DVDD	Power supply voltage	1.65	1.8	2	V
V <sub>IH(DR)</sub>	High-level digital input voltage		V <sub>DVDD</sub>		V
V <sub>IL(DR)</sub>	Low-level digital input voltage		0		V
R <sub>SPK</sub>	Minimum speaker load	3.2			Ω
T <sub>A</sub>	Operating free-air temperature	−25		85	°C
T <sub>J</sub>	Operating junction temperature	−25		150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TAS5722L	UNIT
		RSM (QFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	37.3	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	30.4	
$R_{\theta JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	7.9	
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	0.4	
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	7.7	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	2.5	

- (1) 従来および新しい熱測定値の詳細については、『Semiconductor and IC Package Thermal Metrics』アプリケーション・レポート (SPRA953)を参照してください。
- (2) 自然対流における、接合部と周囲の空気との間の熱抵抗は、JESD51-2aに記述されている環境において、JESD51-7で規定されている JEDEC標準のHigh-Kボード上でのシミュレーションによって求められます。
- (3) 接合部とケース(上面)との間の熱抵抗は、パッケージ上面での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した記述があります。
- (4) 接合部と基板との間の熱抵抗は JESD51-8で説明されているように、PCB温度を制御するリング型冷却板治具で環境をシミュレーションすることにより求められます。
- (5) 接合部とケース上部との間の特性パラメータ $\Psi_{JT}$ は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、 $R_{\theta JA}$ を求めるためのシミュレーションデータから抽出されます。
- (6) 接合部と基板との間の特性パラメータ $\Psi_{JB}$ は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、 $R_{\theta JA}$ を求めるためのシミュレーションデータから抽出されます。
- (7) 接合部とケース(底面)との間の熱抵抗は、露出したパッド(Power PAD)上での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した内容があります。

## 6.5 Electrical Characteristics

$V_{PVD} = 16.5\text{ V}$ ,  $V_{D} = 1.8\text{ V}$ ,  $R_L = 4\ \Omega + 33\ \mu\text{H}$ ,  $f_{PWM} = 576\text{ kHz}$ , 22-Hz to 20- kHz Bandwidth, AP AUX-0025 + AES17 Filter (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL INPUT AND OUTPUT</b>						
$V_{IH}$	High-level digital input logic voltage threshold	All digital pins	70%			
$V_{IL}$	Low-level digital input logic voltage threshold	All digital pins			30%	
$I_{IH}$	Input logic "high" leakage for digital inputs	All digital pins, excluding SDZ			15	$\mu\text{A}$
$I_{IL}$	Input logic "low" leakage for digital inputs	All digital pins, excluding SDZ			–15	$\mu\text{A}$
$I_{IH}(\text{SDZ})$	Input logic "high" leakage for SDZ inputs	SDZ			1	$\mu\text{A}$
$I_{IL}(\text{SDZ})$	Input logic "low" leakage for SDZ inputs	SDZ			–1	$\mu\text{A}$
$V_{OL}$	Output logic "low" for FAULTZ open drain Output	$I_{OL} = -2\text{ mA}$			10% $V_{D}$	
$C_{IN}$	Input capacitance for digital inputs	All digital pins		5		pF
<b>MASTER CLOCK</b>						
$D_{MCLK}$	Allowable MCLK duty cycle		45%	50%	55%	
$f_{MCLK}$	MCLK input frequency				25	MHz
	Supported single-speed MCLK frequencies	values: 64, 128, 256 and 512	2.8		24.6	MHz
	Supported double-speed MCLK frequencies	values: 64, 128 and 256	5.6		24.6	MHz
<b>SERIAL AUDIO PORT</b>						
$D_{BCLK}$	Allowable BCLK duty cycle		45%	50%	55%	
$f_{BCLK}$	BCLK input frequency				25	MHz
	Supported single-speed BCLK frequencies	values: 64, 96, 128, 192 and 256	2.8		12.3	MHz
	Supported double-speed BCLK frequencies	values: 64, 96, 128, 192 and 256	5.6		24.6	MHz
$f_S$	Supported single-speed input sample rates	values: 44.1 and 48	44.1		48	kHz
	Supported double-speed input sample rates	values: 88.2 and 96	88.2		96	kHz
<b>I<sup>2</sup>C CONTROL PORT</b>						
$C_L(\text{I}^2\text{C})$	Allowable load capacitance for each I <sup>2</sup> C Line				400	pF
$f_{SCL}$	SCL frequency	No wait states			400	kHz
<b>PROTECTION</b>						
$OTE_{THRESH}$	Over-temperature error (OTE) threshold			150		$^{\circ}\text{C}$
$OTE_{HYST}$	Over-temperature error (OTE) hysteresis			15		$^{\circ}\text{C}$
$OCE_{THRESH}$	overcurrent error (OCE) threshold	$V_{PVD} = 16.5\text{ V}$ , $T_A = 25^{\circ}\text{C}$		5		A
$DCE_{THRESH}$	DC error (DCE) threshold	$V_{PVD} = 16.5\text{ V}$ , $T_A = 25^{\circ}\text{C}$		2.6		V

## Electrical Characteristics (continued)

$V_{PVDD} = 16.5\text{ V}$ ,  $V_{DVDD} = 1.8\text{ V}$ ,  $R_L = 4\ \Omega + 33\ \mu\text{H}$ ,  $f_{PWM} = 576\text{ kHz}$ , 22-Hz to 20-kHz Bandwidth, AP AUX-0025 + AES17 Filter (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>AMPLIFIER PERFORMANCE</b>						
$P_{OUT}$	Continuous average power	$R_L = 8\ \Omega + 33\ \mu\text{H}$ , 1% THD+N, $V_{PVDD} = 12\text{ V}$ , $f_{IN} = 1\text{ kHz}$		8.2		W
		$R_L = 8\ \Omega + 33\ \mu\text{H}$ , 1% THD+N, $V_{PVDD} = 16.5\text{ V}$ , $f_{IN} = 1\text{ kHz}$		15.25		
		$R_L = 4\ \Omega + 33\ \mu\text{H}$ , 1% THD+N, $V_{PVDD} = 12\text{ V}$ , $f_{IN} = 1\text{ kHz}$		14.25		
		$R_L = 4\ \Omega + 33\ \mu\text{H}$ , 1% THD+N, $V_{PVDD} = 16.5\text{ V}$ , $f_{IN} = 1\text{ kHz}$		16		
THD+N	Total harmonic distortion plus noise	$R_L = 8\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 12\text{ V}$ , $P_{OUT} = 4.25\text{ W}$ , $20\text{ Hz} \leq f_{IN} \leq 20\text{ kHz}$		0.05%		
		$R_L = 8\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 16.5\text{ V}$ , $P_{OUT} = 4.25\text{ W}$ , $20\text{ Hz} \leq f_{IN} \leq 20\text{ kHz}$		0.05%		
		$R_L = 4\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 12\text{ V}$ , $P_{OUT} = 8.25\text{ W}$ , $20\text{ Hz} \leq f_{IN} \leq 20\text{ kHz}$		0.05%		
		$R_L = 4\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 16.5\text{ V}$ , $P_{OUT} = 8.25\text{ W}$ , $20\text{ Hz} \leq f_{IN} \leq 20\text{ kHz}$		0.06%		
$P_{EFF}$	Power efficiency	$R_L = 8\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 16.5\text{ V}$ , $P_{OUT} = 10\text{ W}$		90%		
		$R_L = 4\ \Omega + 33\ \mu\text{H}$ , $V_{PVDD} = 16.5\text{ V}$ , $P_{OUT} = 14\text{ W}$		87%		
$V_N$	Integrated noise floor voltage	A-Weighted, Gain = 20.7dBV, $R_L = 8\ \Omega + 33\ \mu\text{H}$		50		$\mu\text{V}_{rms}$
KCP	Click-pop performance	Into and out of HW reset, into and out of SW shutdown, when SAIF clocks are applied or removed and during power rail cycling. Measured using Maxim click-pop measurement method.		-60		dB
$\varphi_{CC}$	Channel-to-channel phase shift	Output phase shift between multiple devices from 20 Hz to 20 kHz. Across all sample frequencies and SAIF operating modes.		0.2		deg
PSRR	Power supply rejection ratio	AC, $5.5\text{ V} \leq V_{PVDD} \leq 16.5\text{ V}$ , $DVDD = 1.8\text{ V} + 200\text{ mV}_{P-P}$ , $f_{RIPPLE}$ from 20 Hz to 20 kHz		69		dB
		AC, $V_{PVDD} = 16.5\text{ V} + 200\text{ mV}_{P-P}$ , $f_{RIPPLE}$ from 20 Hz to 5 kHz		64		
		AC, $V_{PVDD} = 16.5\text{ V} + 100\text{ mV}_{P-P}$ , $f_{RIPPLE}$ from 5 kHz to 20 kHz		60		
$AV_{00}$	Amplifier analog gain <sup>(1)</sup>	ANALOG_GAIN[1:0] register bits set to "00"		19.2		dBV
$AV_{01}$		ANALOG_GAIN[1:0] register bits set to "01"		20.7		dBV
$AV_{10}$		ANALOG_GAIN[1:0] register bits set to "10"		23.5		dBV
$AV_{11}$		ANALOG_GAIN[1:0] register bits set to "11"		26.3		dBV
$AV_{ERROR}$	Amplifier analog gain error			$\pm 0.15$		dB
$V_{OS}$	DC output offset voltage	Measured between OUTP and OUTN		1.5		mV
$A_{RIPPLE}$	Frequency response	Maximum deviation above or below passband gain.		$\pm 0.15$		dB
$f_{LP}$	-3 dB Output Cutoff Frequency			$0.47 \times f_S$		Hz
$R_{DS(on)FET}$	Power stage FET on-resistance	$T_A = 25^\circ\text{C}$		120		m $\Omega$

(1) When PVDD is less than 5.5 V, the voltage regulator that operates the analog circuitry does not have enough headroom to maintain the nominal 5.4-V internal voltage. The lack of headroom causes a direct reduction in gain (approximately -0.8 dB at 5 V and -1.74 dB at 4.5 V), but the device functions properly down to  $V_{PVDD} = 4.5\text{ V}$ . For operation below 5.5V, the VREG\_LVL bit (register 0x14, bit 2) can be set high, which reduces the internal voltage regulator output voltage to prevent variation in gain. When the bit is set high, all gain settings are reduced by 3dB.



## Electrical Characteristics (continued)

$V_{PVDD} = 16.5\text{ V}$ ,  $V_{DVDD} = 1.8\text{ V}$ ,  $R_L = 4\ \Omega + 33\ \mu\text{H}$ ,  $f_{PWM} = 576\text{ kHz}$ , 22-Hz to 20- kHz Bandwidth, AP AUX-0025 + AES17 Filter (unless otherwise noted)

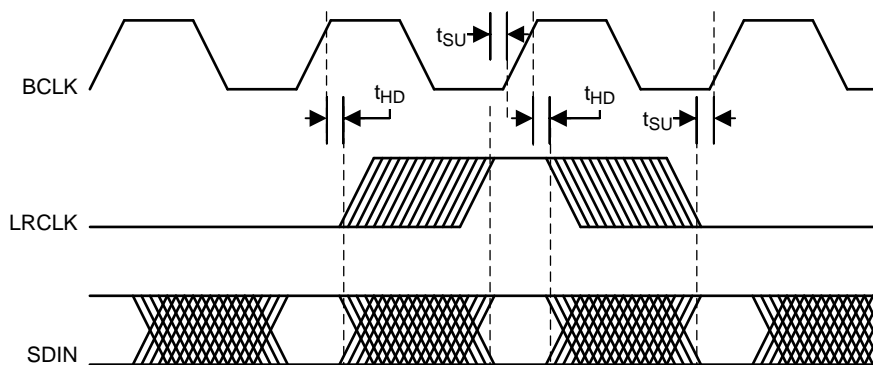
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)TOT}$	Power stage total on-resistance (FET+bond+package)	$T_A = 25^\circ\text{C}$		150		m $\Omega$
$I_{P-P}$	Peak output current	$T_A = 25^\circ\text{C}$		5		A
$f_{PWM}$	PWM switching frequency	values: 6, 8, 10, 12, 14, 16, 20 and 24	6		24	MHz

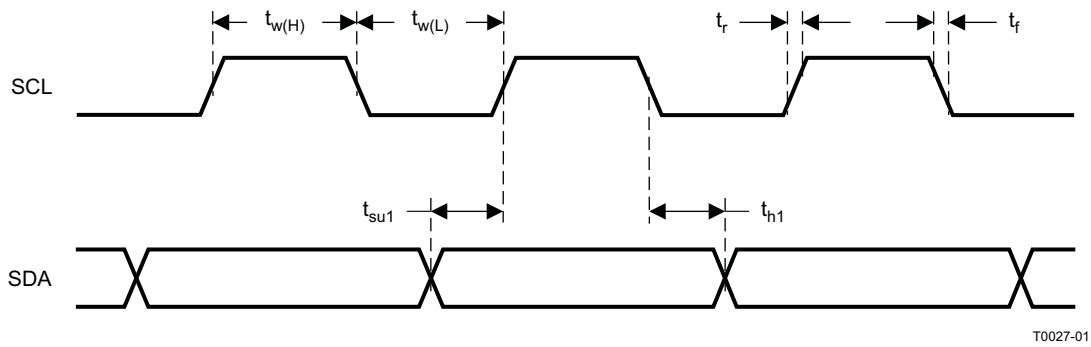
## 6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{ACTIVE}$	Shutdown to Active Time	From deassertion of SDZ (both pin and I <sup>2</sup> C register bit) until the Class-D amplifier begins switching.		25		ms
$t_{WAKE}$	Wake Time	From the deassertion of SLEEP until the Class-D amplifier starts switching.		1		ms
$t_{SLEEP}$	Sleep Time	From the assertion of SLEEP until the Class-D amplifier stops switching.		$t_{vrmp}+1$		ms
$t_{MUTE}$	Play to Mute Time	From the assertion of MUTE until the volume has ramped to the minimum.		$t_{vrmp}$		ms
$t_{PLAY}$	Un-Mute to Play Time	From the deassertion of MUTE until the volume has returned to its current setting.		$t_{vrmp}$		ms
$t_{SD}$	Active to Shutdown Time	From the assertion of SDZ (pin or I <sup>2</sup> C register bit) until the Class-D amplifier stops switching.		$t_{vrmp}+1$		ms

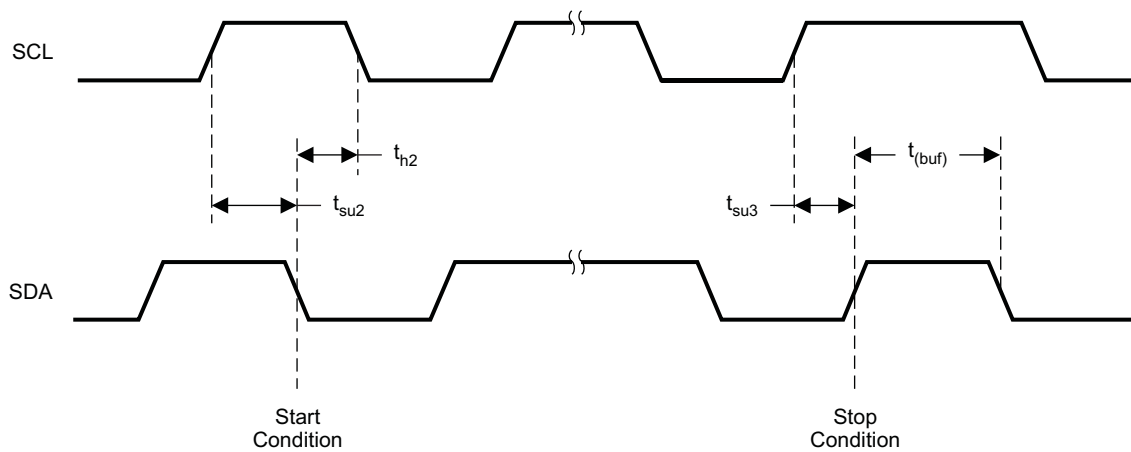
**Timing Requirements (continued)**

			MIN	NOM	MAX	UNIT
<b>SERIAL AUDIO PORT</b>						
$t_{H\_L}$	Time High/Low, BCLK, LRCLK, SDI inputs		10			ns
$t_{SU} / t_{HLD}$	Setup and hold time. LRCLK, SDI input to BCLK edge.	Input $t_{RISE} \leq 1$ ns, input $t_{FALL} \leq 1$ ns	5			ns
		Input $t_{RISE} \leq 4$ ns, input $t_{FALL} \leq 4$ ns	8			
		Input $t_{RISE} \leq 8$ ns, input $t_{FALL} \leq 8$ ns	12			
$t_{RISE}$	Rise-time BCLK, LRCLK, SDI inputs				8	ns
$t_{FALL}$	Fall-time BCLK, LRCLK, SDI inputs				8	ns
<b>I<sup>2</sup>C CONTROL PORT</b>						
$t_{BUF}$	Bus free time between start and stop conditions		1.3			$\mu$ s
$t_{H1(I2C)}$	Hold Time, SCL to SDA		0			ns
$t_{H2(I2C)}$	Hold Time, start condition to SCL		0.6			$\mu$ s
$t_{START(I2C)}$	I2C Startup Time after DVDD Power On Reset				12	ms
$t_{R(I2C)}$	Rise Time, SCL and SDA				300	ns
$t_{F(I2C)}$	Fall Time, SCL and SDA				300	ns
$t_{SU1(I2C)}$	Setup, SDA to SCL		100			ns
$t_{SU2(I2C)}$	Setup, SCL to start condition		0.6			$\mu$ s
$t_{SU3(I2C)}$	Setup, SCL to stop condition		0.6			$\mu$ s
$t_{W(H)}$	Required pulse duration, SCL "HIGH"		0.6			$\mu$ s
$t_{W(L)}$	Required pulse duration, SCL "LOW"		1.3			$\mu$ s
<b>PROTECTION</b>						
$t_{FAULTZ}$	Amplifier fault time-out period	DC detect error		650		ms
		OTE or OCE fault		1.3		s

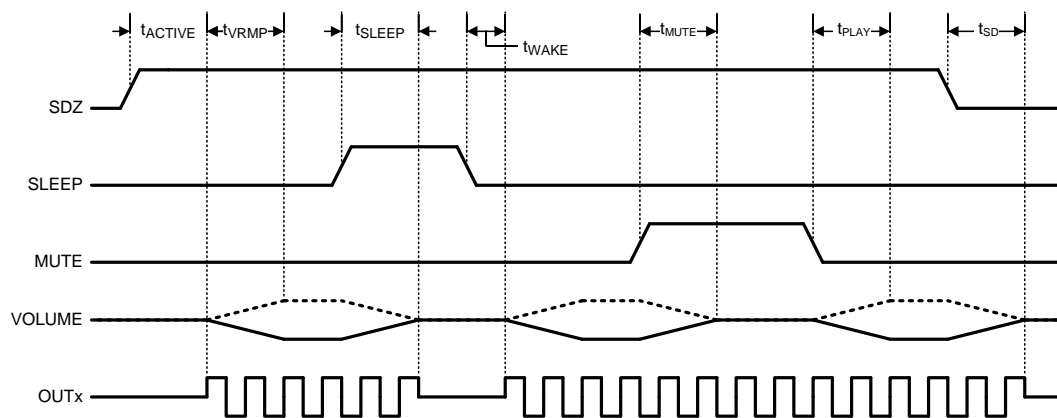

**FIG 1. SAIF Timing**



**2. SCL and SDA Timing**



**3. Start and Stop Conditions Timing**



**4. Mode Timing**

## 6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $f_{IN} = 1\text{ kHz}$ ,  $f_{PWM} = 768\text{ kHz}$ ,  $f_s = 48\text{ kHz}$ , Gain = 20.7 dBV, SDZ = 1, Measured using TAS5722LEVM with an Audio Precision SYS-2722 and AUX-0025 filter with 22-Hz-to-20- kHz un-weighted bandwidth using the 20- kHz pre-analyzer filter + 20- kHz brick-wall filter (unless otherwise specified). 33  $\mu\text{H}$  inductors were added in series with 4  $\Omega$  loads and 68  $\mu\text{H}$  inductors were placed in series with 8  $\Omega$  loads due to the ferrite bead filters.

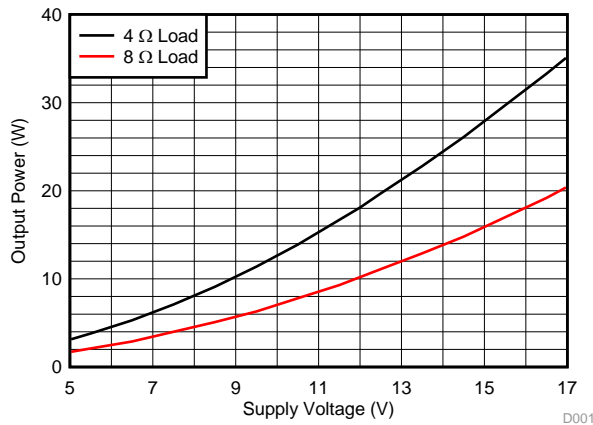


Figure 5. Output Power vs Supply Voltage

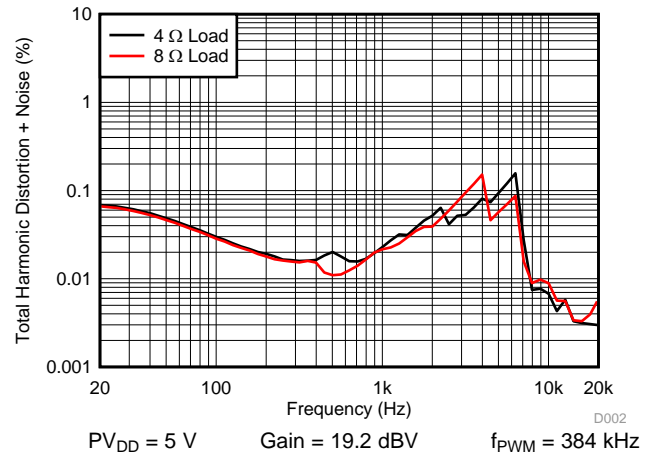


Figure 6. THD+N vs Frequency

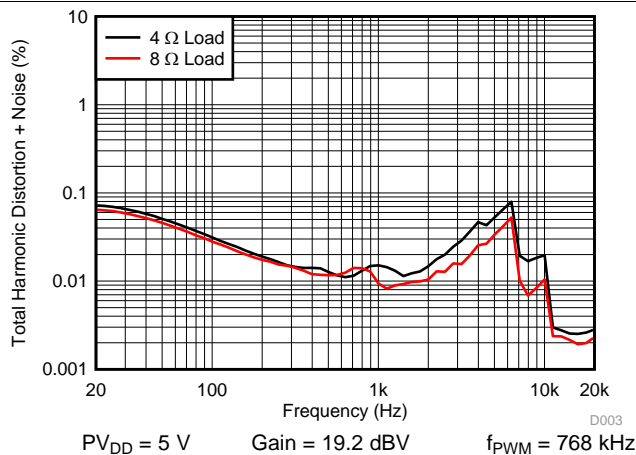


Figure 7. THD+N vs Frequency

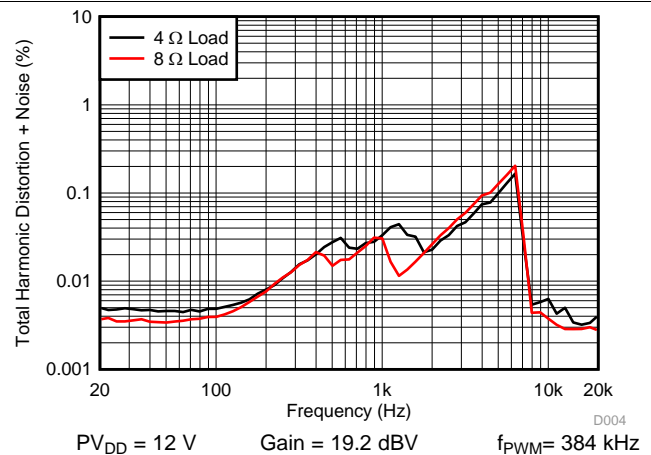


Figure 8. THD+N vs Frequency

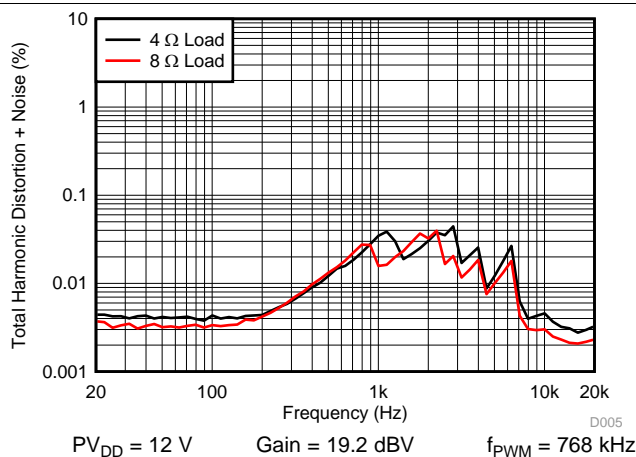


Figure 9. THD+N vs Frequency

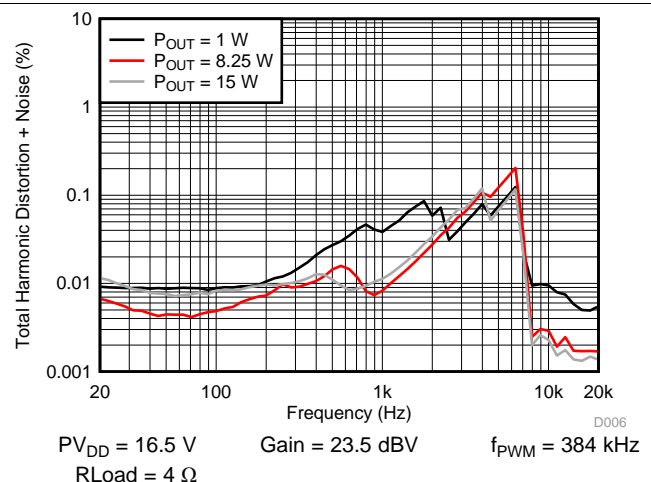


Figure 10. THD+N vs Frequency

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $f_{IN} = 1\text{ kHz}$ ,  $f_{PWM} = 768\text{ kHz}$ ,  $f_s = 48\text{ kHz}$ , Gain = 20.7 dBV, SDZ = 1, Measured using TAS5722LEVM with an Audio Precision SYS-2722 and AUX-0025 filter with 22-Hz-to-20-kHz un-weighted bandwidth using the 20-kHz pre-analyzer filter + 20-kHz brick-wall filter (unless otherwise specified). 33  $\mu\text{H}$  inductors were added in series with 4  $\Omega$  loads and 68  $\mu\text{H}$  inductors were placed in series with 8  $\Omega$  loads due to the ferrite bead filters.

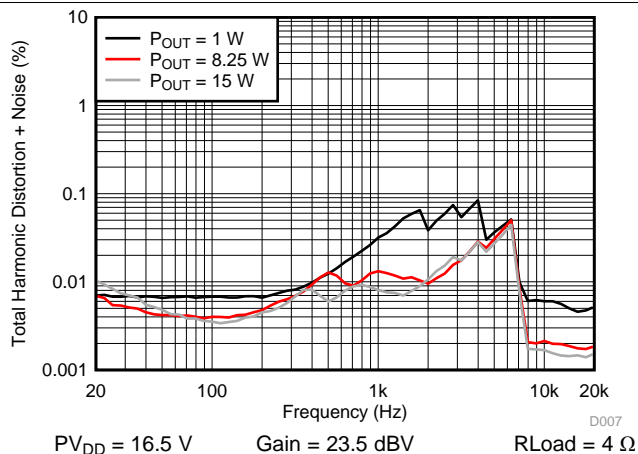


图 11. THD+N vs Frequency

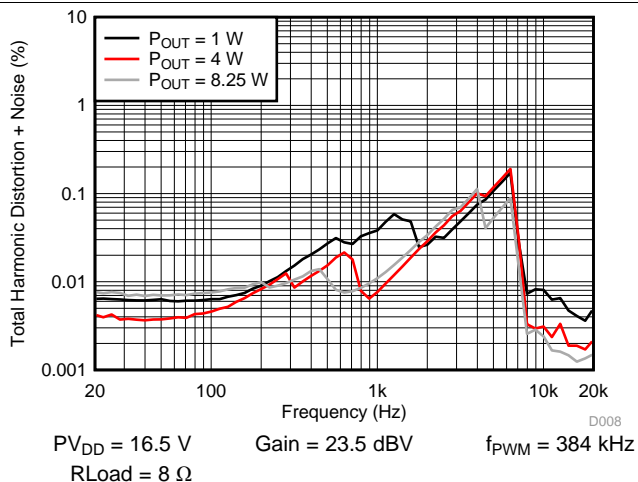


图 12. THD+N vs Frequency

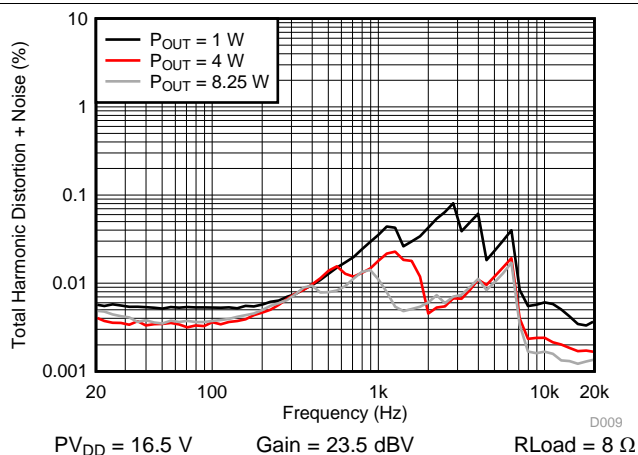


图 13. THD+N vs Frequency

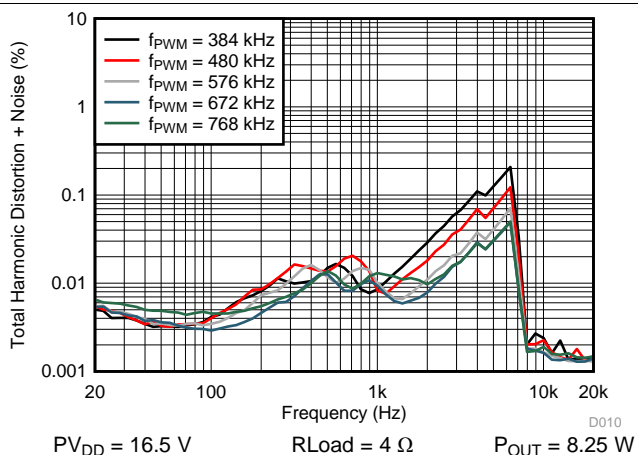
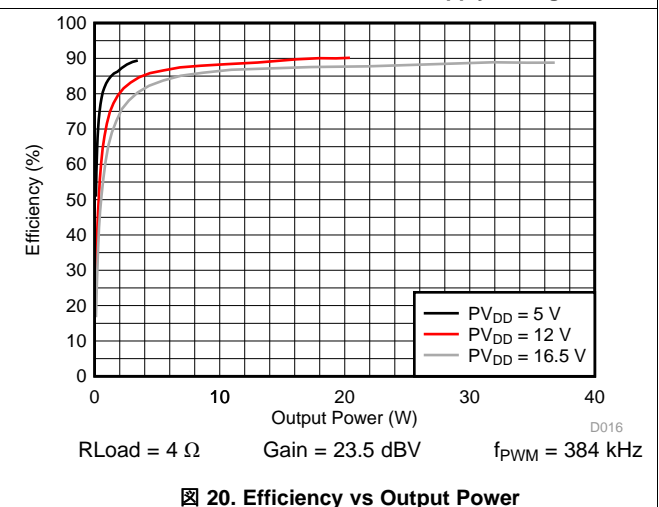
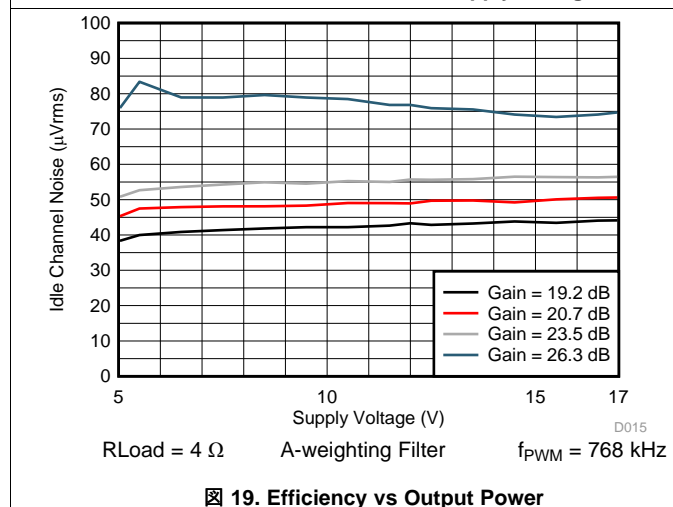
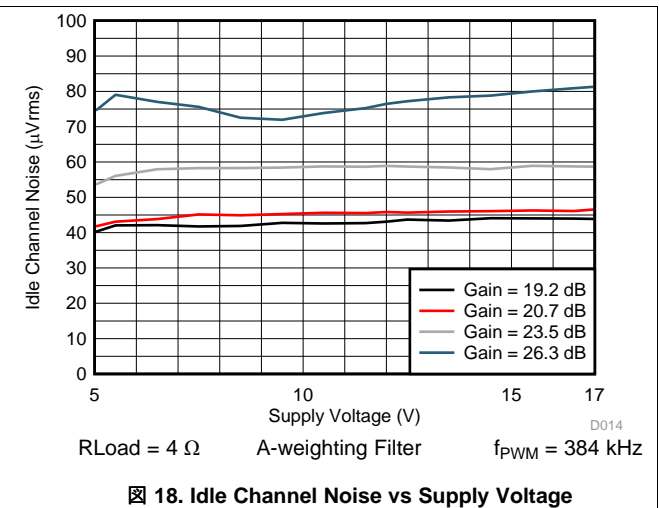
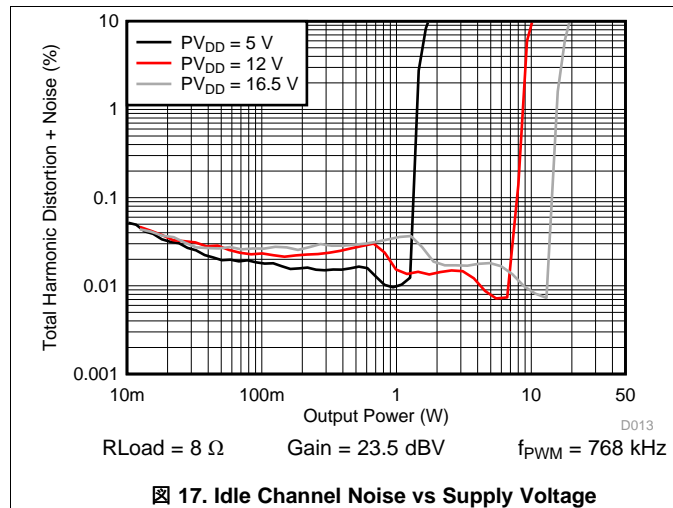
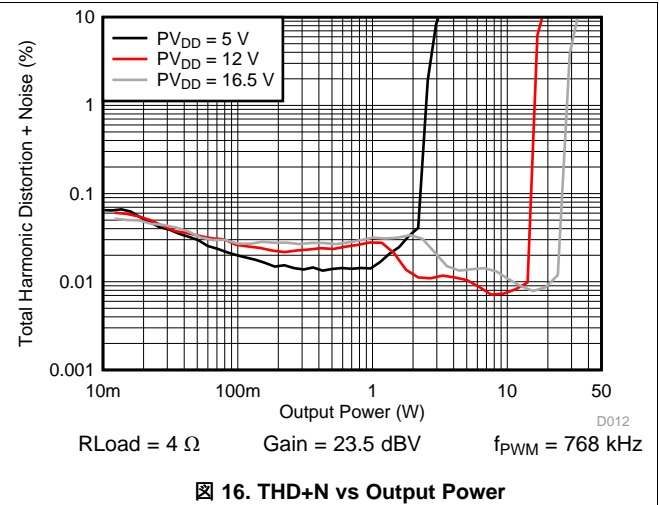
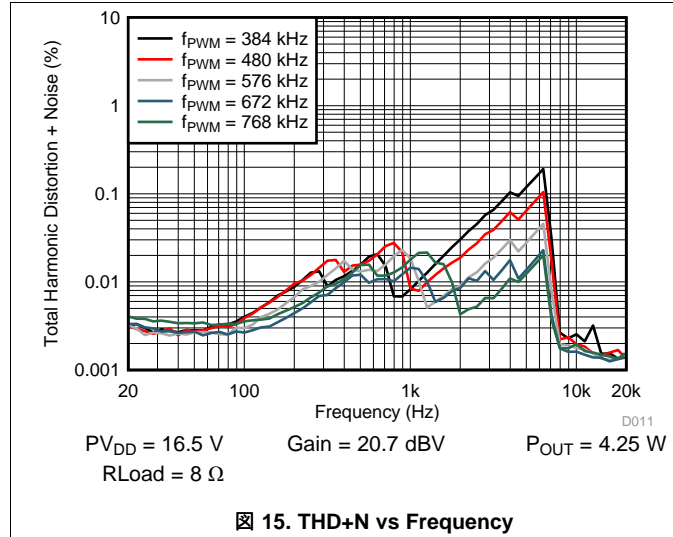


图 14. THD+N vs Frequency

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $f_{IN} = 1\text{ kHz}$ ,  $f_{PWM} = 768\text{ kHz}$ ,  $f_s = 48\text{ kHz}$ , Gain = 20.7 dBV, SDZ = 1, Measured using TAS5722LEVM with an Audio Precision SYS-2722 and AUX-0025 filter with 22-Hz-to-20-kHz un-weighted bandwidth using the 20-kHz pre-analyzer filter + 20-kHz brick-wall filter (unless otherwise specified). 33  $\mu\text{H}$  inductors were added in series with 4  $\Omega$  loads and 68  $\mu\text{H}$  inductors were placed in series with 8  $\Omega$  loads due to the ferrite bead filters.



## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $f_{IN} = 1\text{ kHz}$ ,  $f_{PWM} = 768\text{ kHz}$ ,  $f_s = 48\text{ kHz}$ , Gain = 20.7 dBV, SDZ = 1, Measured using TAS5722LEVM with an Audio Precision SYS-2722 and AUX-0025 filter with 22-Hz-to-20-kHz un-weighted bandwidth using the 20-kHz pre-analyzer filter + 20-kHz brick-wall filter (unless otherwise specified). 33  $\mu\text{H}$  inductors were added in series with 4  $\Omega$  loads and 68  $\mu\text{H}$  inductors were placed in series with 8  $\Omega$  loads due to the ferrite bead filters.

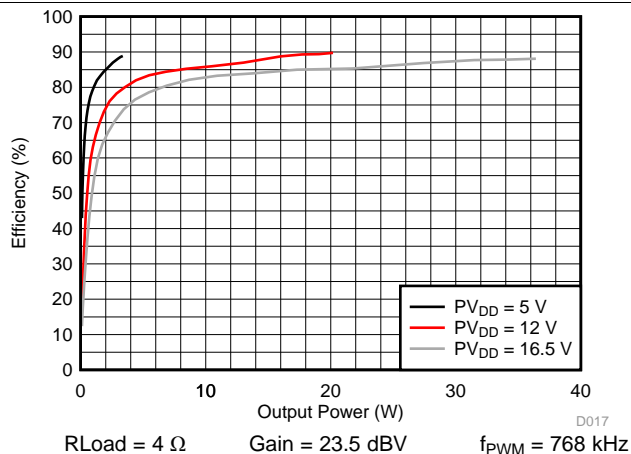


Figure 21. Efficiency vs Output Power

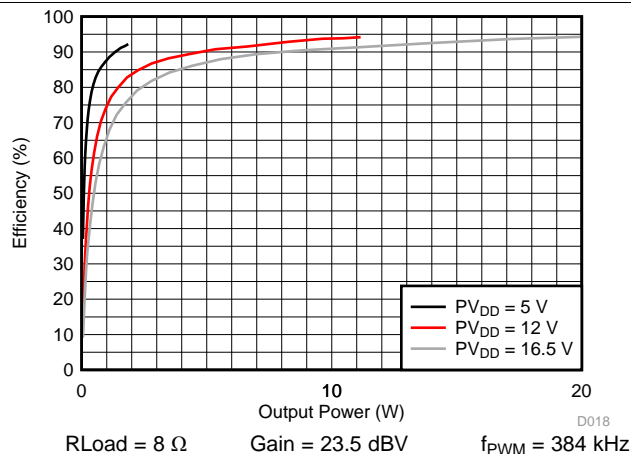


Figure 22. Efficiency vs Output Power

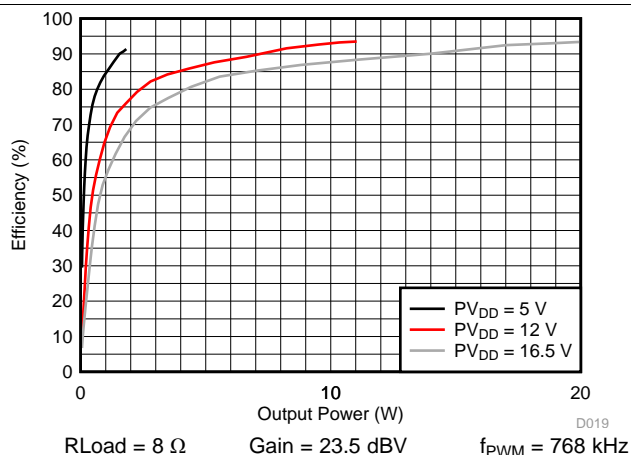


Figure 23.  $PV_{DD}$  PSRR vs Frequency

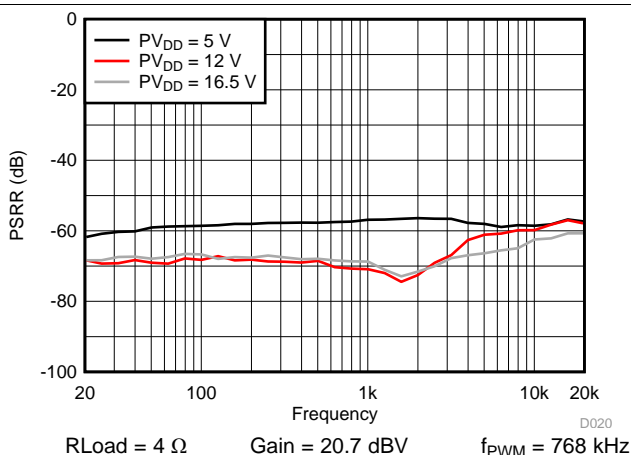


Figure 24.  $DV_{DD}$  PSRR vs Frequency

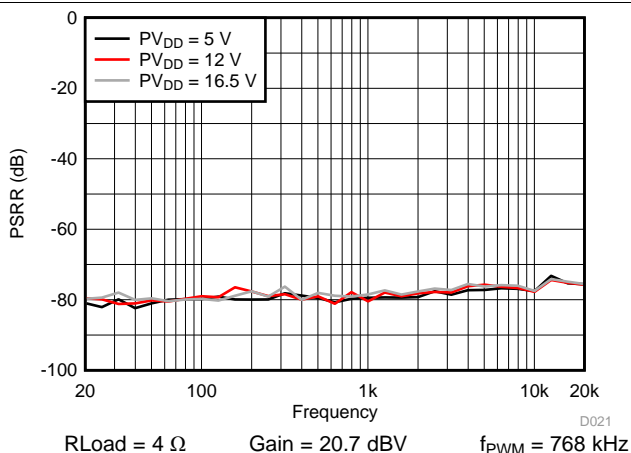


Figure 25. Idle Current vs Supply Voltage

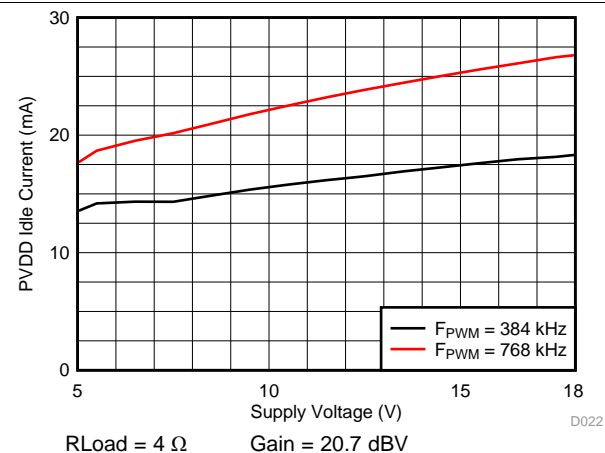


Figure 26. Shutdown Current vs Supply Voltage

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_{D\text{VDD}} = 1.8\text{ V}$ ,  $f_{\text{IN}} = 1\text{ kHz}$ ,  $f_{\text{PWM}} = 768\text{ kHz}$ ,  $f_s = 48\text{ kHz}$ , Gain = 20.7 dBV, SDZ = 1, Measured using TAS5722LEVMM with an Audio Precision SYS-2722 and AUX-0025 filter with 22-Hz-to-20- kHz un-weighted bandwidth using the 20- kHz pre-analyzer filter + 20- kHz brick-wall filter (unless otherwise specified). 33  $\mu\text{H}$  inductors were added in series with 4  $\Omega$  loads and 68  $\mu\text{H}$  inductors were placed in series with 8  $\Omega$  loads due to the ferrite bead filters.

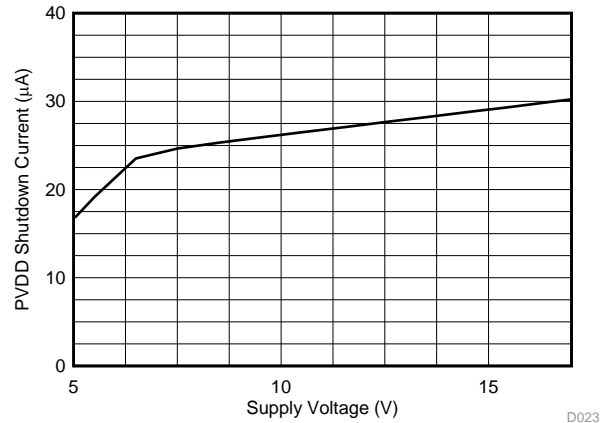


图 27. PVDD Shutdown Current vs Supply Voltage

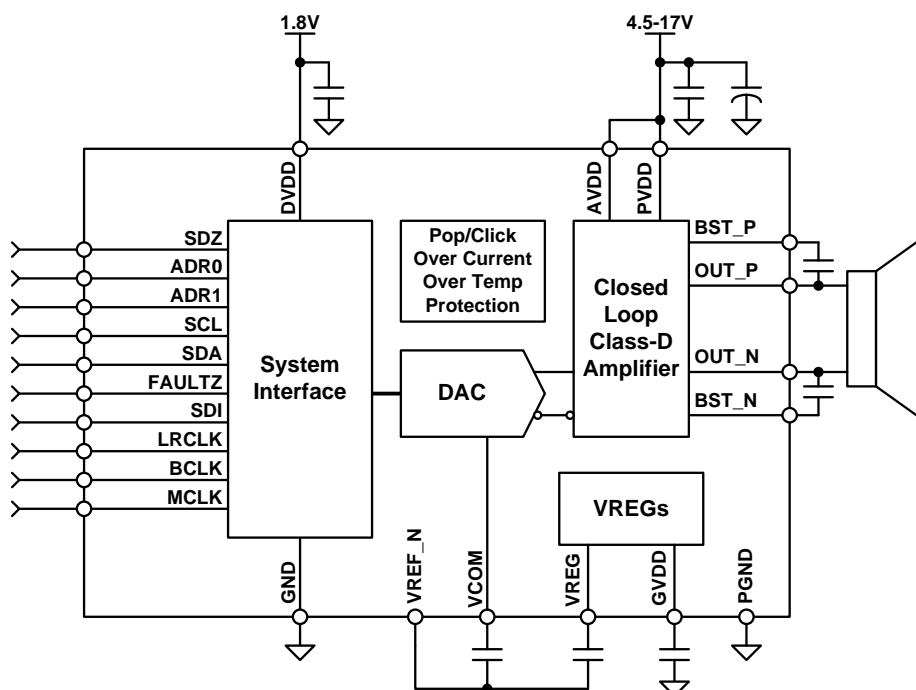


## 7 Detailed Description

### 7.1 Overview

The TAS5722L device is a high-efficiency mono Class-D audio power amplifier optimized for high-transient power capability to utilize the dynamic power headroom of small loudspeakers. The TAS5722L device is capable of delivering more than 14 W continuously into a 4-Ω speaker.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Adjustable I<sup>2</sup>C Address

The TAS5722L device has two address pins, which allow up to 8 I<sup>2</sup>C addressable devices to share a common TDM bus. 表 1 lists each I<sup>2</sup>C Device ID setting.

注

The I<sup>2</sup>C Device ID is the 7 most significant bits of the 8-bit address transaction on the bus (with the read/write bit being the least significant bit). For example, a Device ID of 0x6C would be read as 0xD8 when the read/write bit is 0.

表 1. I<sup>2</sup>C Device Identifier (ID) Generation

ADR1	ADR0	I2C_DEV_ID	DEFAULT TDM SLOT
Short to GND	Short to GND	0x6C	0
	22-kΩ to GND	0x6D	1
	22-kΩ to DVDD	0x6E	2
	Short to DVDD	0x6F	3

**表 1. I<sup>2</sup>C Device Identifier (ID) Generation (continued)**

ADR1	ADR0	I2C_DEV_ID	DEFAULT TDM SLOT
22-kΩ to GND	Short to GND	0x70	4
	22-kΩ to GND	0x71	5
	22-kΩ to DVDD	0x72	6
	Short to DVDD	0x73	7

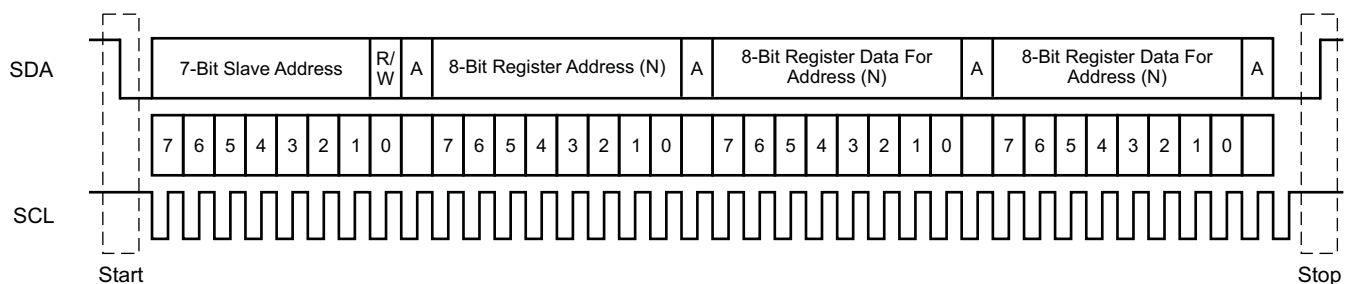
Use a 22-kΩ resistor with a 5% (or better) tolerance as a pull-up or pull-down resistor. By default, the device uses the TDM time slot equal to its offset from the base I<sup>2</sup>C Device ID (see 表 1). The TDM slot can also be manually configured by setting the TDM\_CFG\_SRC bit high (bit 6, reg 0x02) and programming the TDM\_SLOT\_SELECT[3:0] bits to the desired slot (bits 0-3, reg 0x03).

For 2-channel, I<sup>2</sup>S operation, TDM slot 0 and 1 correspond to the right and left channels respectively. For left and right justified formats, TDM slot 0 and 1 correspond to left and right channels respectively.

### 7.3.2 I<sup>2</sup>C Interface

The TAS5722L device has a bidirectional I<sup>2</sup>C interface that is compatible with the Inter-Integrated Circuit (I<sup>2</sup>C) bus protocol and supports both 100 kHz and 400 kHz data transfer rates. The slave-only device does not support a multi-master bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock (SCL) is "HIGH" to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in 图 28. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5722L device holds SDA "LOW" during the acknowledge clock period to indicate an acknowledgment. When the hold occurs, the master transmits the next byte of the sequence. All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the "HIGH" level for the bus.



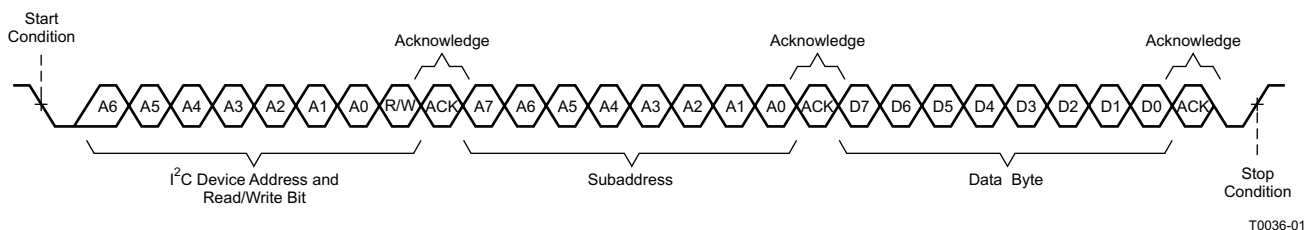
T0035-01

**图 28. Typical I<sup>2</sup>C Timing Sequence**

The number of bytes that can be transmitted between start and stop conditions is unlimited. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in 图 28.

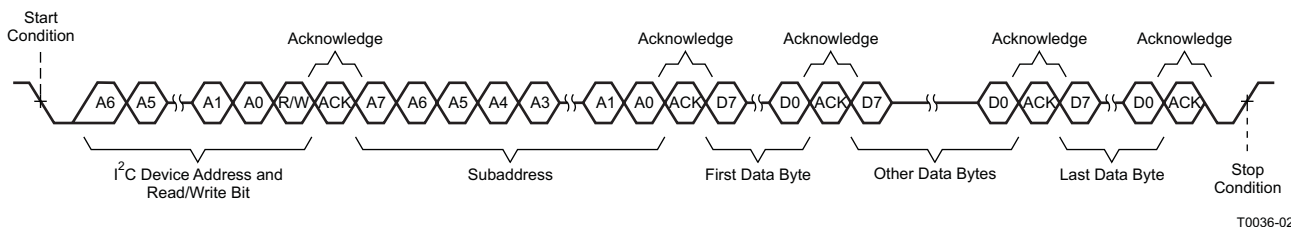
### 7.3.2.1 Writing to the I<sup>2</sup>C Interface

As shown in Figure 29, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C bit and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I<sup>2</sup>C bit and the read/write bit, the TAS5722L device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the TAS5722L device register being accessed. After receiving the address byte, the TAS5722L device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5722L device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.



**Figure 29. Single Byte Write Transfer Timing**

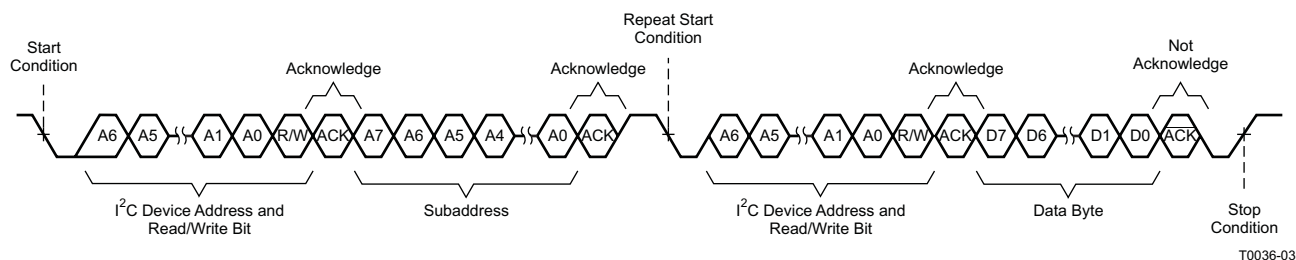
A multi-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted as shown in Figure 30. After receiving each data byte, the TAS5722L device responds with an acknowledge bit. Sequential data bytes are written to sequential addresses.



**Figure 30. Multi-Byte Write Transfer Timing**

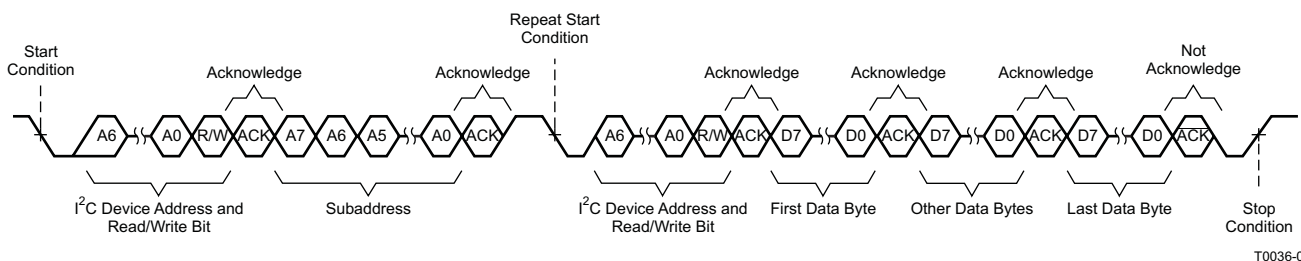
### 7.3.2.2 Reading from the I<sup>2</sup>C Interface

As shown in [Figure 30](#), a data-read transfer begins with the master device transmitting a start condition, followed by the I<sup>2</sup>C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal register to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5722L device address and the read/write bit, TAS5722L device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5722L device address and the read/write bit again. Then the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5722L device again responds with an acknowledge bit. Next, the TAS5722L device transmits the data byte from the register being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the data-read transfer.



**Figure 31. Single Byte Read Transfer Timing**

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5722L to the master device as shown in [Figure 32](#). Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.



**Figure 32. Multi-Byte Read Transfer Timing**

### 7.3.3 Serial Audio Interface (SAIF)

The TAS5722L device SAIF supports a variety of standard stereo serial audio formats including I<sup>2</sup>S, Left Justified and Right Justified. It also supports a time division multiplexed (TDM) format that is capable of transporting up to 8 channels of audio data on a single bus. LRCLK and SDIN are sampled on the rising edge of BCLK.

For the stereo formats (I<sup>2</sup>S, Left Justified and Right Justified), the TAS5722L device supports BCLK to LRCLK ratios of 32, 48 and 64. If the BCLK to LRCLK ratio is 64, MCLK can be derived from BCLK internally. The MCLK\_PIN\_CFG bit (register 0x13, bit 1) controls the source of MCLK and by default derives MCLK from an internal version of BCLK. In this case connect the MCLK pin to a valid logic low value.

If the BCLK to LRCLK ratio is 32 or 48, MCLK must be externally driven. The valid MCLK to LRCLK ratios are 64, 128, 256 and 512 as long as the frequency of MCLK is 37 MHz or less. If the BCLK to LRCLK ratio is 64, it is also acceptable to connect BCLK to MCLK and set the MCLK\_PIN\_CFG bit high.

For TDM operation, the TAS5722L device supports 4 and 8 times slots at both single speed (44.1 kHz or 48 kHz) and double speed (88.2/96 kHz) sample rates. 表 2 lists the supported TDM frame configurations. For 16 and 32-bits per TDM slot, MCLK can be connected to BCLK internally by leaving the MCLK\_PIN\_CFG bit (register 0x13, bit 1) to its default value of 0. For 24-bit time slot operation, MCLK must be externally driven with a valid ratio of 64, 128, 256 or 512 as long as MCLK is less than 37 MHz.

**表 2. TDM Frame Configurations**

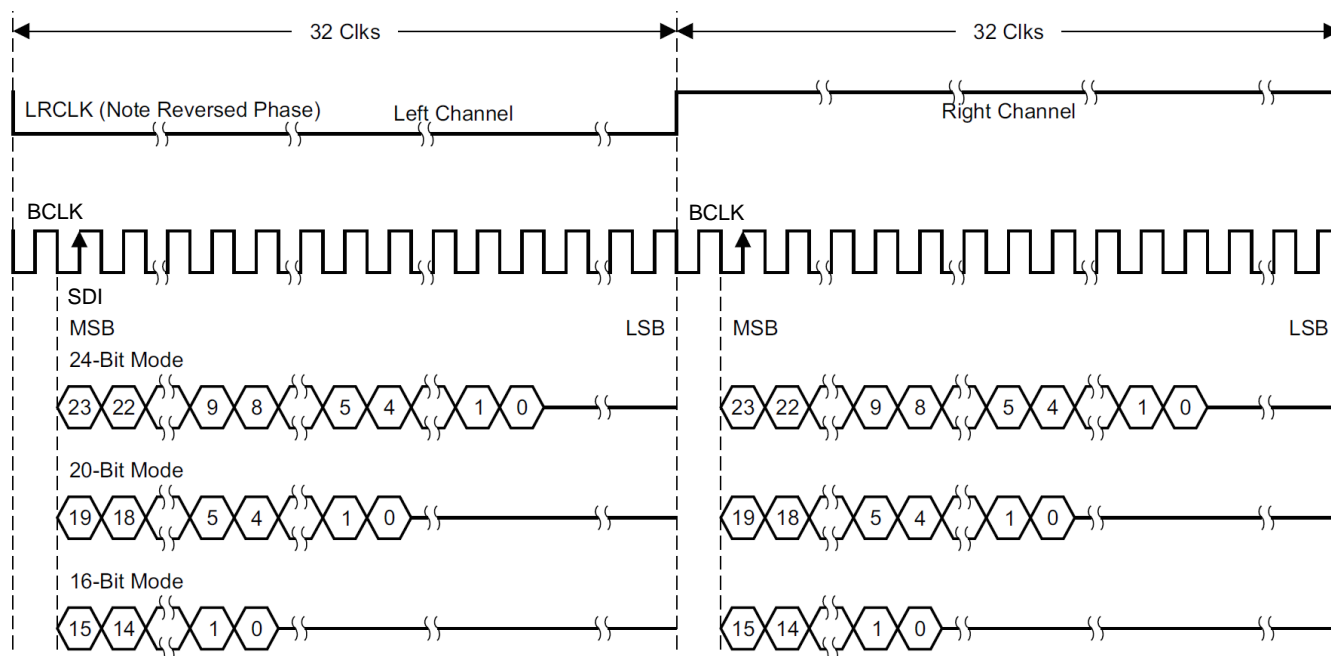
SAMPLE RATE (kHz)	TDM SLOTS	BITS PER TDM SLOT	SUPPORTED	MCLK = BCLK	TDM_SLOT_16B
44.1/48	4	16	Yes	Yes	1
		24	Yes	No	0
		32	Yes	Yes	0
	8	16	Yes	Yes	1
		24	Yes	No	0
		32	Yes	Yes	0
88.2/96	4	16	Yes	Yes	1
		24	Yes	No	0
		32	Yes	Yes	0
	8	16	Yes	Yes	1
		24	Yes	No	0
		32	Yes	Yes	0

If 16-bit time slots are utilized, set the TDM\_SLOT\_16B register bit (register 0x13, bit 2) to a 1. The SAIF auto detects 24-bit vs. 32-bit time slot widths if TDM\_SLOT\_16B is set to a 0.

The TAS5722L device selects the channel for playback based on either its I<sup>2</sup>C base address offset or based on a dedicated time slot selection register. See the [Adjustable I<sup>2</sup>C Address](#) section for more information.

### 7.3.3.1 Stereo I<sup>2</sup>S Format Timing

illustrates the timing of the stereo I<sup>2</sup>S format with 64 BCLK per LRCLK. Two's complement data is transmitted MSB to LSB with the left channel word beginning one BCLK after the falling edge of LRCLK and the right channel beginning one BCLK after the rising edge of LRCLK. Since data is MSB aligned to the beginning of word transmission, data precision does not need to be configured. Set the SAIF\_FORMAT[2:0] register bits to I<sup>2</sup>S (register 0x02, bits 2:0 = 3'b100).

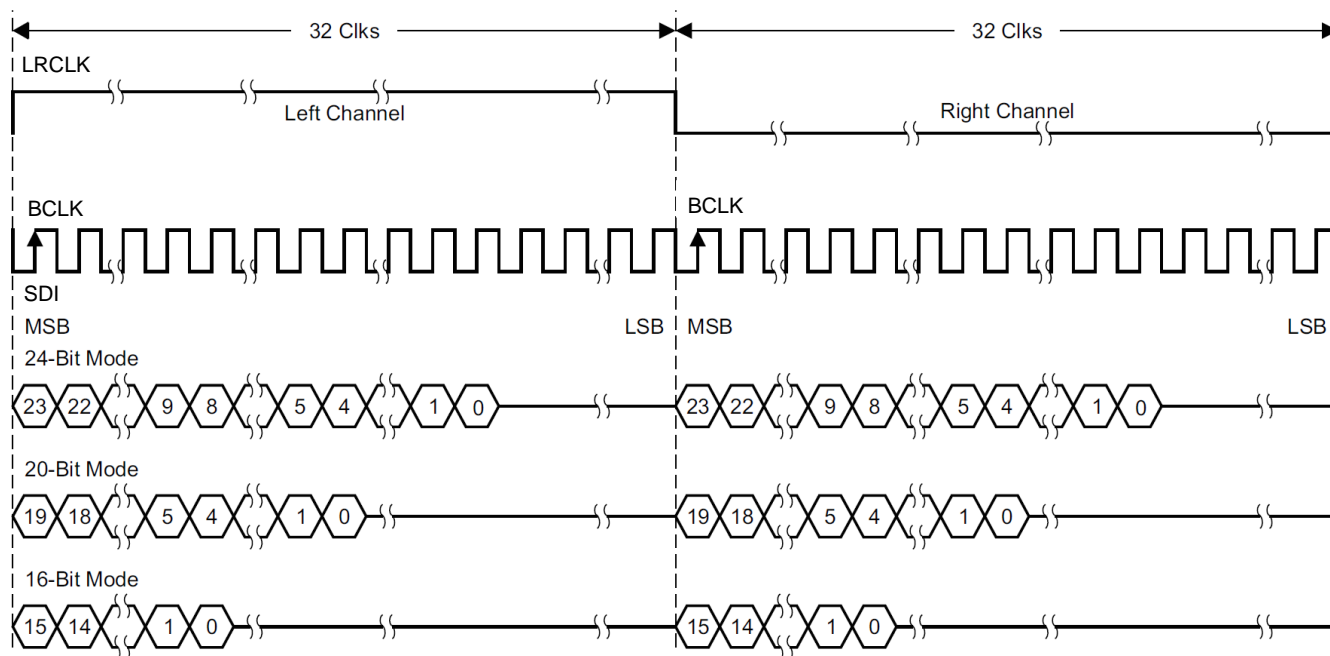


A. Data presented in two's-complement form with most significant bit (MSB) first.

**图 33. I<sup>2</sup>S 64-f<sub>s</sub> Format**

### 7.3.3.2 Stereo Left-Justified Format Timing

The stereo left justified format is very similar to the I<sup>2</sup>S format timing, except the data word begins transmission at the same cycle that LRCLK toggles (when it is shifted by one bit from I<sup>2</sup>S). The phase of LRCLK is also opposite of I<sup>2</sup>S. The left channel begins transmission when LRCLK transitions from low to high and the right channel begins transmission when LRCLK transitions from high-to-low. Set the SAIF\_FORMAT[2:0] register bits to left-justified (register 0x02, bits 2:0 = 3'b101). The timing is illustrated in .

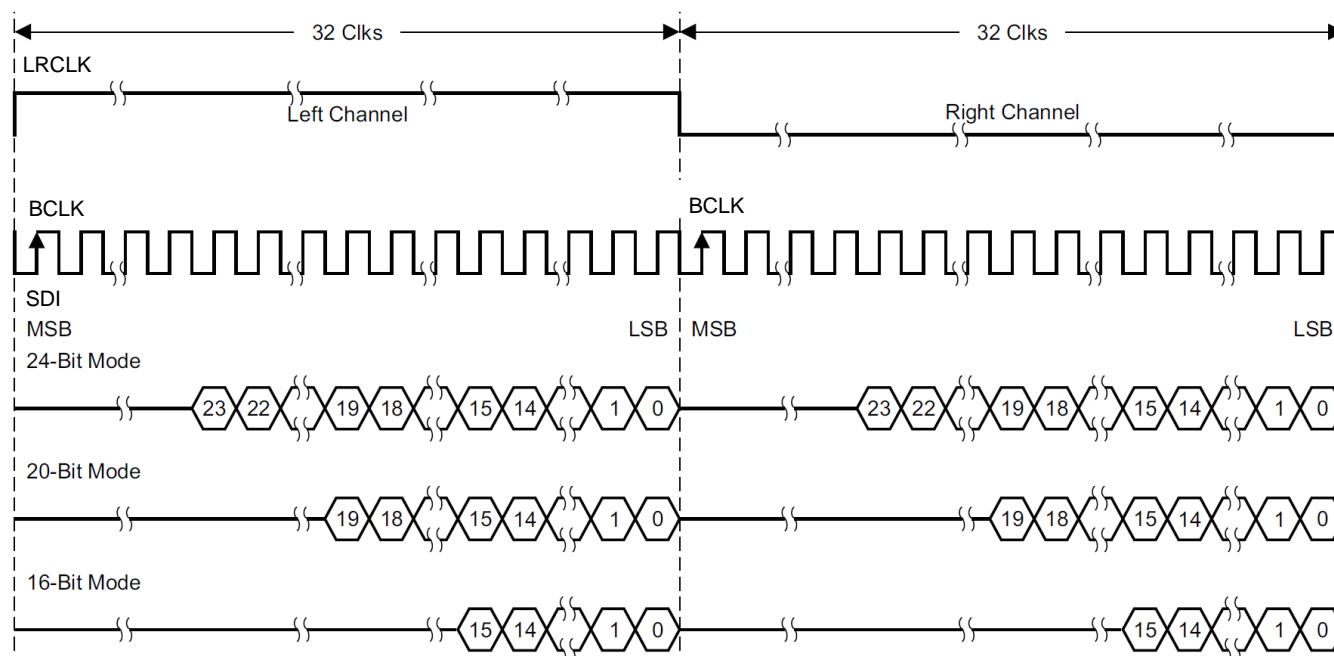


A. Data presented in two's-complement form with most significant bit (MSB) first.

**Figure 34. Left-Justified 64-f<sub>s</sub> Format**

### 7.3.3.3 Stereo Right-Justified Format Timing

The stereo right justified format aligns the LSB of left channel data to the high to low transition of LRCLK and the LSB of the right channel data to the low to high transition of LRCLK. To insure data is received correctly, the SAIF must be configured for the proper data precision. The TAS5722L supports 16, 18, 20 and 24-bit data precision in right justified format. Set the SAIF\_FORMAT[2:0] register bits (register 0x02, bits 2:0) to the appropriate right-justified setting based on bit precision (value = 3'b000 for 24-bit, 3'b001 for 20-bit, 3'b010 for 18-bit and 3'b011 for 16-bit). The timing is illustrated in .



✎ 35. Right-Justified 64-f<sub>s</sub> Format



### 7.3.3.4 TDM Format Timing

A TDM frame begins with the low to high transition of LRCLK. As long as LRCLK is high for at least one BCLK period and low for one BCLK period, duty cycle is irrelevant. The SAIF automatically detects the number of time slots as long as valid BCLK to LRCLK ratios are utilized (see SAIF introduction above).

For I<sup>2</sup>S aligned TDM operation (when time slot 0 begins, one clock cycle after the low to high transition of LRCLK), set SAIF\_FORMAT[2:0] register bits to I<sup>2</sup>S (register 0x02, bits 2:0 = 3'b100). Data is MSB aligned within the 32-bit time slots, so data precision does not need to be configured. The TDM format timing is illustrated in .

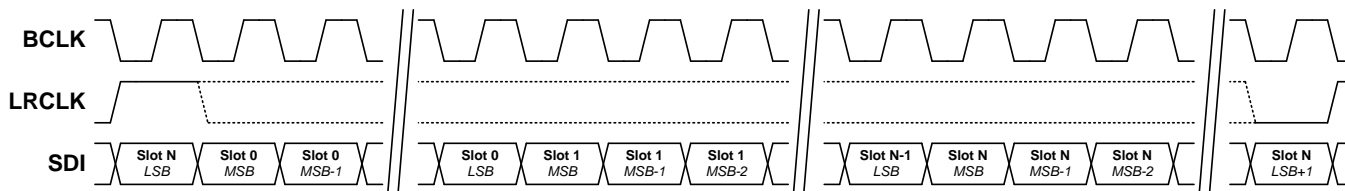


图 36. TDM I<sup>2</sup>S Format

For left-justified TDM operation (when time slot 0 begins the cycle LRCLK transitions from low to high), set SAIF\_FORMAT[2:0] register bits to left-justified(register 0x02, bits 2:0 = 3'b101). As with I<sup>2</sup>S, data is MSB aligned. The timing is illustrated in .

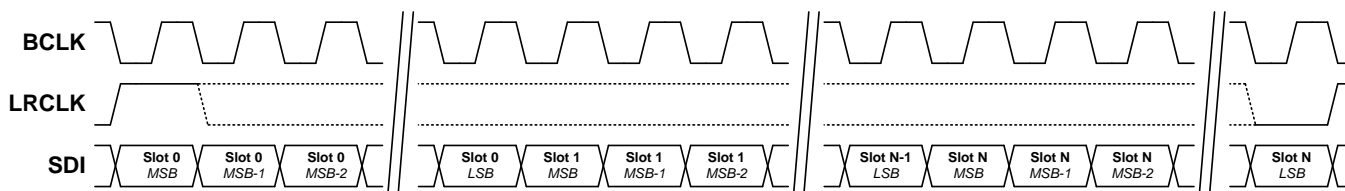


图 37. TDM Left- and Right-Justified Format

For right-justified TDM operation (when time slot 0 begins the cycle LRCLK transitions from low to high), data is LSB aligned to the 32-bit time slot. As with stereo right-justified formats, the TAS5722L must have the data precision configured. Set the SAIF\_FORMAT[2:0] register bits (register 0x02, bits 2:0) to the appropriate right-justified setting based on bit precision (value = 3'b000 for 24-bit, 3'b001 for 20-bit, 3'b010 for 18-bit and 3'b011 for 16-bit). The timing shown in is the same as left-justified TDM, with the data LSB aligned.

### 7.3.4 Audio Signal Path

illustrates the audio signal flow from the TDM SAIF to the speaker.

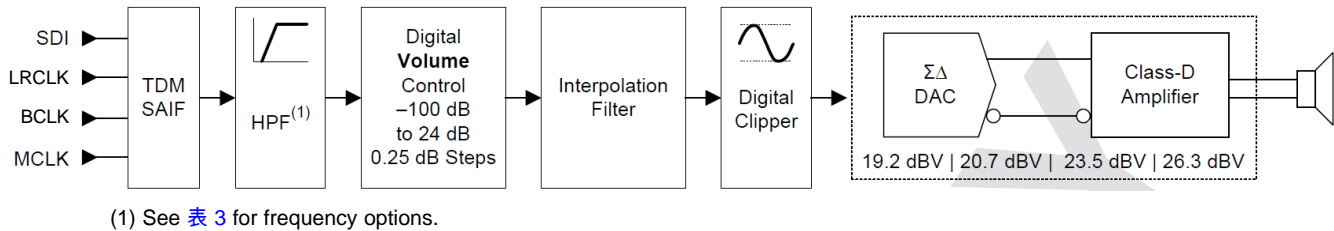


图 38. Audio Signal Path

#### 7.3.4.1 High-Pass Filter (HPF)

Excessive DC in audio content can damage loudspeakers, so the amplifier employs a DC detect circuit that shuts down the power stage and issues a latching fault if this condition occurs. A high-pass filter is provided in the TAS5722L device to remove DC from incoming audio data to prevent this from occurring. 表 3 shows the high-pass, –3 dB corner frequencies for each sample rate. The filter can be bypassed by writing a 1 into bit 7 of register 0x02. The high pass corner frequency can be adjusted by setting the HPF\_CORNER bits in the Digital Control 3 register (B[5:7], register 0x13).

表 3. High-Pass Filter –3 dB Corner Frequencies by Sample Rate

SAMPLE RATE (kHz)	-3dB CORNER FREQUENCY (Hz) vs. HPF_CORNER [2:0]							
	000	001	010	011	100	101	110	111
44.1	3.675	7.35	14.7	29.4	58.8	117.6	235.2	470.4
48	4	8	16	32	64	128	256	512
88.2	7.35	14.7	29.4	58.8	117.6	235.2	470.4	940.8
96	8	16	32	64	128	256	512	1024

#### 7.3.4.2 Amplifier Analog Gain and Digital Volume Control

The gain from TDM SAIF to speaker is controlled by setting the amplifier's analog gain and digital volume control. Amplifier analog gain settings are presented as the output level in dBV (dB relative to 1 Vrms) with a full scale serial audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only.

表 4 outlines each gain setting expressed in dBV and  $V_{PK}$ .

表 4. Amplifier Gain Settings

ANALOG_GAIN [1:0] SETTING	FULL SCALE OUTPUT	
	dBV	$V_{PEAK}$ (V)
00	19.2	12.9
01	20.7	15.3
10	23.5	21.2
11	26.3	29.2

式 1 calculates the amplifiers output voltage.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \text{ dBV}$$

where

- $V_{AMP}$  is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- $A_{dvc}$  is the digital volume control setting, –100 dB to 24dB in 0.25-dB steps
- $A_{AMP}$  is the amplifier analog gain setting (19.2, 20.7, 23.5, or 26.3) in dBV

(1)

Clipping in the digital domain occurs if the input level (in dB relative to 0 dBFS) plus the digital volume control setting (in dB) are greater than 0 dB. The signal path has approximately 0.5 dB of headroom, but TI does not recommend utilizing it.

The digital volume control (DVC) can be adjusted from –100 dB to 24 dB in 0.25-dB steps. 式 2 illustrates how to set the 9-bit volume control bits. The top 8 MSBs of the DVCvalue are stored in Volume Control register (register 0x04) and the LSB is stored in the Digital Control 3 register (register 0x13, bit 0).

$$DVC_{\text{value}} = 0x19E + \frac{A_{\text{dvc}}}{0.25} \quad (2)$$

For example, digital volume settings of 0 dB, 24 dB and –100 dB map to 0x19E, 0x1FE and 0x0E respectively. Values below 0x0E are equivalent to mute (the amplifier continues to switch with no audio). When a change in digital volume control occurs, the device ramps the volume to the new setting in 0.25 dB steps either every LRCLK or every 8 LRCLK depending on the value of the VOL\_RAMP\_RATE bit (bit 6, reg 0x03).

The Class-D amplifier uses a closed-loop architecture, so the gain does not depend on the supply input ( $V_{\text{PVDD}}$ ). The approximate threshold for the onset of analog clipping is calculated in 式 3.

$$V_{\text{PK(max,preclip)}} = V_{\text{PVDD}} \times \left( \frac{R_L}{2 \times R_{\text{DS(on)}} + R_{\text{interconnect}} + R_L} \right) V$$

where

- $V_{\text{PK(max,preclip)}}$  is the maximum peak unclipped output voltage in V
- $V_{\text{PVDD}}$  is the power supply voltage
- $R_L$  is the speaker load in  $\Omega$
- $R_{\text{interconnect}}$  is the additional resistance in the PCB (such as cabling and filters) in  $\Omega$
- $R_{\text{DS(on)}}$  is the power stage total on resistance (FET+bonding+packaging) in  $\Omega$

The effective on-resistance for the device (including FETs, bonding and packaging leads) is approximately 150 m $\Omega$  at room temperature and increases by approximately 1.6 times over +100°C rise in temperature.表 5 shows approximate maximum unclipped peak output voltages at room temperature (excluding interconnect resistances).

**表 5. Approximate Maximum Unclipped Peak Output Voltage at Room Temperature**

SUPPLY VOLTAGE $V_{\text{PVDD}}$ (V)	MAXIMUM UNCLIPPED PEAK VOLTAGE $V_{\text{PK}}$ (V)	
	$R_L = 4 \Omega$	$R_L = 8 \Omega$
12	11.16	11.57
17	15.81	16.39

### 7.3.4.3 Digital Clipper

The digital clipper hard limits the maximum DAC sample value, which provides a simple hardware mechanism to control the largest signal applied to the speaker. Because the block resides in the digital domain, the actual maximum output voltage also depends on the amplifier gain setting and the supply voltage ( $V_{\text{PVDD}}$ ) limited amplifier voltage swing (For example, analog clipping may occur before digital clipping).

The maximum amplifier output voltage (excluding limitation due to swing) is calculated in 式 4.

$$V_{\text{AMP(max,dc)}} = 20 \times \log_{10} \left( \frac{DC_{\text{level}}}{0xFFFFF} \right) + 0.5 + A_{\text{AMP}}$$

where

- $V_{\text{AMP(max,dc)}}$  is the amplifier maximum output voltage in dBV
- $DC_{\text{level}}$  is the digital clipper level
- $A_{\text{AMP}}$  is the amplifier analog gain setting (19.2, 20.7, 23.5, or 26.3) in dBV

Configure the digital clipper by writing the 20-bit  $DC_{\text{level}}$  to registers 0x01, 0x10 and 0x11. Set the  $DC_{\text{level}}$  to 0xFFFFF effectively bypasses the digital clipper.

### 7.3.4.4 Class-D Amplifier Settings

The PWM switching rate of the Class-D amplifier is a phase locked multiple of the input audio sample rate. 表 6 lists the PWM switching rate settings as programmed in bit 4 through bit 6 in register 0x06. The double-speed sample rates (for example 88.2 kHz, 96 kHz) have the same PWM switching frequencies as their equivalent single-speed sample rates.

**表 6. PWM Switching Rates**

PWM_RATE [2:0]	SINGLE-SPEED PWM RATE ( $\times f_{LRCLK}$ )	DOUBLE-SPEED PWM RATE $\times f_{LRCLK}$	44.1 kHz, 88.2 kHz $f_{PWM}(kHz)$	48 kHz, 96 kHz $f_{PWM}(kHz)$
000	6	3	264.6	288
001	8	4	352.8	384
010	10	5	441	480
011	12	6	529.2	576
100	14	7	617.4	672
101	16	8	705.6	768
110	20	10	882	960
111	24	12	1058.4	1152

The Class-D power stage overcurrent detector issues a latching fault if the load current exceeds the safe limit for the device. This threshold can be proportionately adjusted if desired by programming bits 4-5 of register 0x08. 表 7 shows the relative setting for each overcurrent setting.

**表 7. Overcurrent Threshold Settings**

OC_THRESH [1:0]	OVERCURRENT THRESHOLD (%)
00	100
01	75
10	50
11	25

## 7.4 Device Functional Modes

This section describes the modes of operation for the TAS5722L device.

**表 8. Typical Current Consumption<sup>(1)</sup>**

INPUT VOLTAGE $V_{PVDD}$ (V)	MODE	PWM FREQUENCY $f_{PWM}$ (kHz)	$I_{PVDD}+I_{AVDD}$ (mA)	INPUT CURRENT $I_{DVDD}$ (mA)
5	Idle and Mute	384	11.45	1.30
		480	12.21	
		576	12.94	
		672	13.70	
		768	14.41	
	Sleep	—	8.48	0.32
	Shutdown	—	0.021	0.046
12.5	Idle and Mute	384	13.06	1.30
		480	14.46	
		576	15.79	
		672	17.18	
		768	18.49	
	Sleep	—	7.49	0.32
	Shutdown	—	0.042	0.046
16.5	Idle and Mute	384	14.00	1.30
		480	15.60	
		576	17.10	
		672	18.66	
		768	20.15	
	Sleep	—	7.61	0.32
	Shutdown	—	0.045	0.046

(1)  $T_A = 25^\circ\text{C}$ , PVDD pin tied to AVDD pin,  $V_{DVDD} = 1.8\text{ V}$ ,  $R_{LOAD} = 4\Omega + 33\text{ }\mu\text{H}$ ,  $f_{IN} = \text{Idle}$ ,  $f_S = 48\text{ kHz}$ , Gain = 20.7 dBV, PWR\_TUNE bit = 1

### 7.4.1 Shutdown Mode (SDZ)

The device enters shutdown mode if either the SDZ pin is asserted low or the I<sup>2</sup>C SDZ register bit is set low (bit 0, reg 0x01). In shutdown mode, the device consumes the minimum quiescent current with most analog and digital blocks powered down. The Class-D amplifier power stage powers down and the output pins are in a Hi-Z state. I<sup>2</sup>C communication remains possible in shutdown mode and register bits states are retained.

If a latching fault condition has occurred (Over Temperature, Over Current or DC detect), the SDZ pin or I<sup>2</sup>C bit must toggle low before the fault register can be cleared. For more information on faults and recovery, see the [Faults and Status](#) section.

When the device exits shutdown mode (either by releasing the SDZ pin high or setting the I<sup>2</sup>C SDZ register bit high), the device powers up the internal analog and digital blocks required for operation. If the I<sup>2</sup>C SLEEP bit is set low (bit 1, reg 0x01), the device powers up the Class-D amplifier and begins the switching of the power stage. If the I<sup>2</sup>C MUTE bit is set low (bit 4, reg 0x03), the device ramps up the volume to the current setting and begins playing audio.

If shutdown mode is asserted while audio is playing, the device ramps down the volume on the audio, stops the Class-D switching, puts the Class-D power stage output pins in a Hi-Z state and powers down the analog and digital blocks.

### 7.4.2 Sleep Mode

Sleep mode is similar to shutdown mode, except analog and digital blocks required to begin playing audio quickly remain powered up. Sleep mode operates as a *hard mute* where the Class-D amplifier stops switching, but the device does not power down completely. Entering sleep mode does not clear latching faults.

### 7.4.3 Mode Timing

When SDZ is deasserted (and the device is not in sleep mode), the amplifier begins to switch after a period of  $t_{\text{ACTIVE}}$ . At this point, the volume ramps from –100 dB to the programmed digital volume control (DVC) setting in a length of time  $t_{\text{VRMP}}$ .  $t_{\text{VRMP}}$  is determined by the DVC setting, sample rate and volume ramp rate bit, VOL\_RAMP\_RATE (bit 6 of register 0x03). Ramping the volume prevents audible artifacts that can occur if discontinuous volume changes are applied while audio is being played back. This period,  $t_{\text{VRMP}}$ , depends on the DVC setting and sample rate. Typical values for  $t_{\text{VRMP}}$  for a DVC of 0 dB are shown in [Timing Requirements](#). [Figure 4](#) illustrates mode timing.

The time to enter or exit sleep or mute and the time to enter shutdown are dominated by  $t_{\text{VRMP}}$ . [Table 9](#) lists the timing parameters based on  $t_{\text{VRMP}}$ .

**表 9. Typical DVC Ramp Times**

SAMPLE RATE (kHz)	RAMP TIMES ( $t_{\text{VRMP}}$ ) FROM –100 dB to 0 dB (ms)	
	VOL_RAMP_RATE = 0	VOL_RAMP_RATE = 1
44.1	72.6	9.1
48	66.7	8.3
88.2	36.3	4.5
96	33.3	4.2

### 7.4.4 Auto Sleep Mode

Auto sleep mode is an optional feature that automatically moves the amplifier from active mode to sleep mode when the device presents an idle audio input (i.e. zero value) to the SAIF for a prescribed number of samples. The device automatically returns to active mode when the device presents a non-idle audio input sample to the SAIF. Auto sleep mode takes advantage of the TAS5722L device's ability to rapidly enter and exit sleep mode from active mode. Because the device applies idle audio samples to the SAIF before entering sleep mode, a volume ramp can be avoided. When exiting sleep mode, the amplifier can resume switching before input sample has propagated through the signal path, which avoids any audible artifacts when resuming playback. AUTO\_SLEEP[1:0] (bits 4:3 in register 0x13) configures the number of idle samples required to enter auto sleep.

### 7.4.5 Active Mode

If shutdown mode and sleep mode are not asserted, the device is in active mode. During active mode, audio playback is enabled.

### 7.4.6 Mute Mode

When the I<sup>2</sup>C\_MUTE bit is set high (bit 4, reg 0x03) and the device is in active mode, the volume is ramped down and the Class-D amplifier continues to operate with an idle audio input.

### 7.4.7 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the DVDD pin domain releases all registers from reset (including the I<sup>2</sup>C registers) once DVDD is valid. The device does not exit shutdown mode until the PVDD pin has a valid voltage between the undervoltage lockout (UVLO) and overvoltage lockout (OVLO) thresholds. If DVDD drops below the POR threshold the device transitions into shutdown mode with all registers held in reset. If UVLO or OVLO thresholds are violated by PVDD, the device transitions into sleep mode, but registers are not forced into reset. Both of these conditions are non-latching and the device operates normally once supply voltages are valid again. The device can be reset only by reducing DVDD below the POR threshold.

The device transitions into sleep mode if it detects any faults with the SAIF clocks such as

- Invalid MCLK to LRCLK and BCLK to LRCLK ratios
- Invalid MCLK and LRCLK frequencies
- Halting of MCLK, BCLK or LRCLK clocks

Upon detection of a SAIF clock error, the device transitions into sleep mode as quickly as possible to limit the possibility of audio artifacts. Once all SAIF clock errors are resolved, the device volume ramps back to its previous playback state. During an SAIF clock error, the FAULTZ pin asserts low and the CLKE bit asserts high (register 0x08, bit 3).

While operating in shutdown mode, the SAIF clock error detect circuitry powers down and the CLKE bit reads high. This reading is not an indication of a SAIF clock error. If the device has not entered active mode after a power-up sequence or after transitioning out of shutdown mode, the FAULTZ pin pulses low for only approximately 10  $\mu$ s every 350  $\mu$ s. This action prevents a possible locking condition if the FAULTZ is connected to the SDZ pin to accomplish automatic recovery. Once the device has entered active mode one time (after power up or deassertion of shutdown mode), the SAIF clock errors pull the FAULTZ pin low continuously until the fault has cleared.

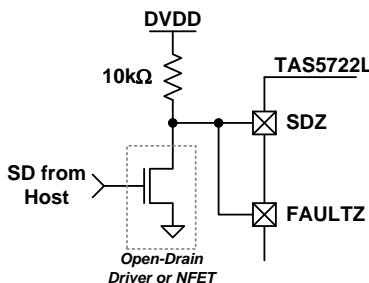
The device also monitors die temperature, power stage load current and amplifier output DC content and issues latching faults if any of these conditions occur. A die temperature of approximately 150°C causes the device to enter sleep mode and issue an over-temperature error (OTE) readable via I<sup>2</sup>C (bit 0, reg 0x08).

Sustained excessive DC content at the output of the Class-D amplifier can damage loudspeakers via voice coil heating. The amplifier has an internal circuit to detect significant DC content that forces the device into sleep mode. The device issues a DC detect error (DCE) readable via I<sup>2</sup>C (bit 1, reg 0x08).

If the Class-D amplifier load current exceeds the threshold set by the OC\_THRESH register bits (bits 5-4, reg 0x08), the device enters sleep mode and issues an overcurrent error (OCE) that is readable via I<sup>2</sup>C (bit 2, reg 0x08).

During OTE, DCE and OCE, the FAULTZ pin asserts low until the latched fault is cleared. FAULTZ is an open drain pin and requires a pull-up resistor to the DVDD pin to achieve a logic high level when no faults exist. This can be accomplished either with an internal pull up asserting FAULTZ\_PU high (register 0x14, bit 3) or with an external pull up resistor to DVDD.

Latched faults can be cleared only by toggling the SDZ pin or SDZ I<sup>2</sup>C bit (bit 0, reg 0x01). This toggle does not clear I<sup>2</sup>C registers (except the fault status of OTE, OCE and DCE). If it is desirable for the device to attempt automatic recovery after latching faults, implement a circuit like the one shown in . The device waits approximately 650 ms after a DCE fault has cleared and 1.3 s after an OTE or OCE fault has cleared before releasing FAULTZ high and allowing the device to enter active mode.



**39. Auto Recovery Circuit**

## 7.5 Register Maps

When writing to registers with reserved bits, maintain the values shown in 表 10 to ensure proper device operation. Default register values are loaded during the power-up sequence or any time the DVDD voltage falls below the power-on-reset (POR) threshold and then returns to valid operation.

**TAS5722L**

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**7.5.1 I<sup>2</sup>C Register Map Summary**
**表 10. I<sup>2</sup>C Register Map Summary**

ADDR (Dec)	ADDR (Hex)	REGISTER NAME	REGISTER BITS								DEFAULT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
0	0x00	Device ID	DEVICE_ID								0x12
			0	0	0	1	0	0	1	0	
1	0x01	Power Control	DIGITAL_CLIP_LEVEL [19:14]						SLEEP	SDZ	0xFD
			1	1	1	1	1	1	0	1	
2	0x02	Digital Control 1	HPF_BYPASS	TDM_CFG_SRC	RSV		SSZ/DS	SAIF_FORMAT			0x04
			0	0	0	0	0	1	0	0	
3	0x03	Digital Control 2	RSV	VOL_RAMP_RATE	RSV	MUTE	RSV	TDM_SLOT_SELECT[2:0]			0x80
			1	0	0	0	0	0	0	0	
4	0x04	Volume Control	VOLUME_CONTROL [8:1]								0xCF
			1	1	0	0	1	1	1	1	
6	0x06	Analog Control	RSV	PWM_RATE			ANALOG_GAIN		RSV		0x51
			0	1	0	1	0	0	0	1	
8	0x08	Fault Config and Error Status	RSV		OC_THRESH		CLKE	OCE	DCE	OTE	0x00
			0	0	0	0	0	0	0	0	
16	0x10	Digital Clipper 2	DIGITAL_CLIP_LEVEL[13:6]								0xFF
			1	1	1	1	1	1	1	1	
17	0x11	Digital Clipper 1	DIGITAL_CLIP_LEVEL[5:0]						RSV		0xFC
			1	1	1	1	1	1	0	0	
19	0x13	Digital Control 3	HPF_CORNER			AUTO_SLEEP		TDM_SLOT_16B	MCLK_PIN_CFG	VOL_CONTROL[0]	0x00
			0	0	0	0	0	0	0	0	
20	0x14	Analog Control 2	RSV				FAULTZ_P U	VREG_LVL	RSV	PWR_TUNE	0x02
			0	0	0	0	0	0	1	0	



## 7.5.2 Register Maps

### 7.5.2.1 Device Identification Register (0x00)

☒ 40. Device Identification Register

7	6	5	4	3	2	1	0
DEVICE_ID[7:0]							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. Device Identification Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID[7:0]	R	0	This register returns a value of 0x12 when read.

### 7.5.2.2 Power Control Register (0x01)

☒ 41. Power Control Register

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL[19:14]						SLEEP	SDZ
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. Power Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	DIGITAL_CLIP_LEVEL[19:14]	R/W	1	This register holds the top 6-bits of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the <a href="#">Digital Clipper</a> section for more information.
1	SLEEP	R/W	0	When the device enters SLEEP mode, volume ramps down and the Class-D output stage powers down to a Hi-Z state. The rest of the blocks maintain a state such that audio playback can be restarted as quickly as possible. This mode has lower dissipation than MUTE, but higher than SHUTDOWN. For more information see the <a href="#">Device Functional Modes</a> section. 0: Exit Sleep (default). 1: Enter Sleep.
0	SDZ	R/W	1	The device enters SHUTDOWN mode if either this bit is set to a 0 or the SDZ pin is pulled low externally. In SHUTDOWN, the device holds the lowest dissipation state. I <sup>2</sup> C communication remains functional and all registers are retained. For more information see the <a href="#">Device Functional Modes</a> section. 0: Enter SHUTDOWN. 1: Exit SHUTDOWN (default).

### 7.5.2.3 Digital Control Register 1 (0x02)

☒ 42. Digital Control Register 1

7	6	5	4	3	2	1	0
HPF_BYPASS	TDM_CFG_SRC	Reserved		SSZ/DS	SAIF_FORMAT[2:0]		
R/W	R/W	R/W		R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 13. Digital Control Register 1 Field Descriptions**

Bit	Field	Type	Reset	Description
7	HPF_BYPASS	R/W	0	The high-pass filter removes any DC component in the audio content that could trip the DC detect protection feature in the amplifier, which is a latching fault. Setting this bit bypasses the high-pass filter. See the "High-Pass Filter" section under "Audio Signal Path" for more information. 0: Enable high-pass filter (default). 1: Bypass high-pass filter.
6	TDM_CFG_SRC	R/W	0	This bit determines how the device selects which audio channel direct to the playback stream. See the <a href="#">Serial Audio Interface (SAIF)</a> section for more information. 0: Set TDM Channel to I <sup>2</sup> C Device ID (default). 1: Set TDM Channel to TDM_SLOT_SELECT in register 0x03.
5-4	Reserved	R/W	0	These bits are reserved and should be set to 00 when writing to this register.
3	SSZ/DS	R/W	0	This bit sets the sample rate to single speed or double speed operation. See the <a href="#">Serial Audio Interface (SAIF)</a> section for more information. 0: Single speed operation (44.1 kHz/48 kHz) - default. 1: Double speed operation (88.2 kHz/96 kHz)
2-0	SAIF_FORMAT[2:0]	R/W	100	These bits set the Serial Audio Interface format. See the <a href="#">Serial Audio Interface (SAIF)</a> section for more information. 000: Right justified, 24-bit 001: Right justified, 20-bit 010: Right justified, 18-bit 011: Right justified, 16-bit 100: I <sup>2</sup> S (default) 101: Left Justified, 16-24 bits 110: Reserved. Do not select this value. 111: Reserved. Do not select this value.

**7.5.2.4 Register Name (offset = ) [reset = ] or (address = ) [reset = ]**
**图 43. 8-bit, 1 Row**

7	6	5	4	3	2	1	0
Reserved	VOL_RAMP_RATE	Reserved	MUTE	Reserved	TDM_SLOT_SELECT[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 14. (For example, CONTROL\_REVISION Register) Field Descriptions**

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1	This bit is reserved and should be set to 1 when writing to this address
6	VOL_RAMP_RATE	R/W	0	This bit determines the volume ramp rate when entering or exiting Mute, Shutdown or Sleep 0: Ramp 0.25 dB every 8 LRCLK periods (default) 1: Ramp 0.25 dB every LRCLK period
5	Reserved	R/W	0	This bit is reserved and should be set to 1 when writing to this address

**表 14. (For example, CONTROL\_REVISION Register) Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
4	MUTE	R/W	0	When set the device ramps down volume and play idle audio. See the <a href="#">Amplifier Analog Gain and Digital Volume Control</a> section for more information. 0: Exit mute mode (default). 1: Enter mute mode.
3	Reserved	R/W	0	This bit is reserved and should be set to 0 when writing to this address
2-0	TDM_SLOT_SELECT[2:0]	R/W	0	When the TDM_CFG_SRC bit is set to 1 in register 0x02, these bits select which TDM channel is directed to audio playback. See the <a href="#">Serial Audio Interface (SAIF)</a> section for more information.

### 7.5.2.5 Volume Control Register (0x04)

**图 44. Volume Control Register**

7	6	5	4	3	2	1	0
VOLUME_CONTROL[8:1]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 15. Volume Control Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	VOLUME_CONTROL[8:1]	R/W	11001111	This register sets the top 8 bits of the 9-bit Digital Volume Control (DVC). The DVC ranges from –100 dB to +24 dB in 0.25 dB steps and has a default setting of 0 dB. Register settings of less than 0x008 are equivalent to MUTE. Register 0x13 bit 0 sets the LSB value. See the <a href="#">Amplifier Analog Gain and Digital Volume Control</a> for more information.

### 7.5.2.6 Analog Control Register (0x06)

**图 45. Analog Control Register**

7	6	5	4	3	2	1	0
Reserved	PWM_RATE[2:0]			ANALOG_GAIN[1:0]		Reserved	
R/W	R/W			R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 16. Analog Control Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	This bit is reserved and should be set to 0 when writing to this address
6-4	PWM_RATE[2:0]	R/W	101	These bits set the PWM switching rate, which is a locked ratio of LRCLK. For more information see the <a href="#">Class-D Amplifier Settings</a> section. 000: 6 × LRCLK (single speed), 3 × LRCLK (double speed) 001: 8 × LRCLK (single speed), 4 × LRCLK (double speed) 010: 10 × LRCLK (single speed), 5 × LRCLK (double speed) 011: 12 × LRCLK (single speed), 6 × LRCLK (double speed) 100: 14 × LRCLK (single speed), 7 × LRCLK (double speed) 101: 16 × LRCLK (single speed), 8 × LRCLK (double speed) - default 110: 20 × LRCLK (single speed), 10 × LRCLK (double speed) 111: 24 × LRCLK (single speed), 12 × LRCLK (double speed)

**表 16. Analog Control Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-2	ANALOG_GAIN[1:0]	R/W	01	These bits set the analog gain of the Class-D amplifier. The values shown indicate the output level with digital volume control set to 0 dB and a full scale digital input (0 dBFS). This level may not be achievable because of analog clipping. See the <a href="#">Amplifier Analog Gain and Digital Volume Control</a> section for more information.  00: 19.2 dBV (default) 01: 20.7 dBV 10: 23.5 dBV 11: 26.3 dBV
1-0	Reserved	R/W	01	These bits are reserved and should be set to 01 when writing to this address

### 7.5.2.7 Fault Configuration and Error Status Register (0x08)

**图 46. Fault Configuration and Error Status Register**

7	6	5	4	3	2	1	0
Reserved		OC_THRESH[1:0]		CLKE	OCE	DCE	OTE
R/W		R/W		R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 17. Fault Configuration and Error Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	00	These bits are reserved and should be set to 00 when writing to this address.
5-4	OC_THRESH[1:0]	R/W	00	This register sets the Over Current detector threshold. For more information see the <a href="#">Class-D Amplifier Settings</a> section. 00: 100% of overcurrent limit (default) 01: 75% of overcurrent limit 10: 50% of overcurrent limit 11: 25% of overcurrent limit
3	CLKE	R	0	This bit indicates the status of the SAIF clock error detector. This is a self clearing value. 0: No SAIF clock errors. 1: SAIF clock errors are present.
2	OCE	R	0	This bit indicates the status of the overcurrent error detector. This is a latching value. 0: The Class-D output stage has not experienced an over current event. 1: The Class-D output stage has experienced an over current event.
1	DCE	R	0	This bit indicates the status of the DC detector. This is a latching value. 0: The Class-D output stage has not experienced a DC detect error. 1: The Class-D output stage has experienced a DC detect error.
0	OTE	R	0	This bit indicates the status of the over temperature detector. This is a latching value. 0: The Class-D output stage has not experienced an over temperature error. 1: The Class-D output stage has experienced an over temperature error.

### 7.5.2.8 Digital Clipper 2 Register (0x10)

**图 47. Digital Clipper 2 Register**

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL[13:6]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 18. Digital Clipper 2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	DIGITAL_CLIP_LEVEL[13:6]	R/W	1	This register holds the bits 13 through 6 of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the <a href="#">Digital Clipper</a> section for more information.

### 7.5.2.9 Digital Clipper 1 Register (0x11)

**图 48. Digital Clipper 1 Register**

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL[5:0]						Reserved	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 19. Digital Clipper 1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	DIGITAL_CLIP_LEVEL[5:0]	R/W	1	This register holds the bits 5 through 0 of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the <a href="#">Digital Clipper</a> section for more information.
1-0	Reserved	R/W	00	These bits are reserved and should be set to 00 when writing to this register.

### 7.5.2.10 Digital Control Register 3 (0x13)

**图 49. Digital Control Register 3**

7	6	5	4	3	2	1	0
HPF_CORNER			AUTO_SLEEP		TDM_SLOT_16 B	MCLK_PIN_CF G	VOL_CONTROL[0]
R/W			R/W		R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 20. Digital Control Register 3 Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	HPF_CORNER	R/W	0	These bits set the High Pass Filter corner frequency. Values for 44.1-kHz sample rate are shown in this table. See <a href="#">表 3</a> in the <a href="#">Audio Signal Path</a> section for more information. 000: 3.7-Hz High Pass Corner at 44.1-kHz Sample Rate (Default) 001: 7.4-Hz High Pass Corner at 44.1-kHz Sample Rate 010: 14.9-Hz High Pass Corner at 44.1-kHz Sample Rate 011: 29.7-Hz High Pass Corner at 44.1-kHz Sample Rate 100: 59.4-Hz High Pass Corner at 44.1-kHz Sample Rate 101: 118.4-Hz High Pass Corner at 44.1-kHz Sample Rate 110: 235.0-Hz High Pass Corner at 44.1-kHz Sample Rate 111: 463.2-Hz High Pass Corner at 44.1-kHz Sample Rate

**表 20. Digital Control Register 3 Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
4-3	AUTO_SLEEP	R/W	0	These bits control the auto sleep function that disables the power stage if no audio input has been zero for a prescribed number of samples. 00: Auto Sleep Disabled (Default) 01: Auto Sleep after 1024 LRCLK's with idle input 10: Auto Sleep after 64 × 1024 LRCLK with idle input 11: Auto Sleep after 256 × 1024 LRCLK with idle input
2	TDM_SLOT_16B	R/W	0	This bit indicates the time slot bit width. 0: Each time slot is 24 or 32 bits in width (Default). 1: Each time slot is 16 bits in width.
1	MCLK_PIN_CFG	R/W	0	This bit indicates the source of MCLK. 0: MCLK signal is derived from BCLK internally. Connect MCLK pin to GND on PCB (Default). 1: MCLK signal is derived from MCLK pin.
0	VOL_CONTROL[0]	R/W	0	This is the LSB of the Digital Volume Control.

**7.5.2.11 Analog Control Register 2 (0x14)**
**图 50. Analog Control Register 2**

7	6	5	4	3	2	1	0
Reserved				FAULTZ_PU	VREG_LVL	Reserved	PWR_TUNE
R/W				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 21. Analog Control Register 2 Field Descriptions**

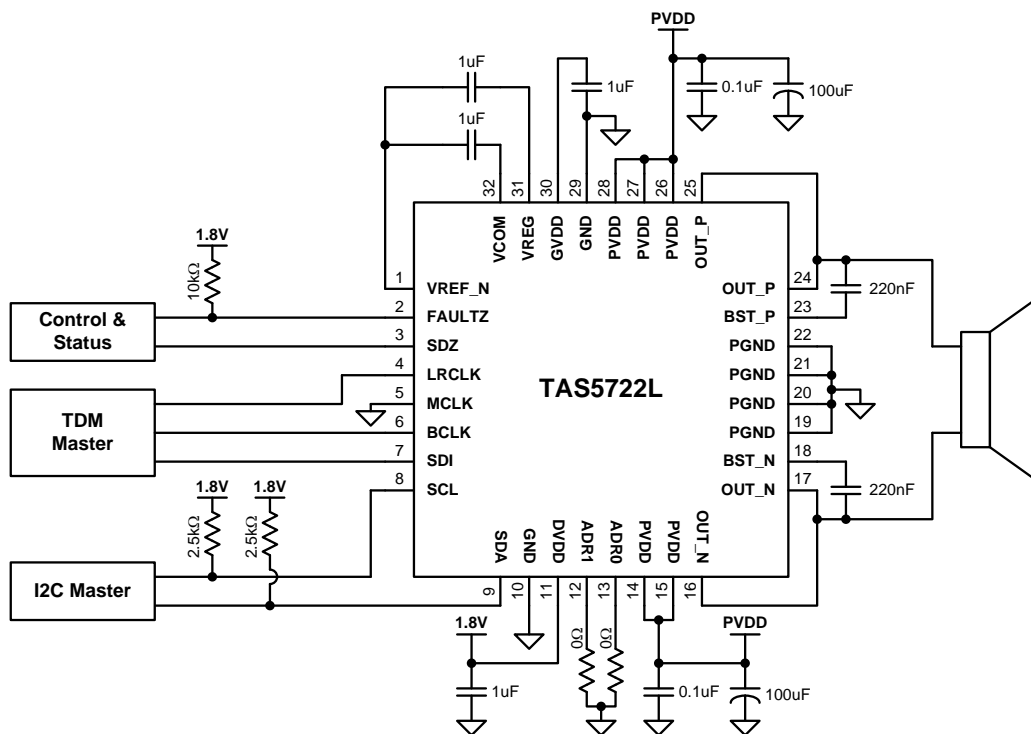
Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	These bits are reserved and should be set to 0000 when writing to this register.
3	FAULTZ_PU	R/W	0	This bit controls an internal 20-kΩ pull-up resistor on the FAULTZ pin. 0: Disable pull-up resistor (Default). 1: Enable pull-up resistor.
2	VREG_LVL	R/W	0	This bit reduces the analog voltage regulator during low PVDD < 5.5-V operation. 0: Default regulator level of 5.4 V (Default). 1: Reduced regulator level of 3.9 V.
1	Reserved	R/W	1	This bit is reserved and should be set to 1 when writing to this register.
0	PWR_TUNE	R/W	0	This bit reduces static analog current in the analog domain by approximately 0.9 mA. 0: Do not reduce analog supply current (Default). 1: Reduce analog supply current.

## 8 Applications and Implementation

### 8.1 Application Information

This section describes a filter-free, TDM application.

### 8.2 Typical Application



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✎ 51. Filter Free 3-Wire TDM Application Circuit (I2C\_DEV\_ID = 0x6C)

#### 8.2.1 Design Requirements

- Input voltage range PVDD and AVDD: 4.5 V to 17 V
- Input voltage range DVDD: 1.65 V to 2 V
- Input sample rate: 44.1 kHz to 48 kHz or 88.2 kHz to 96 kHz
- I<sup>2</sup>C clock frequency: up to 400 kHz
- Maximum output power: 15 W

#### 8.2.2 Design Procedure

##### 8.2.2.1 Overview

The TAS5722L is a very flexible and easy to use Class D amplifier; therefore the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVDD rail planned for the design
- Speaker or load impedance
- Audio sample rate
- Maximum output power requirement
- Desired PWM frequency

## Typical Application (continued)

### 8.2.2.2 Select the PWM Frequency

Set the PWM frequency by writing to the PWM\_RATE bits (bits 6-4, reg 0x06). The default setting for this register is 101, which is  $16 \times \text{LRCLK}$  for single speed applications and  $8 \times \text{LRCLK}$  for double speed application. This value equates to a default PWM frequency of 768 kHz for a 48 kHz sample rate.

### 8.2.2.3 Select the Amplifier Gain and Digital Volume Control

In order to select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that produces an output voltage swing greater than the required output swing for maximum power. The analog gain can be set by writing to the ANALOG\_GAIN bits (bits 3-2, reg 0x06). The default gain setting is 20.7 dBV referenced to 0dBFS input.

### 8.2.2.4 Select Input Capacitance

Select the bulk capacitors at the PVDD inputs for proper voltage margin and adequate capacitance to support the power requirements. The TAS5722L has very good PVDD PSRR, so the capacitor is more about limiting the ripple and droop for the rest of system than preserving good audio performance. The amount of bulk decoupling can be reduced as long as the droop and ripple is acceptable. One capacitor should be placed near the PVDD inputs at each side of the device. PVDD capacitors should be a low ESR type because they are being used in a high-speed switching application.

### 8.2.2.5 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVDD inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVDD and GND connections to the device in order to minimize series inductances.

### 8.2.2.6 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22- $\mu\text{F}$ , 25-V capacitors of X5R quality or better.

## 8.2.3 Application Performance Plots

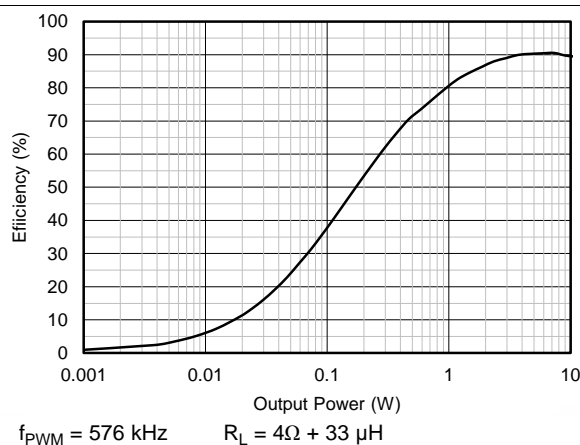


FIG 52. Efficiency vs. Output Power

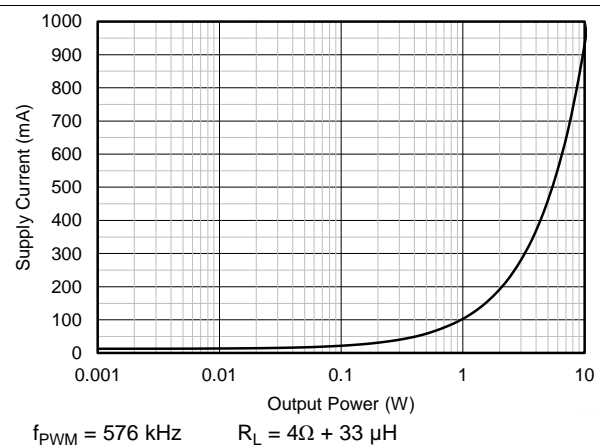


FIG 53. Supply Current vs. Output Power



## 9 Power Supply Recommendations

The power supply requirements for the TAS5722L device consist of one 1.8-V supply to power the low-voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TAS5722L device to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device.

The TAS5722L requires two power supplies. A 1.8-V supply, called DVDD, is required to power the digital section of the device. A higher-voltage supply, between 4.5 V and 17 V, supplies the analog circuitry (AVDD) and the power stage (PVDD). The AVDD supply feeds several LDOs including GVDD, VREG, and VCOM. These LDO outputs are connected to external pins for filtering purposes, but should not be connected to external circuits. These LDO outputs have been sized to provide current necessary for internal functions but not for external loading.

## 10 Layout

### 10.1 Layout Guidelines

- Pay special attention to the power stage power supply layout. Each half bridge has two PVDD input pins so that decoupling capacitors can be placed nearby. Use at least a 0.1-μF capacitor of X5R quality or better for each set of inputs.
- Keep the current circulating loops containing the supply decoupling capacitors, the H-bridges in the device and the connections to the speakers as tight as possible to reduce emissions.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. The area directly under the device should be treated as a central ground area for the device, and all device grounds must be connected directly to that area.
- Use a via pattern to connect the area directly under the device to the ground planes in copper layers below the surface. This connection helps to dissipate heat from the device.
- Avoid interrupting the ground plane with circular traces around the device. Interruption disconnects the copper and interrupt flow of heat and current. Radial copper traces are better to use if necessary.

## 10.2 Layout Example

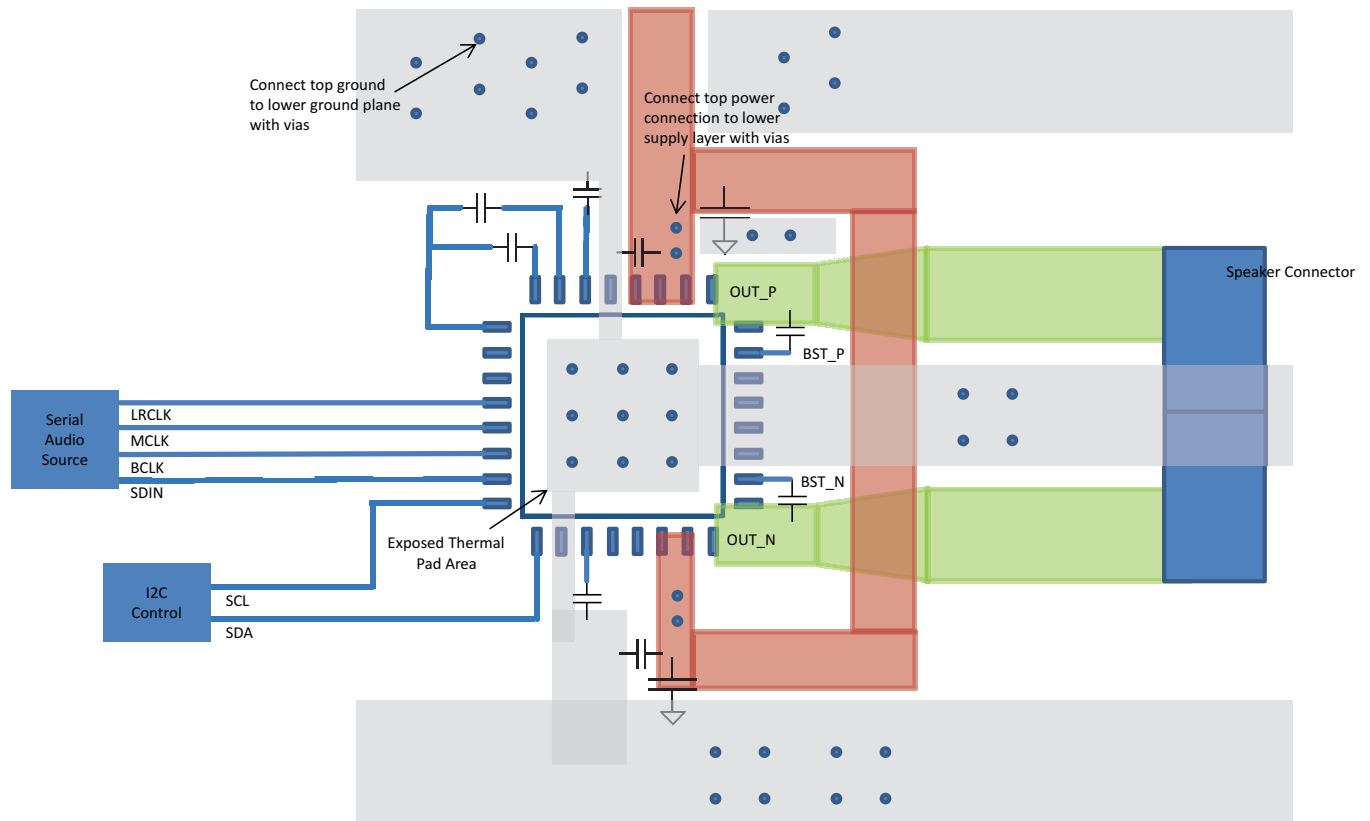


图 54. Layout Example

## 11 デバイスおよびドキュメントのサポート

### 11.1 商標

All trademarks are the property of their respective owners.

### 11.2 静電気放電に関する注意事項



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### 11.3 用語集

[SLYZ022](#) — TI用語集.

この用語集には、用語や略語の一覧および定義が記載されています。

## 12 メカニカル、パッケージ、および注文情報

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## 12.1 Package Option Addendum

### 12.1.1 Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4)(5)</sup>
TAS5722LRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	–25 to 85	TAS 5722L
TAS5722LRSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	–25 to 85	TAS 5722L

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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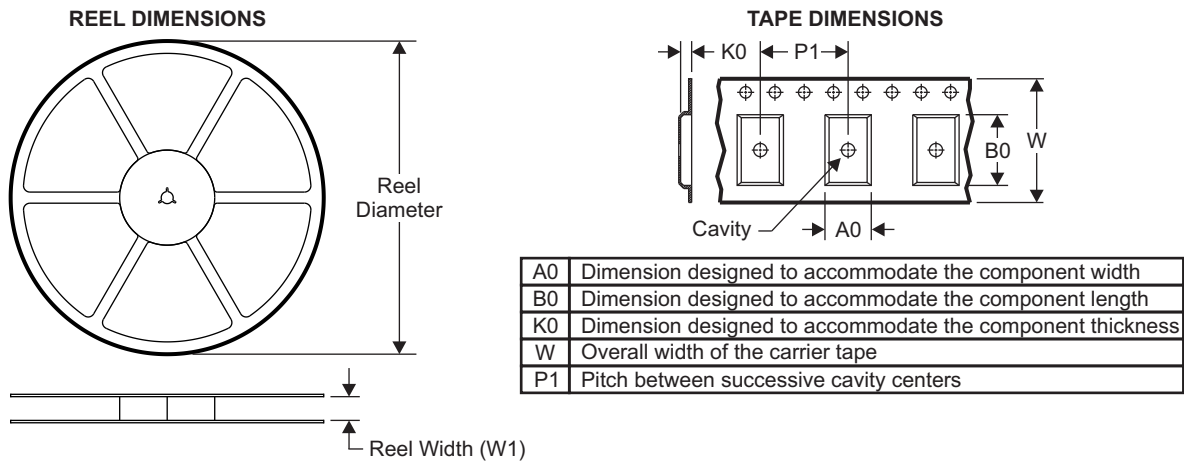
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# TAS5722L

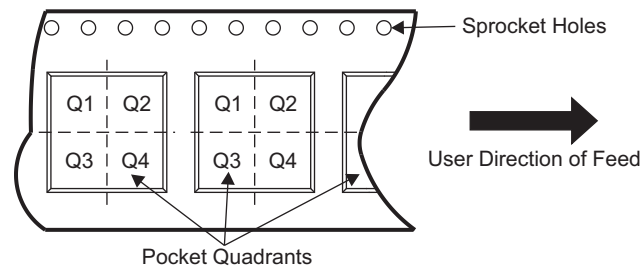
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## 12.1.2 Tape and Reel Information

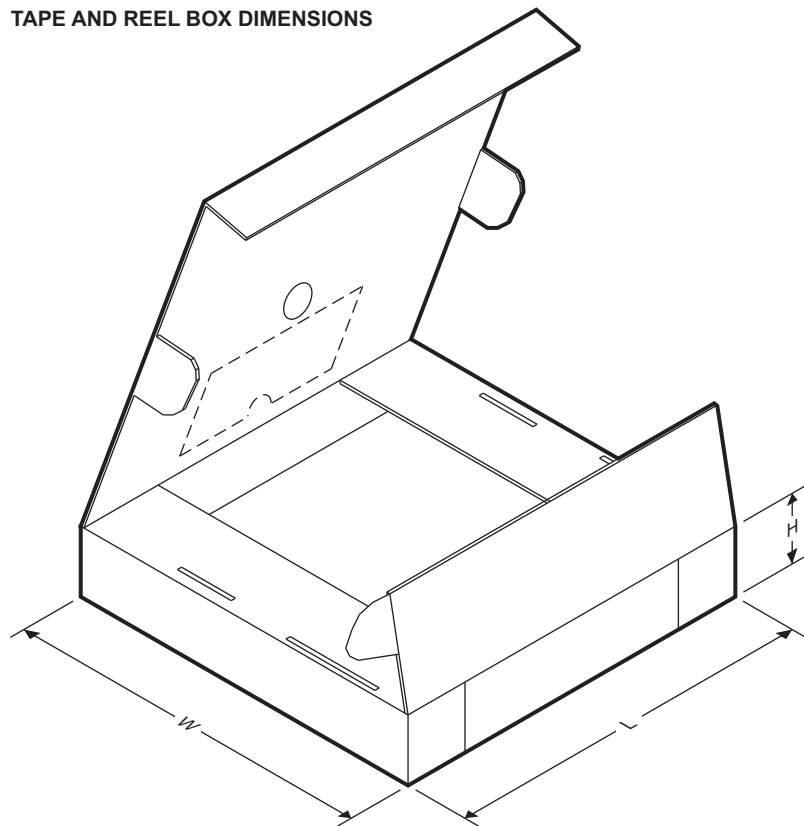


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5722LRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TAS5722LRSMR	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5722LRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TAS5722LRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5722LRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	TAS 5722L	<a href="#">Samples</a>
TAS5722LRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	TAS 5722L	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5722LRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TAS5722LRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5722LRSMR	VQFN	RSM	32	3000	346.0	346.0	33.0
TAS5722LRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

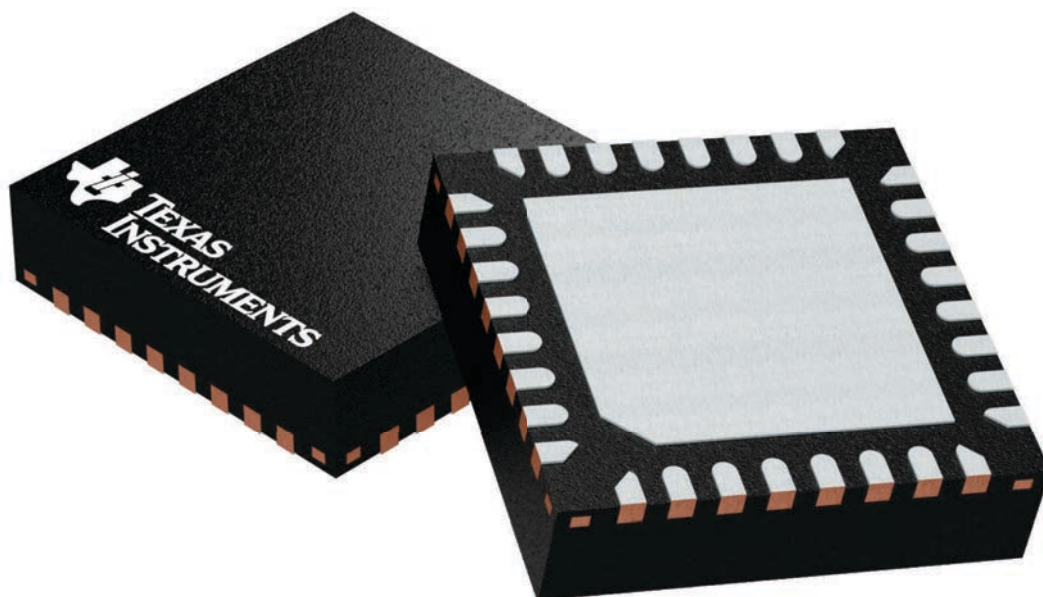
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

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