

TCA9509 レベル変換 I²C および SMBUS バス・リピーター

1 特長

- 2 チャンネルの双方向バッファ
- I²C バスおよび SMBus 互換
- B 側の動作電源電圧範囲: 2.7V~5.5V
- A 側の動作電源電圧範囲: 0.9V~5.5V
- 0.9V~5.5V と 2.7V~5.5V の電圧レベル変換
- アクティブ HIGH のリピーター・イネーブル入力
- 低電圧ポート A に外付けプルアップ抵抗は不要
- オープン・ドレインの I²C I/O
- 5.5V 許容の I²C およびイネーブル入力で、混在モードの信号動作に対応
- ロックアップの発生しない動作
- 標準モードおよびファースト・モード I²C デバイスおよび複数のマスタに対応
- リピーター越しの調停およびクロック・ストレッチングをサポート
- 電源オフ時に高インピーダンスになる I²C バス・ピン
- 400kHz 高速 I²C バスの動作速度をサポート
- 利用可能なバージョン:
 - 1.6mm × 1.6mm、高さ 0.4mm、0.5mm ピッチの QFN パッケージ
 - 3mm × 3mm の業界標準 MSOP パッケージ
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
 - 2000V、人体モデル (A114-A)
 - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- サーバー
- ルーター (テレコム・スイッチング機器)
- 産業用機器
- 多くの I²C ターゲットや長い PCB 配線を持つ製品

3 概要

この TCA9509 IC は、I²C/SMBus システム用の I²C バス / SMBus リピーターです。混在モード・アプリケーションで、低電圧 (最低 0.9V) と、より高い電圧 (2.7V~5.5V) との間の双方向電圧レベル変換 (昇圧変換 / 降圧変換) も行うことができます。このデバイスにより、I²C および同様のバス・システムを拡張でき、レベル・シフト時にも性能劣化を防ぐことができます。

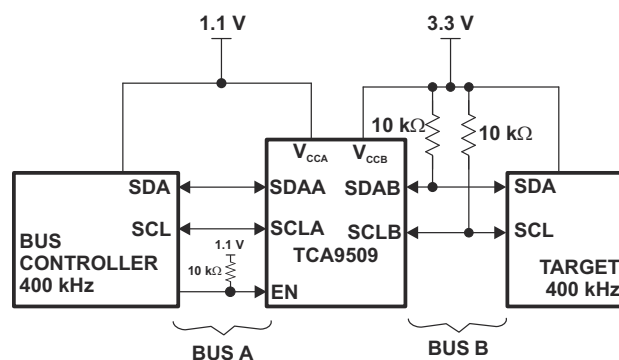
TCA9509 は、I²C バス上のシリアル・データ (SDA) 信号とシリアル・クロック (SCL) 信号の両方をバッファリングすることで、400pF の B 側バス容量を可能にします。このデバイスを使ってバスを 2 つに分割し、電圧や容量を分離することもできます。

TCA9509 には、A 側ドライバと B 側ドライバの 2 種類のドライバがあります。すべての入力と B 側 I/O は、5.5V の過電圧耐性を備えています。A 側 I/O は、デバイスの電源がオフ (VCCB および / または VCCA = 0V) の場合 5.5V の過電圧耐性を備えています。

製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
TCA9509	VSSOP (8)	3.00mm × 3.00mm
	X2QFN (8)	1.60mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



Table of Contents

1 特長	1	9.2 Functional Block Diagram.....	10
2 アプリケーション	1	9.3 Feature Description.....	11
3 概要	1	9.4 Device Functional Modes.....	11
4 Revision History	2	10 Application and Implementation	12
5 Description (continued)	3	10.1 Application Information.....	12
6 Pin Configuration and Functions	4	10.2 Typical Application.....	12
7 Specifications	5	11 Power Supply Recommendations	15
7.1 Absolute Maximum Ratings.....	5	12 Layout	16
7.2 ESD Ratings.....	5	12.1 Layout Guidelines.....	16
7.3 Recommended Operating Conditions.....	5	12.2 Layout Example.....	16
7.4 Thermal Information.....	6	13 Device and Documentation Support	17
7.5 Electrical Characteristics.....	6	13.1 Receiving Notification of Documentation Updates..	17
7.6 Timing Requirements.....	7	13.2 サポート・リソース.....	17
7.7 I ² C Interface Timing Requirements.....	7	13.3 Trademarks.....	17
8 Parameter Measurement Information	9	13.4 静電気放電に関する注意事項.....	17
9 Detailed Description	10	13.5 用語集.....	17
9.1 Overview.....	10		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2017) to Revision D (April 2021)	Page
• データシート全体で用語「マスタ、スレーブ」を「コントローラ、ターゲット」に変更	1
• Changed I _{CC} Quiescent supply current for V _{CCB} MIN value from 0.5 mA to 0.20 mA and the TYP value from 0.9 mA to 0.5 mA in the <i>Electrical Characteristics</i> table.....	6
• Changed text From: "Multiple B-sides of TCA9509 s..." To: "Multiple B-sides of TCA9509..."	13

Changes from Revision B (January 2012) to Revision C (December 2017)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• Added junction temperature to the <i>Absolute Maximum Ratings</i>	5
• Changed thermal information for RVH and DGK packages	6
• Changed V _{ILC} , added Test Conditions with new MIN and TYP values in the <i>Electrical Characteristics</i> table....	6
• Updated Bus A (0.9-V to 5.5-V Bus) Waveform.....	7
• Updated Bus B (2.7-V to 5.5-V Bus) Waveform.....	7

Changes from Revision A (October 2011) to Revision B (January 2012)	Page
• DGK パッケージとパッケージ情報をデータシートに追加.....	1

Changes from Revision * (August 2011) to Revision A (October 2011)	Page
• ドキュメント内の複数の事例で、V _{CCA} の動作電圧の下限を 0.9V に訂正.....	1
• 「特長」の B 側の動作電源電圧範囲の値の誤記を変更。「B 側: 0.9V~5.5V」を「B 側: 2.7V~5.5V」に変更。	1
• 「特長」の A 側の動作電源電圧範囲の値の誤記を変更。「A 側: 2.7V~(V _{CCB} – 1V)」を「A 側: 0.9V~(V _{CCB} – 1V)」に変更。	1

5 Description (continued)

The bus port B drivers are compliant with SMBus I/O levels, while the A-side uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The A-side uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the A-side accommodating smaller voltage swings. The output pull-down on the A-side internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the A-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the B-side drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables B side to connect to any other I²C-bus devices or buffer.

The TCA9509 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

6 Pin Configuration and Functions

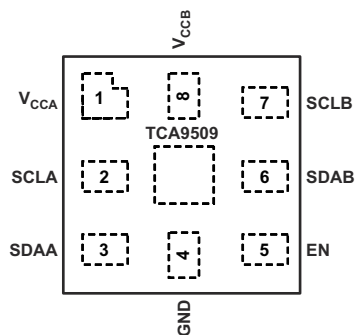


图 6-1. RVH Package, 8-Pin X2QFN, Top View

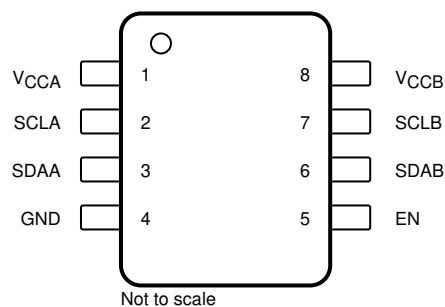


图 6-2. DGK Package, 8-Pin VSSOP, Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V _{CCA}	1	Supply	A-side supply voltage (0.9 V to 5.5 V)
SCLA	2	I/O	Serial clock bus, A side.
SDAA	3	I/O	Serial data bus, A side.
GND	4	Supply	Supply ground
EN	5	Input	Active-high repeater enable input
SDAB	6	I/O	Serial data bus, B side. Connect to V _{CCB} through a pull-up resistor.
SCLB	7	I/O	Serial clock bus, B side. Connect to V _{CCB} through a pull-up resistor.
V _{CCB}	8	Supply	B-side and device supply voltage (2.7 V to 5.5 V)
Thermal Attach Pad	-	-	Thermal Attach Pad is not electrically connected and it is recommended to be attached to GND for best thermal performance. This is for the RVH package only.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCB}	Supply voltage		–0.5	6	V
V _{CCA}	Supply voltage		–0.5	6	V
V _I	Enable input voltage ⁽²⁾		–0.5	6	V
V _{I/O}	I ² C bus voltage ⁽²⁾		–0.5	6	V
I _{IK}	Input clamp current	V _I < 0		–20	mA
I _{OK}	Output clamp current	V _O < 0		–20	
P _d	Max power dissipation			100	mW
T _J	Junction temperature			125	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-side bus		0.9 ⁽¹⁾	5.5	V
V _{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V _{IH}	High-level input voltage	SDAA, SCLA	0.7 × V _{CCA}	V _{CCA}	V
		SDAB, SCLB	0.7 × V _{CCB}	5.5	
		EN	0.7 × V _{CCA}	5.5	
V _{IL}	Low-level input voltage	SDAA, SCLA	–0.5	0.3	V
		SDAB, SCLB	–0.5	0.3 × V _{CCB}	
		EN	–0.5	0.3 × V _{CCA}	
I _{OL}	Low-level output current	SDAA, SCLA		10	μA
		SDAB, SCLB		6	mA
T _A	Operating free-air temperature		–40	85	°C

- (1) Low-level supply voltage

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TCA9509		UNIT
		RVH (X2QFN)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	160.3	222.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	109.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	115.9	144.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	34.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	116.2	142.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	80.5	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

$V_{CCB} = 2.7\text{ V to }5.5\text{ V}$, $V_{CCA} = 0.9\text{ V to } (V_{CCB}-1)$, $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18\text{ mA}$	-1.5		-0.5	V
V_{OL}	Low-level output voltage	SDAA, SCLA $I_{OL} = 10\text{ }\mu\text{A}$, $V_{ILA} = V_{ILB} = 0\text{ V}$, $V_{CCA} = 0.9\text{ to }1.2\text{ V}$		0.18	0.25	V
		SDAA, SCLA $I_{OL} = 20\text{ }\mu\text{A}$, $V_{ILA} = V_{ILB} = 0\text{ V}$, $1.2\text{ V} < V_{CCA} \leq (V_{CCB} - 1\text{ V})$		0.2	0.3	
$V_{OL} - V_{ILc}$	Low-level input voltage below low-level output voltage	SDAA, SCLA		50		mV
V_{ILc}	SDA and SCL low-level input voltage contention	SDAA, SCLA $V_{CCA} \geq 1.5\text{ V}$ and $V_{CCB} \geq 3.15\text{ V}$	110	150		mV
		$V_{CCA} < 1.5\text{ V}$ or $V_{CCB} < 3.15\text{ V}$	50	100		
V_{OLB}	Low-level output voltage	SDAB, SCLB $I_{OL} = 6\text{ mA}$		0.1	0.2	V
I_{CC}	Quiescent supply current for V_{CCA}	All port A Static high	0.25	0.45	0.9	mA
		All port A Static low	1.25			
I_{CC}	Quiescent supply current for V_{CCB}	All port B Static high	0.2	0.5	1.1	mA
I_I	Input leakage current	SDAB, SCLB $V_I = V_{CCB}$			± 1	μA
		$V_I = 0.2\text{ V}$			10	
	SDAA, SCLA	$V_I = V_{CCA}$			± 1	
		$V_I = 0.2\text{ V}$			10	
	EN	$V_I = V_{CCB}$			± 1	
		$V_I = 0.2\text{ V}$			-10	
I_{OH}	High-level output leakage current	SDAB, SCLB $V_O = 3.6\text{ V}$			10	μA
		SDAA, SCLA			10	
C_{IOA}	I/O capacitance of A-side	SCLA, SDAA $V_I = 0\text{ V}$		6.5	7	pF
C_{IOB}	I/O capacitance of B-side	SCLB, SDAB $V_I = 0\text{ V}$	5.5		6.2	pF

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition ⁽¹⁾	100		ns
t_h	Hold time, EN high after Stop condition ⁽¹⁾	100		ns

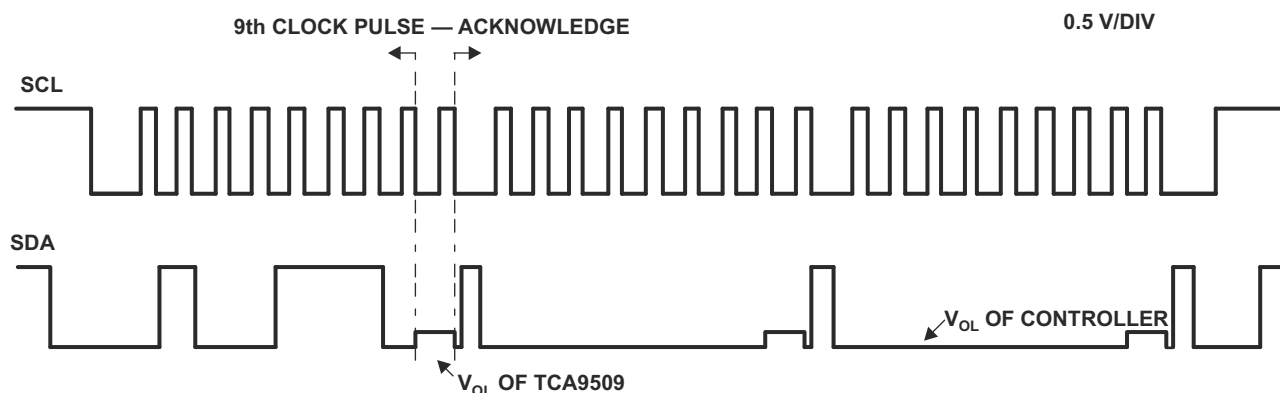
(1) EN should change state only when the global bus and the repeater port are in an idle state.

7.7 I²C Interface Timing Requirements

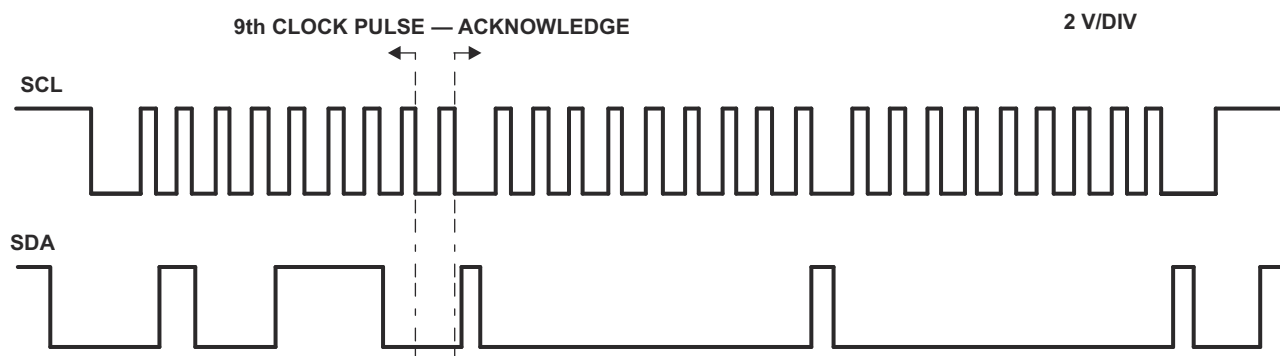
$T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER			V_{CCA} (INPUT)	V_{CCB} (OUTPUT)	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PHL}	Propagation delay	port A to port B	1.9 V	5 V	EN High	123.1	127.2	132.8	ns
		port B to port A				88.1	88.8	89.8	
t_{PLH}	Propagation delay	port A to port B	1.9 V	5 V	EN High	122.6	125.7	131.7	ns
		port B to port A				123	124.1	126.9	
t_{rise}	Transition time	port A	1.9 V	5 V	EN High	40.1	40.9	41.9	ns
		port B				57.3	57.5	58.4	
t_{fall}	Transition time	port A	1.9 V	5 V	EN High	14.5	16.4	17.9	ns
		port B				18.7	19.4	20.2	
t_{PLH2}	Propagation delay 50% of initial low on Port A to 1.5 V on Port B	port A to port B	1.9 V	5 V		176	177.3	178	ns
f_{MAX}	Maximum switching frequency					400			KHz

(1) Typical values were measured with $V_{CCA} = V_{CCB} = 2.7\text{ V}$ at $T_A = 25^\circ\text{C}$, unless otherwise noted.

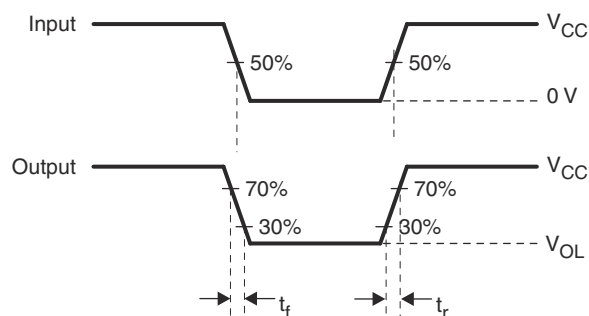
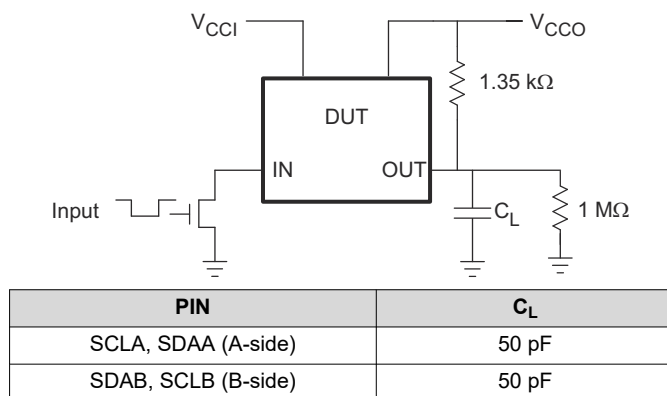


7-1. Bus A (0.9-V to 5.5-V Bus) Waveform



7-2. Bus B (2.7-V to 5.5-V Bus) Waveform

8 Parameter Measurement Information



- A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
- B. C_L includes probe and jig capacitance.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .

8-1. Test Circuit and Voltage Waveforms

9 Detailed Description

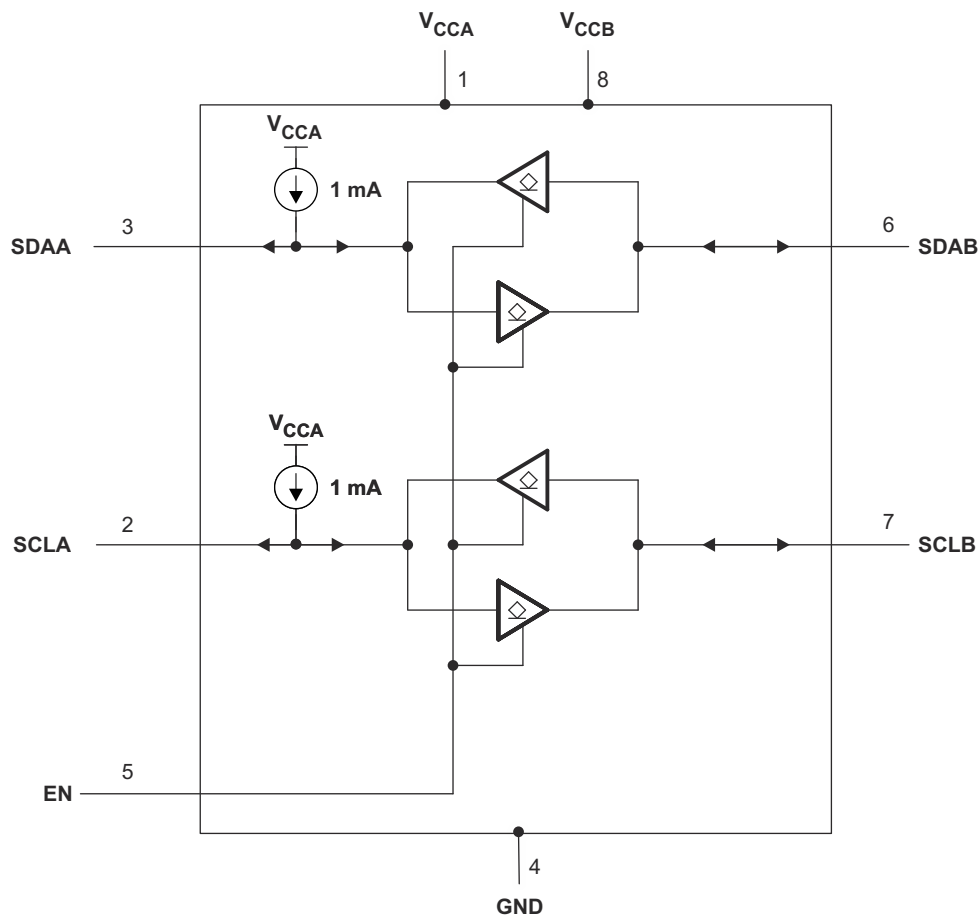
9.1 Overview

This TCA9509 integrated circuit is an I²C bus/SMBus Repeater for use in I²C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing 400-pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/O's are overvoltage tolerant to 5.5V. The A-side I/O's are overvoltage tolerant to 5.5 V when the device is unpowered (V_{CCB} and/or $V_{CCA} = 0V$).

9.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9509 is a two-channel bidirectional buffer with level-shifting capabilities, featuring an integrated current source on the A-side.

9.3.2 Integrated A-Side Current Source

The A-side ports of the TCA9509 feature an integrated 1 mA current source, eliminating the need for external pull-up resistors on SDAA and SCLA.

9.3.3 Standard Mode and Fast Mode Support

The TCA9509 supports standard mode as well as fast mode I²C. The maximum system operating frequency will depend on system design and delays added by the repeater.

9.4 Device Functional Modes

表 9-1 lists the functional modes for the TCA9509.

表 9-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TCA9509 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the B-side of the TCA9509 is pulled low by a driver on the I²C bus and the falling edge goes below 0.3 V_{CCB}, it causes the internal driver on the A-side to turn on, causing the A-side to pull down to about 0.2 V (V_{OL}). When the A-side of the TCA9509 falls, a comparator detects the falling edge and causes the internal driver on the B-side to turn on and pull the B-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to [Figure 7-1](#). If the bus controller in [Figure 10-1](#) were to write to the target through the TCA9509, waveforms shown in [Figure 7-2](#) would be observed on the B bus. This looks like a normal I²C bus transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the A-side bus of the TCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9509. After the eighth clock pulse, the data line is pulled to the V_{OL} of the controller device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9509 for a short delay, while the B-bus side rises above 0.3 V_{CCB} and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the A-bus side at the input of the TCA9509 (V_{IL}) be at or below V_{ILC} to be recognized by the TCA9509 and then transmitted to the B-bus side.

10.2 Typical Application

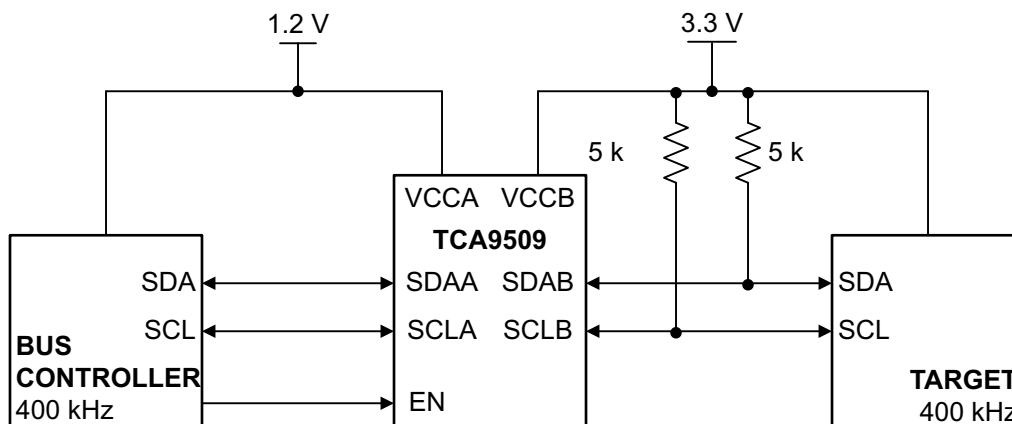


Figure 10-1. Typical Application, A-side Connected to controller

10.2.1 Design Requirements

A typical application is shown in [Figure 10-1](#). In this example, the system controller is running on a 1.2-V I²C bus, and the target is connected to a 3.3-V bus. Both buses run at 400 kHz. Controller devices can be placed on either bus. For the level translating application, the following should be true: V_{CCA} ≤ (V_{CCB} – 1 V)

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- A-side ports must not be connected together
- Pullup resistors should not be placed on the A-side ports

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9509 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value on B-side ports.

10.2.2.2 V_{ILC} and Pulldown Strength Requirements

For the TCA9509 to function correctly, all devices on the A-side must be able to pull the A-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the A-side must be below V_{ILC} min.

The V_{OL} can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the A-side must be carefully selected to ensure that the logic levels will be transferred correctly to the B-side.

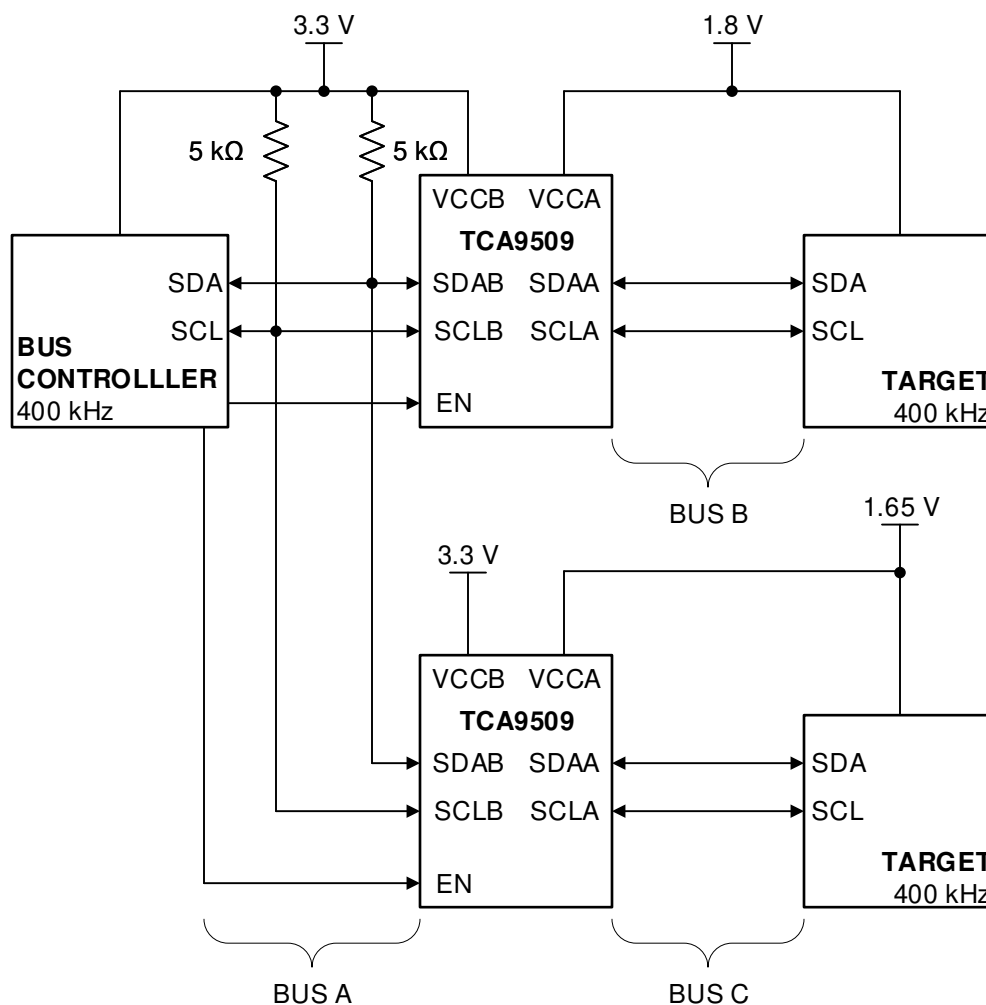
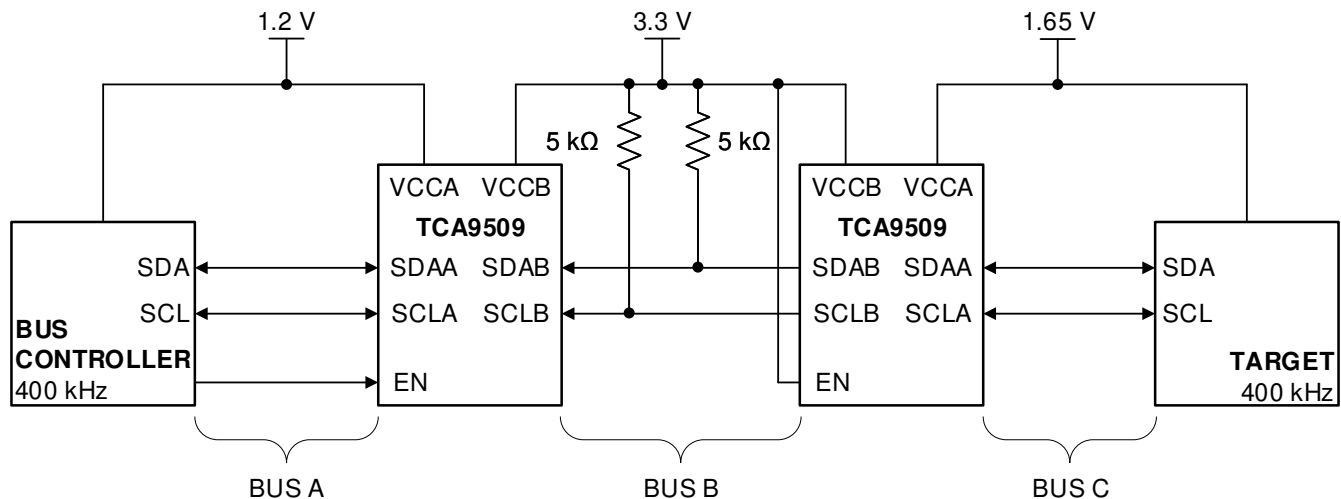
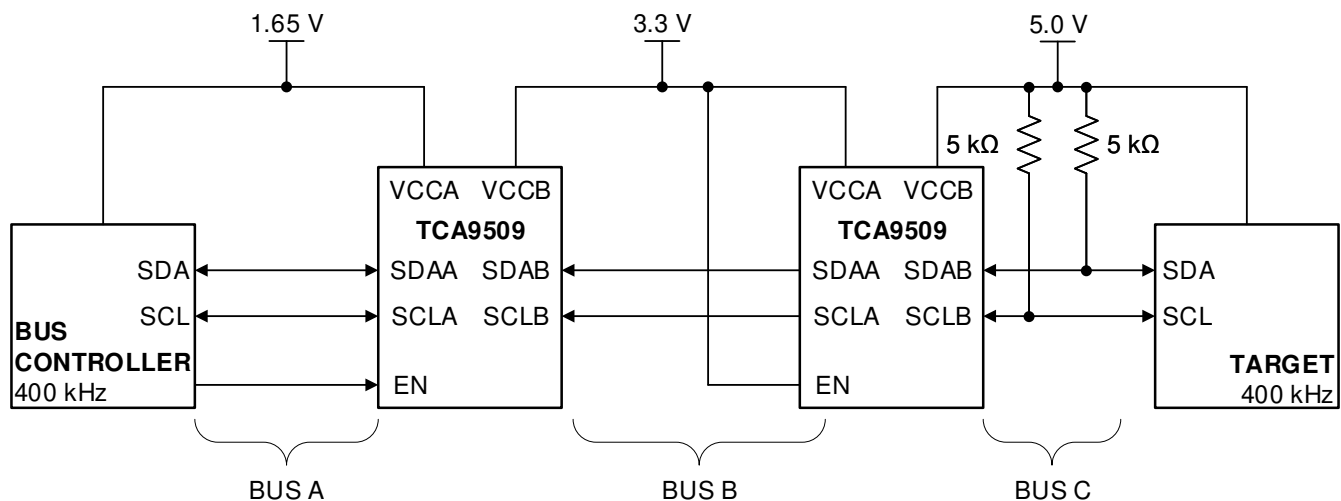


图 10-2. Typical Star Application

Multiple B-sides of TCA9509 can be connected in a star configuration, allowing all nodes to communicate with each other. The A-sides should not be connected together when used in a star/parallel configuration.



10-3. Typical Series Application, Two B-Sides Connected Together



10-4. Typical Series Application, A-side Connected to B-Side

To further extend the I²C bus for long traces/cables, multiple TCA9509 devices can be connected in series as long as the A-side is connected to the B-side and $V_{CCA} \leq (V_{CCB} - 1 \text{ V})$ must also be met. Series connections can also be made by connecting both B-sides together while following power supply rule $V_{CCA} \leq (V_{CCB} - 1 \text{ V})$. I²C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9509 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the B-side (below $0.3 \times V_{CCB}$) turns the corresponding A-side driver (either SDA or SCL) on and drives the A-side down to approximately 0.2 V. When the B-side rises above $0.3 \times V_{CCB}$, the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the A-side falls first and goes below $0.3 \times V_{CCA}$, the B-side driver is turned on and the B-side pulls down to 0 V. The A-side pull-down is not enabled unless the A-side voltage goes below 0.4 V. If the A-side low voltage does not go below 0.5 V, the B-side driver turns off when the A-side voltage is above $0.7 \times V_{CCA}$. If the A-side low voltage goes below 0.4 V, the A-side pull-down driver is enabled, and the A-side is able to rise to only 0.5 V until the B-side rises above $0.3 \times V_{CCB}$.

A 100 nF a decoupling capacitor should be placed as close to the V_{CCA} and V_{CCB} pins in order to provide proper filtering of supply noise.

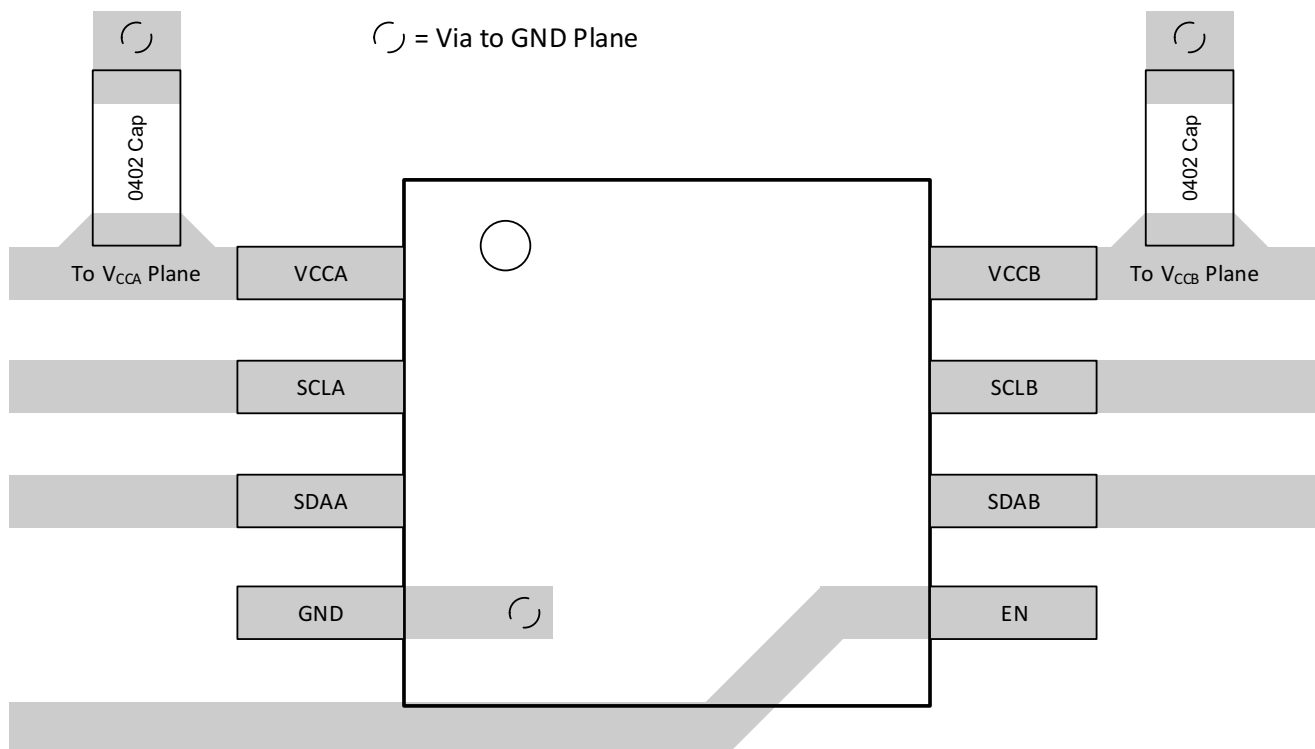
12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9509.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example



✎ 12-1. Example Layout

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

13.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.5 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9509DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 85	(7KO, 7KQ)	Samples
TCA9509MRVHR	ACTIVE	X2QFN	RVH	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K	Samples
TCA9509RVHR	ACTIVE	X2QFN	RVH	8	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

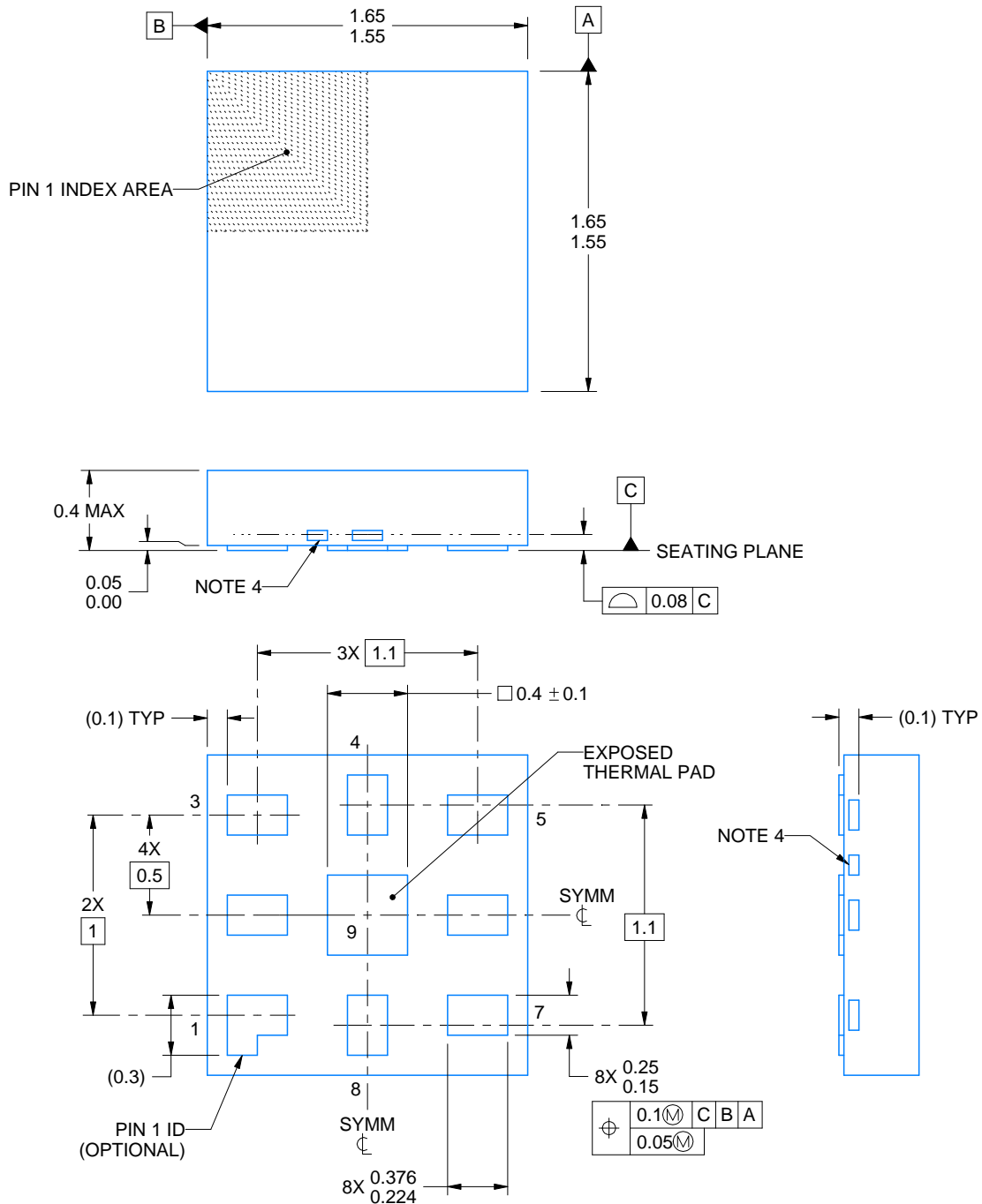
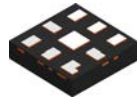
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509MRVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9509MRVHR	X2QFN	RVH	8	5000	183.0	183.0	20.0
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0



4219153/B 02/2017

NOTES:

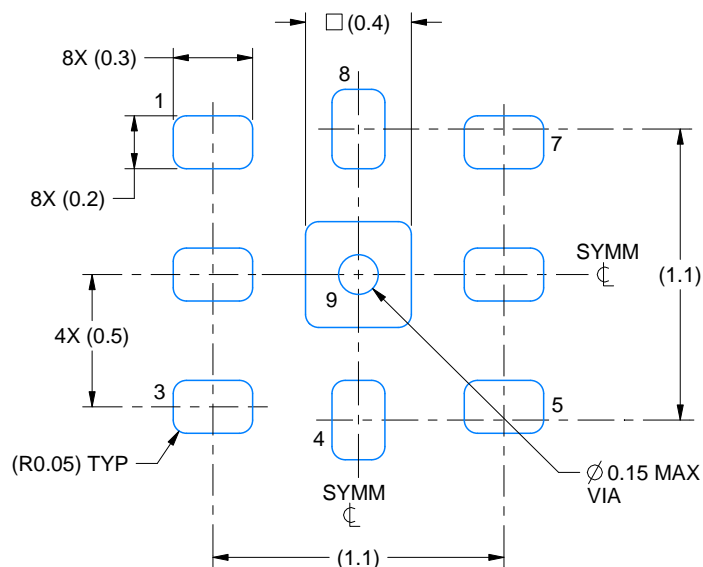
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed tie bars may vary in size and location.

EXAMPLE BOARD LAYOUT

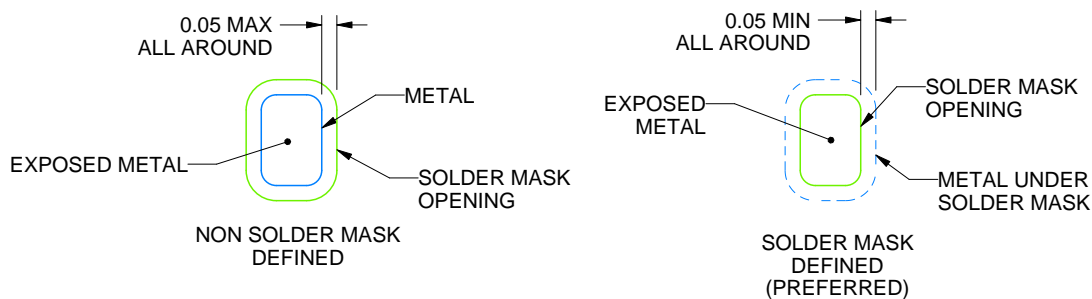
RVH0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:35X



SOLDER MASK DETAILS

4219153/B 02/2017

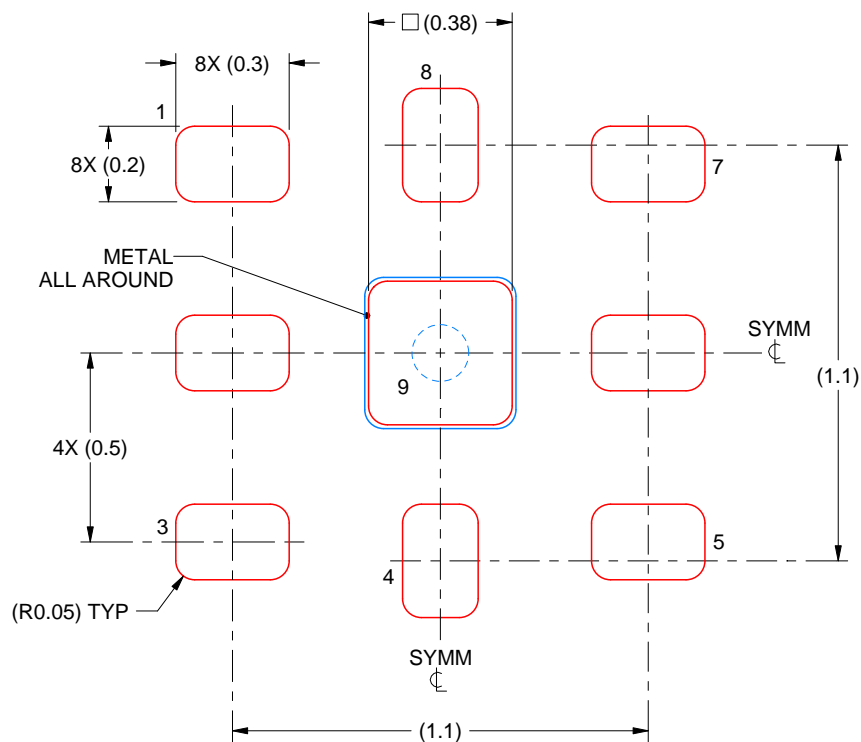
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RVH0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4219153/B 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated