TCA9517A レベル変換I²Cバス・リピータ

1 特長

- 2チャネルの双方向バッファ
- I²CバスおよびSMBus互換
- A側の動作電源電圧範囲：0.9V～5.5V
- B側の動作電源電圧範囲：2.7V～5.5V
- 0.9V～5.5Vと2.7V～5.5Vの電圧レベル変換
- フットプリントと機能においてPCA9515Bを代替可能
- アクティブHIGHのリピーター・イネーブル入力
- オープン・ドレインのI²C I/O
- 5.5V許容のI²Cおよびイネーブル入力で、混在モードの信号動作に対応
- 標準モードおよびファースト・モードI²Cデバイスおよび複数のマスタに対応
- 電源オフ時にI²Cピンが高インピーダンス
- JESD 78、Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
  - 5500V、人体モデル(A114-A)
  - 200V、マシン・モデル(A115-A)
  - 1000V、荷電デバイス・モデル(C101)

2 アプリケーション

- サーバー
- ルーター(テレコム・スイッチング機器)
- 産業用機器
- 多くのI²Cスレーブや長いPCB配線を持つ製品

3 概要

TCA9517Aは、I²CおよびSMBusシステム用のレベル・シフト機能付き双方向バッファです。混在モード・アプリケーションで、低電圧（最低0.9V）と、より高い電圧（2.7V～5.5V）との間の双方向電圧レベル変換（昇圧変換/降圧変換）を行います。このデバイスにより、I²CおよびSMBusシステムを拡張でき、レベル・シフト時にも性能劣化を防ぐことができます。

TCA9517Aは、I²Cバス上でシリアル・データ(SDA)信号とシリアル・クロック(SCL)信号の両方をバッファするため、最大400pFのバス容量を持つ2つのバスをI²Cアプリケーション内で接続できます。

TCA9517Aには、A側ドライバとB側ドライバの2種類のドライバがあります。すべての入力とI/Oは、デバイスの電源がオフのとき（V_{CCB}とV_{CCA}の両方またはどちらかが0V）も含めて、5.5Vまでの過電圧を許容します。

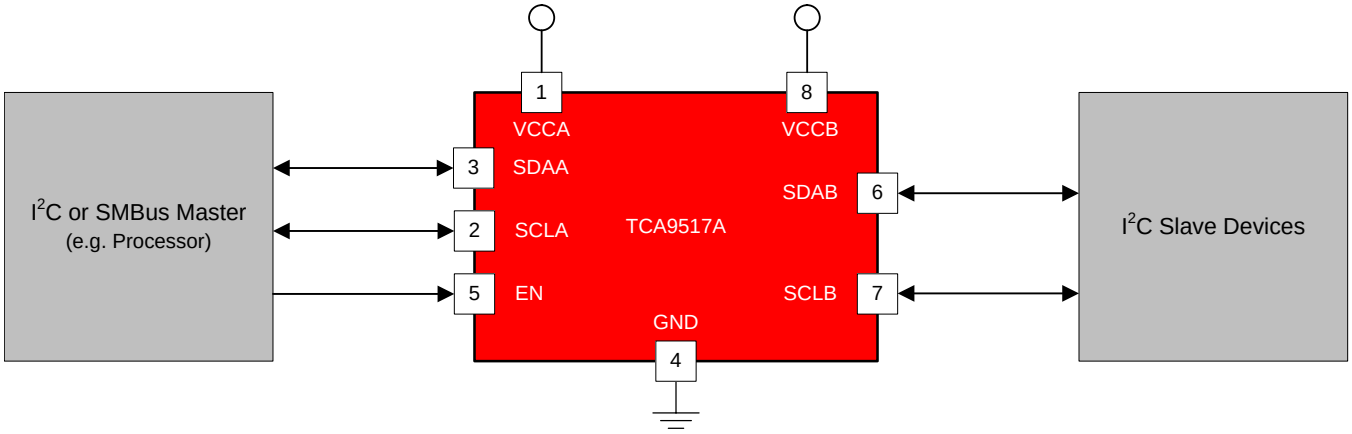
TCA9517Aは、競合レベル・スレッショルド(V_{ILC})がTCA9517よりも高いため、プルダウン能力が小さいスレーブに接続できます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
TCA9517A	VSSOP (8)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (June 2015) から **Revision C** に変更 **Page**

- Changed the appearance of the DGK pin out image ... 4
- Deleted $V_{CCA} < V_{CCB}$ from the *Design Requirements* list ... 12

Revision A (April 2013) から **Revision B** に変更 **Page**

- 「*ピン構成および機能*」セクション、「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「注文情報」表を削除 ... 3

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- 「注文情報」表の「上面のマーキング」列を更新 ... 3

5 概要（続き）

B側のバッファ設計のタイプに起因して、本デバイスは、静的電圧オフセットを使用するデバイスと直列にして使用することはできません。これは、これらのデバイスがバッファされたLOW信号を有効なLOWとは認識せず、バッファされたLOWとして再伝搬しないことが理由です。

B側のドライバは、2.7V～5.5Vで動作します。この内部バッファの出力LOWレベルは約0.5Vですが、出力が内部的にLOWに駆動される場合、入力電圧は出力LOWレベルよりも70mV以上低い必要があります。より電圧の高いLOW信号は、バッファされたLOWと呼ばれます。B側のI/Oが内部でLOWに駆動されるとき、このLOWは入力によってLOWと認識されません。この機能により、入力LOW条件が解除されたとき、ロックアップ状況が発生することが防止されます。

A側のドライバは0.9V～5.5Vで動作し、より大きな電流を駆動します。これらのドライバには、バッファされたLOWの機能（すなわち静的オフセット電圧）は不要です。つまり、B側のLOW信号は、A側でほぼ0VのLOWに変換され、低電圧ロジックの小さな電圧スイングにも対応できるということです。A側の出力プルダウンがハードLOWを駆動するようにし、入力レベルを$0.3\times V_{CCA}$に設定することで、低電圧側の電源電圧が低いシステム（最小0.9V）でより低いLOWレベルが必要な場合にも対応できます。

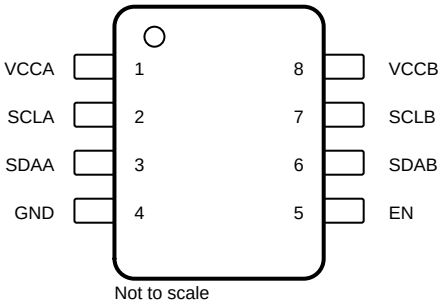
複数のTCA9517AのA側を互いに接続することで、A側を共通バスとして使った各種回路配置を利用できます（図8および図9を参照）。またA側は、静的または動的オフセット電圧を持つその他の任意のバッファに直接接続できます。複数のTCA9517AをA側からB側へ直列に接続できます。この場合、オフセット電圧の増加を考慮する必要はなく、タイム・オブ・フライト遅延のみを考慮すれば十分です。B側からのバッファされたLOW電圧の関係で、TCA9517AをB側からB側に接続することはできません。B側は、立ち上がり時間アクセラレータを持つデバイスには接続できません。

VCCAは、A側の入力コンパレータに$0.3\times V_{CCA}$の基準電圧を供給するためと、パワー・グッド検出回路にのみ使用されます。TCA9517Aのロジックとすべての I/Oは、VCCBピンから電力が供給されます。

標準のI^2Cシステムと同様に、バッファされたバスにロジックHIGHレベルを供給するにはプルアップ抵抗が必要です。TCA9517Aには、I^2Cバスの標準オープン・ドレイン構成があります。これらのプルアップ抵抗の大きさはシステムに依存しますが、リピーターのそれぞれの側にプルアップ抵抗が必要です。このデバイスは、SMBusデバイスに加えて、標準モードおよびファースト・モードのI^2Cデバイスとともに動作するよう設計されています。標準モードのI^2Cデバイスは、一般的なI^2Cシステムで3mAのみが規定されており、標準モード・デバイスと複数のマスタを使用可能です。特定の条件では、より大きな終端電流を使用できます。

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9 V to 5.5 V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7 V to 5.5 V)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9 (1)	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	5.5	V
		SDAB, SCLB	0.7 × V_{CCB}	5.5	
		EN	0.7 × V_{CCB}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB (2)		0.3 × V_{CCB}	
		EN		0.3 × V_{CCB}	
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage
(2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See *V_{ILC} and Pullup Resistor Sizing* for V_{ILC} application information

7.4 Thermal Information

THERMAL METRIC (1)		TCA9517A DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.7 V to 5.5 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100 μA or 6 mA, V_{ILA} = V_{ILB} = 0 V	2.7 V to 5.5 V	0.45	0.52	0.6	V
		SDAA, SCLA	I_{OL} = 6 mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB	ensured by design	2.7 V to 5.5 V		70		mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7 V to 5.5 V		0.45		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.5 V		1.5	5	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			3	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7 V to 5.5 V			±1	μA
			V_I = 0.2 V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2 V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2 V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V	2.7 V to 5.5 V			10	μA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V		6	10	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V		8	13	
				0 V		7	11	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V		8	13	pF
				0 V		7	11	

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

7.7 I²C Interface Switching Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(4) (see Figure 6)	SDAA, SCLA(4) (see Figure 6)		80	141	350	ns
			SDAA, SCLA(5) (see Figure 5)	SDAB, SCLB(5) (see Figure 5)		25	74	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	V_{CCA} ≤ 2.7 V (see Figure 4)	30	76(6)	110	ns
					V_{CCA} ≥ 3 V (see Figure 4)	10	86	230	
			SDAA, SCLA(5) (see Figure 5)	SDAB, SCLB(5) (see Figure 5)		60	107	230	
t_{TLH}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see Figure 5)	10	12	15	ns
					V_{CCA} ≥ 3 V (see Figure 5)	40	42	45	
		A side to B-side (see Figure 4)				110	125	140	
t_{THL}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see Figure 5)	1	52(6)	105	ns
					V_{CCA} ≥ 3 V (see Figure 5)	20	67	175	
		A side to B-side (see Figure 4)				30	48	90	

(1) Times are specified with loads of 1.35-kΩ pull-up resistance and 50-pF load capacitance on the B-side and 167-Ω pull-up and 57-pF load capacitance on the A side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
(3) Typical values were measured with V_{CCA} = V_{CCB} = 3.3 V at T_A = 25°C, unless otherwise noted.
(4) The t_{PLH} delay data from B to A side is measured at 0.4 V on the B-side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(5) The proportional delay data from A to B-side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B-side.
(6) Typical value measured with V_{CCA} = 2.7 V at T_A = 25°C

7.8 Typical Characteristics

V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

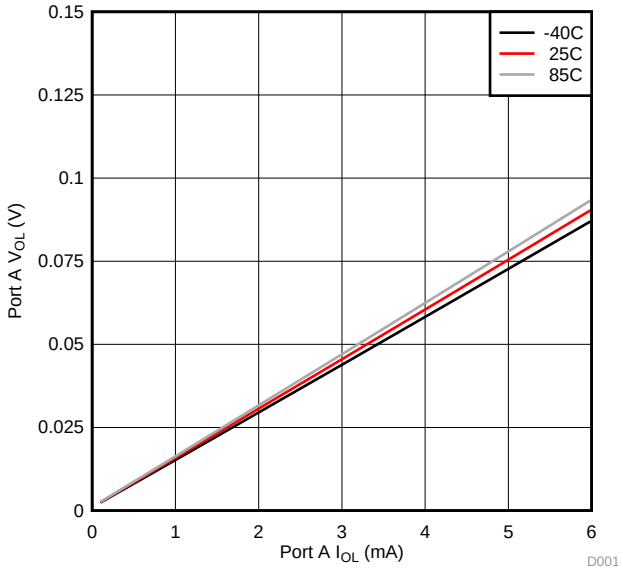


Figure 1. Port A V_{OL} vs I_{OL}

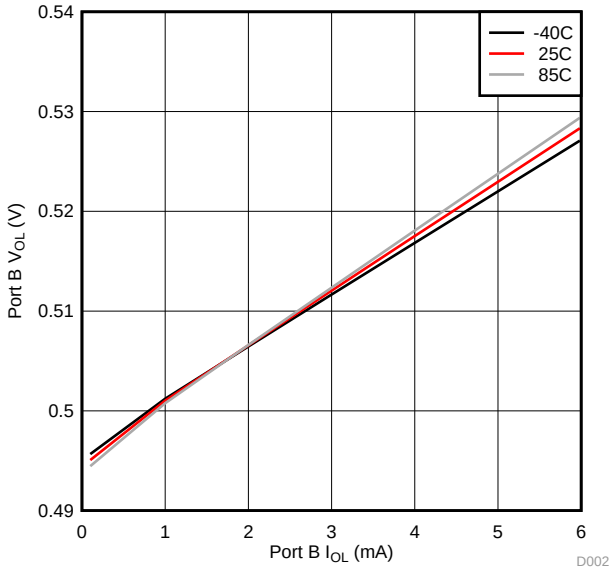
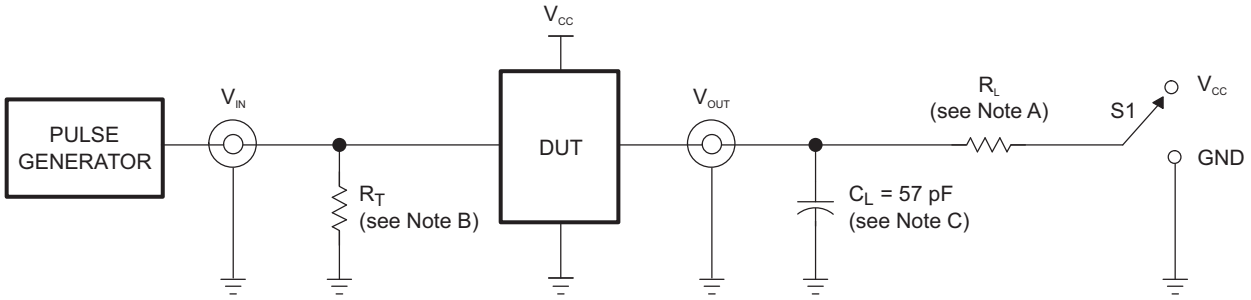


Figure 2. Port B V_{OL} vs I_{OL}

8 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

A. R_L = 167 Ω (0.9 V to 2.7 V) and R_L = 450 Ω (3.0 V to 5.5 V) on the A side and 1.35 kΩ on the B-side

B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

C. C_L includes probe and jig capacitance.

D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

H. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 3. Test Circuit

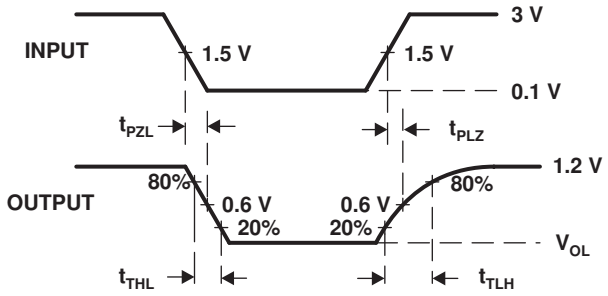


Figure 4. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

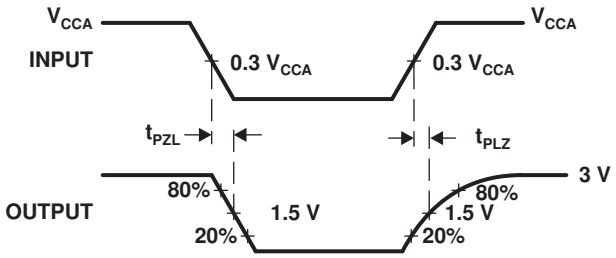


Figure 5. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

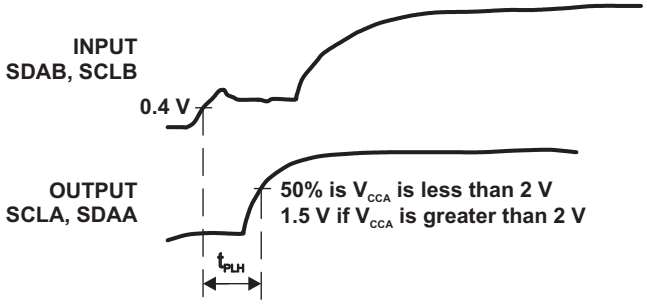


Figure 6. Waveform 3 – Propagation Delay for B-side to A-side

9 Detailed Description

9.1 Overview

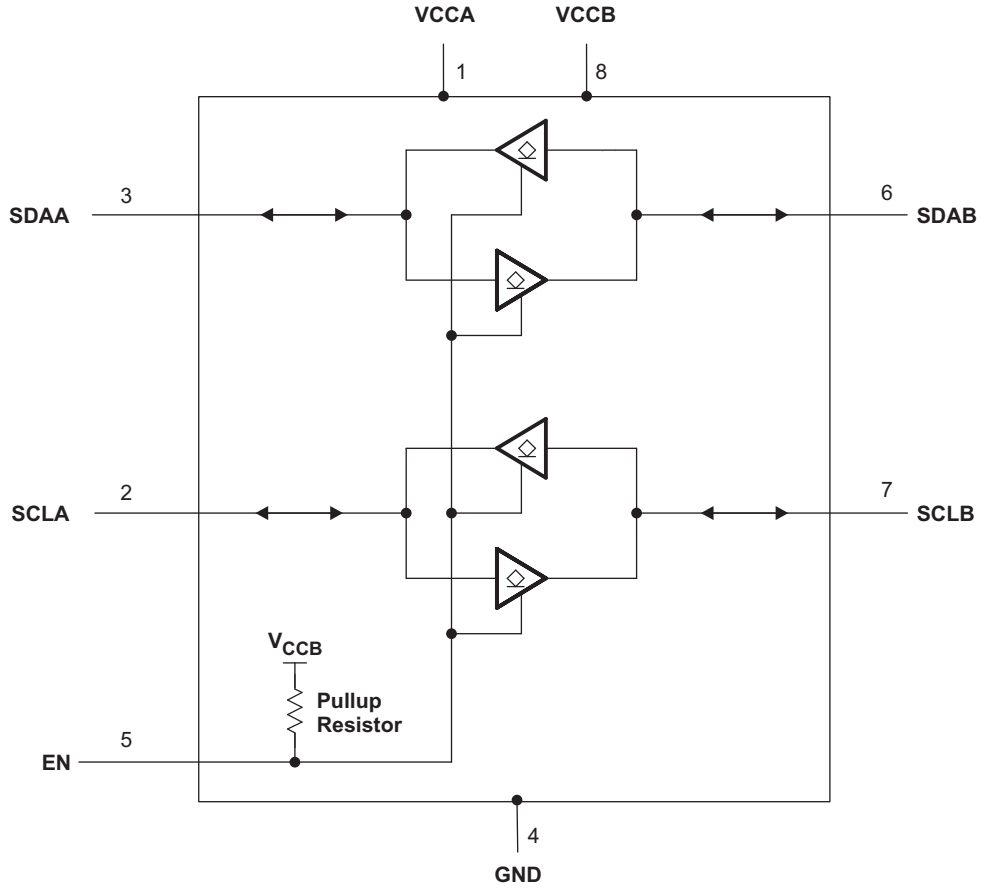
The TCA9517A is a bidirectional buffer with level shifting capabilities for I^2C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I^2C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I^2C application.

The TCA9517A has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

The TCA9517A offers a higher contention level threshold, V_{ILC}, than the TCA9517, which allows connections to slaves which have weaker pull-down ability.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517A is a two-channel bidirectional buffer with level-shifting capabilities

9.3.2 Active-High Repeater-Enable Input

The TCA9517A has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517A supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517A can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical application is shown in Figure 7. In this example, the system master is running on a 3.3 V I^2C bus, and the slave is connected to a 1.2 V I^2C bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9517A is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the TCA9517A is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517A falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 7 were to write to the slave through the TCA9517A, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517A for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

10.2 Typical Application

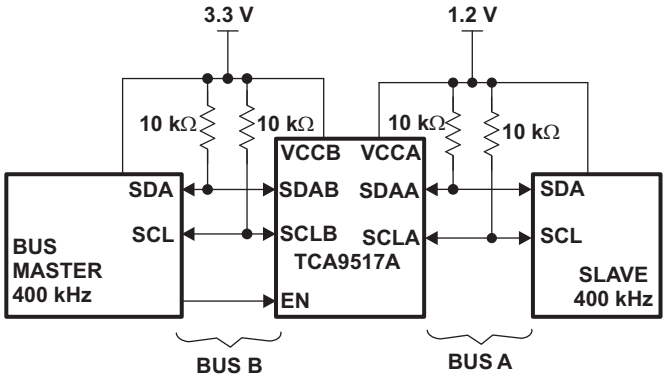


Figure 7. Typical Application Schematic

10.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- B-side ports must not be connected together

Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9517A can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

10.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517A to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.45 V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

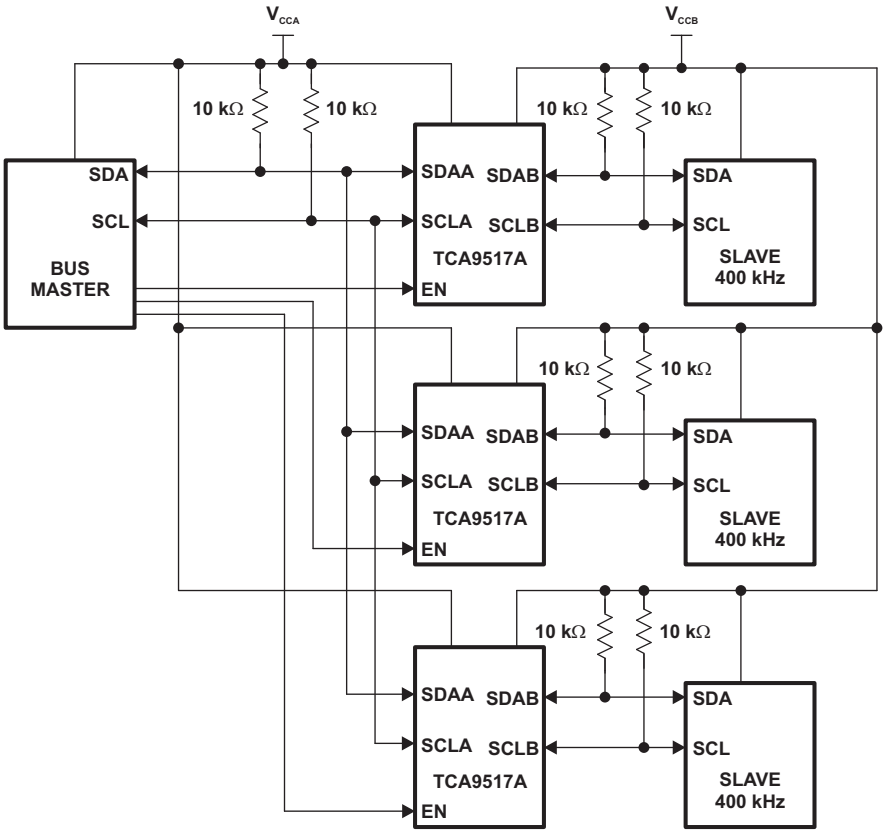


Figure 8. Typical Star Application

Multiple A sides of TCA9517As can be connected in a star configuration, allowing all nodes to communicate with each other.

Typical Application (continued)

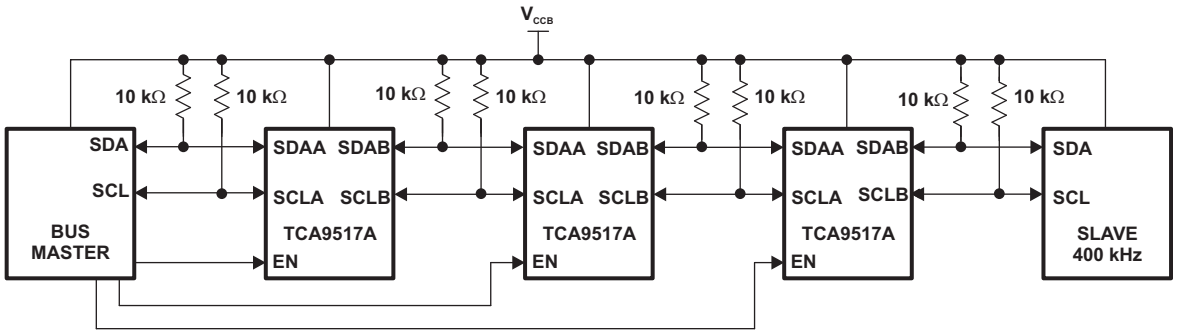


Figure 9. Typical Series Application

To further extend the I^2C bus for long traces/cables, multiple TCA9517As can be connected in series as long as the A-side is connected to the B-side. I^2C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

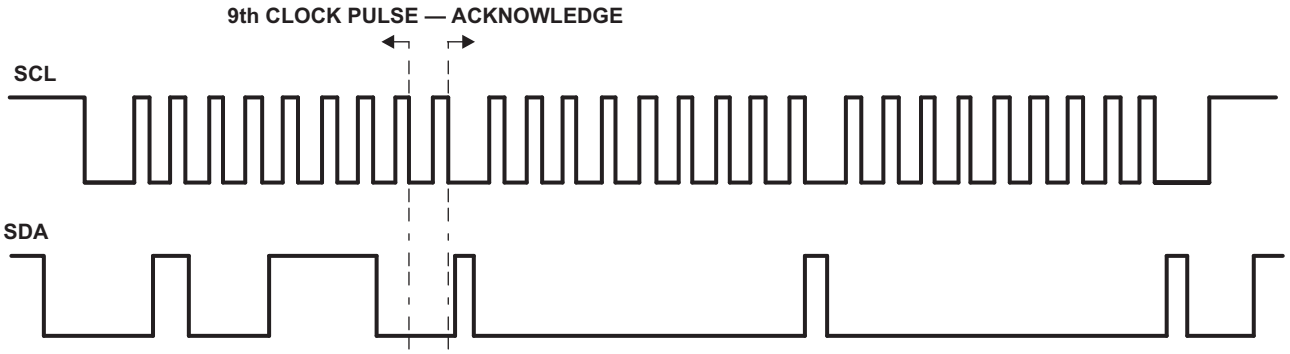


Figure 10. Bus A (0.9 V to 5.5 V Bus) Waveform

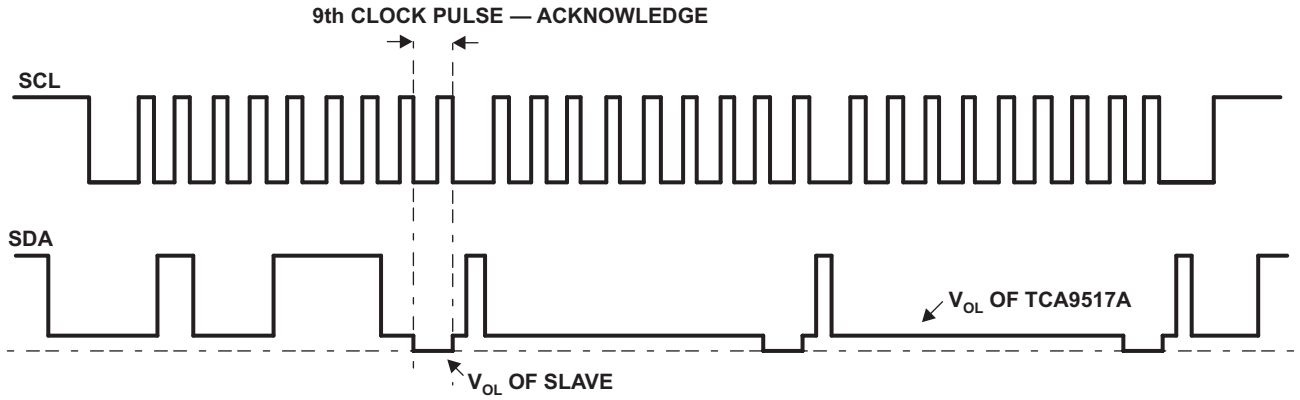


Figure 11. Bus B (2.7 V to 5.5 V Bus) Waveform

Typical Application (continued)

10.2.3 Application Curve

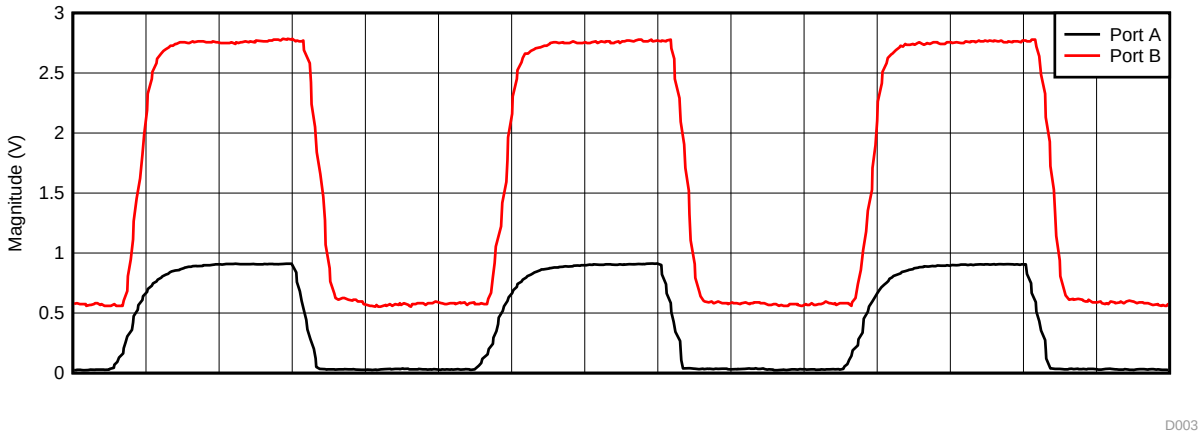


Figure 12. Voltage Translation at 400 kHz, V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517A includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the A-side (below 0.3 × V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above 0.3 × V_{CCA}, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below 0.3 × V_{CCB}, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above 0.7 × V_{CCB}. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above 0.3 × V_{CCA}.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.

12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517A.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

Figure 13 shows an example layout of the DGK package.

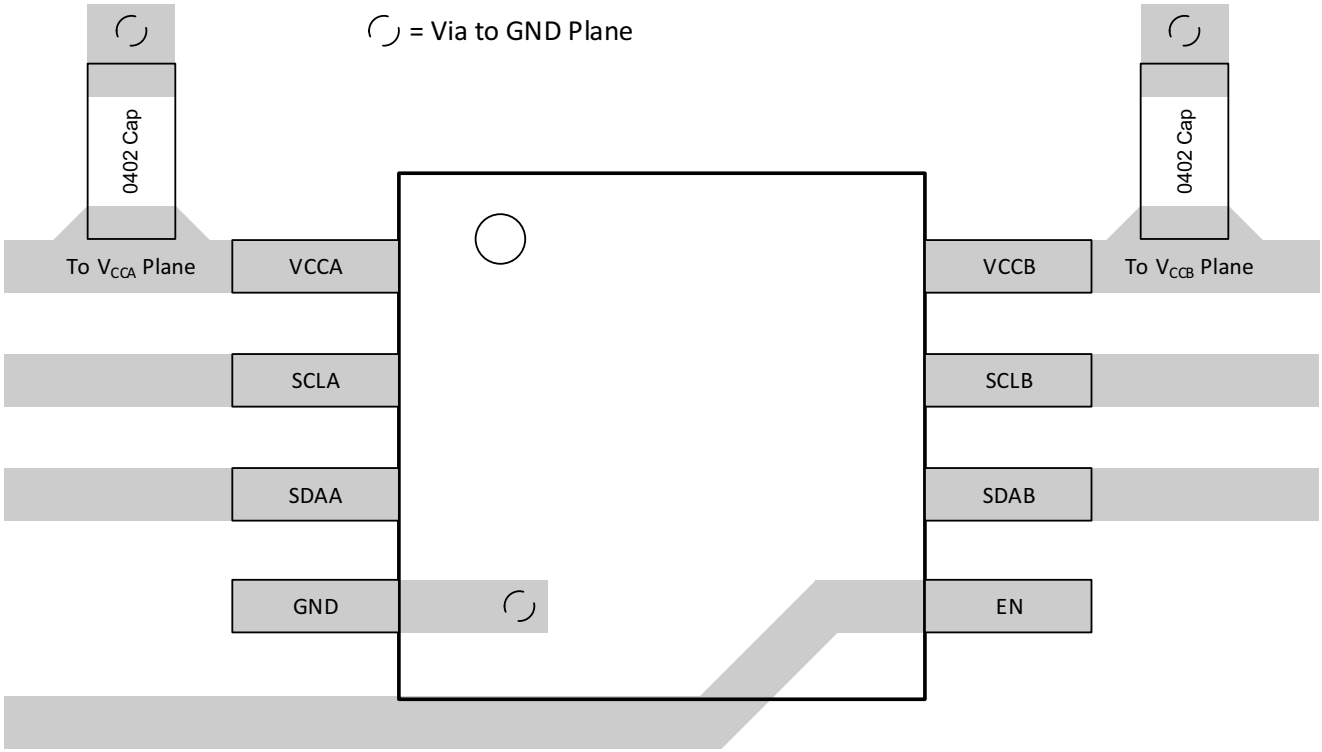


Figure 13. TCA9517A Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

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13.2 コミュニティ・リソース

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13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9517ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	BSK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

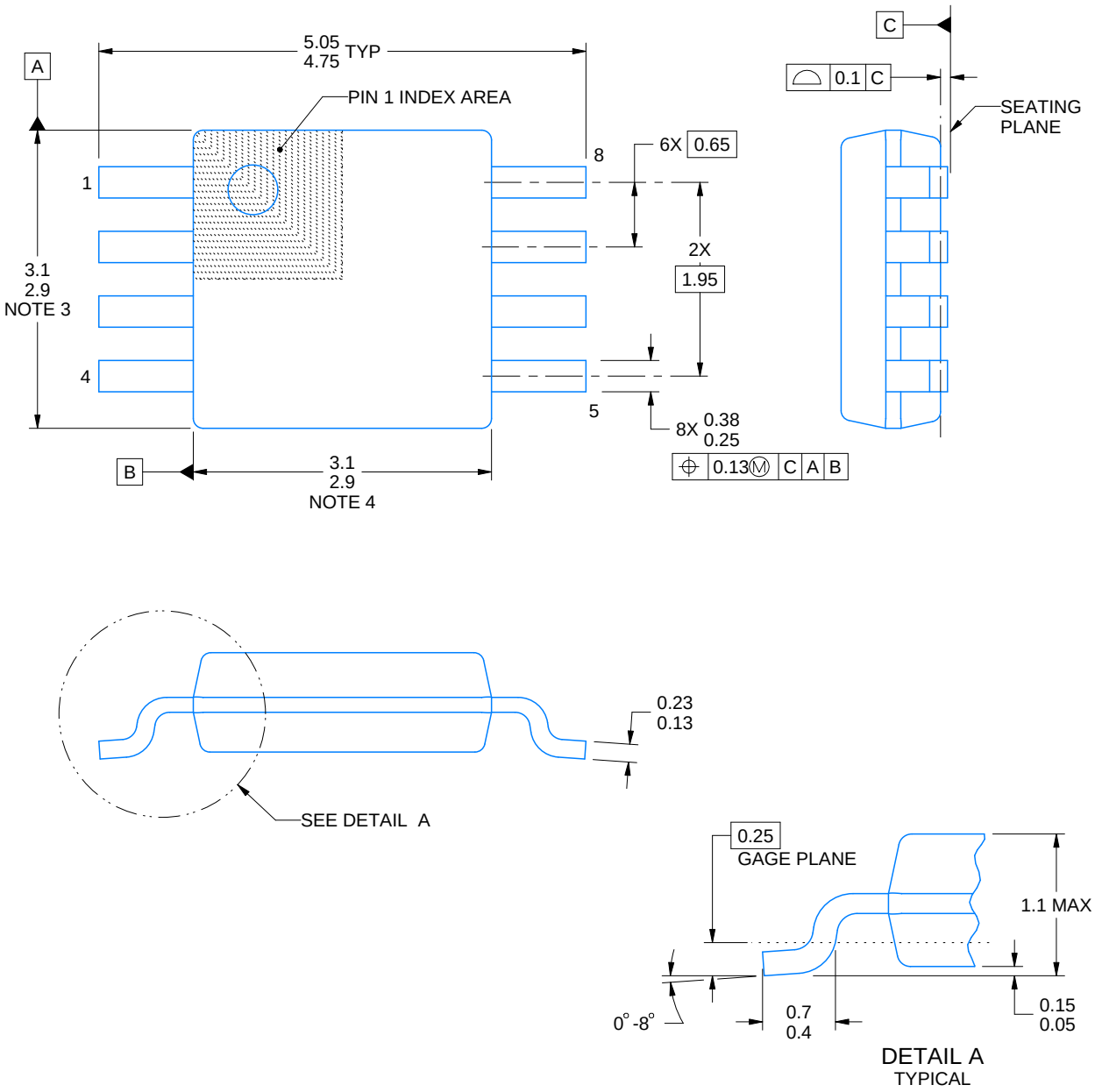
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

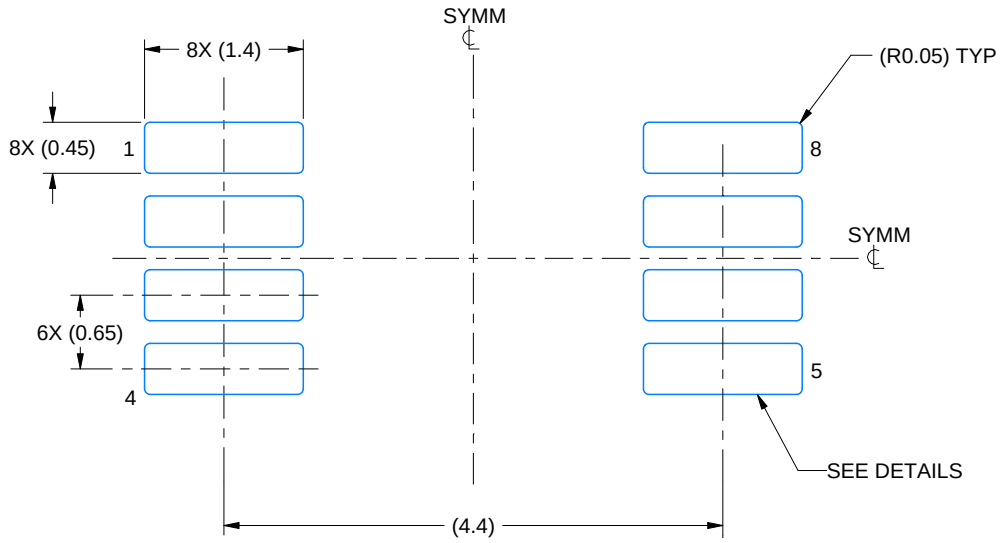
SMALL OUTLINE PACKAGE



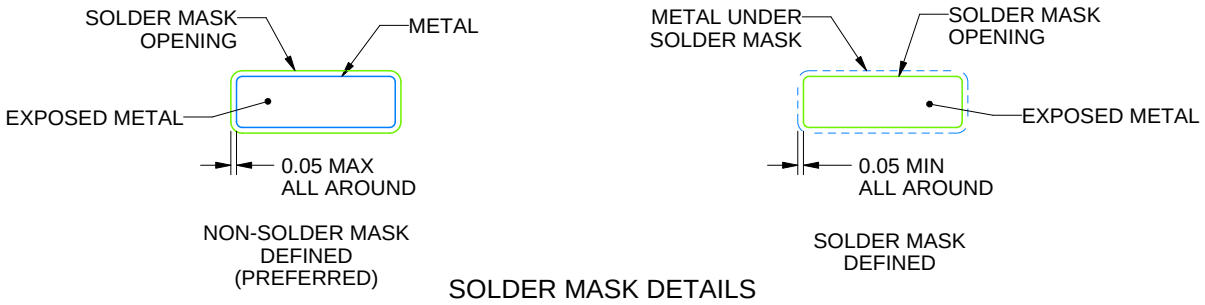
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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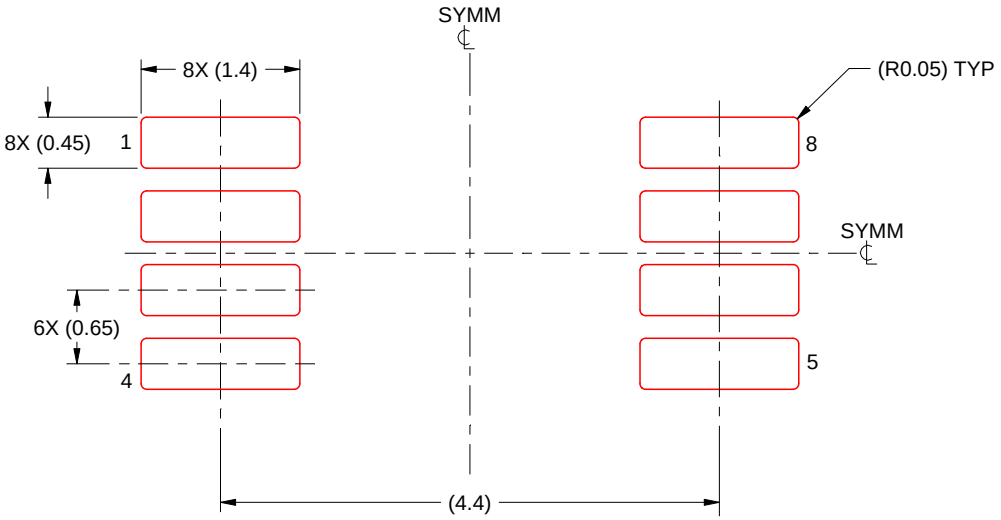
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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