TL103Wx 内部基準電圧付き、デュアル・オペアンプ

1 特長

- TL103W および TL103WA のピン互換アップグレード製品である新しい TL103WB
- B バージョンの仕様を以下のように改善:
  - 電源電圧範囲:3V～36V
  - 低い最大入力オフセット電圧:±2mV (25℃) および ±2.5mV (全温度範囲)
  - ゲイン帯域幅:1.2MHz
  - 合計消費電流:550µA
  - EMI 除去:RF および EMI フィルタを内蔵
  - 温度範囲:-40℃～125℃
- B バージョンの基準電圧の仕様を改善:
  - 2.5V の固定基準電圧
  - 厳しいトレランス:最大 0.44% (25℃) および 1.04% (全温度範囲)
  - 広いシンク電流範囲:100mA で 0.2mA (代表値)

2 アプリケーション

- バッテリ充電器
- スイッチモード電源
- リニア電圧レギュレーション
- データ収集システム
- 高精度定電流シンク

3 概要

TL103Wx デバイスは、デュアル・オペアンプと固定基準電圧の構築ブロックを組み合わせたものです。どちらも、スイッチモード電源とリニア電源の制御回路によく使用されます。オペアンプ 1 は非反転入力が 2.5V の固定基準電圧に内部で接続されているのに対し、オペアンプ 2 は独立しており、両方の入力は不確定です。

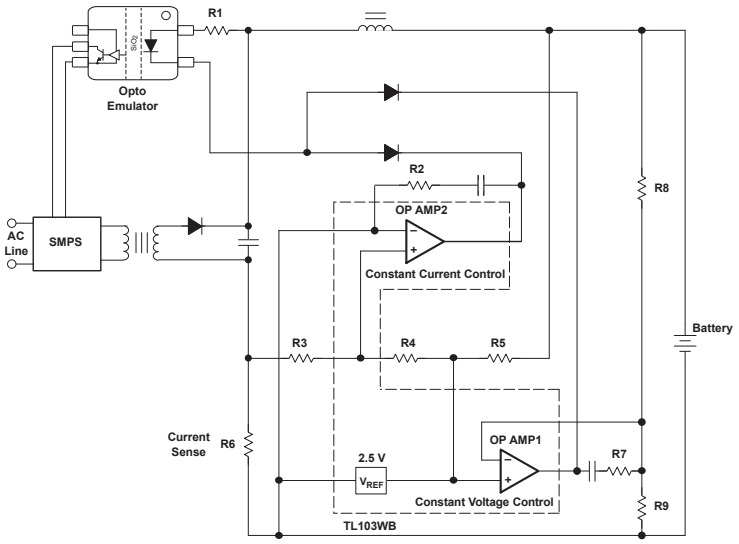
アップグレードされた TL103WB は、より広い電源電圧範囲 (最大 36V)、より小さい消費電流 (275µA/amp)、より厳しい電圧レギュレーションなどの点で改良されています。このレギュレーションは、両オペアンプ向けの低いオフセット電圧 (代表値 0.3mV) と、基準電圧の厳しいトレランス (25℃で 0.44%、動作温度範囲全体にわたって 1.04%) により達成されます。

TL103WB は、-40℃～125℃の広い温度範囲に対応しています。

製品情報

部品番号	チャネル数	パッケージ (1)	パッケージ サイズ (3)
TL103W TL103WA	デュアル + 基準電圧	D (SOIC、8)	4.9mm × 6mm
TL103WB		D (SOIC、8)	4.9mm × 6mm
		DDF (SOT-23、8)(2)	2.9mm × 2.8mm

(1) 詳細については、セクション 10 を参照してください。
(2) このパッケージはプレビューのみです。
(3) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

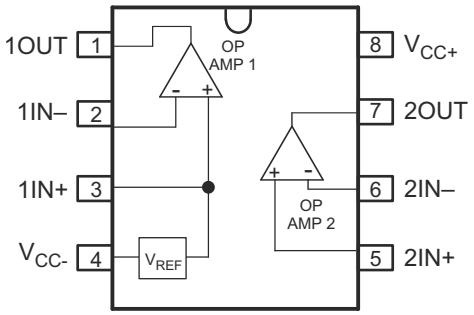


**図 4-1. D and DDF Packages,
8-Pin SOIC and SOT-23-THN
(Top View)**

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OUT	1	O	Opamp 1 output
1IN–	2	I	Opamp 1 inverting input
1IN+	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
$V_{CC–}$	4	I	Negative Supply Voltage
2IN+	5	I	Opamp 2 non-inverting input
2IN–	6	I	Opamp 2 inverting input
2OUT	7	O	Opamp 2 output
V_{CC+}	8	I	Positive Supply Voltage

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	0	36	V
		TL103WB	0	40	
V_{ID}	Operational amplifier input differential voltage			36	V
V_I	Operational amplifier input voltage range(2)		(V_{CC-}) - 0.3	V_{CC+}	V
I_{KA}	Voltage reference cathode current			100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not applicable to pin 4 (1IN+)

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	3	32	V
		TL103WB	3	36	
V_{ICR}	Input common-mode voltage range		V_{CC-}	(V_{CC+}) - 2	V
I_K	Cathode current	TL103W/TL103WA	0.5	100	mA
		TL103WB	0.2	100	
T_A	Operating free-air temperature	TL103W/TL103WA	–40	105	°C
		TL103WB	–40	125	

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5.4 Thermal Information

THERMAL METRIC[1]		TL103Wx		UNIT
		SOIC (D)	SOT-23 (DDF)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.4	170.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.3	89.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.9	87.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.4	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.1	87.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input)

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
AMPLIFIER									
V_{IO}	Input offset voltage	V_{ICM} = 0V		TL103W			±1	±4	mV
					Full range			±5	
				TL103WA			±0.5	±3.0	
					Full range			±5	
				TL103WB			±0.3	±2	
					Full range			±2.5	
αV_{IO}	Input offset-voltage drift			TL103W/TL103WA	Full range		±7		µV/°C
				TL103WB	Full range		±2		
I_{IB}	Input bias current (negative input)			TL103W/TL103WA			-20		nA
				TL103WB			-15		
A_{VD}	Large-signal voltage gain	V_{CC+} = 15V, R_L = 2kΩ, V_{ICM} = 0 V		TL103W/TL103WA			100		V/mV
				TL103WB			210		
PSRR	Supply-voltage rejection ratio	V_{CC+} = 5V to 30V, V_{ICM} = 0V		TL103W/TL103WA		65	100		dB
				TL103WB		99	114		
I_O	Output current	V_{CC+} = 15V, V_O = 2V, V_{ID} = 1V	Source			20	40		mA
			Sink	TL103W/TL103WA		10	12		
				TL103WB		10	24		
		V_{CC+} = 15V, V_O = 0.2V, V_{ID} = -1V	Sink	TL103W/TL103WA		12	50		µA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15V					±40	±68	mA
V_O	Voltage output swing from rail	V_{CC+} = 30V, R_L = 2kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.3		
					Full range	27.4			
		V_{CC+} = 30V, R_L = 10kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
		R_L = 10kΩ	Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15V, C_L = 100pF, R_L = 2kΩ, V_I = 0.5V to 2V, unity gain		TL103W/TL103WA		0.2	0.4		V/µs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103W/TL103WA		0.5[1]	0.9		MHz
		V_{CC+} = 36V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103WB		0.7[1]	1.2		

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5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input) (続き)

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_{CC+} = 30V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB	TL103W/TL103WA			0.02		%
		V_{CC+} = 36V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB	TL103WB			0.005		
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5V, no load	TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30V, no load		Full range			2	
		V_{CC+} = 5V, no load	TL103WB			0.55	0.77	
		V_{CC+} = 36V, no load		Full range			1.35	
VOLTAGE REFERENCE								
V_{ref}	Reference Voltage	I_K = 10mA	TL103W		2.482	2.5	2.518	V
				Full Range	2.465		2.535	V
			TL103WA/TL103WB		2.489	2.5	2.511	V
				Full Range	2.474		2.526	V
ΔV_{ref}	Reference input voltage deviation over temperature range	I_K = 10mA	TL103W	Full Range		7	35(1)	mV
			TL103WA/TL103WB	Full Range		7	26(1)	mV
I_{min}	Minimum cathode current for regulation		TL103W/TL103Wx			0.5	1	mA
			TL103WB			0.2	1	
$\|Z_{KA}\|$	Dynamic impedance	I_{KA} = 1mA to 100mA, f < 1kHz				0.45	0.8	Ω

(1) Not tested in production, limits set by characterization and simulation.

5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier)

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{ICM} = 0V	TL103W			±1	±4	mV
				Full range			±5	
			TL103WA			±0.5	±3.0	
				Full range			±5	
			TL103WB			±0.3	±2	
				Full range			±2.5	
αV_{IO}	Input offset-voltage drift		TL103W/TL103WA	Full range		±7		µV/°C
			TL103WB	Full range		±2		
I_{IO}	Input offset current		TL103W/TL103WA			±2	±75	nA
				Full range			±150	
			TL103WB			±0.5	±4	
				Full range			±5	
I_{IB}	Input bias current		TL103W/TL103WA			-20	-150	nA
				Full range			-200	
			TL103WB			-15	-35	
				Full range			-50	
A_{VD}	Large-signal voltage gain	V_{CC+} = 15V, R_L = 2kΩ, VO = 1.4V to 11.4V	TL103W/TL103WA		50	100		V/mV
				Full range	25	100		
			TL103WB		77	210		
				Full range	45	210		
PSRR	Supply-voltage rejection ratio	V_{CC+} = 5V to 30V	TL103W/TL103WA		65	100		dB
			TL103WB		99	114		
V_{ICR}	Input common-mode voltage range	V_{CC+} = 30V			V_{CC-}		(V_{CC+}) – 1.5	V
				Full range	V_{CC-}		(V_{CC+}) – 2	

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5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier) (続き)

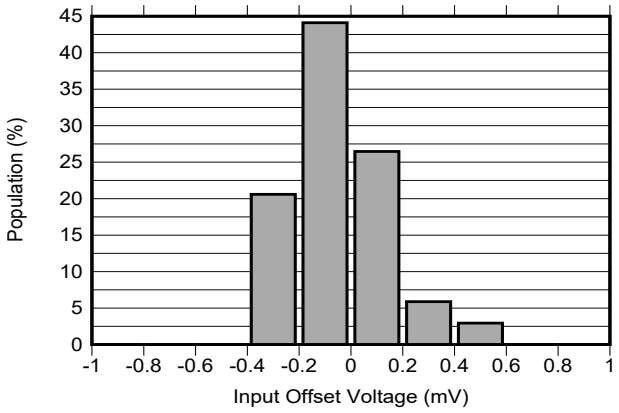
V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_{CC+} = 30V		TL103W/TL103WA		70	95		dB
					Full range	60			
				TL103WB		93	104		
					Full range	70			
I_O	Output current	V_{CC+} = 15V, V_O = 2V, V_{ID} = 1V	Source			20	40		mA
			Sink	TL103W/TL103WA		10	12		
				TL103WB		10	24		
		V_{CC+} = 15V, V_O = 0.2V, V_{ID} = -1V	Sink	TL103W/TL103WA		12	50		µA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15V					±40	±68	mA
V_O	Voltage output swing from rail	V_{CC+} = 30V, R_L = 2kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.3		
					Full range	27.4			
		V_{CC+} = 30V, R_L = 10kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
		R_L = 10kΩ	Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15V, C_L = 100pF, R_L = 2kΩ, V_I = 0.5V to 2V, unity gain		TL103W/TL103WA		0.2	0.4		V/µs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103W/TL103WA		0.5(1)	0.9		MHz
		V_{CC+} = 36V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103WB		0.7(1)	1.2		
THD	Total harmonic distortion	V_{CC+} = 30V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB		TL103W/TL103WA			0.02		%
		V_{CC+} = 36V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB		TL103WB			0.005		
V_n	Equivalent input noise voltage	V_{CC+} = 30V, R_S = 100 Ω, f = 1kHz		TL103W/TL103WA			50		nV/√Hz
		V_{CC+} = 36V, R_S = 100 Ω, f = 1kHz		TL103WB			38		
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5V, no load		TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30V, no load			Full range			2	
		V_{CC+} = 5V, no load		TL103WB			0.55	0.77	
		V_{CC+} = 36V, no load			Full range			1.35	

(1) Not tested in production, limits set by characterization and simulation.

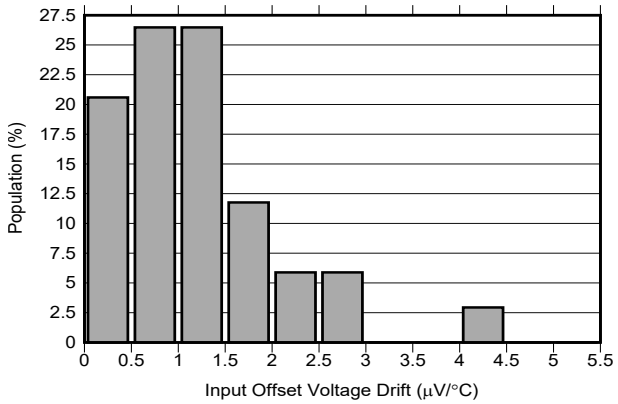
5.7 Typical Characteristics: TL103WB

at T_A ≅ 25°C, V_{CC} = 36V (±18V), V_{CM} = V_{CC} / 2, R_L = 10kΩ connected to V_{CC} / 2 (unless otherwise noted)



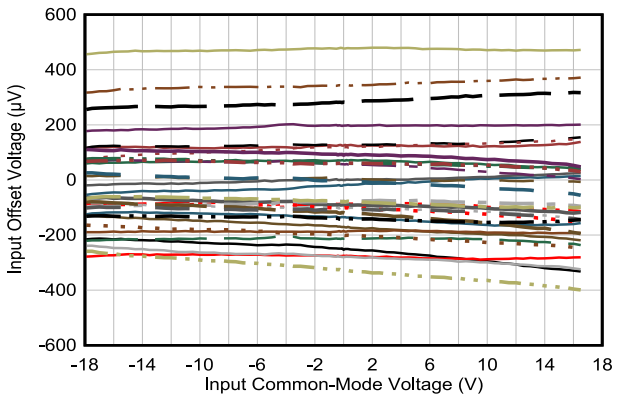
V_{CC} = 5V, No. of devices = 34
μ = 61.4 μV, σ = 166.5 μV

図 5-1. Offset Voltage Distribution Histogram



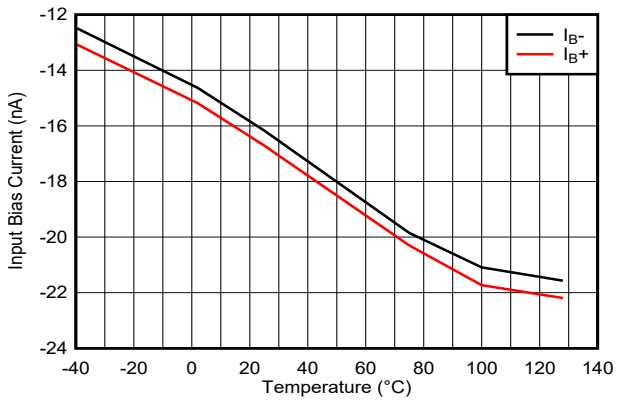
V_{CC} = 5V, No. of devices = 34
μ = 1.18 μV/°C, σ = 0.81 μV/°C

図 5-2. Offset Voltage Drift Distribution Histogram



No. of devices = 34

図 5-3. Offset Voltage vs Common-Mode



V_{CC} = 5V

図 5-4. Bias Current vs Temperature

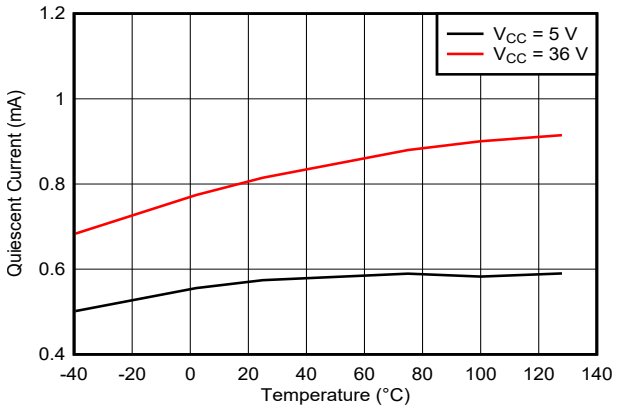
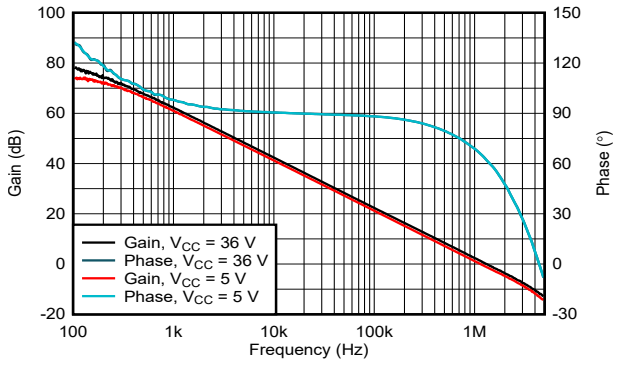


図 5-5. Quiescent Current vs Temperature



R_L = 2kΩ

図 5-6. Open-Loop Gain and Phase vs Frequency

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5.7 Typical Characteristics: TL103WB (continued)

at T_A ≅ 25°C, V_{CC} = 36V (±18V), V_{CM} = V_{CC} / 2, R_L = 10kΩ connected to V_{CC} / 2 (unless otherwise noted)

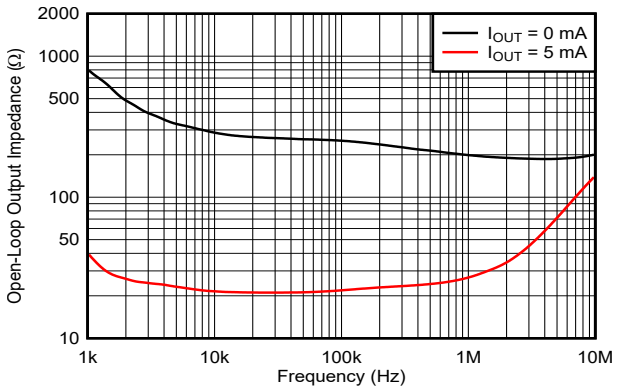


図 5-7. Open-Loop Output Impedance vs Frequency

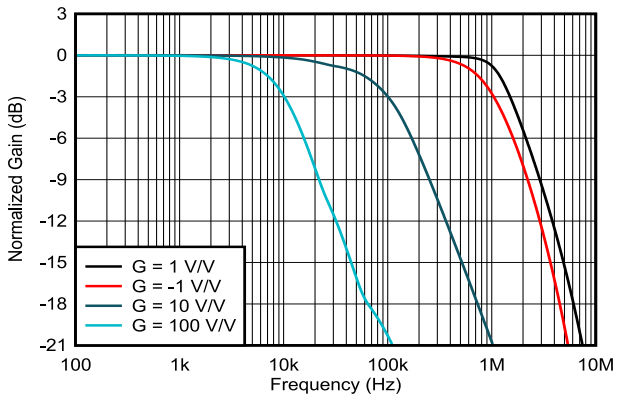


図 5-8. Closed-Loop Gain vs Frequency

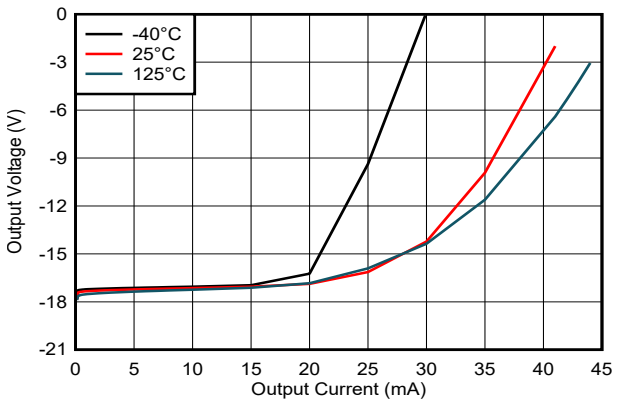


図 5-9. Output Voltage vs Output Current (Sinking)

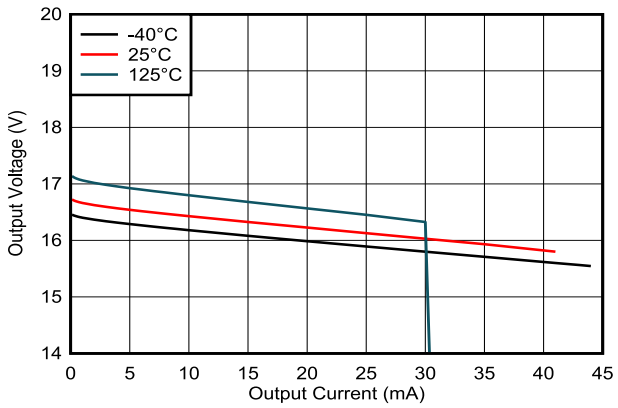


図 5-10. Output Voltage vs Output Current (Sourcing)

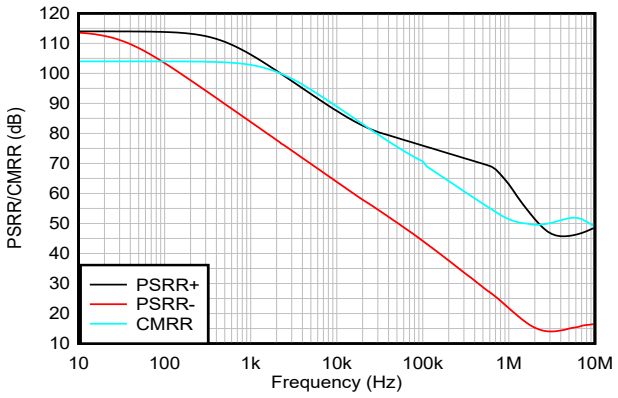


図 5-11. PSRR and CMRR vs Frequency

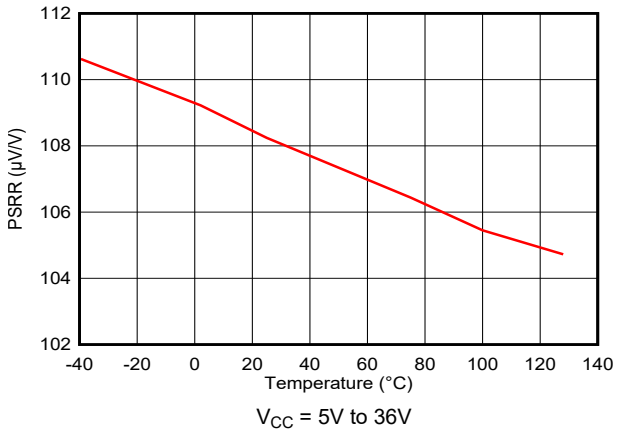


図 5-12. Supply-Voltage Rejection Ratio vs Temperature

5.7 Typical Characteristics: TL103WB (continued)

at T_A ≅ 25°C, V_{CC} = 36V (±18V), V_{CM} = V_{CC} / 2, R_L = 10kΩ connected to V_{CC} / 2 (unless otherwise noted)

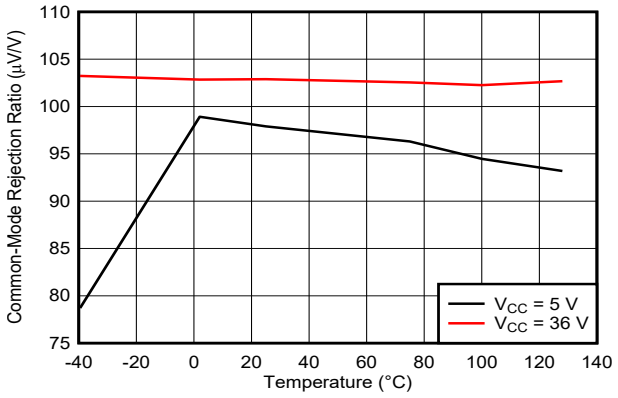


図 5-13. CMRR vs Temperature

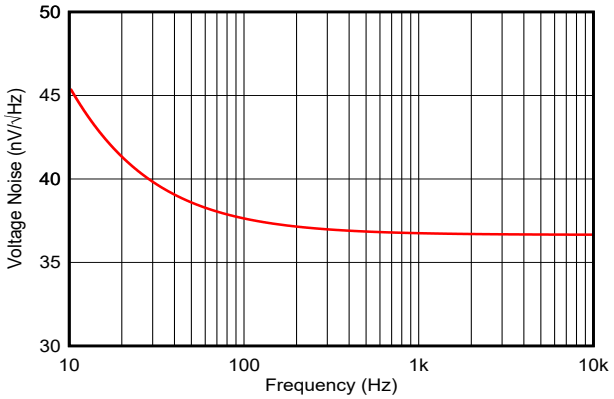
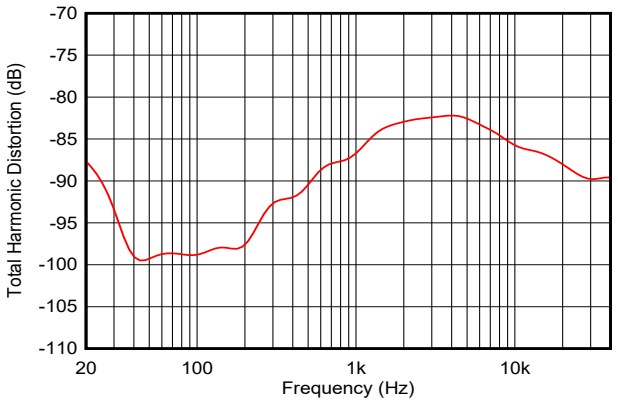
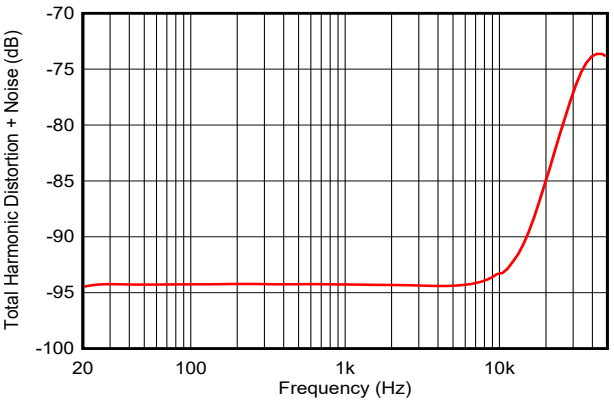


図 5-14. Input Voltage Noise Spectral Density vs Frequency



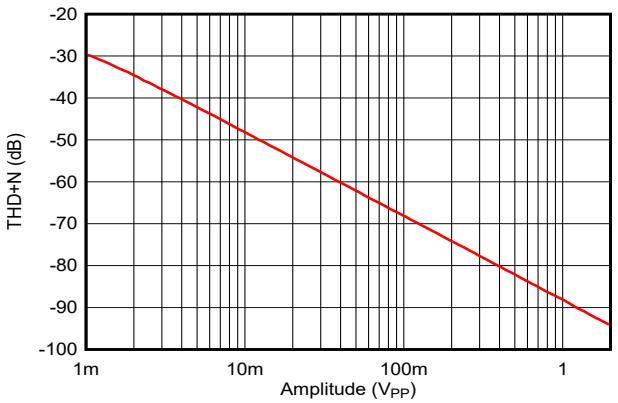
V_{CC} = 30V, V_{OUT} = 2V_{PP}, R_L = 2kΩ, C_L = 100pF, A_V = 20dB

図 5-15. Total Harmonic Distortion vs Frequency



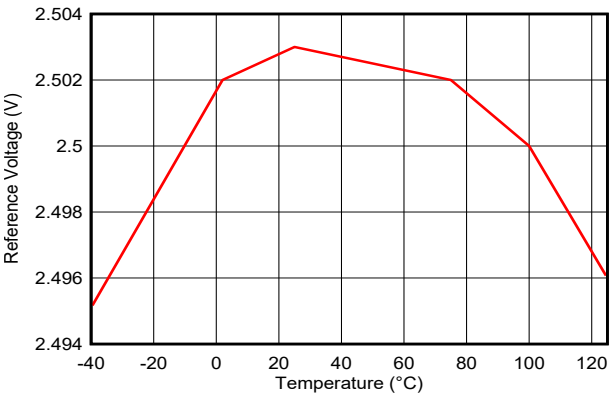
V_{OUT} = 2V_{PP}, R_L = 2kΩ, BW = 80kHz, A_V = 0dB

図 5-16. Total Harmonic Distortion + Noise vs Frequency



f = 1kHz, R_L = 2kΩ, BW = 80kHz, A_V = 0dB

図 5-17. Total Harmonic Distortion + Noise vs Amplitude



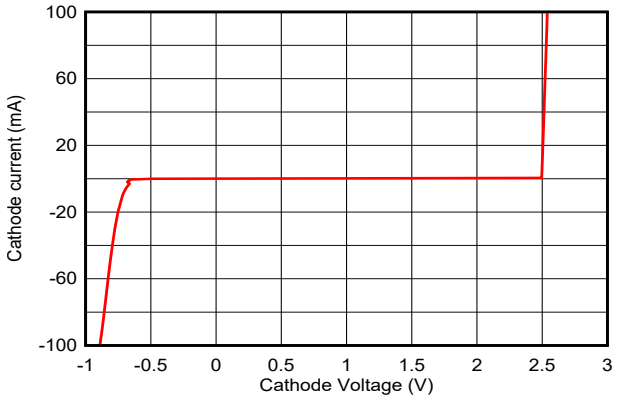
V_{CC} = 5V, I_K= 10 mA

図 5-18. Reference Voltage vs Temperature

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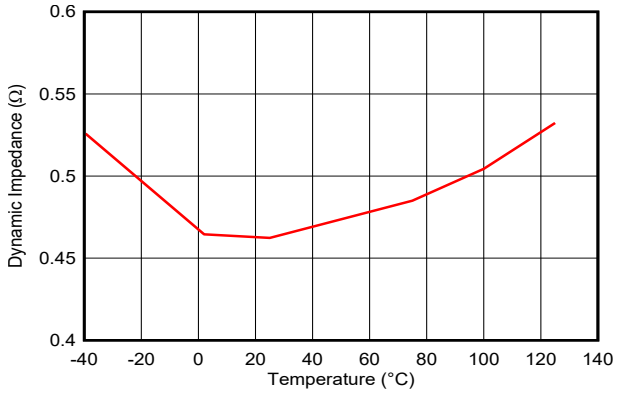
5.7 Typical Characteristics: TL103WB (continued)

at T_A ≅ 25°C, V_{CC} = 36V (±18V), V_{CM} = V_{CC} / 2, R_L = 10kΩ connected to V_{CC} / 2 (unless otherwise noted)



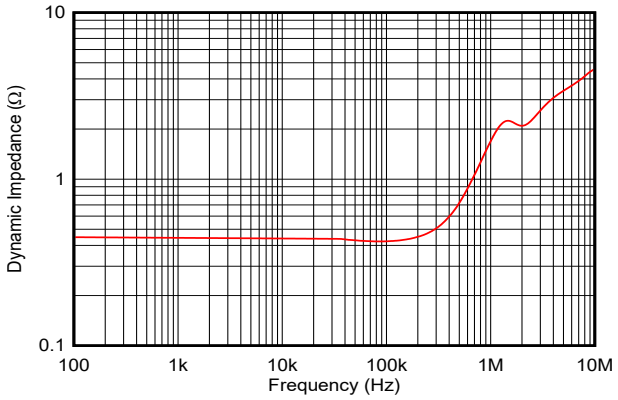
V_{CC} = 5V

図 5-19. Cathode Current vs Cathode Voltage



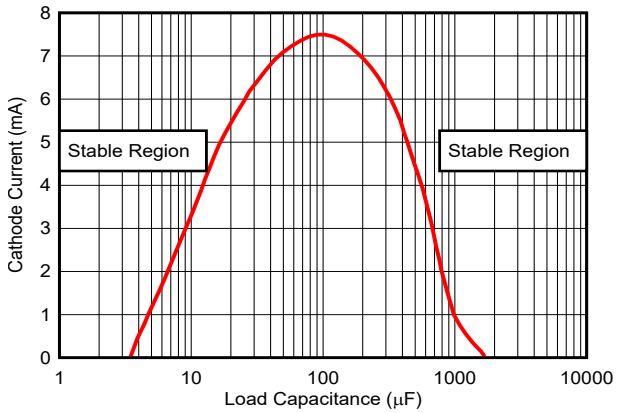
V_{CC} = 5V

図 5-20. Reference Dynamic Impedance vs Temperature



V_{CC} = 5V, I_K = 10 mA

図 5-21. Reference Dynamic Impedance vs Frequency



The area under the curve represents typical conditions that can cause the device to oscillate

図 5-22. Reference Stability vs Capacitive Load

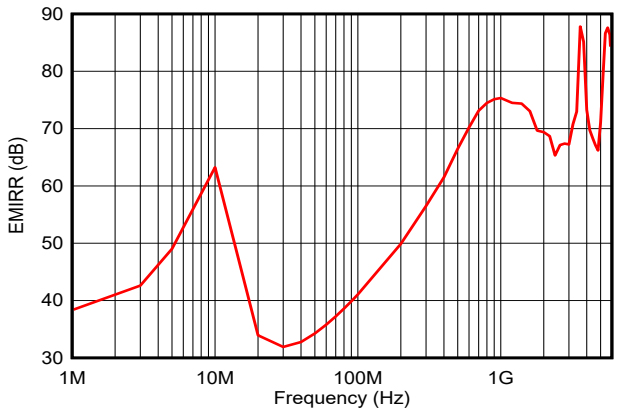


図 5-23. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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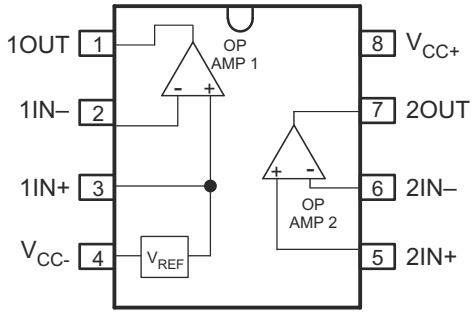
6 Detailed Description

6.1 Overview

The TL103Wx features two high-voltage amplifiers and a shunt voltage reference to allow for cost-sensitive and compact battery charger CC/CV feedback circuits. The upgraded TL103WB features is designed to provide a wide supply range (up to 36V), low offset voltage (±0.3mV typical) and a 1.2MHz bandwidth. The integrated voltage reference is tied to the non-inverting pin of one of OP AMP 1 and provides a fixed 2.5V referenced to the negative supply of the device. The shunt reference of the TL103WA/TL103WB features a tight tolerance of 0.44% at 25°C.

When a single supply voltage of 5V is used (or ±2.5V split supply), the TL103Wx internal reference allows for a more accurate and power-efficient mid-supply signal to be used throughout your circuit. The TL103W/TL103WA devices are characterized for operation from -40°C to 85°C, the TL103WB devices are characterized for operation from –40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Reference

The TL103Wx family features an internal shunt reference, tied to the non-inverting pin of one of the devices amplifiers. When supplied with enough voltage headroom (≥ 2.5V) and cathode current (0.5mA typical), the reference of the TL103Wx is forced to a fixed 2.5V. To not exceed the maximum cathode current, be sure that the reference input is current limited. Unlike many linear regulators, the reference of the TL103W is internally compensated to be stable without an output capacitor between the cathode and anode. If the reference is used to supply a load, stability criteria shown in 図 5-22 needs to be met.

Reference voltage tolerance varies based off the device grade chosen. At 25°C the TL103W features a reference tolerance of 0.72%, while the TL103WA/TL103WB both feature reference tolerances of 0.44%.

6.3.2 Input Common Mode Range

The valid common mode range is from device ground to V_{CC+} – 1.5V (V_{CC+} – 2V across temperature). Inputs may exceed V_{CC+} up to the absolute maximum voltage without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input is more than 0.3V below V_{CC-} then input current should be limited to 1mA and the output phase is undefined.

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6.3.3 EMI Rejection

The TL103WB uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TL103WB benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 図 6-1 shows the results of this testing on the TL103WB. 表 6-1 shows the EMIRR IN+ values for the TL103WB at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

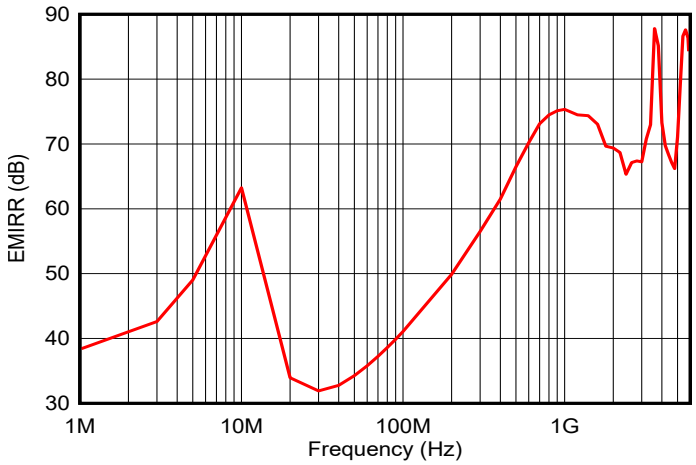


図 6-1. EMIRR Testing

表 6-1. TL103WB EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	75dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2GHz)	70dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	65dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	71dB

6.4 Device Functional Modes

This device has one mode of operation that applies when operated within the recommended operating conditions.

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

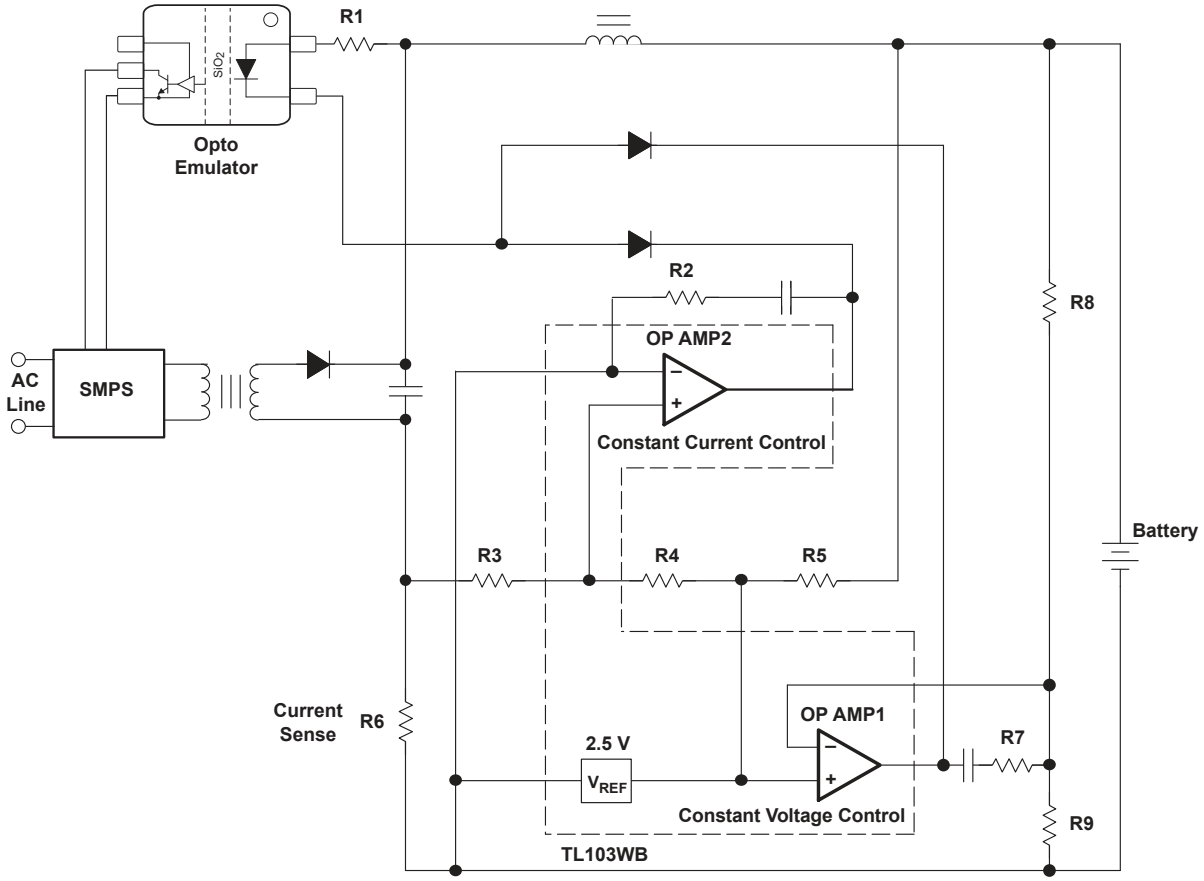
7.1 Application Information

The TL103Wx family offers a cost-effective and compact device for applications requiring both an accurate DC signal and signal conditioning. These devices offer a fixed 2.5V reference, wide bandwidth (1 to 1.2 MHz) and a low total supply current (0.55 to 0.7mA).

7.2 Typical Applications

7.2.1 Isolated Flyback CC/CV Feedback

As shown in 図 7-1, the TL103Wx is often used alongside an opto-coupler/opto-emulator to provide feedback to an isolated flyback. Utilizing the TL103Wx in this way allows for both an accurate and cost-optimized battery charger design that can achieve a stable CC/CV (Constant Current/Constant Voltage) charging profile. In this example, a simplified design procedure will be discussed. Additional details can be found in *Designing CC-CV Feedback Circuits With the TL103WB*.



Typical Application Circuit

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7.2.1.1 Design Requirements

The objective is to design an accurate CC-CV feedback circuit with the requirements provided in 表 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Maximum Charge Current	6A
Battery Voltage Range	6V to 20V

7.2.1.2 Detailed Design Procedure

To switch between CV control and CC control, diodes are utilized to achieve an OR logic function as shown in 図 7-1. Designing the circuit in this way allows one of the amplifiers (configured in either CC or CV mode) to dominate the feedback in the design. In this design, *GND* refers to the negative node at the secondary side of the switch-mode power supply.

The fixed 2.5V of the TL103Wx reference provides a stable DC voltage that is used to specify the CC current and CV voltage. One of the requirements of achieving this fixed value, however, is that the cathode of the reference must be supplied with a voltage of 2.5V or above.

7.2.1.2.1 Constant Current Circuit

For the constant current feedback circuit, the amplifier is configured in a low-side current sense configuration. Resistor R6 is used as the current sensing resistor to sense the current flowing between the battery and flyback converter. This is shown in 式 1, where I_{BAT} is the output current delivered to the battery. The voltage at the non-inverting input of the amplifier specifies the maximum current (or constant current) that is delivered to the battery.

$$V_{BAT\,-} = I_{BAT} \times R6 \tag{1}$$

The reference of the TL103Wx is powered by the battery voltage. To be able to achieve a constant current, this reference needs to be provided with 2.5V or greater to provide a fixed 2.5V. The first step in designing a constant current circuit is to specify that 2.5V can be achieved at the battery's minimum voltage. The value of R5 must also be designed so that a sink-current between 0.5mA to 100 mA (for TL103W or TL103WA) is achieved across the specified range of the battery voltage. These two steps are shown below.

$$V_{BAT}(min) \times \frac{R4 + R3}{R4 + R3 + R5 + R6} \geq 2.5\ \text{V} \tag{2}$$

$$0.5\ \text{mA} \leq \frac{\text{V}_{BAT} - V_{REF}}{R5} \leq 100\ \text{mA} \tag{3}$$

For this design R5 is chosen to be 2kΩ. Knowing this and the specified battery range of 6V to 20V, we can calculate that the reference sinks anywhere from 1.75mA to 10mA using 式 2.

Once a fixed 2.5V reference is achieved, we can use this accurate DC voltage to specify a constant current target on the non-inverting input of the amplifier. This can be done by calculating the voltage at the amplifier's inverting input when a constant current target is achieved. Specifying R6 to be 10mΩ along with a constant current design target of 6A, we find that this voltage to be 60 mV using 式 1. The voltage at the non-inverting pin of the amplifier is specified by 式 4.

$$V_{IN\,+} = 2.5\ V \times \frac{R3}{R4 + R3} \tag{4}$$

Using the component values and design targets calculated so far, 式 2 and 式 4 can be updated to:

$$6\ V \times \frac{R4 + R3}{R4 + R3 + 2\ k\Omega + 10\ m\Omega} \geq 2.5\ \text{V} \tag{5}$$

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$$60\ mV = 2.5\ V \times \frac{R3}{R4 + R3} \quad (6)$$

Using both 式 5 and 式 6, we calculate that R3 needs to be greater than around 34.28Ω. Adding additional headroom to this, we can calculate R3 = 36Ω and R4 = 1464Ω.

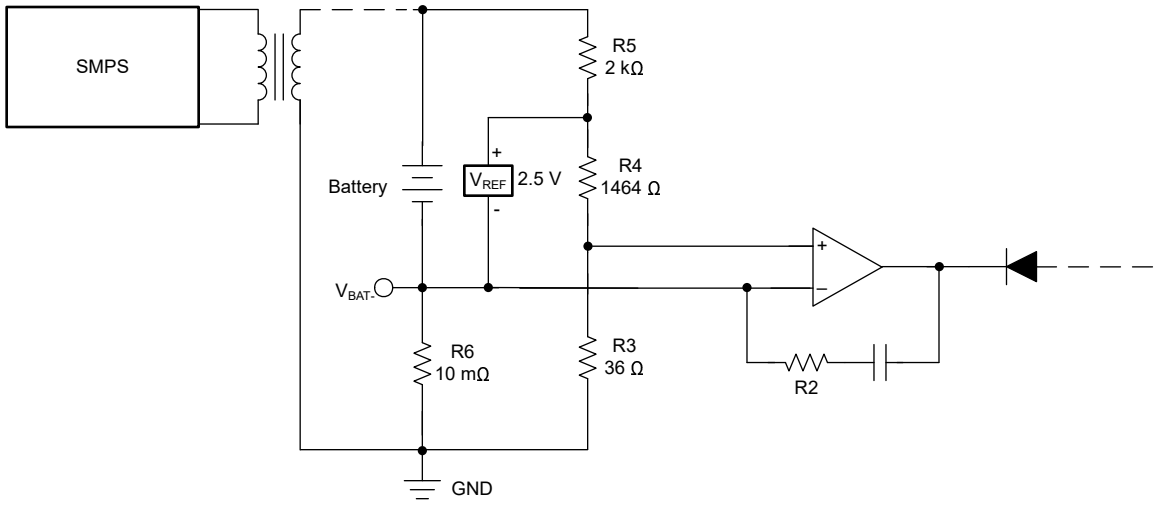


図 7-1. Constant Current Feedback Circuit

7.2.1.2.2 Constant Voltage Circuit

For the constant voltage feedback circuit, resistors R8 and R9 divide down the battery voltage to compare against the TL103Wx's reference. This is shown in 図 7-2. The voltage at the inverting input of the amplifier is designed to equal 2.5V when the battery reaches its maximum specified voltage (or desired constant voltage value). This is shown in for a maximum voltage of 20V provided in 表 7-1.

$$V_{BAT} \times \frac{R9}{R8 + R9} = 2.5\ V \quad (7)$$

$$20\ V \times \frac{R9}{R8 + R9} = 2.5\ V \quad (8)$$

To mimic the constant current circuit and achieve a total impedance and 2kΩ across the battery, R8 is set to 1.96kΩ and R9 to 280Ω.

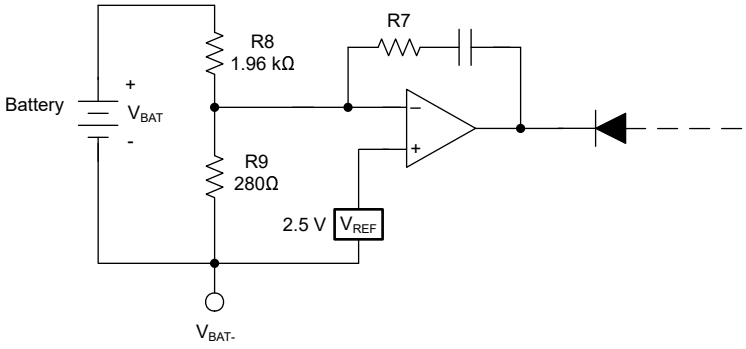


図 7-2. Constant Voltage Circuit

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7.2.2 Constant Current Sink

図 7-3 shows the use of the TL103Wx along with a transistor to provide a constant current sink source. This type of circuit is common in LED drivers and can provide accurate performance and high bandwidth with minimal external components. Accuracy of this circuit is dominated by the reference voltage tolerance, amplifier offset voltage, and resistor tolerance. R_{LIM} is placed to limit the shunt current of the circuit's reference to a maximum of 100mA.

$$I_{SINK} = \left(V_{REF} \times \frac{R_2}{R_1 + R_2}\right) \times R_S \quad (9)$$

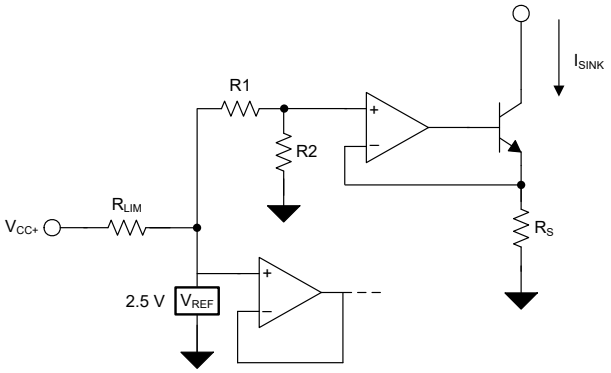


図 7-3. TL103Wx as Constant Current Sink

7.3 Power Supply Recommendations

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see セクション 7.4

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - If a bypass capacitor is needed to help stabilize the reference, place this capacitor as close to the reference pin as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in セクション 7.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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- For applications shunting high currents through the reference, pay attention to the cathode and anode traces. Ensure the width of these traces are designed with proper current density.

7.4.2 Layout Example

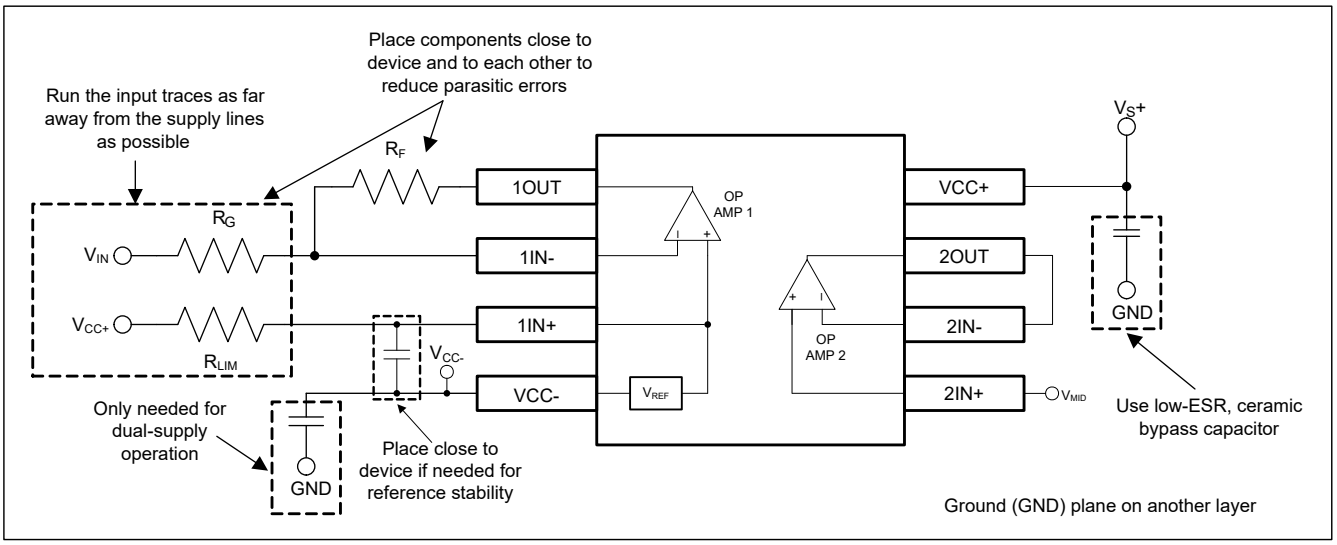


図 7-4. Operational Amplifier Board Layout for Inverting Configuration

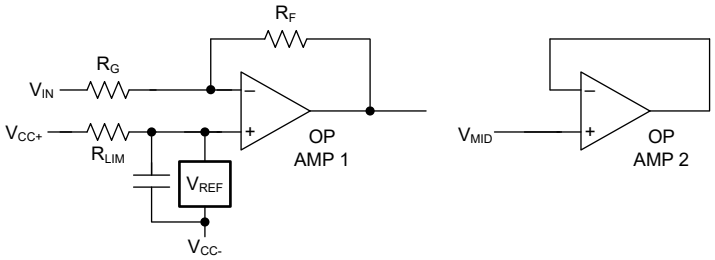


図 7-5. Operational Amplifier Schematic for Inverting Configuration

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Designing CC-CV Feedback Circuits With the TL103WB*

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision P (November 2023) to Revision Q (December 2023)	Page
• Updated maximum dynamic impedance from 0.5 Ω to 0.8 Ω in *Electrical Characteristics* table	5
• Updated EMIRR IN+ values in *EMIRR IN+ for Frequencies of Interest* table	13

Changes from Revision O (October 2023) to Revision P (November 2023)	Page
• Updated typical large-signal voltage gain of TL103WB from 140V/mV to 210 V/mV	5
• Updated minimum limit of supply-voltage rejection ratio of TL103WB from 80 dB to 99dB	5
• Added footnote in Electrical Characteristics tables to specify specifications which have limits set by characterization	5
• Updated minimum limit of gain bandwidth product for TL103WB from 0.5MHz to 0.7MHz	5
• Updated maximum limit of total supply current for TL103WB at 25°C from 0.92 mA to 0.77mA	5
• Updated maximum limit of total supply current for TL103WB at full temperature range from 1.6mA to 1.35mA	5

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- Updated minimum limit of large-signal voltage gain for TL103WB at 25°C from 70V/mV to 77V/mV 6
- Updated minimum limit of large-signal voltage gain for TL103WB at full temperature range from 35V/mV to 45V/mV 6
- Added new CMRR specifications for TL103WB 6

Changes from Revision N (August 2023) to Revision O (October 2023) **Page**

- 「特長」セクションの最大入力オフセット電圧、基準電圧のトレランス、合計消費電流、シンク電流範囲を変更 1
- TL103WB とフォトカプラ・エミュレータを含めるよう「代表的なアプリケーション回路」図を変更 1
- TL103WB D (SOIC、8) のステータスを事前情報 (プレビュー) から量産データ (アクティブ) に変更 1
- Changed *Thermal Information* table to include latest thermal metrics 5
- Added DDF information to *Thermal Information* table 5
- Updated k_{SVR} term to PSRR 5
- Changed maximum short circuit current from ±60mA to ±68 mA 5
- Maximum reference input voltage deviation over temperature range for TL103W was changed from 30mV to 35mV 5
- Maximum reference input voltage deviation over temperature range for TL103WA was changed from 30mV to 26mV 5
- Added figures to the *Typical Characteristics* section to highlight the TL103WB device 8
- Added the *Detailed Description* and *Application and Implementation* sections 12
- Added the *Application and Implementation* sections 14

Changes from Revision M (October 2016) to Revision N (August 2023) **Page**

- 「特長」セクションを更新し、TL103WB を強調 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- ドキュメント全体を通して TL103WB の製品情報を追加 1
- 「概要」セクションを更新 1
- チャネル数を含めるよう「製品情報」表を更新 1
- Removed DRJ package details and added DDF package for preview 3
- Updated formatting for *Electrical Characteristics* tables 5
- Updated typical dynamic impedance from 0.2 Ω to 0.45 Ω in *Electrical Characteristics* tables 5

Changes from Revision L (February 2016) to Revision M (October 2016) **Page**

- Changed positive and negative terminals OP AMP 2 in the D Package image of *Pin Configuration and Functions* 3

Changes from Revision K (October 2010) to Revision L (February 2016) **Page**

- 「製品情報」表、「ピン構成および機能」、「ESD 定格」、「熱に関する情報」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- 「特長」を「2kV の ESD 保護 (HBM)」から「2.5kV の ESD 保護 (HBM)」に変更 1
- 「代表的なアプリケーション回路」のツェナー・ダイオード部品を V_{REF} に変更 1
- Changed the Zener diode component to V_{REF} in the D Package of *Pin Configuration and Functions* 3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTL103WBIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TL103WAID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	
TL103WAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WBIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL103D	Samples
TL103WID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	
TL103WIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

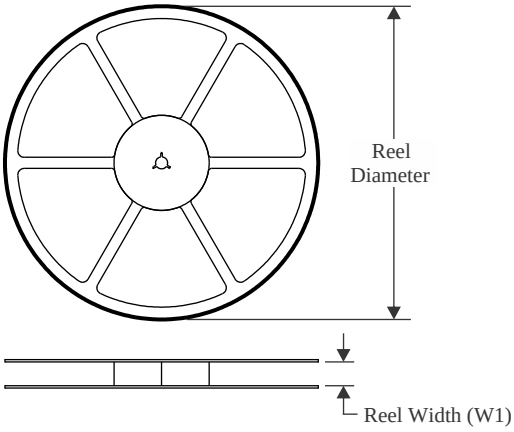
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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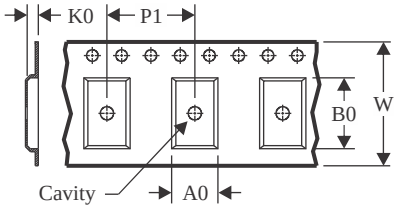
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

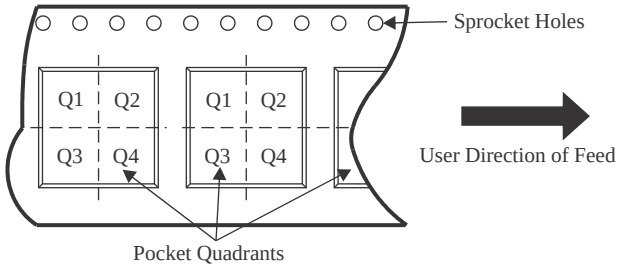


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

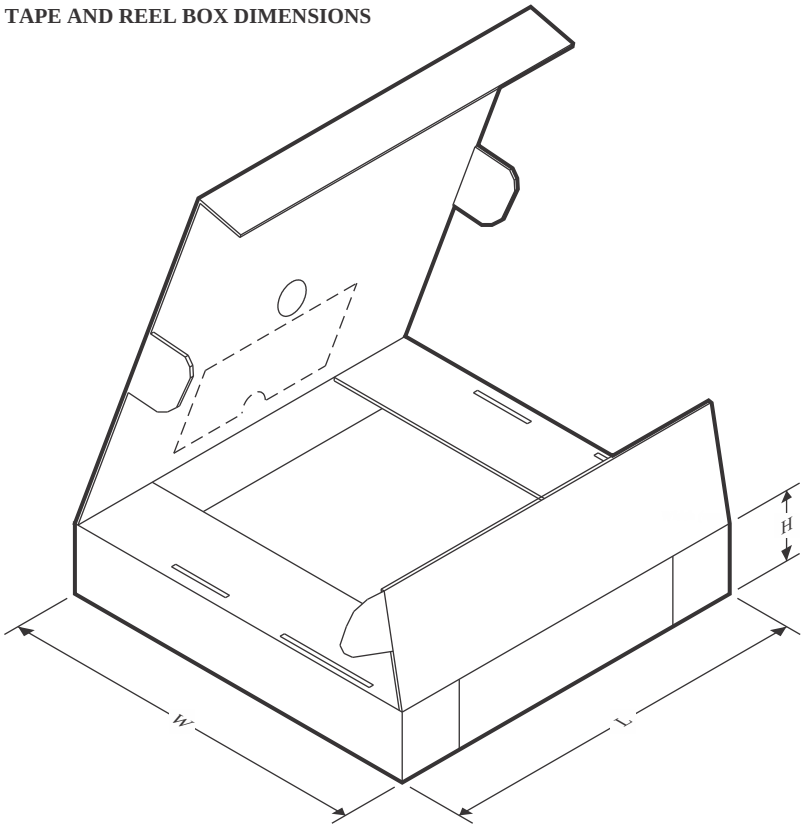
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WBIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

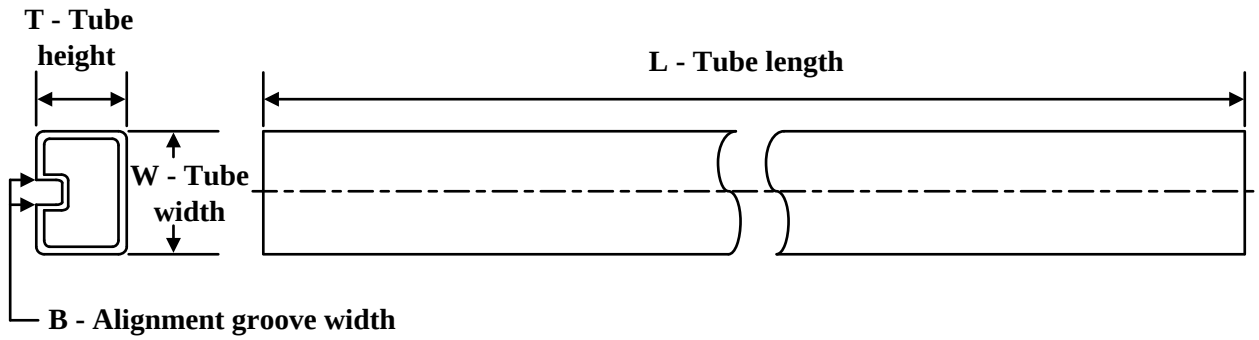
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL103WBIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL103WIDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

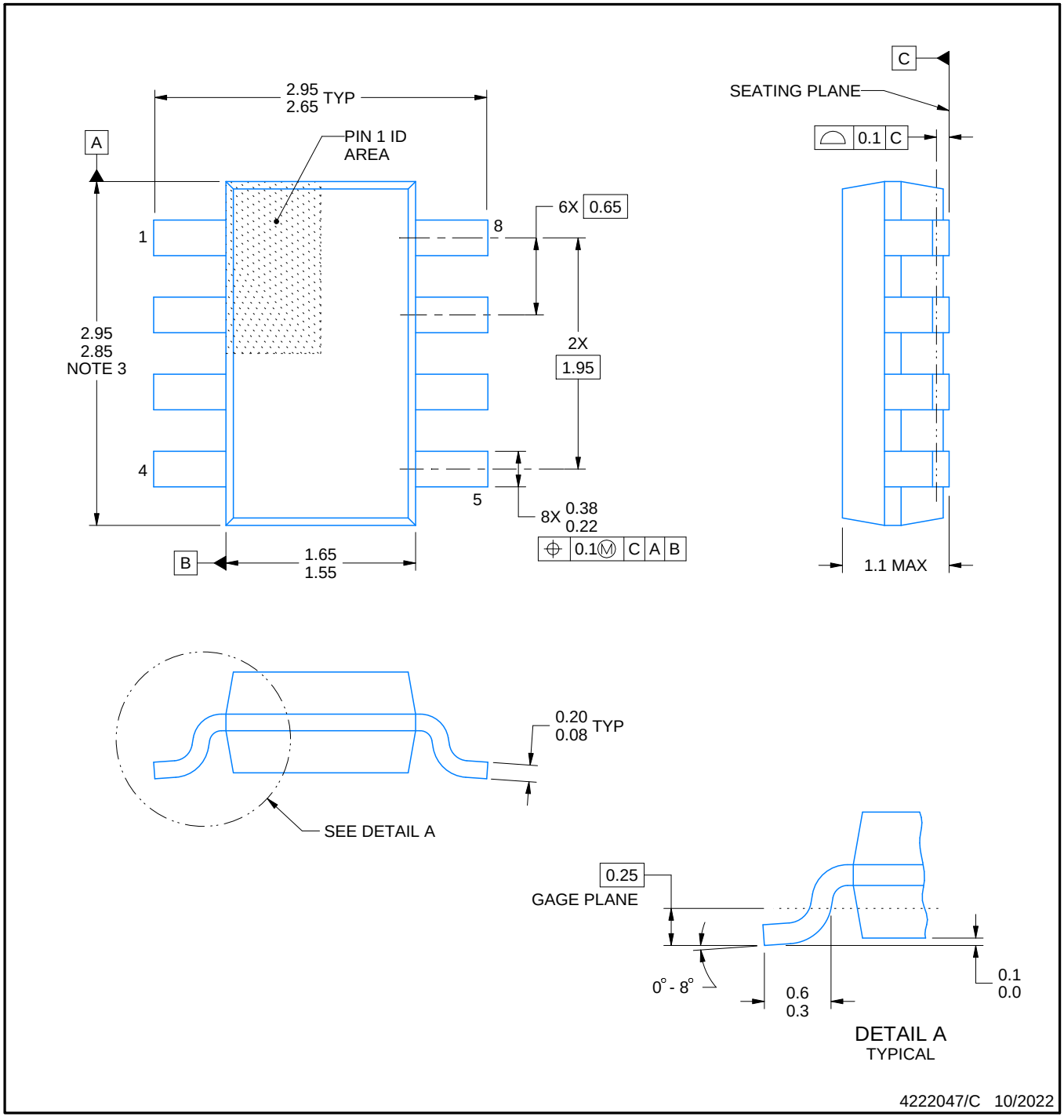
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL103WAID	D	SOIC	8	75	507	8	3940	4.32
TL103WID	D	SOIC	8	75	507	8	3940	4.32

PACKAGE OUTLINE

DDF0008A

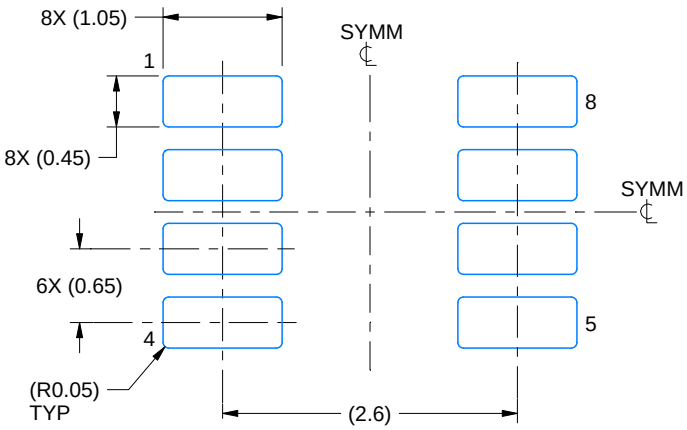
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

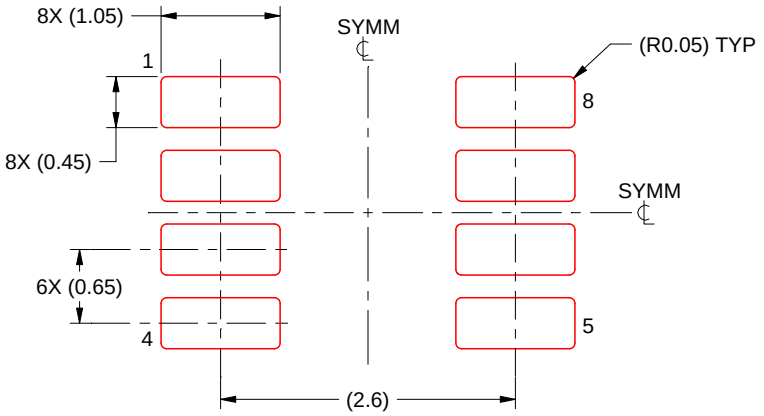
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

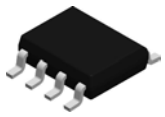


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

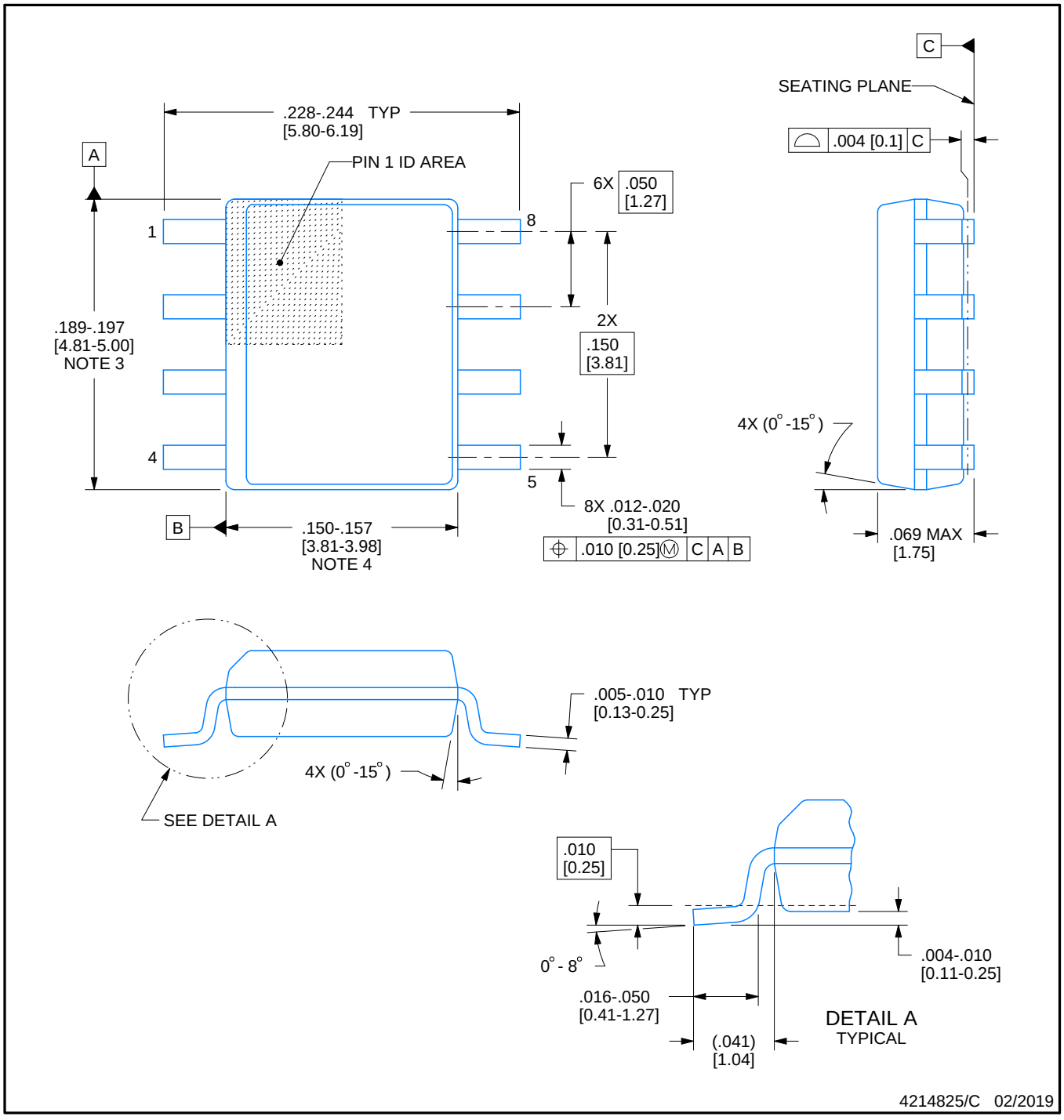


PACKAGE OUTLINE

D0008A

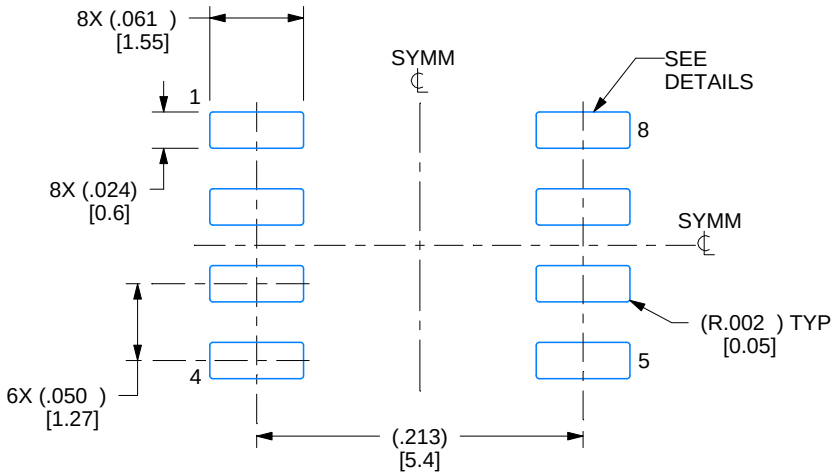
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

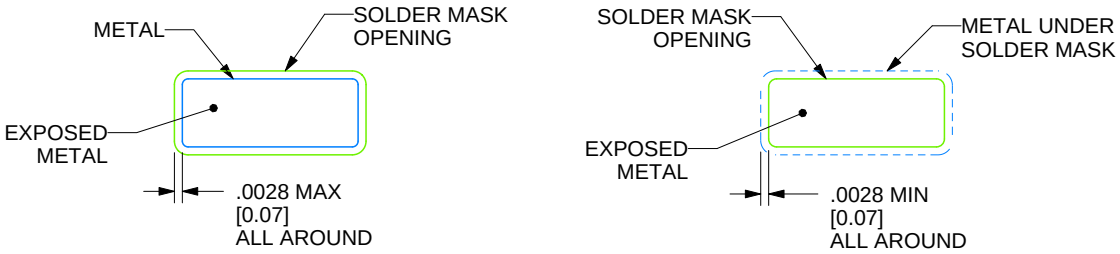


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

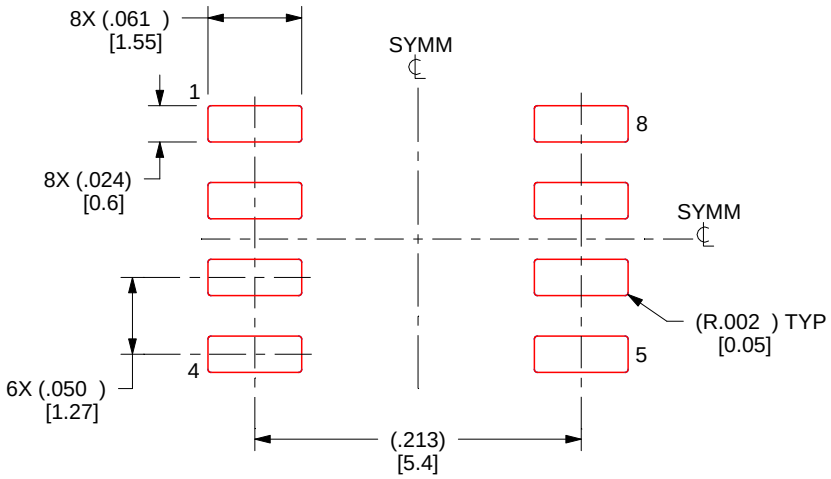
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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